

Lahore University of Management Sciences EE340 – Devices and Electronics

Fall 2023

Instructor	Nauman Ahmad Zaffar
Room No.	9-213A
Office Hours	
Email	nauman.zaffar@lums.edu.pk
Telephone	x8311
TA	
TA Office Hours	TBA
Course URL (if any)	

Course Basics				
Credit Hours	3	3		
Lecture(s)	Nbr of Lec(s) Per Week	2	Duration	75 minutes each
Recitation (per week)	Nbr of Lec(s) Per Week	0	Duration	N/A
Lab (per week)	Nbr of Lec(s) Per Week		Duration	

Course Distribution		
Core	Υ	
Elective	N	
Open for Student Category	Electrical Engineering, Physics	
Close for Student Category		

COURSE DESCRIPTION

This course lays down the foundations for the design of electronic devices and systems for a variety of applications. This includes the construction, characteristics and working of diodes and field effect transistors (FET). It will cover topics on modeling of microelectronic devices, basic microelectronic circuit analysis and design, physical electronics of semiconductor junction and MOS devices, development of circuit models, and understanding the uses and limitations of various models. The semiconductor fundamentals, doping and carrier densities, carrier transport and generation-recombination, and the "semiconductor equations," which provide a mathematical description of electrons and holes in semiconductors will be covered. The course will use incremental and large-signal techniques to analyze and design field effect transistor circuits as well as an overview of multistage amplifiers. The small signal behavior of FET transistors is studied along with appropriate mathematical models and frequency response. The course also provides an introduction to the design of power amplifiers and switching circuits. BJTs will also be covered to provide historic reference to their operation, DC biasing and amplifier circuits.

COURSE PREREQUISITE(S)			
• EE240	Circuits I (required)		

COURSE OBJECTIVES		
1.	To introduce the students to the fundamentals of semiconductors and semiconductor devices.	
2.	Study the structure, characteristics and behavior of fundamental set of discrete electronic devices.	
3.	Develop skills needed for analysis and design of electronic circuits and systems using these components and present them in	
	an articulate way	

	Course Learning Outcomes
EE340:	The students should be able to:
CLO1:	Analyze the semiconductor carrier properties, carrier motion, PN junction physics and junction capacitive effects.
CLO2:	Analyze different diode-based application circuits (rectifiers, clippers, clampers and multipliers)



Lahore University of Management Sciences

Analyze MOSFET and BJT based circuits (Biasing/DC Analysis, Different Amplifier CLO3: Configurations, frequency response and application as a switch) Design MOSFET based circuits (Biasing/DC Operating Point, Different Amplifier CLO4: Configurations)

Relation to EE Program Outcomes

EE-340 CLOs	Related PLOs	Levels of learning	Teaching Methods	CLO Attainment checked in
CLO1	PLO2	Cog 4	Instruction, Tutorial, Assignments	Quiz, Final
CLO2	PLO2	Cog 3	Instruction, Tutorial, Assignments	Quiz, Final
CLO3	PLO2	Cog 3	Instruction, Tutorial, Assignments	Quiz, Final
CLO4	PLO3	Cog 5	Instruction, Tutorial, Assignments	Quiz, Final

Grading Breakup and Policy

Assignment(s):

Home Work ~5: → 15% Quiz(s): ~8→ 15%

Midterm Examination: 01 → 30%

Final Examination 01: Comprehensive → 40%

Lecture	Topics	Recommended Readings	Related CLOs & Additional Remarks
1.	Semiconductors – General Introduction	SDF Ch. 1	CLO1
2.	Carrier modeling – energy bands and band gaps	SDF Ch. 2	CLO1
3.	Density of States, Fermi Energy	SDF Ch. 2	CLO1
4.	Doping/carrier concentration	SDF Ch. 2	CLO1
5.	Transport mechanism	SDF Ch. 3	CLO1
6.	Drift and Diffusion Currents	SDF Ch. 3	CLO1
7.	Recombination/Generation	SDF Ch. 3	CLO1
8.	Junction structure and electrostatics	SDF Ch. 5	CLO1
9.	Electrostatics and Junction I-V characteristics	SDF Ch. 5	CLO1
10.	I-V characteristics, Small signal admittance	SDF Ch. 6	CLO1
11.	Junction capacitance, diffusion admittance	SDF Ch. 6	CLO1
12.	Diode circuits – models and applications	S&S: Ch. 4	CLO2
13.	Diode circuits – analysis and applications	S&S: Ch. 4	CLO2
14.	Midterm		
	MOSFET – Structure and device operation, models	S&S: Ch. 5	CLO3
15.	MOSFET – Biasing and DC analysis	S&S: Ch. 5	CLO3
16.	MOSFET – Biasing and DC Design	S&S: Ch. 5	CLO4
17.	MOSFET – Amplifier configurations	S&S: Ch. 5	CLO3
18.	MOSFET – Small signal models and analysis	S&S: Ch. 5	CLO3
19.	MOSFET – Small signal models/Design	S&S: Ch. 5	CLO4
20.	MOSFET – Amplifier characteristics	S&S: Ch. 5	CLO3
21.	Transistor Switch and Inverter	S&S: Ch. 13	CLO3
22.	Current Mirror configurations	S&S: Ch. 7	CLO3, CLO4
23.	Multistage amplifiers	S&S: Ch. 7	CLO3, CLO4
24.	Frequency response of amplifiers – low freq.	S&S: Ch. 9	CLO3, CLO4
25.	High Frequency response	S&S: Ch. 9	CLO3, CLO4
26.	BJT – Structure and device operation, models and Biasing	S&S: Ch. 6	CLO3
27.	BJT – Small signal models and amplifier analysis	S&S: Ch. 6	CLO3



Lahore University of Management Sciences

Textbook(s)/Supplementary Readings

Textbook:

Semiconductor Device Fundamentals (SDF) by Robert Pierret, Addison Wesley, 1996 Microelectronic Circuits by Sedra and Smith, 6th Edition, Oxford University Press, 2010

Supplementary Reading:

Fundamentals of Microelectronics by Behzad Razavi

Microelectronic Devices & Circuits by Clifton Fonstad, 2006 Electronic Edition, http://dspace.mit.edu/handle/1721.1/34219

Examination De	
Midterm Exam	Yes/No: No Combine/Separate: Combined Duration: 03 hrs Preferred Date: During Mid-week Exam Specifications: Closed book, closed notes, One A4, double-sided, hand-written help sheet, calculators
Final Exam	Yes/No: No Combine/Separate: Combined Duration: 03 hrs Exam Specifications: Closed book, closed notes, Two A4, double-sided, hand-written help sheets, calculators

Complex Engine	Complex Engineering Problem/Activity:		
Complex Engineering Problem Details	Included: No Assessment in: N/A		
Complex Engineering Activity Details	Included: No Assessment in: N/A		

Rubric Based Asse	Rubric Based Assessment of CLO		
Rubric Details	Rubric used for CLOs: CLO-wise details of each rubric design per assessment module: N/A		

Prepared and Revised by:	Nauman Ahmad Zaffar	
Revision Date:	July 18, 2023	