Lahore University of Management Sciences

EE 421 / CS 425 – Digital System Design

(Fall 2023)

Course Catalog Description
This course explains how to go about designing complex, high-speed digital circuits and systems. Complete digital design-flow through the use of modern design automation tools in description, simulation, logic synthesis and implementation technology is explored. Application of a hardware description language such as Verilog (or VHDL) to model digital systems at Behavior and RTL level is studied. Advanced methods of logic minimization and state-machine design are discussed. Design and implementation of digital functional building blocks such as arithmetic circuits, datapaths, microprocessors, I/O modules, interfacing, UARTs, frequency generators, memories, encryption, etc. is included. BIST and Scan techniques for testing of digital systems are also covered. Study of architecture of modern FPGA is included.

Course Details	
Credit Hours	**3 (Theory)** + 1 Lab (separate enrolment)
Core	MS EE (Electronics and Embedded Systems Stream), MS (Digital Embedded Systems)
Elective	BS EE / CS , MS EE Elective
Open for Student Category	Senior / MS
Closed for Student Category	Freshman / Sophomore / Junior

Course Prerequisite(s)/Co-Requisite(s)
Pre-requisites: EE 322 OR EE 324 OR CS 320/EE320 OR CS 225 OR Grad Standing Co-requisites: EE 421 Lab

Course Offering Details (online offering may require some changes)						
Lecture(s)	Nbr of Lec(s) Per Week	2	Duration	75 min	Timings and Venue	TBA
Recitation (per week)	Nbr of Rec (s) Per Week	X	Duration			
Lab (if any) per week	Nbr of Session(s) Per Week	X	Duration			
Tutorial (per week)	Nbr of Tut(s) Per Week	X	Duration			

Instructor	Dr. Shahid Masud
Room No.	EE Dept. 9-223A, Maxwell Wing
Office Hours	Tue, Thu, 1100 to 1130 hrs
Email	smasud@lums.edu.pk
Telephone	8199
Secretary/TA	Will be announced on LMS
TA Office Hours	Will be announced on LMS
Course URL (if any)	LMS will be used

Course Teaching Methodology (Please mention following details in plain text)
• Teaching Methodology: On-Campus classes are expected. • Lecture details: Class-room lectures are expected unless there are Covid related restrictions.

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Course Learning Outcomes	
	The students completing EE 421 / CS 425 should be able to:
CLO1:	Understand and describe different abstractions of designing complex combinational and sequential logic circuits and their implementation on FPGA platform.
CLO2:	Describe the concepts of timing hazards and how timing parameters influence circuit performance.
CLO3:	Describe and analyze complex digital circuits like advanced binary adders, integer and FP multipliers, binary dividers, DSP filters, ASM charts, other digital system design case studies, etc.
CLO4:	Describe different techniques for testing faults in digital systems such as stuck-at faults, SCAN test, BIST, etc.

Relation to EE Program Outcomes

EE/421 CLOs	Related PLOs	Levels of Learning	Teaching Methods	CLO Attainment checked in
CLO1	PLO1	Cog-3	Instruction, Assignments	Midterm, Final, Quizzes
CLO2	PLO1	Cog-3	Instruction, Assignments	Midterm, Final, Quizzes
CLO3	PLO2	Cog-3	Instruction, Assignments	Midterm, Final, Quizzes
CLO4	PLO2	Cog-3	Instruction, Assignments	Final, Quizzes

Academic Honesty

The principles of truth and honesty are recognized as fundamental to a community of teachers and students. This means that all academic work will be done by the student to whom it is assigned without unauthorized aid of any kind. Plagiarism, cheating and other forms of academic dishonesty are prohibited. Any instances of academic dishonesty in this course (intentional or unintentional) will be dealt with swiftly and severely. Potential penalties include receiving a failing grade on the assignment in question or in the course overall. For further information, students should make themselves familiar with the relevant section of the LUMS student handbook.

Harassment Policy

SSE, LUMS and particularly this class, is a harassment free zone. There is absolutely zero tolerance for any behavior that is intended or has the expected result of making anyone uncomfortable and negatively impacts the class environment, or any individual's ability to work to the best of their potential.

In case a differently abled student requires accommodations for fully participating in the course, students are advised to contact the instructor so that they can be facilitated accordingly.

If you think that you may be a victim of harassment, or if you have observed any harassment occurring in the purview of this class, please reach out and speak to me. If you are a victim, I strongly encourage you to reach out to the Office of Accessibility and Inclusion at oai@lums.edu.pk or the sexual harassment inquiry committee at harassment@lums.edu.pk for any queries, clarifications, or advice. You may choose to file an informal or a formal complaint to put an end of offending behavior. You can find more details regarding the LUMS sexual harassment policy here.

To file a complaint, please write to harassment@lums.edu.pk.

SSE Council on Equity and Belonging

In addition to LUMS resources, SSE's Council on Belonging and Equity is committed to devising ways to provide a safe, inclusive, and respectful learning environment for students, faculty and staff. To seek counsel related to any issues, please feel free to approach either a member of the council or email at cbe.sse@lums.edu.pk

Rights and Code of Conduct for Online Teaching

The misuse of online modes of communication is unacceptable. TAs and Faculty will seek consent before the recording of live online lectures or tutorials. Please ensure, if you do not wish to be recorded during a session to inform the faculty member. Please also ensure that you prioritize formal means of communication (email, lms) over informal means to communicate with course staff.

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Grading Breakup and Policy
Class quizzes: (5 – 6 quizzes, one dropped): 20% Assignments: (1 - 2): 10% Midterm exam: 30% Final exam: 40% *Note: The lab component for MS students will be included in the final grade of theory as explained in the class!

Lecture / Week	Course Topics	Readings	Lab / Quiz
1 / Wk 1	Introduction to digital systems and their design flow	Ciletti	
2 / Wk 1	Review of combinational logic, logic minimization	Ciletti	
3 / Wk 2	Advanced Logic Minimization Techniques	Ciletti	
4 / Wk 2	Timing in Combinational Circuits, Hazards and Glitches	Notes	
5 / Wk 3	Review of sequential logic	Ciletti	
6 / Wk 3	Design using flip-flop and latches, State machines	Ciletti	
7 / Wk 4	State reduction, timing issues	Ciletti	
8 / Wk 4	Design of Adders and Subtractors, Carry Lookahead Adders	Ciletti	
9 / Wk 5	Serial Adders, Array Multipliers, Critical Paths	Ciletti	
10 / Wk 5	Booth and Radix-4 Encoded Signed Multipliers		
11 / Wk 6	Further Verilog (or VHDL) modeling, parameterization	Ciletti	
12 / Wk 6	Design of dividers and other arithmetic circuits	Notes	
13 / Wk 7	Circuits for Floating Point Implementation	Ciletti	
14/Wk 7	Serial Multipliers, Signed Multiplication of Fractions		
15 / Wk 7	**Midterm Exam**		
16 / Wk 8	Introducing Programmable logic, PAL, PLA, CPLD	Ciletti	
17 / Wk 8	Construction, operation, examples of FPGA and CPLD	Ciletti	
18 / Wk 9	Controller design using ASM charts	Ciletti	
19 / Wk 9	Controller Design for Sequential Multipliers and Dividers	Ciletti	
20 / Wk 10	Faults and Testability – BIST and SCAN techniques	Ciletti	
21 / Wk 10	Design for test – JTAG	Ciletti	
22 / Wk 11	LFSR, BRM, Function Generators, Design Examples	Ciletti	
23 / Wk 11	Parity and Error Detection, Correction Circuits	Note	
24 / Wk 11	HDL Synthesis Issues / Xilinx DSP Blocks	Ciletti	
25 / Wk 12	Advanced HDL / Examples of Digital Systems / UART	Notes	
26 / Wk 13	Asynchronous Sequential Design	Zwolinski	
27 / Wk 14	Digital Design Case Study / Frequency Synthesizer	Notes	
	Final Exam Week 15 or 16		

Textbook(s)/Supplementary Readings
Textbook: Advanced Digital Design with the Verilog HDL, Michael D. Ciletti, Prentice Hall Supplementary Reading**: (Additional Notes, articles, and slides will be provided where needed)** 1.Verilog HDL Samir Palnitkar 2.Principles of Digital Systems Design using Verilog, Charles H. Roth, Lizy K. John, CEngage Learning 3.Digital System Design with VHDL, Second edition, Mark Zwolinski, Pearson Education, 2004
Examination Detail

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Midterm Exam (online modalities)	Yes/No: Yes Combine Separate: NA Duration: TBD based on practical modalities Preferred Date: TBA Exam Specifications: TBA
Final Exam (online modalities)	Yes/No: Yes Combine Separate: NA Duration: TBD based on practical modalities Exam Specifications: TBA

Prepared by:	**Dr. Shahid Masud**
Date:	**Updated: 19 July 2023**