Lahore University of Management Sciences

CS/EE-220 Digital Logic Circuits

Spring 2024

Course Catalog Description
This course focuses on the principles and practices of Digital Logic Circuit Design and is a first course in this area. Topics covered include: Boolean Algebra, Number Systems, Logic Gates, Logic Technologies, DRAM, SRAM, ROM, Inverters, Circuit Implementation of Logic Gates, Speed of Logic Gates and Operating Frequencies, Logic implementation of Boolean expressions, Karnaugh Maps, Analysis and Design of Combinational Logic Circuits, Analysis and Design of Sequential Logic Circuits, Circuits for Arithmetic Calculations, Circuits using memories and Flip-Flops, Registers and Register files, State-Machines, Memory Systems, Basic Processor and Control Unit Design.

Course Details	
Credit Hours	3
Core	BS EE
Elective	For all LUMS students
Open for Student Category	
Closed for Student Category	

Course Prerequisite(s)/Co-Requisite(s)
Pre-requisites: None Co-requisites: None

Course Offering Details						
Lecture(s)	No. of Lec(s) Per Week	2	Duration	75 min	Timings and Venue	
Recitation (per week)	No. of Rec (s) Per Week	X	Duration			
Lab (if any) per week	N0. of Session(s) Per Week	X	Duration			
Tutorial (per week)	N0. of Tut(s) Per Week	X	Duration			

Instructor	Dr. Jahangir Ikram
Room No.	317
Office Hours	TBA
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Secretary/TA	TBA
TA Office Hours	Mentioned on LMS
Course URL (if any)	LMS will be used

Course Learning Outcomes	
	The students should be able to:

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CLO1	Develop and Apply Basic Knowledge in Number Systems, Boolean Algebra
CLO2	Analyze complex Combinational Logic Circuits
CLO3	Design complex combinational Logic Circuits
CLO4	Analyze complex Sequential Logic Circuits
CLO5	Design complex Sequential Logic Circuits

Relation to EE Program Outcomes

EE-220	Related PLOs	Level of Learning	Teaching Methods	CLO Attainment checked in
CLO1	PLO1	Cog-3	Instruction, Assignments	Midterm, Final
CLO2	PLO2	Cog-4	Instruction, Assignments	Midterm, Final
CLO3	PLO3	Cog-5	Instruction, Assignments	Midterm, Final
CLO4	PLO2	Cog-4	Instruction, Assignments	Midterm, Final
CLO5	PLO3	Cog-5	Instruction, Assignments	Midterm, Final

Grading Breakup and Policy

CEP:	10% (5% CEP, 5% CEP Viva)
Quizzes (8):	20%
Assignments (4):	15%
Midterm Exam:	22%
Final Examination:	33%

Course Overview

Lecture	Topics	Recommended Readings	CLO Covered
1.	Course introduction and DLC basics	Chap-1 (MM[1])	CLO 1
2.	Number Systems, Arithmetic Operations, Standard Codes	Chap-1 (MM[1])	
3.			
4.	Logic Gates, Boolean Algebra, Truth Tables and K-Maps	Chap-2 (MM[1])	
5.			
6.			
7.			
8.			
9.	Combinational Circuits: Analysis and Design, Multiplexers, Decoders	Chap-3 (MM[1]) Chap-4 (MM[1])	CLO2, CLO3
10.			
11.			
12.			
13.	Sequential Circuits: Introduction to Latches and Flip-Flops, Sequential Circuits Analysis	Chap-5 (MM[1])	CLO 4
14.			
Midterm Exam			

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15. 16. 17.	Sequential Circuits: Sequential Circuits Design: State Diagrams and State Tables	Chap-5 (MM[1])	CLO 5
18. 19. 20. 21.	Registers and Counters: Shift Registers, Parallel Loading of Registers, Synchronous and Asynchronous Counters	Chap-7 (MM[1])	CLO2 - CLO5
22.	ROM, Combinational Logic Circuit Design through ROM	Chap-6 (MM[1])	
23. 24.	Random Access Memory (RAM), Memory Decoding	Chap-8 (MM[1])	
25.	Register Transfer Operations, Buses	Chap-7 (MM[1])	
26. 27. 28.	Intro to Processor: Arithmetic Logic Unit (ALU) and Control Unit	Chap-9 (MM[1])	
Final Exam			

Textbook(s)/Supplementary Readings
[1] Textbook: "Logic and Computer Design Fundamentals" by M. Morris Mano & Charles R. Kime, 4th Edition, 2008, (Prentice Hall Inc.) [2] Reference Book1: "Digital Fundamentals" by Thomas L. Floyd, 10th Edition (Pearson) [3] Reference Book2: "Digital Systems (Principles and Applications)" by Ronald J. Tocci, Neal S. Widmer & Gregory L. Moss, 10th Edition (Pearson)

Examination Detail	
Midterm Exam	Yes/No: **Yes**
Final Exam	Yes/No: **Yes** Combine / Separate: **Combine** Duration: 3:00 hrs Exam Specifications: Closed Book, Closed Notes, Calculator Allowed

Prepared by:	**Dr. Jahangir Ikram**
Date:	**December 12, 2023 (updated)**