Advanced VLSI Design
Exercise 03
Assignments

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Assignments

1. Apply the same setting for qhsim as in Exercise 02. Create a new directory, create a new project, implement and compile two Verilog files: one Verilog file with a multiplexer and one Verilog file with the testbench for the multiplexer. Apply the same sequence in the port declaration as in the VHDL description of Exercise 02.
2. Simulate the Verilog multiplexer and exit `qhsim`.
3. Create a new directory and copy the file(s) of the VHDL multiplexer of Exercise 02 and the Verilog testbench for the multiplexer from (1) of this assignment.
   Open `qhsim`, open a new project, add the VHDL multiplexer and the Verilog testbench, compile and simulate.
   The Verilog testbench should instantiate in Verilog the VHDL multiplexer by its entity name, where Verilog `reg` should be assigned to VHDL `input ports` and Verilog `wire` to VHDL `output ports`.

   Example:
   The following VHDL entitiy
   "`entity my_e (a: in std_logic; b: in std_logic; c: out std_logic); end my_e;`"
   has to be instantiated in Verilog as
   "

   ```
   …
   reg x, y; wire z;
   …
   my_e (x, y, z);
   …
   ```

   "
   Instead, you can also use "`my_e (.a(x), .b(y), .c(z));`".