ANJUMAN - I - ISLAM'S
A. R. KALSEKAR
POLYTECHNIC, NEW PANVEL
ISO 9001:2015 CERTIFIED
Symbol of Secularism & National Integration
DTE Institute Code 3278 Raigad District
Approved by : All India Council for Technical Education (A.I.C.T.E.)
Recognized by : Directorate of Technical Education (D.T.E.) & Govt. of Maharashtra
Affiliated to : Maharashtra State Board of Technical Education (M.S.B.T.E.)
Vision : To be the most sought-after Polytechnic that others would wish to emulate.
Mission : Creating Exuberant Technical Professionals

A Micro-Project Report on

Analyze the fuctional block of 8086 microprocessor

Submitted on : /04/2023

By

1. Adil Faridi

2. Tanishq Maske

3.

4.

Under Guidance of

Hafsah Ma'am

In

Three Years Diploma Program in Engineering & Technology of Maharashtra State Board of Technical Education, Mumbai (Autonomous)

ISO 9001 : 2015

At

Anjuman-I-Islam's Abdul Razzaq Kalsekar Polytechnic

Academic Year (2022-2023)

MAHARASHTRA STATE BOARD OF TECHNICAL EDUCATION, MUMBAI

Certificate

This is to certify that Mr. /~~Ms./Mrs.~~ **Mohd Adil Faridi**

Enrollment No: **2105690148** of **4th** **Semester** of **Diploma in Computer Engineering** at **Anjuman I Islam's Abdul Razzak Kalsekar Polytechnic,** has completed the **Micro Project** satisfactorily in Subject **MIC** in the academic year 20**22** - 20**23** as per the MSBTE prescribed curriculum of I Scheme.

Place:

Date: / /2022

Enrollment No: **2105690148**

Exam Seat No:

Project Guide **Head of the Department** **Principal**

Head of Institute

MAHARASHTRA STATE BOARD OF TECHNICAL EDUCATION, MUMBAI

Certificate

This is to certify that Mr. /~~Ms./Mrs.~~ **Tanishq Maske**

Enrollment No: **2205690384** of **4th** **Semester** of **Diploma in Computer Engineering** at **Anjuman I Islam's Abdul Razzak Kalsekar Polytechnic,** has completed the **Micro Project** satisfactorily in Subject **MIC** in the academic year 20**22**-20**23** as per the MSBTE prescribed curriculum of I Scheme.

Place:

Date: / /2022

Enrollment No: **2205690384**

Exam Seat No: _____

Project Guide **Head of the Department** **Principal**

Head of Institute

MAHARASHTRA STATE BOARD OF TECHNICAL EDUCATION, MUMBAI

Certificate

This is to certify that Mr. /~~Ms./Mrs.~~ _____

Enrollment No: _____ of 4th **Semester** of **Diploma in Computer Engineering** at **Anjuman I Islam's Abdul Razzak Kalsekar Polytechnic,** has completed the **Micro Project** satisfactorily in Subject MIC in the academic year 2022 - 2023 as per the MSBTE prescribed curriculum of I Scheme.

Place: Enrollment No: _____

Date: / /2022 Exam Seat No: _____

Project Guide **Head of the Department** **Principal**

Head of Institute

MAHARASHTRA STATE BOARD OF TECHNICAL EDUCATION, MUMBAI

Certificate

This is to certify that Mr. /~~Ms./Mrs.~~ _____

Enrollment No: _____ of 4th **Semester** of **Diploma in Computer Engineering** at **Anjuman I Islam's Abdul Razzak Kalsekar Polytechnic,** has completed the **Micro Project** satisfactorily in Subject MIC in the academic year 2023 - 2023 as per the MSBTE prescribed curriculum of I Scheme.

Place: Enrollment No: _____

Date: / /2022 Exam Seat No: _____

Project Guide **Head of the Department** **Principal**

Head of Institute

INDEX

Introduction

The microprocessor is the main component of the computer where 8086 is the base of all upward developed processors till current processors.

This course will cover the basics of 8086 and its architecture along with instruction set, assembly language programming with effective use of the procedure, and macros. This course also covers architectural issues such as instruction set programs and data types.

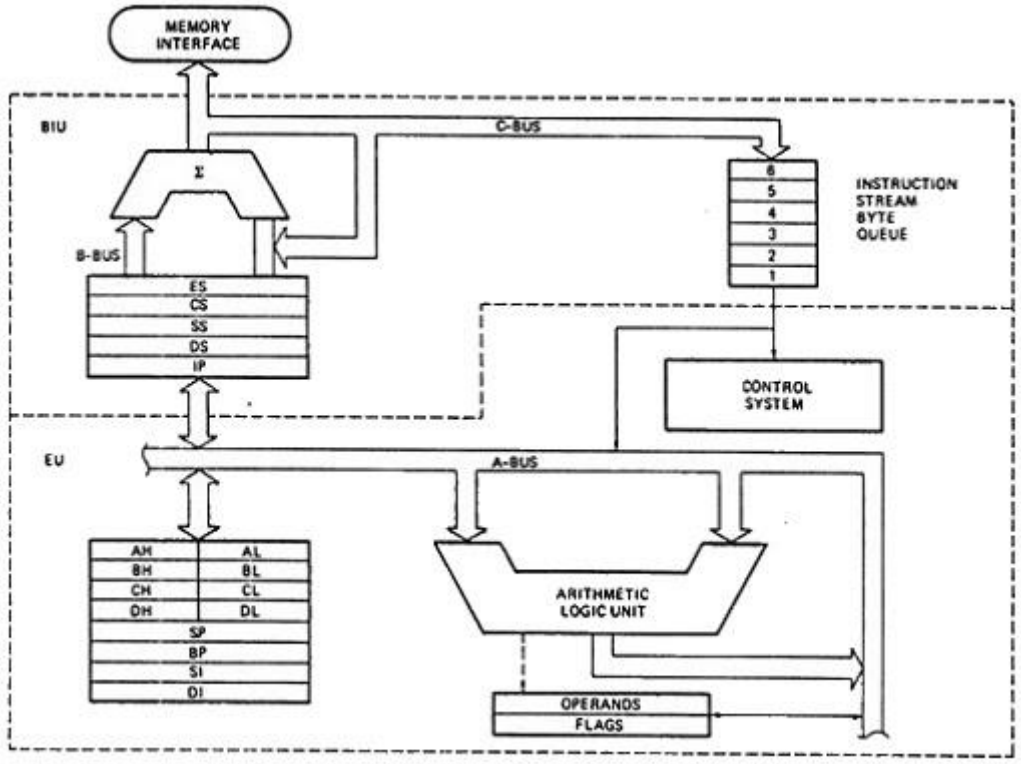
On top of that, the students are also introduced to the increasingly important area of parallel organization. This subject serves as a basis to develop hardware-related projects. This course will enable the students to inculcate assembly language programming concepts and methodology to solve problems.

Brief Description

The 8086 is a sixteen-bit microprocessor. The term sixteen-bit means that its arithmetic logic unit, its inner registers, and the maximum of its commands are meant to work with sixteen-bit binary statistics.

The 8086 has a sixteen-bit statistics bus, so it may read data from or write data to memory and ports both sixteen bits or eight bits at a time. The 8086 has a 20 bit deal with bus, so it may deal with any one of 220, or 1,048,576 memory locations.

8086 CPU is split into 2 unbiased useful components to hurry up the processing specifically BIU (Bus interface unit) & EU (execution unit).



The functional block diagram of 8086 is split into functional units.
(1) Bus Interface Unit and (2) Execution Unit

They are defined below.
1. Bus Interface Unit:
Bus Interface Unit is a gate (enhance) interface among peripheral devices and processors. Through the bus interface only, the processor can transfer and obtain data. The bus interface unit contains

(a) Instruction Queue
(b) Segment Registers
(c) Instruction Pointers

(a) Instruction Queue

In 8086 Processor, the instruction queue is a six-byte register used to keep everlasting data from the Input/Output (I/O) devices or processor. The queue operates withinside the precept of First In First Out (FIFO) precept. i.e., the primary data is fetched, and data might be taken out first.

(b) Segment Register:

In the 8086 Processor, there are 4 phase registers. They are

ES - Extra Segment
CS - Code Segment
DS - Data Segment
SS - Stack Segment

The most memory access of the 8086 processor is 1 MB. Each section has a few predefined functions.
In the 8086 processor, every phase has a potential of sixty-four KB. So the 4 segments will save 256 KB of memory places. The remaining memory places are free and in those places, the user can carry out every other process. These 4 phase registers will preserve the bottom address of the corresponding section.

(c) Instruction Pointer (IP):

The instruction pointer will deliver the subsequent address of the instruction to be executed. Instruction Point can't be used for different purposes.

2. Execution Unit:

The execution unit contains

(a) Control Unit

(b) Instruction Decoders

(c) ALU

(d) General Purpose Registers

(e) Flag Registers

Address Generation:

The I/O processor can acquire data from the memory only if those data have to is going out via the address generation.

General Purpose Registers:

AX, BX, CX, DX, SP, BP, SI, DI are General Purpose Registers.

1. AX register (Accumulator):

AX register can keep sixteen-bit data only.

2. BX register:

BX register is the bottom register. It is used to keep the bottom data (value).

3. CX register:

CX register is a code register (Count Register)

4. DX Register:

DX register is the data register. DX register is used to store data.

5. SP (Stack Pointer):

Stack Pointer maintains the top of the stack. The stack pointer operates withinside the principle of Last In First Out (LIFO). Since one region can store only eight-bit data, with the purpose to store sixteen-bit data, memory places are needed. So the stack pointer will decrease via way of means of memory places if data is taken.

6. BP (Base Pointer):

A base pointer is used to keep the base address of the memory or stack.

7. SI (Source Index):

Source Index is used to keep the index value of the supplied operand for string instructions.

8. DI (Destination Index):

DI is used to maintain the index value of the destination operand for string instructions.

General cause registers are used for containing data, intermediate results, counters, mode of address, and additionally for storing powerful addresses.

Flag Registers:

The 3 control flags are,

1. Trap Flag (TF)

2. Interrupt flag (IF)

3. Direction Flag (DF)

1. Trap Flag (TP):

It is used for single-step control.

It lets the user execute one guidance of program at a time for debugging.

When entice flag is set, the program may be run in unmarried step mode.

2. Interrupt Flag (IF):

It is an interrupt enable/disable flag.

If it's far set, the maskable interrupt of 8086 is enabled and if it's far reset, the interrupt is disabled.

It may be set with the aid of using executing guidance take a seat down and may be cleared with the aid of using executing CLI instruction.

3. Direction Flag (DF):

It is utilized in string operation.

If it's far set, string bytes are accessed from a better reminiscence address to decrease the memory address.

When it's far reset, the string bytes are accessed from decreased memory address to a better memory address.

APPLICATION

Intel 8086 microprocessor is the improved model of the Intel 8085 microprocessor. It turned into the design with the aid of using Intel in 1976. The 8086 microprocessor is a16-bit, N-channel, HMOS microprocessor. Where the HMOs are used for "High-speed Metal Oxide Semiconductor".

CONCLUSION

The microprocessor is the main component of the computer where 8086 is the base of all upward developed processors till current processors.

This course will cover the basics of 8086 and its architecture along with instruction set, assembly language programming with effective use of the procedure, and macros.

This course also covers architectural issues such as instruction set programs and data types.

REFERENCE

1. https://www.msbtemicroproject.tech/2022/03/Microprocessors-22415-Diploma-Micro-Project-I-Scheme-MSBTE.

2. https://www.google.com