

Sir Syed University of Engineering & Technology, Karachi

Department of Computer Science
3rd Semester, Batch 2019
Comprehensive Assignment

Dear Students,

You are given a comprehensive assignment attached herewith as suggested by the Honourable Vice Chancellor as per university policy.

The questions given, cover most of the major topics included in your curriculum, that will help you out in developing your skills to complete the given task within the specified time.

You are encouraged to attempt all the questions and not to share your work with your fellow students, however share of knowledge through any possible way of communications will highly be appreciated.

Sooner or later, you may be assigned one more task that may cover the minor topics too.

In case of any difficulty, you may approach me through your CRs. Moreover, I would suggest you to show all the necessary steps/work done.

I wish you good luck and suggest you to stay home during your vacations as suggested by the Government of Pakistan also, until the situation returns to normal.

The assignments may be submitted by the **17th of April, 2020** through email to the following address:

LDSTASSIGNMENTS@HOTMAIL.COM

The email address given, may not be used for any other sort of communication, however only assignments may be submitted to the above-mentioned email address.

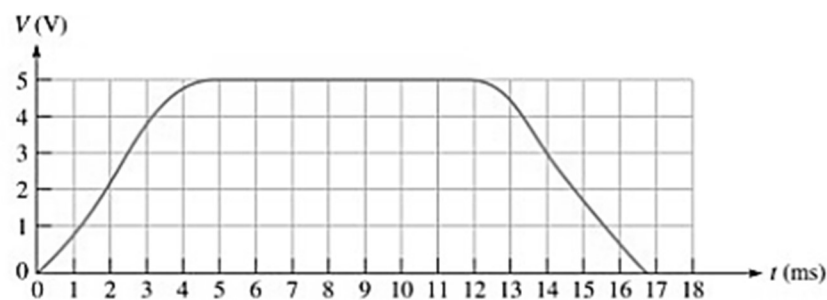
Please, mention your Roll Number as 2019-CS-XYZ in subject field. Only PDF format is acceptable and questions must be attempted in order. PDF file must also be named as 2019-CS-XYZ. No late submitted assignments will be considered.

Sir Syed University of Engineering & Technology, Karachi

Department of Computer Science
3rd Semester, Batch 2019
Comprehensive Assignment

Digital Fundamental Concepts and Number System:

- Q1. Give an example of a system that is analog and one that is a combination of both digital and analog. Name a system that is entirely digital.
- Q2. A periodic digital waveform has a pulse width of 35 μs and a period of 210 μs . Determine the frequency and the duty cycle.
- Q3. For the pulse shown in the following Figure, graphically determine the following:
- (a) Rise time (b) fall time (c) pulse width (d) amplitude



(Hint: The bottom 10% and the top 10% of the pulse are not included in the rise and fall times because of the nonlinearities in the waveform in these areas. The pulse width (t_{IV}) is a measure of the duration of the pulse and is often defined as the time interval between the 50% points on the rising and falling. The bottom 10% and the top 10% of the pulse are not included in the rise and fall times because of the nonlinearities in the waveform in these areas. The pulse width is a measure of the duration of the pulse and is often defined as the time interval between the 50% points on the rising and falling)

- Q4. List the octal and hexadecimal numbers from 8 to 64. Using A and B for the last two digits, list the numbers from 4 to 32 in base 12.
- Q5. What is the exact number of bytes in a system that contains (a) 32K bytes, (b) 64M bytes and (c) 6.4G bytes?
- Q6. Convert the following numbers with the indicated bases to decimal:
(a) $(4230)_5$ (b) $(1A8)_{12}$ (c) $(735)_8$ (d) $(452)_6$
- Q7. What is the largest binary number that can be expressed with 16 bits? What are the equivalent decimal and hexadecimal numbers?
- Q8. Determine the base of the numbers in each case for the following operations to be correct:
(a) $14/2 = 5$ (b) $54/4 = 13$ (c) $24 + 17 = 40$.
- Q9. The solutions to the quadratic equation $x^2 - 11x + 22 = 0$ are $x = 3$ and $x = 6$. What is the base of the numbers?

Sir Syed University of Engineering & Technology, Karachi

Department of Computer Science
3rd Semester, Batch 2019
Comprehensive Assignment

- Q10. Convert the hexadecimal number 73DC to binary, and then convert it from binary to octal.
- Q11. Convert the decimal number 523 to binary in two ways: (a) convert directly to binary; (b) convert first to hexadecimal and then from hexadecimal to binary. Which method is faster?
- Q12. Express the following numbers in decimal:
(a) $(10110.0101)_2$ (b) $(16.5)_{16}$ (c) $(26.24)_8$ (d) $(DADA.B)_{16}$
(e) $(1010.1101)_2$

Boolean Algebra and Logic Gates:

- Q13. Simplify the following Boolean expressions to a minimum number of literals:

(a) $ABC + \overline{A}B + ABC$ (b) $\overline{X}YZ + XZ$
(c) $\overline{(X+Y)}(\overline{X} + \overline{Y})$ (d) $XY + X(WZ + \overline{WZ})$
(e) $(B\overline{C} + \overline{A}D)(A\overline{B} + C\overline{D})$ (f) $(\overline{A} + \overline{C})(A + \overline{B} + \overline{C})$

- Q14. Reduce the following Boolean expressions at their most:

(a) $\overline{A}\overline{C} + ABC + A\overline{C}$
(b) $\overline{(\overline{X}\overline{Y} + Z)} + Z + XY + WZ$
(c) $\overline{A}B(\overline{D} + \overline{C}D) + B(A + \overline{A}CD)$
(d) $(\overline{A} + C)(\overline{A} + \overline{C})(A + B + \overline{C}D)$
(e) $AB\overline{C}D + \overline{A}BD + ABCD$

- Q15. Find the complement of $F = AB + CD$; then show that $F\overline{F} = 0$ and $F + \overline{F} = 1$.

- Q16. Draw logic diagrams to implement the following Boolean expressions:

(a) $A = [(U + \overline{X})(\overline{Y} + Z)]$
(b) $B = (\overline{u \oplus y}) + x$
(c) $C = (\overline{U} + \overline{X})(Y + \overline{Z})$

- Q17. Show that the dual of the exclusive-OR is equal to its complement.

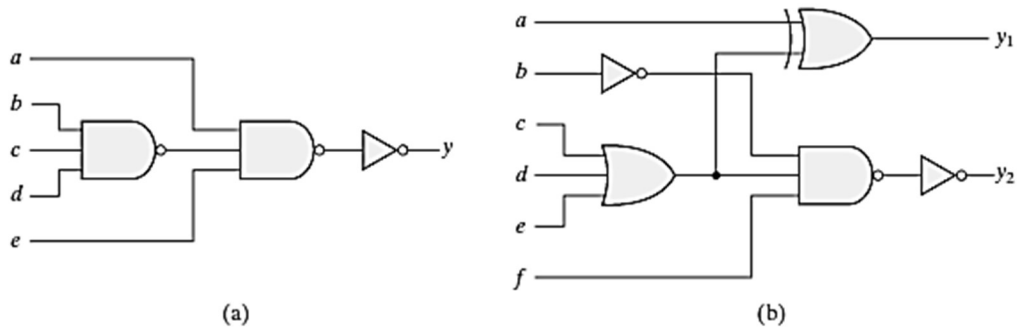
- Q18. Determine whether the following Boolean equation is true or false.

$$\overline{x}\overline{y} + \overline{x}z + \overline{x}\overline{z} = \overline{x}\overline{z} + y\overline{z} + \overline{x}z$$

Sir Syed University of Engineering & Technology, Karachi

Department of Computer Science
3rd Semester, Batch 2019
Comprehensive Assignment

- Q19. Write Boolean expressions and construct the truth tables describing the outputs of the circuits described by the logic diagrams in the following Figures (a) and (b).



- Q20. Write the following Boolean expressions in sum of products form:

$$(B + D)(\bar{A} + \bar{B} + C)$$

- Q21. Write the following Boolean expression in product of sums form:

$$\bar{A}B + \bar{A}\bar{C} + ABC$$

- Q22. Simplify the following Boolean functions into a sum-of-products form using Karnaugh's Map. (Hint: Firstly, convert the given function to Standard-SOP form)

a. $F(x, y, z) = \sum (0, 2, 4, 5, 6)$

b. $F(x, y, z) = \sum (3, 4, 6, 7)$

c. $F(A, B, C) = \sum (1, 2, 3, 5, 7)$

d. $F(w, x, y, z) = \sum (0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$

e. $F(A, B, C, D) = \sum (0, 2, 3, 5, 7, 8, 9, 10, 11, 13, 15)$

- Q23. Simplify the following Boolean functions into a product-of-sums form using Karnaugh's Map. (Hint: Firstly, convert the given function to Standard-POS form)

a. $F(A, B, C, D) = \sum (0, 1, 2, 5, 8, 9, 10)$

b. $F(x, y, z) = \sum (1, 3, 4, 6)$

c. $F(x, y, z) = \sum (1, 2, 3, 4, 5, 7)$

d. $F(w, x, y, z) = \sum (2, 3, 12, 13, 14, 15)$

e. $F(A, B, C, D) = \sum (3, 7, 11, 13, 14, 15)$

Sir Syed University of Engineering & Technology, Karachi

Department of Computer Science
3rd Semester, Batch 2019
Comprehensive Assignment

Q24. Construct the following function using basic logic gates only.

$$\overline{(A \oplus B) \oplus C}$$

Q25. Design a combinational circuit with three inputs and one output. The output is equal to logic- 1 when the binary value of the input is a prime number*. The output is logic- 0 otherwise.

Q26. A majority gate** is a digital circuit whose output is a logic- 1 if the majority of the inputs are a 1 otherwise the output is a logic- 0. Design a logic circuit for a 3-input majority gate.

* a number that is divisible only by itself. Zero is not prime, since it has more than 2 divisors.

** a majority gate returns true if and only if more than 50% of its inputs are true.

Combinational logic:

Q27. Determine the sum (Σ) and the output carry (C_{OUT}) of a half-adder for each set of input bits:

(a) 01 (b) 00 (c) 10 (d) 11

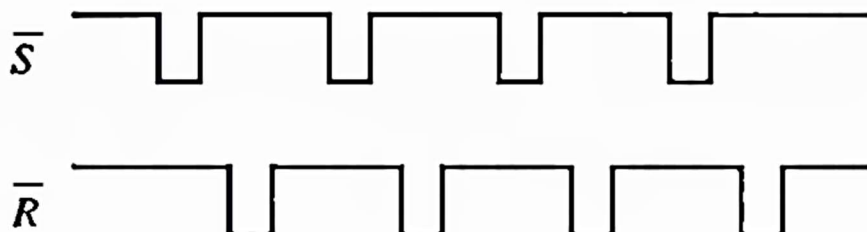
Q28. A full-adder has $C_{in} = 1$. What are the sum (Σ) and the output carry (C_{OUT}), when $A = 1$ and $B = 0$?

Q29. Two 4-bit numbers (1010 and 1001) are applied to a 4-bit parallel adder. The input carry is 1. Determine the sum (Σ) and the output carry.

Sequential Logic:

Q30.

(a) If the waveforms in the following figure are applied to an active-LOW input S-R latch, draw the resulting Q output waveform in relation to the inputs. Assume that Q is initially LOW.



Sir Syed University of Engineering & Technology, Karachi

Department of Computer Science

3rd Semester, Batch 2019

Comprehensive Assignment

- (b) If the waveforms in the following figure are applied to an active-HIGH input S-R latch, draw the resulting Q output waveform in relation to the inputs. Assume that Q is initially HIGH this time.

