Floating Point Unit on RISC-V

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Abstract

The RISC-V architecture of a CPU requires specific modules to compute mathematical operations using regular and floating-point numbers. An ALU covers the standard non-floating numbers. However, an FPU (Floating-Point-Unit) is needed for floating-point calculations, which run parallel with ALU. The FPU we are working on is rated for the 32-bit architecture of the single-precision RISC-V standard. It follows IEEE-754 standard floating-point numbers, which consist of 32 bits. The most significant bit is the sign, the next eight are the exponential, and the last 23 are the mantissa. The FPU will consist of 5 operations, which are also sub-modules. Those sub-modules are addition, subtraction, multiplication, and conversion between formats.

We first researched a variety of research papers to understand the concept of floating-point units on RISC-V. Next, we worked on the RTL diagram for the adder and subtractor module, which we later implemented in System Verilog with the guidance of our mentor. To ensure correctness between the modules, we created and verified testbenches for each module with Verilator and FuseSoC. Our expected results are that two floating point values can be added and subtracted without truncating any values in the RISC-V architecture.

Our goal was to accurately add and subtract two floating point values without truncation in RISC-V architecture. Our work demonstrates the feasibility of implementing a single-precision, 32-bit IEE-754 compliant FPU for RISC-V architecture, which can enhance CPU performance in floating-point computations. This lays the groundwork for further optimizations in FPU design for open-source architectures like RISC-V.

Introduction

RISC-V, an open-source CPU architecture, is gaining popularity due to its adaptability. However, it currently lacks a dedicated unit for floating-point calculations, which are essential for tasks in scientific computing, data analysis, and engineering. While the ALU in RISC-V handles integer operations, floating-point computations require a specialized unit to ensure precision and prevent performance loss.

To address this, our project focuses on creating a 32-bit, single-precision Floating-Point Unit (FPU) that follows the IEEE-754 standard. This FPU is designed to perform addition, subtraction, multiplication, and format conversions, providing essential functionality for floating-point operations. Using System Verilog for implementation and tools like Verilator and FuseSoC for verification, we aim to integrate this FPU with the ALU to enhance RISC-V's capabilities, supporting more complex computational tasks in open-source environments.

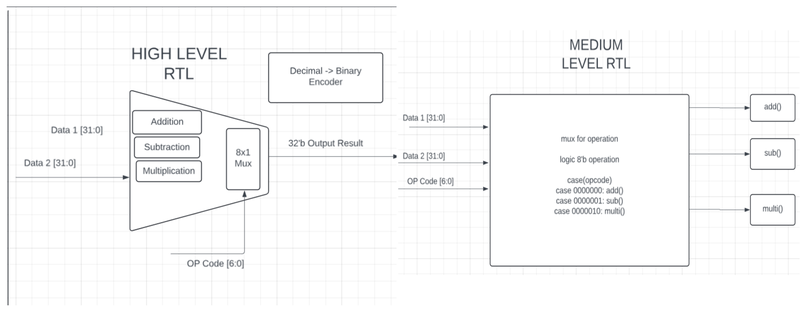

Figure A : High-Level and Medium-Level RTL Representation for Arithmetic Operations

Our Research

First, we worked on designing how the FPU ALU would be conducted. This consisted of creating RTLs for the adder, subtractor, multiplicator, divider, and beyond. As of now, we have concentrated on the adder and subtractor for a foundation of understanding FPU. As seen in Figure A, two different 32-bit data streams are inputted into the system According to the opcode, the MUX would decide which operation to use. Based on the operation, a certain module would be addressed, such as add() or sub().

When it comes to the 32 bits that are inputted into the add() or sub() modules, there are different sections of the whole data stream that undergo different processes. For instance, the first 23 bits go under a "fractional adder" or "fractional subtractor" (Figure C, Figure D). The reason for this is that the system needs to know which of the data streams is the larger value, which is consisted in the most significant 23 bits. This way, we can effectively find the difference between the two data streams without having to worry about negative numbers as negative numbers are not prevalent in RISC-V architecture. Finding the difference is important because this information tells us how many bits we should shift the mantissa of the smaller data stream, which is the least significant 9 bits. This shifting is how the exponents are added or subtracted in FPU.

Testing the design on FuseSOC requires the incorporation of core files in system verilog (Figure B). This consisted of trial and error as there were complications with the Makefile. The testbench on the other hand consists of multiple test cases that test each module (Figure E). There are cases of two different data streams, including cases that require two's complement. Suppose the output of the module does not match the expected output for the corresponding opcode, then there will be an error message that signifies the expected output along with the two included data streams. This form of testing makes it easier to detect which test case is failing. Finding the error is shown in the waves on GTKWave (Figure F). We would track the mantissa and difference between the two data streams to determine where and why the miscalculation occurred. In some instances, depending on the edge case, the mantissa would not shift enough bits or the expected difference would be incorrect. Tracking the bits on the waves assist in modifying the system verilog code to yield a correct output.

```
socet211@asicfab:~/FPU/core (fpu_fa24)$ fusesoc --cores-root . list-cores

Available cores:

Core                              Cache status  Description
================================================================================
socet:fpu_adder_file:1.0.0:0      :     local : FPU adder
socet:fpu_subtractor_file:1.0.0:0 :     local : FPU subtractor
socet211@asicfab:~/FPU/core (fpu_fa24)$
```

Figure B: The Incorporation of Core Files

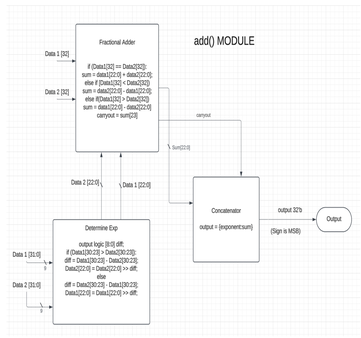

Figure C: Low-Level RTL of add() module

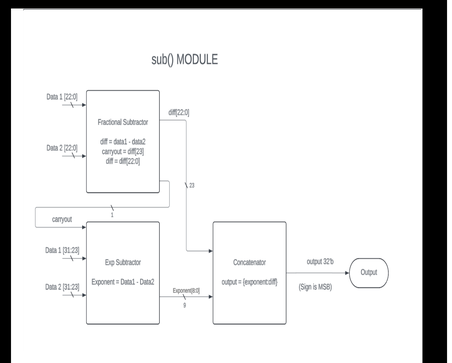

Figure D: Low-Level RTL of sub() module

```
//POS POS no carry
tb_data1 = 32'b01000010110010000110011001100110; // 100.2
tb_data2 = 32'b01000010101110101000000000000000; // 90.5
if(result != 32'b01000011001111101011001100110011) begin
    $display("Wrong output, actual value 190.7")
end

//POS POS with carry
tb_data1 = 32'b01000010010010011001100110011010; // 50.4
tb_data2 = 32'b01000010110010011001100110011010; // 100.8
if(result != 32'b01000011000101110011001100110011) begin
    $display("Wrong output, actual value 151.2")
end
```

Figure E: Testbench for sub() module

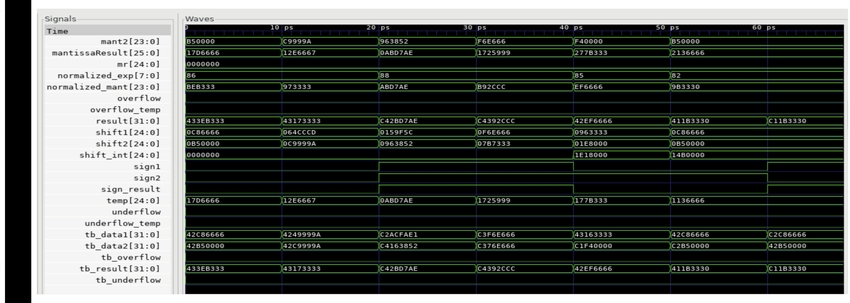

Figure F: Simulation of add() through GTKWave

Future Plans

In the future, we plan to extend the functionality of our Floating-Point Unit (FPU) by implementing and refining the multiplication and division modules, as well as adding a square root operation. These additional modules will further expand the computational capabilities of the FPU, enabling it to handle a broader range of mathematical operations in scientific and engineering contexts. For accurate handling, we aim to thoroughly test these modules against edge cases such as extreme values (e.g., max/min exponent and mantissa), subnormal numbers, and rounding scenarios, which are crucial for compliance with the IEEE-754 standard. Additionally, we will focus on optimizing the latency and area of each module to achieve a balance between performance and resource efficiency, essential for embedding the FPU in open-source RISC-V architectures without compromising scalability. We also intend to explore error detection and correction mechanisms to improve reliability in scenarios with high computational demands. Lastly, as RISC-V continues to evolve, we will examine potential enhancements to our FPU's design for compatibility with future versions of the architecture and support for double-precision floating-point calculations.

References

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