STOPWATCH CONSISTING OF LAP OPTION

SUBMITTED BY :-

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AIM: To design a stopwatch consisting of lap option.

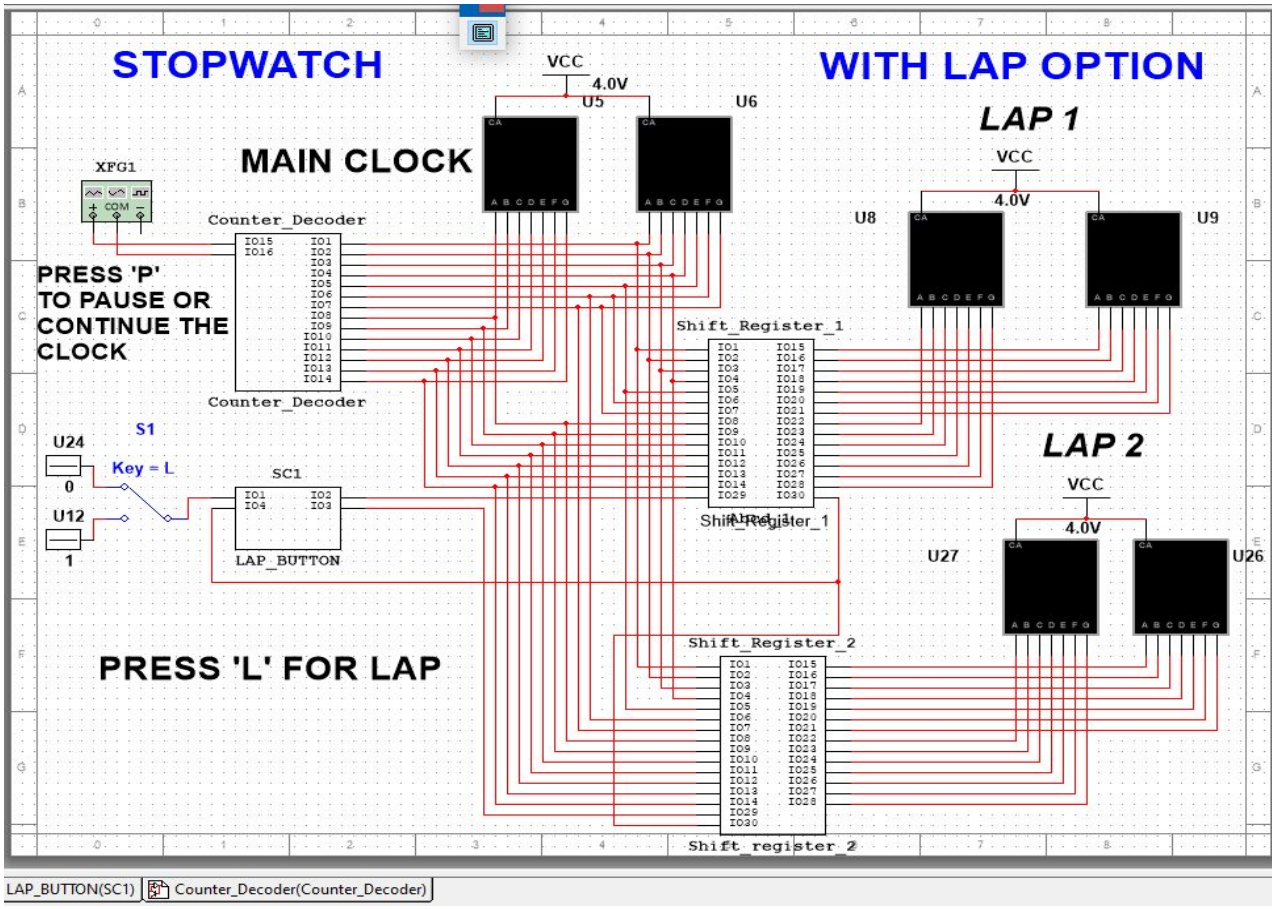
COMPONENTS REQUIRED

Sr .no	COMPONENTS	REQUIREMENT	DATASHEETS
1.	**IC 7408N**	**8**	**https://drive.google.com/file/d/1PCW9aLAiGBcsusWtOF_Yn9CsueWtX9Fd/view?usp=drivesdk**
2.	**IC 7490N**	**2**	**https://drive.google.com/file/d/1Oo8ZGcv_5lloG6SPunKLeayoF6OFyUxg/view?usp=drivesdk**
3.	**IC 7447N**	**2**	**https://drive.google.com/file/d/1Omh-JS_T2BeOcdsuXIdx3yu8VYa8QPJY/view?usp=drivesdk**
4.	**IC 74199N**	**5**	**https://drive.google.com/file/d/1PCSFjiPhepI8QnFzswL0vFR6DGTVbTFg/view?usp=drivesdk**
5.	**IC 7404N**	**2**	**https://drive.google.com/file/d/1PGQF7MxFYQJAjP_6k1xYZPDjQSt981KA/view?usp=drivesdk**
6.	**Function generator**		

INTRODUCTION:

In this project we have made a stopwatch that measures the amount of time(in seconds) elapsed between its activation and deactivation. The maximum time which can be measured is 60 seconds(1 minute). Laps in time can also be recorded which will be displayed using the 7 segment display.
In our project we have provided 2 lap options.

CIRCUIT DIAGRAM



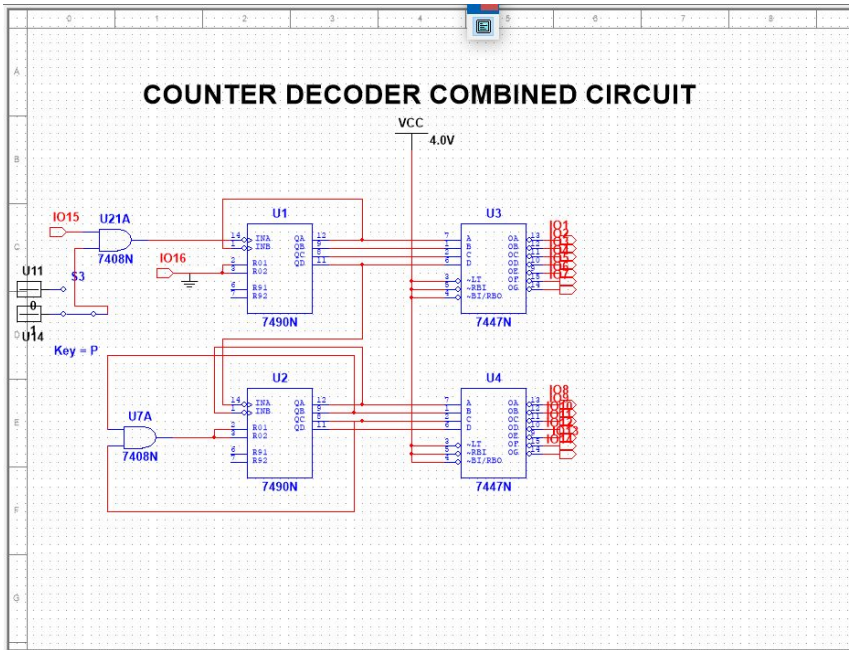
CIRCUIT EXPLANATION:

For the sake of explanation,we have divided our project in 3 subdivisions :

- COUNTER AND DECODER
- SHIFT REGISTER
- LAP BUTTON

COUNTER AND DECODER

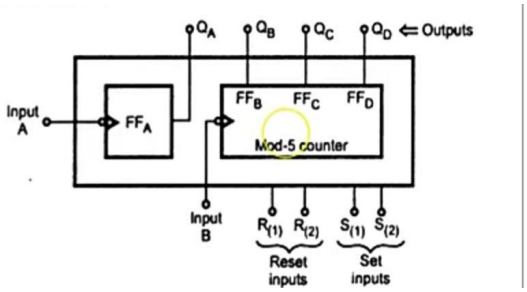
The internal circuit of counter and decoder is:



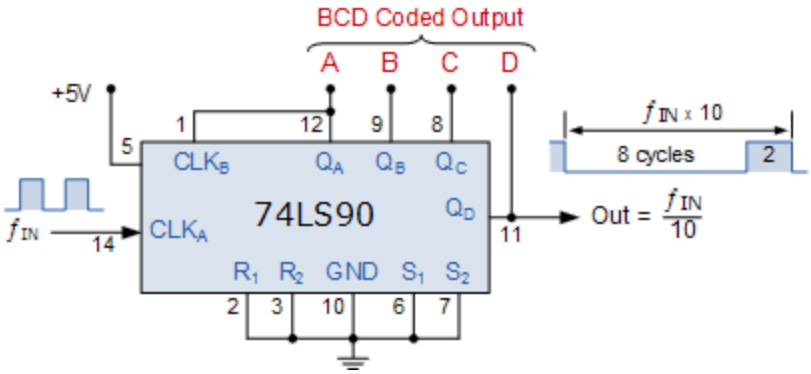
In our counter as shown in the figure IC U1 is used as a MOD 10 counter which counts from 0 to 9 whereas the second IC U2 is used as MOD 7 counter which counts from 0to 6. The additional input pins R1 and R2 are counter "reset" pins which reset the counter back to 0000, while input pins S1 and S2 are connected to logic 1 that " set" the counter to maximum count. The output QA is connected to input B for cascading the first flip-flop to Mod 5 counter

P BUTTON : P button controls the clock pulse which is input to the counter.When there is no clock pulse i.e P button is in "OFF" mode the counter stops counting and represents its previous (memory) state.When it is "ON" the counter starts counting again from the previous stores state.

BLOCK SCHEMATIC OF IC 7490



IC 7490 as MOD 10 counter:

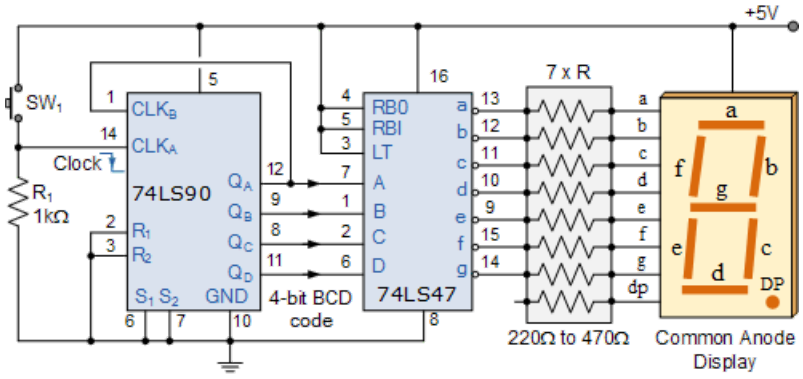


IC 7490 as MOD 7 counter:

The QA and QB is connected to the AND gate (7408N) and its output is given to reset pins . When QA=QB=QC=1 i.e 7 ,QA given to the input B and the output of the AND gate to reset pins resets the flip flop to 0000. Thus the counter counts from 0 t0 6. The output of 1st IC "QD" is given to the clock input A of the second IC .

IC 7447 BCD to 7 segment driver

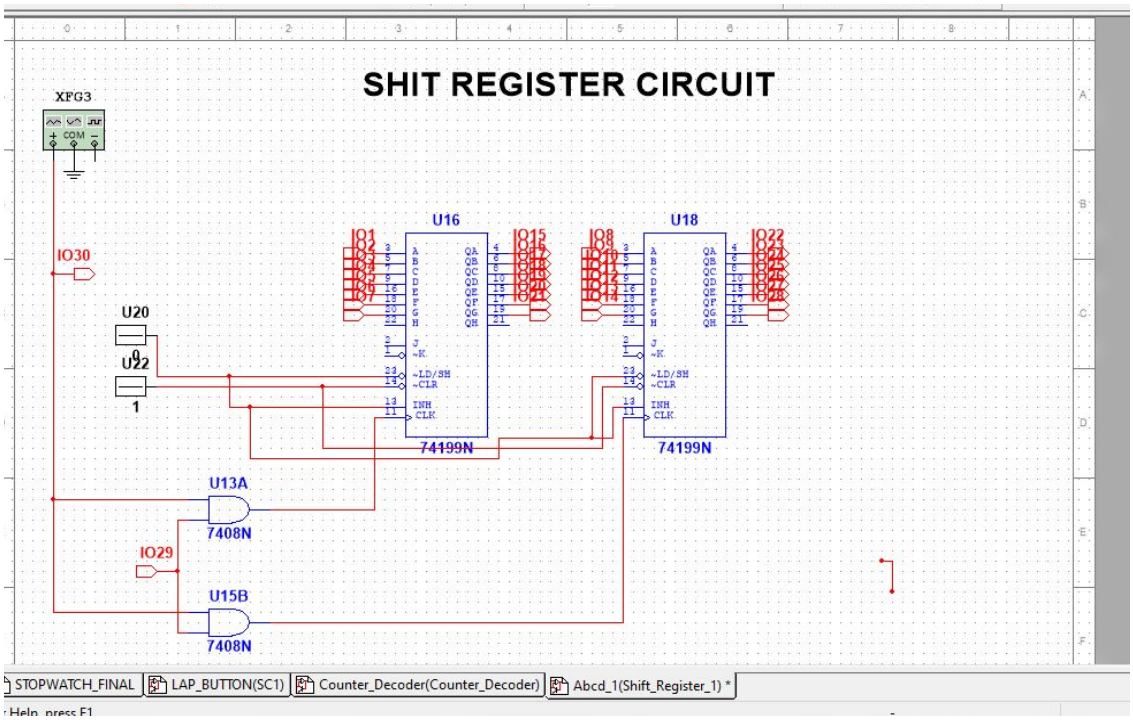
For normal operation , LT(lamp test),BI/RBO(blanking input,ripple blanking input) and RBI(ripple blanking input) is connected to +Vcc i.e logic 1. Output of 7490 IC is given to 7447 as shown in the fig:



SHIFT REGISTER

We have used 2 shift registers in PIPO (parallel in parallel out) mode.
The output from the counter_decoder circuit is given to the both the shift registers.
For eg. Io1 from the counter_decoder is connected to Io1 of shift register 1 and shift register 2 . Similar for all the output pins of the decoder.

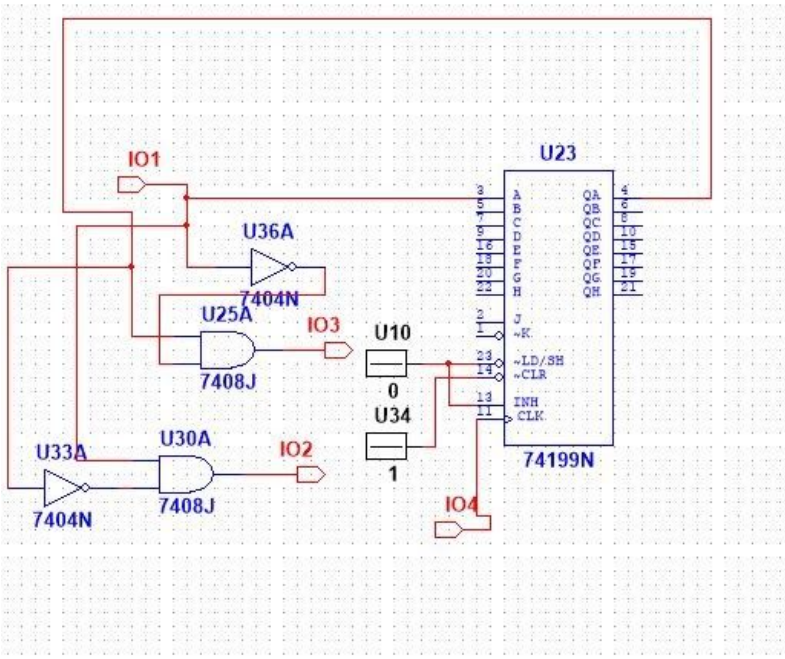
The internal circuit of shift register is:



IC 74199 is used for shift register in PIPO mode as shown above.

LAP BUTTON

The internal circuit for lap button is shown below:



The **TRUTH TABLE** for lap button is:

INPUTS		**OUTPUTS**		
B	**R**	**O1**	**O2**	**O3**
0	0	0	0	0
0	1	0	1	0
1	0	1	0	1
1	1	0	0	1

Where B-button/switch
R-shift register (stored bit)
O1-signal for 1st lap
O2-signal for 2nd lap
O3-next bit stored in shift register

WORKING

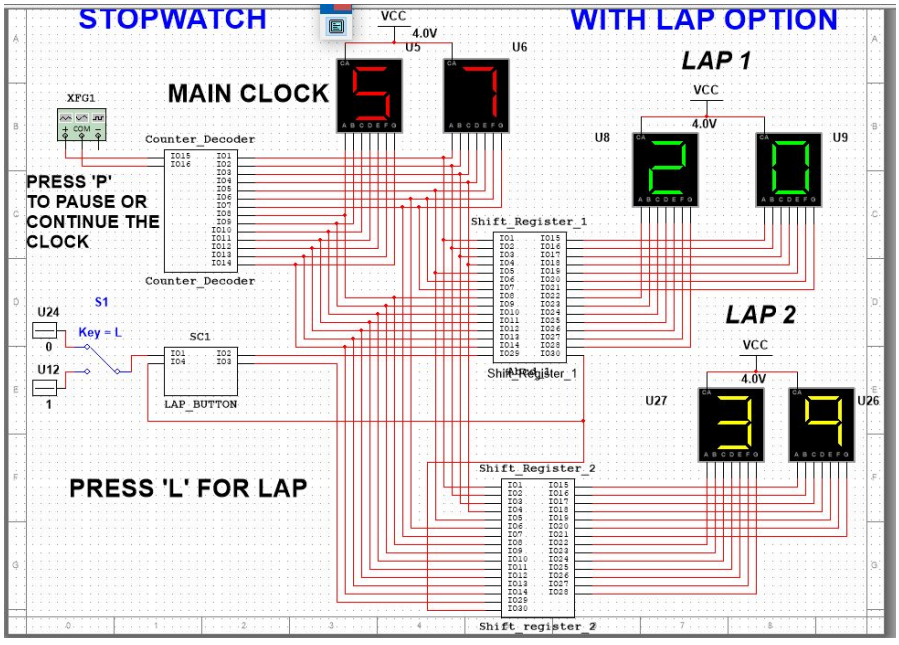
For our project's running simulation ,click herehttps://drive.google.com/file/d/1PO2PiTlux8AV51f6gUAUl9K1jG1U4xbw/view?usp=drivesdk

1. Select **RUN** option
2. The main clock starts counting from 00
3. For the first lap ,press the **LAP** key and the second at which the LAP key is pressed will be displayed at the U8 and U9(seven segment display).
4. For the second lap,again press the **LAP** key and then the corresponding second will be displayed at component U26 and U27.
5. To pause the watch press **P** button

EXPECTED RESULTS :

The circuit is intended to count seconds and 2 laps within 60 seconds .

OBSERVED RESULTS:



After running the simulation,when the lap button is pressed for the first time, here at 20 seconds ,the no. 20 gets displayed on the seven segment display and the main clock continues to run. When the lap button is pressed for the second time,here at 39 seconds ,the no. 39 gets displayed on the 2nd seven segment display and the clock counts further till 60 seconds and after it gets reset to 00.

CONCLUSION:

So,we have successfully understood ,designed and implemented our stopwatch (via multisim And verified the **expected** results and the **observed** results(through simulation) are the same.A digital clock has a wide range of application in real world.