EEE/INSTR F313
ANALOG AND DIGITAL VLSI DESIGN

ANALOG ASSIGNMENT

BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI

PROBLEM 14

SUBMITTED BY

NIRANJAN CHAUDHARI	2020B5A30929P
SUKRITI MATHUR	2020B5A81399P
SAARTHAK VIJAYVARGIYA	2021A3PS1044P

UNDER GUIDANCE OF

DR. ANU GUPTA

Acknowledgement

We would like to express our sincere gratitude towards Dr. Anu Gupta and the entire ADVD faculty, along with the EEE department, for their constant guidance and support in the project work. Without their assistance, this project couldn't have been completed.

We are also thankful to our batchmates and TAs for their help with software-related issues and for helping us understand the various steps, protocols and how to proceed with our project.

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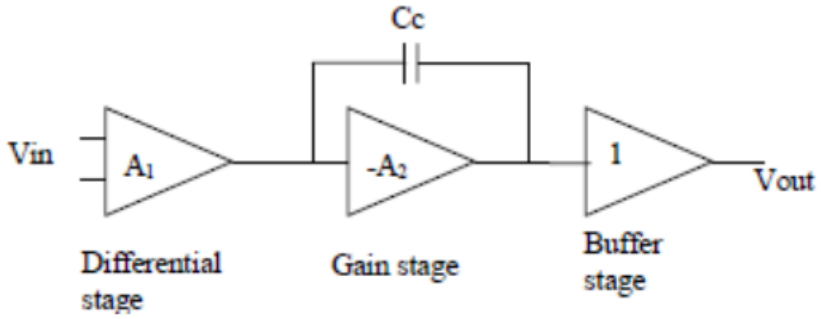
Problem Statement and Specifications

Q14. Design a CMOS OPAMP.



a) Analog schematic for the above model,
b) Analysis of all equations of your design, with a systematic derivation of all transistors W/L ratios and spectre simulation of circuit for the following specifications:

i) CMRR ≥ 140 dB

ii) PSRR ≥ 120dB

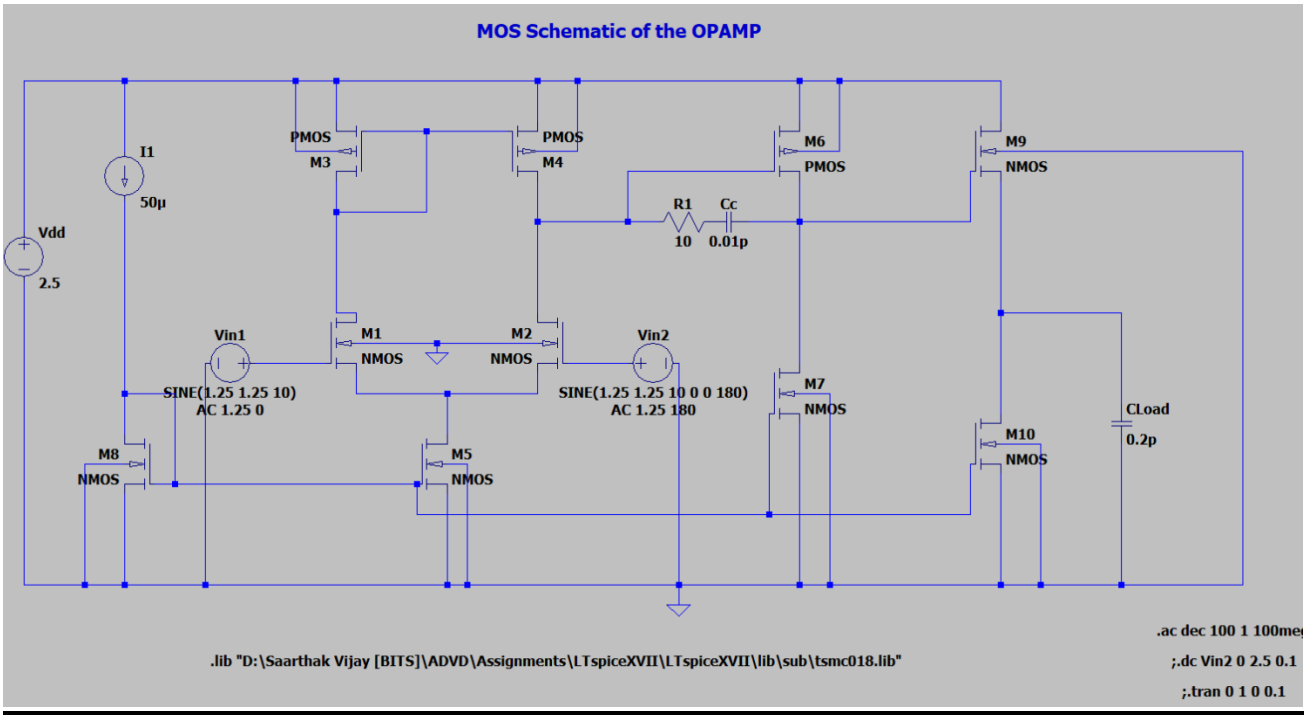
iii) Output Swing ≥ 1.6V

c) Use STB Analysis to find the closed loop gain and phase margin for your OPAMP.
d) Calculate and plot the following parameters for your OPAMP: DC gain, Bode plot for AC gain and phase, CMRR plot, ICMR plot, PSRR plot, slew rate, settling time, output voltage swing (dc + Transient), power consumption, and input and output offset voltage.

Specifications Required:

CMRR	≥ 140dB
PSRR	≥ 120dB
Output Swing	≥ 1.6V

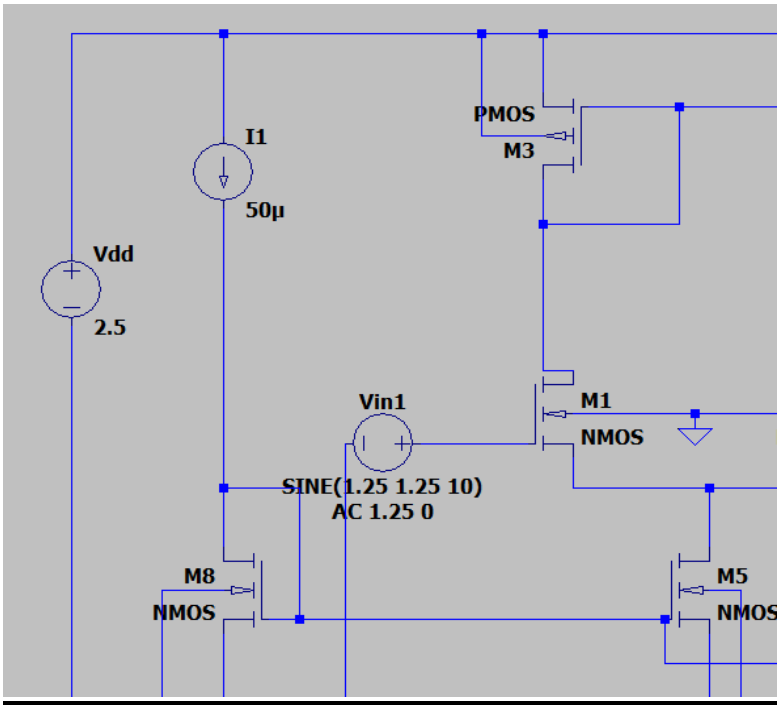
Schematic:



Breakdown of Circuit

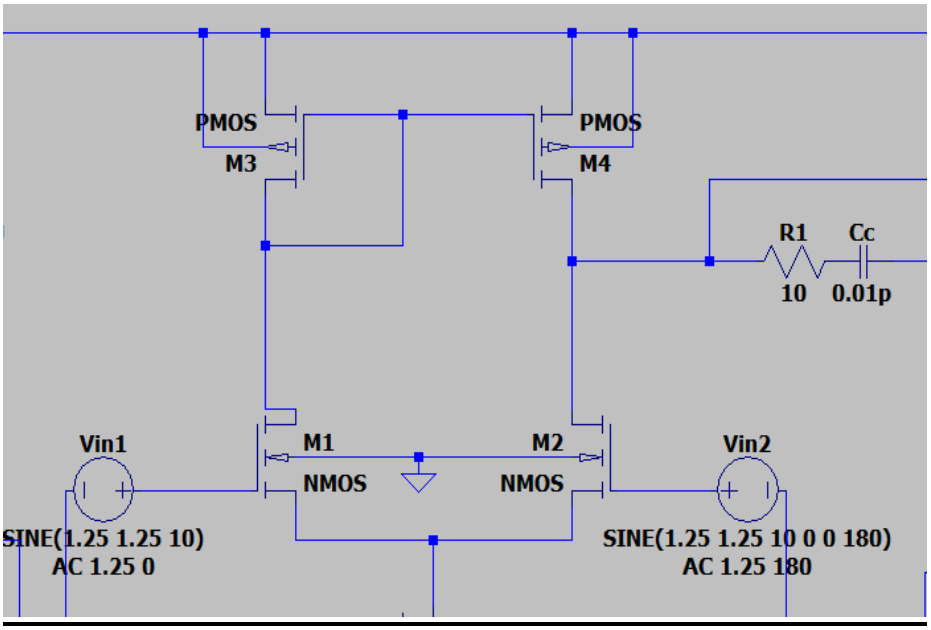
(A) Biasing circuitry

Reference current of 50uA was used in the current mirror circuit.



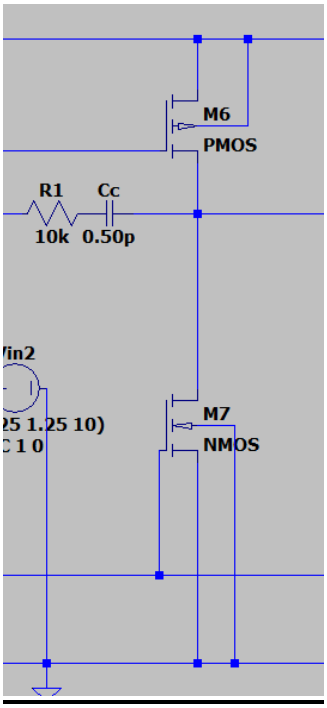
(B) Differential Stage

Single-ended differential amplifier was used with diode connected load. The output was passed through the R-C circuit.



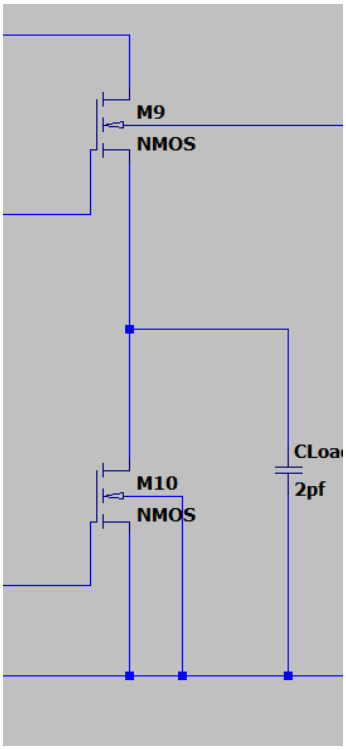
(C) Gain Stage

Common source amplifier was used as a gain stage amplifier.



(D) Buffer Stage

Buffer stage with negligible gain was added after second stage. It decreases loading effect and increases output swing.



Calculations:

To calculate the width of transistors, inputs of the first stage are grounded and perfectly matched. The drain current of M5 is equally divided between M1 and M2, then:

$$I_{D1} = I_{D2} = \frac{I_{D5}}{2}$$

since $I_{D3}=I_{D1}$ and $I_{D4}=I_{D2}$
Drain current through M3 and M4 can be calculated as:

$$I_{D3} = \frac{I_{D5}}{2} = I_{D4}$$

The drain current densities of M3, M4, M6 and M7 are equal

$$\frac{I_{D3}}{(W/L)_3} = \frac{I_{D4}}{(W/L)_4} = \frac{I_{D6}}{(W/L)_6} = \frac{I_{D7}}{(W/L)_7}$$

Transistors M5 and M7 have equal gate-source voltage ($V_{GS5}=V_{GS7}$), so transistor sizes can be calculated as:

$$\frac{I_{D5}}{I_{D6}} = \frac{I_{D5}}{I_{D7}} = \frac{2(W/L)_{3,4}}{(W/L)_6} = \frac{2(W/L)_{3,4}}{(W/L)_7}$$

The bias current (Ib) determines the drain to source voltages of the current sources of devices M5, M7 and M8, so:

$$I_{D5} = \frac{(W/L)_5}{(W/L)_8} I_b$$

And for M7:

$$I_{D7} = \frac{(W/L)_7}{(W/L)_8} I_b$$

So drain current through M1 and M2 are calculated as:

$$I_{D1} = I_{D2} = \frac{(W_5)(L_8)}{2(W_8)(L_5)}(I_b)$$

Transistor Specifications:

The length was set to minimum transistor length 180 nm.

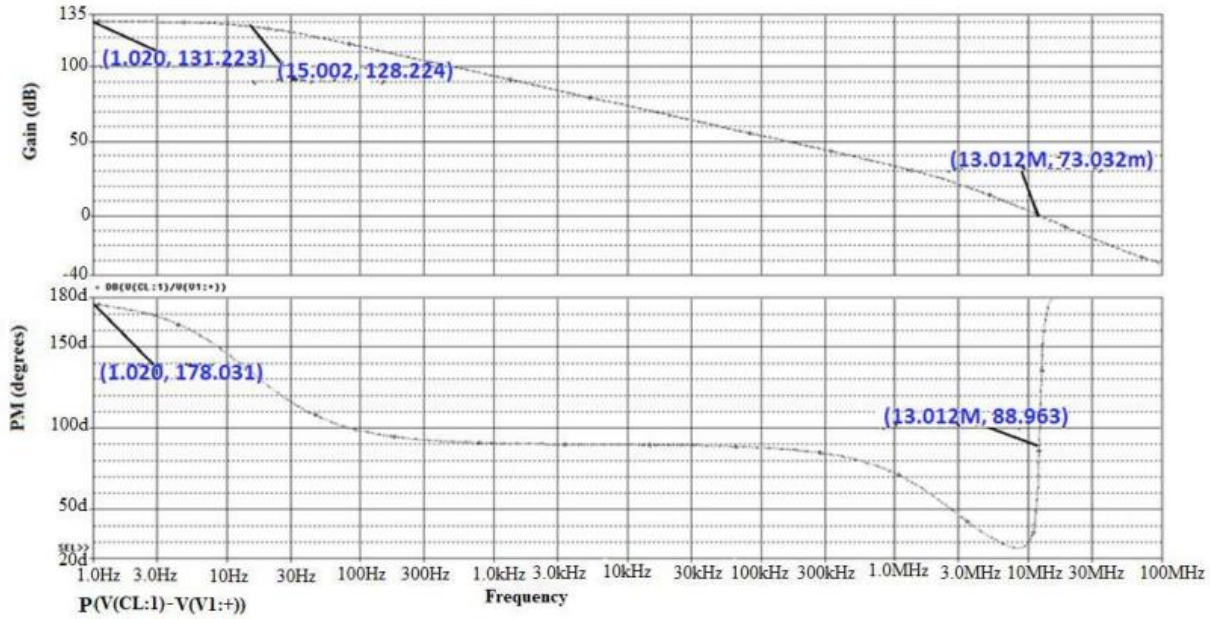
MOS Transistor	Aspect Ratio (W/L)	Channel width
M1	8	1.44
M2	8	1.44
M3	4	0.72
M4	4	0.72
M5	1	0.40
M6	40	7.20
M7	8	1.44
M8	1	0.40
M9	8	1.44
M10	8	1.44

LTSpice Netlist

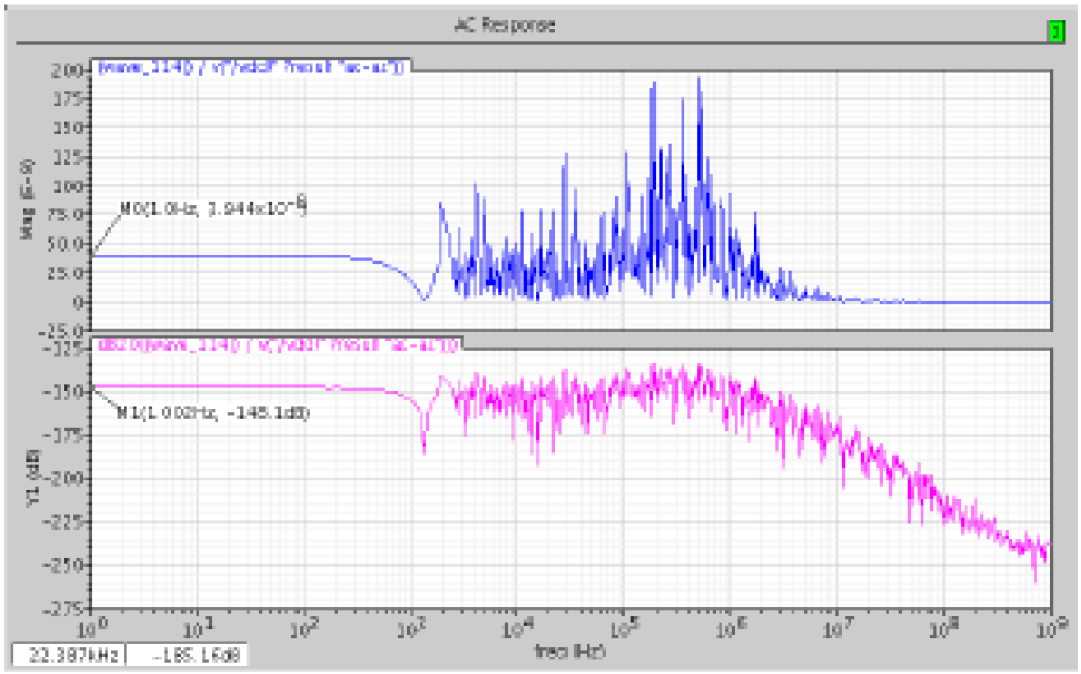
```
* D:\Saarthak Vijay [BITS]\ADVD\Assignments\Analog\Advd1.asc

* – Differential Stage –

M1 N002 N006 N009 0 NMOS W={w1} L={l}
Vin1 N006 0 SINE(1.25 1.25 10) AC 1.25 0
M2 N003 N007 N009 0 NMOS W={w2} L={l}
Vin2 N007 0 SINE(1.25 1.25 10) AC 1.25 180
M3 N002 N002 N001 N001 PMOS W={w3} L={l}
M4 N003 N002 N001 N001 PMOS W={w4} L={l}
M5 N009 N008 0 0 NMOS W={w5} L={l}
R1 P001 N003 10k
Cc N004 P001 0.50pf

* – Gain Stage –

M6 N001 N003 N004 N001 PMOS W={w6} L={l}
M7 N004 N008 0 0 NMOS W={w7} L={l}
M8 N008 N008 0 0 NMOS W={w8} L={l}
I1 N001 N008 100µ
Vdd N001 0 2.5

* – Buffer Stage –

M9 N001 N004 N005 0 NMOS W={w9} L={l}
M10 N005 N008 0 0 NMOS W={w10} L={l}

.param l=0.18u
.param w1=1.44u
.param w2=1.44u
```

```
.param w3=0.72u
.param w4=0.72u
.param w5=0.4u
.param w6=7.20u
.param w7=1.44u
.param w8=0.4u
.param w9=1.44u
.param w10=1.44u

CLoad N005 0 2pf
.model NMOS NMOS
.model PMOS PMOS
.lib C:\Users\saart\OneDrive\Documents\LTspiceXVII\lib\cmp\standard.mos
* MOS Schematic of the OPAMP
.lib "D:\Saarthak Vijay
[BITS]\ADVD\Assignments\LTspiceXVII\LTspiceXVII\lib\sub\tsmc018.lib"
* Bode plot (CMRR)
.ac dec 100 1 100meg
* For ICMR
;.dc Vin2 0 2.5 0.1
* For swing
;.tran 0 1 0 0.1
.backanno
.end
```

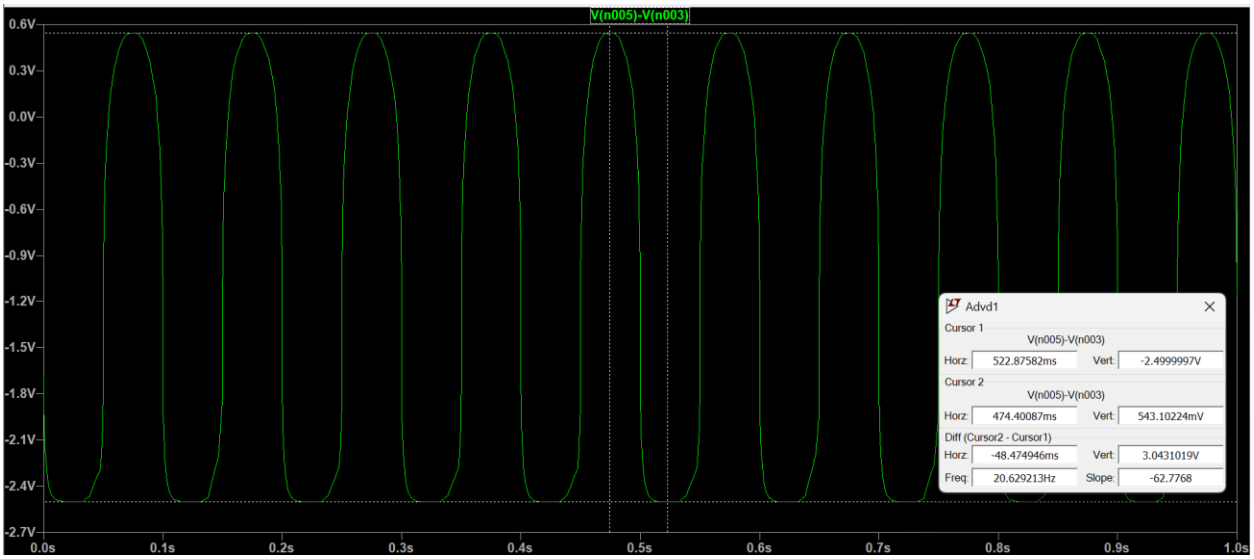
CMRR[2]


(1.020, 131.223)
(15.002, 128.224)
(13.012M, 73.032m)
Gain (dB)
(1.020, 178.031)
(13.012M, 88.963)
PM (degrees)
Frequency
P(V(CL:1)-V(V1:+))

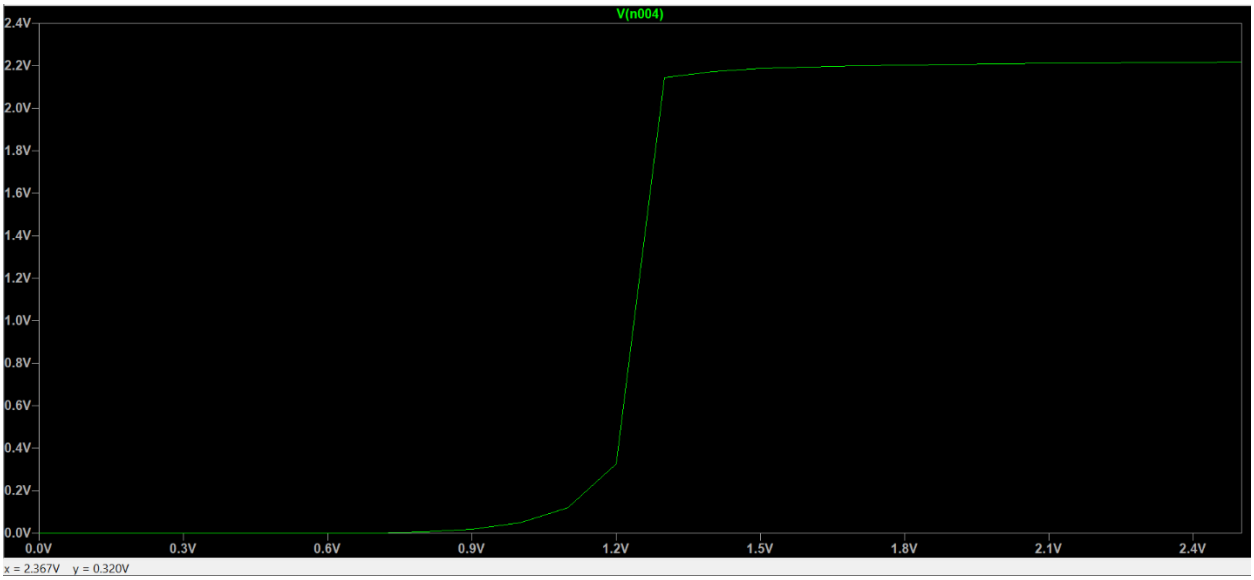
PSRR[1]


AC Response
M0(1.00Hz, 1.944x10^-9)
M1(1.002Hz, -145.1dB)
Mag (G-Ω)
Y1 (dB)
freq (Hz)
22.387kHz
-185.1dB

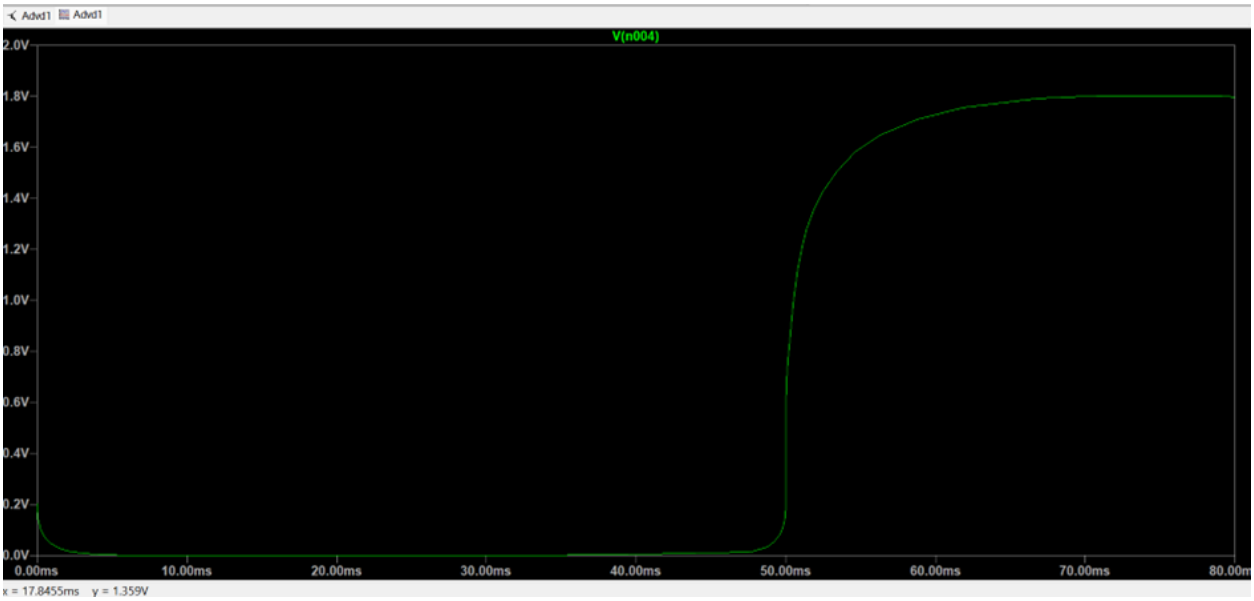
Voltage Swing:



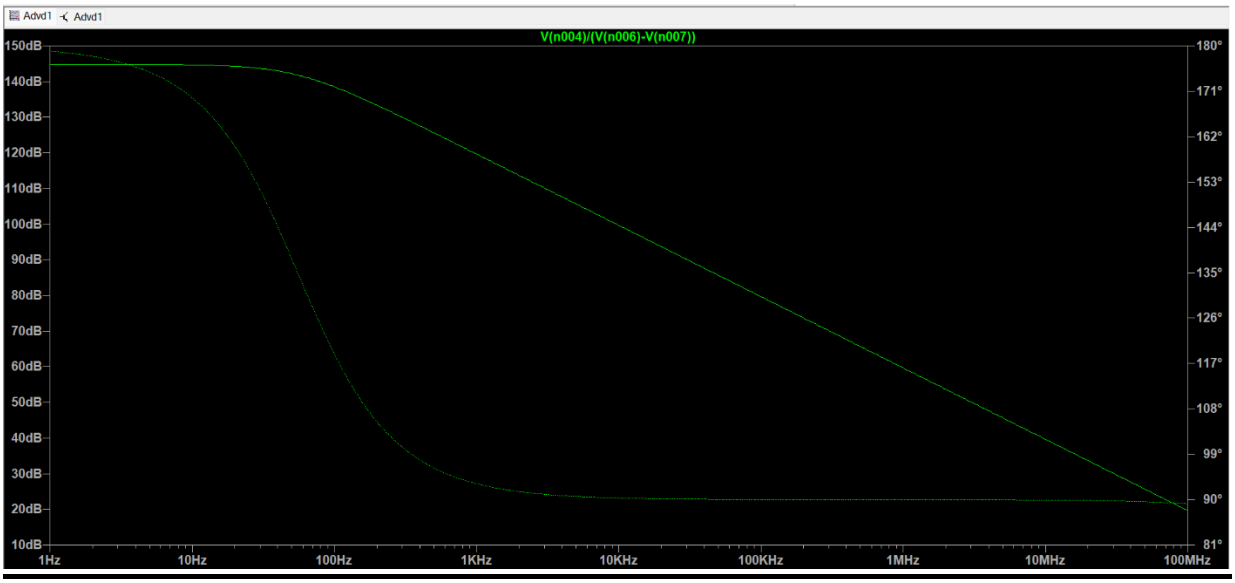
ICMR:



Slew rate:



Bode Plot:



Comparison Between Theoretical and Simulation Results:

Specification	Actual Value	Simulated Value
Open loop gain	40 dB	36.747 dB
Phase margin	60	48.1
Slew Rate	10 V/uS	12.5 V/uS
CMRR	140 dB	144.69 dB
PSRR	120 dB	179.38 dB
Output swing	1.6 V	3.4 V
Power dissipation	2mW	0.804 mW

Problems Faced in Design:

- The concepts required to design the circuit were not covered in the lectures. This required us to refer to materials across the web, books etc. to design the circuit.
- It was very challenging to meet all the specifications given in the problem statement simultaneously. Several trade-offs were employed to satisfy the constraints mentioned in the problem.

Innovation Implemented in Design:

- We tried implementing the current source using the current mirror. In the biasing circuit, we first calculated the gate voltages that were required for biasing. The reference current in the ideal current source is taken to be 50uA.
- Using this reference current and the Vgs-Vt values for the biasing MOSFETs, we calculated the W/L values. The biasing circuit used is made using λ mismatch.

- The PMOS bias resulted in saturation of the cascode stage PMOSs. But the W/L of the PMOS had to be adjusted in order to bring both MOSFETs of the cascode stage to saturation.

References:

1. Bandyopadhyay, S., Mukherjee, D., & Chatterjee, R. (2014). Design of two stage cmos operational amplifier in 180nm technology with low power and high cmrr. *Int. J. of Recent Trends in Engineering & Technology*, *11*.
2. Genzebu, T. M. (2023). Design of High Gain and High Slew Rate Two-Stage CMOS Operational Amplifier for Medical Instrumentation.