

CMOS PROJECT REPORT



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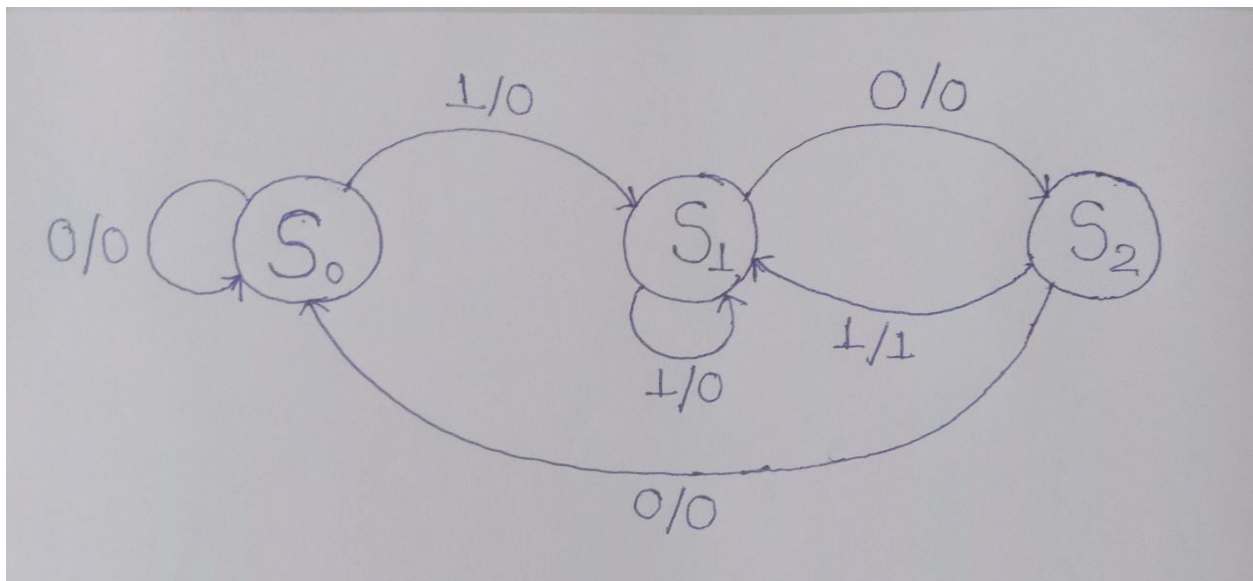
101 Overlapping Mealy Sequence Detector Using JK Flip Flop

Introduction :

Sequence detector is designed using its CMOS layout and draws the layout using **Microwind** and writes the netlist in **Ngspice**. When the detector receives a sequence 101, its output will be high at the end of the sequence and for any other sequence, output will be low.

Circuit is overlapping thus, an overlapping sequence like 10101 the first part of the sequence 101, it will make output high at that position and second 101 after 10 will also make output high at the end of the sequence, Circuit is designed as a Mealy machine, so it will change its output, both by its current state and the current inputs are changed. Input does affect the output directly as soon as logic is done.

State Diagram :



S₀ , S₁ and S₂ are states and from each state there are values that show x/output. Number of flip flops(N) , $2^N \geq \text{Number of States}$,so $N=2$

State table :

Present State (PS)	Input (x)	Next State (NS)	Output (y)
S ₀	0	S ₀	0
S ₀	1	S ₁	0
S ₁	0	S ₂	0
S ₁	1	S ₁	0
S ₂	0	S ₀	0
S ₂	1	S ₁	0

S₀ -> 00 , S₁ -> 01 , S₂->10

Transition Table :

PS	x	NS	y
Q ₁ Q ₀		Q* ₁ Q* ₀	
00	0	00	0
00	1	01	0
01	0	10	0
01	1	01	0
10	0	00	0
10	1	01	0

Excitation Table of JK Flip Flop :

Q _n	Q _{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Excitation Table for the Circuit :

PS (Q_1Q_0)	Input(x)	NS($Q^*_1Q^*_0$)	FF I/P (J_0K_0)	FF I/P(J_1K_1)	Output(y)
00	0	00	0X	0X	0
00	1	01	1X	0X	0
01	0	10	X1	1X	0
01	1	01	X0	0X	0
10	0	00	0X	X1	0
10	1	01	1X	X1	1

Equation of J_0, K_0, J_1, K_1 and y using K-map :

Handwritten K-maps for the circuit:

- For J_0 :**

$Q_1 \backslash Q_0$	00	01	11	01
0	0	1	X	X
1	0	1	X	X
- For K_0 :**

$Q_1 \backslash Q_0$	00	01	11	01
0	X	X	0	1
1	X	X	X	X
- For J_1 :**

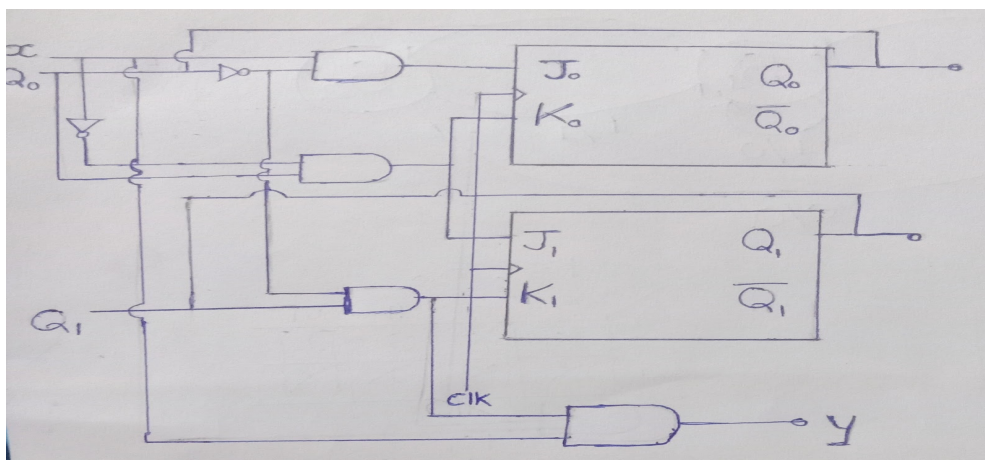
$Q_1 \backslash Q_0$	00	01	11	01
0	0	0	0	1
1	X	X	X	X
- For K_1 :**

$Q_1 \backslash Q_0$	00	01	11	01
0	X	X	X	X
1	1	1	X	X
- For Output (y):**

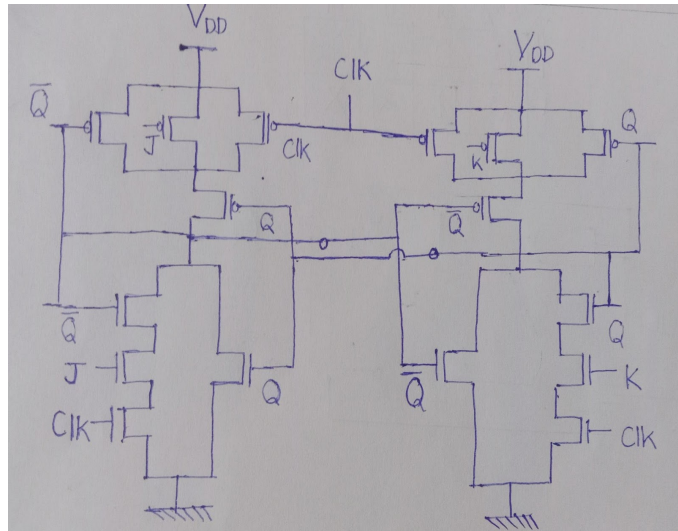
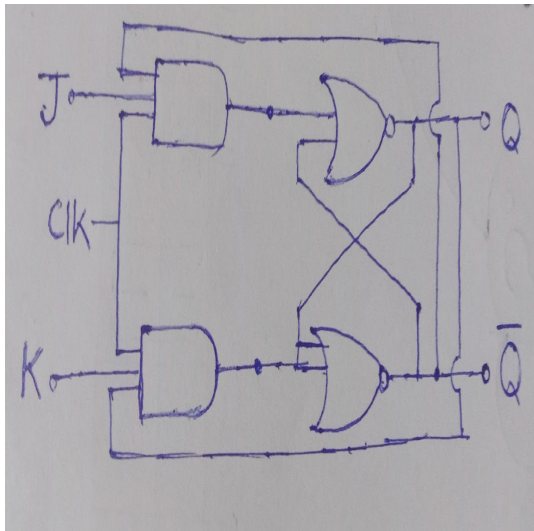
$Q_1 \backslash Q_0$	00	01	11	01
0	0	0	0	0
1	0	1	X	X

$J_0 = Q_0' \cdot x$, $K_0 = Q_0 \cdot x'$, $J_1 = Q_0 \cdot x'$, $K_1 = Q_1 \cdot Q_0'$ and Output (y) = $Q_1 \cdot Q_0' \cdot x$

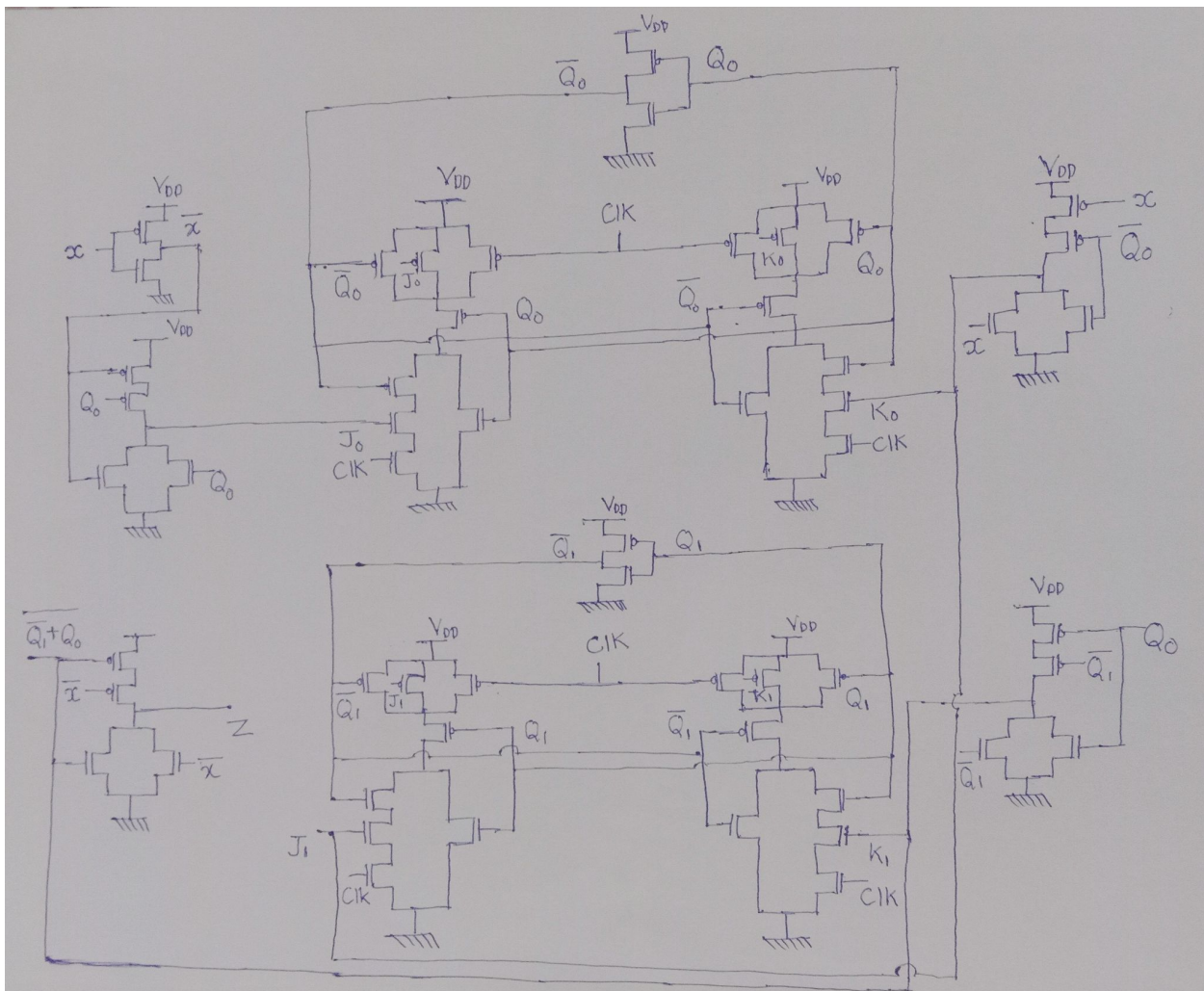
Circuit Diagram :



JK flip flop using NOR gate and using CMOS technology :



101 Sequence detector circuit using CMOS technology :



Netlist Code for Sequence Detector :

The Edit Format View Help
**sequence detector using jk flip flop 101

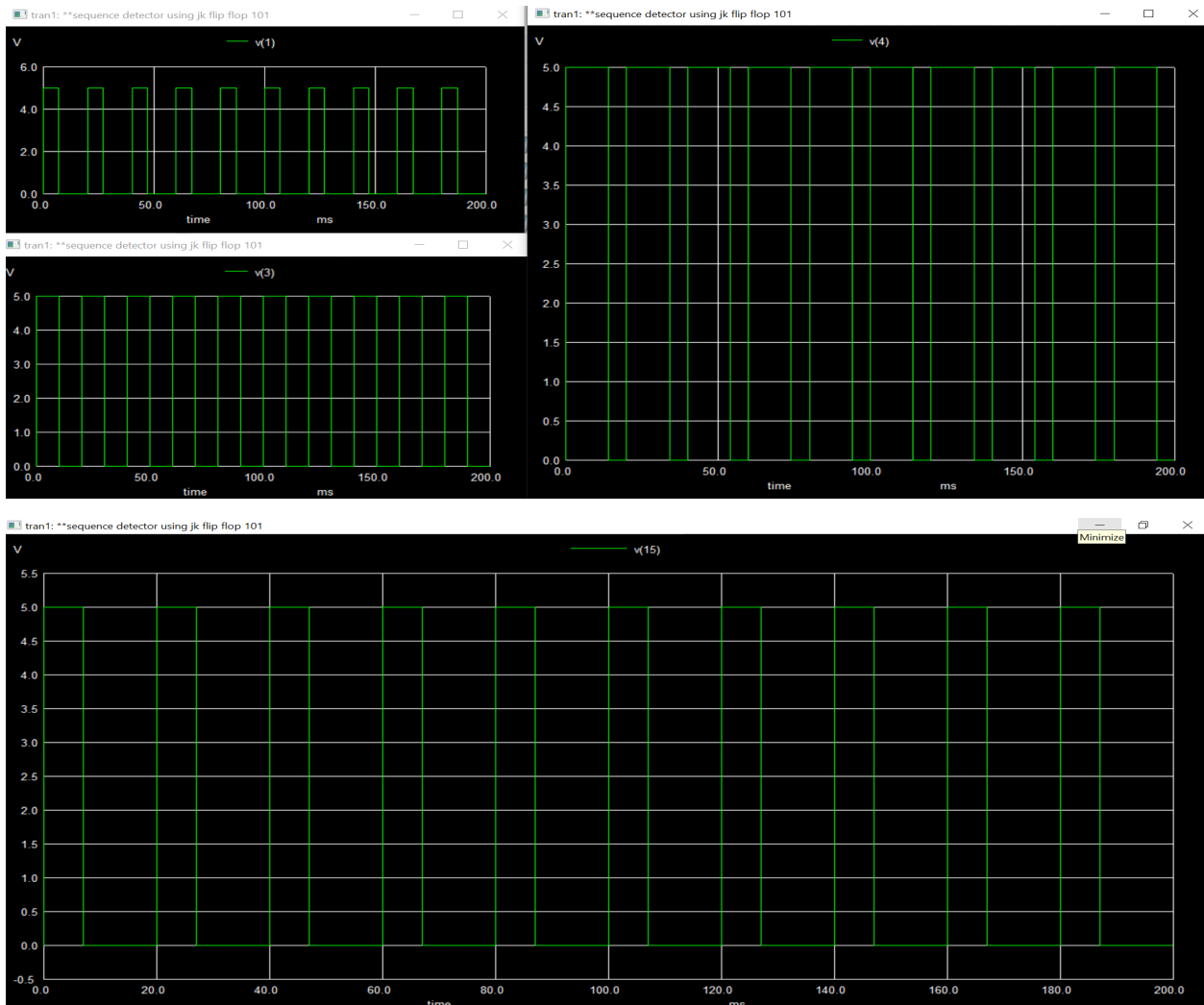
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Vd 8 0 dc 5v
Vc 5 0 pulse (0 5 0 0 0 5ms 20ms)
V1 1 0 pulse(0 5 0 0 0 7ms 20ms)
V2 3 0 pulse(0 5 0 0 0 10ms 20ms)
V3 4 0 pulse(0 5 0 0 0 14ms 20ms)
.model nmod nmos level=54 version=4.7
.model pmod pmos level=54 version=4.7
m1 2 1 8 8 pmod w=100u l=10u
m2 2 1 0 0 nmod w=100u l=10u
m3 6 3 8 8 pmod w=100u l=10u
m4 6 3 0 0 nmod w=100u l=10u
m5 7 4 8 8 pmod w=100u l=10u
m6 7 4 0 0 nmod w=100u l=10u
m7 10 3 8 8 pmod w=100u l=10u
m8 9 2 10 8 pmod w=100u l=10u
m9 9 2 0 0 nmod w=100u l=10u
m10 9 3 0 0 nmod w=100u l=10u
m11 12 6 8 8 pmod w=100u l=10u
m12 11 1 12 8 pmod w=100u l=10u
m13 11 1 0 0 nmod w=100u l=10u
m14 11 6 0 0 nmod w=100u l=10u
m15 14 7 8 8 pmod w=100u l=10u
m16 13 3 14 8 pmod w=100u l=10u
m17 13 3 0 0 nmod w=100u l=10u
m18 13 6 0 0 nmod w=100u l=10u
m19 16 13 8 8 pmod w=100u l=10u
m20 15 2 16 8 pmod w=100u l=10u
m21 15 13 0 0 nmod w=100u l=10u
m22 15 2 0 0 nmod w=100u l=10u
m23 20 6 8 8 pmod w=100u l=10u
m24 20 9 8 8 pmod w=100u l=10u
m25 20 5 8 8 pmod w=100u l=10u
m26 19 23 21 8 pmod w=100u l=10u
m27 19 6 18 0 nmod w=100u l=10u
m28 18 9 17 0 nmod w=100u l=10u
m29 17 5 0 0 nmod w=100u l=10u
m30 19 23 0 0 nmod w=100u l=10u
m31 24 5 8 8 pmod w=100u l=10u
m32 24 11 8 8 pmod w=100u l=10u
m33 24 3 8 8 pmod w=100u l=10u
m34 23 19 24 8 pmod w=100u l=10u
m35 23 19 0 0 nmod w=100u l=10u
m36 23 3 22 0 nmod w=100u l=10u
m37 22 11 21 0 nmod w=100u l=10u
m38 21 5 0 0 nmod w=100u l=10u
m39 28 7 8 8 pmod w=100u l=10u
m40 28 11 8 8 pmod w=100u l=10u
m41 28 5 8 8 pmod w=100u l=10u
m42 27 31 28 8 pmod w=100u l=10u
m43 27 7 26 0 nmod w=100u l=10u
m44 26 11 25 0 nmod w=100u l=10u
m45 25 5 0 0 nmod w=100u l=10u
m46 27 31 0 0 nmod w=100u l=10u
m47 32 13 8 8 pmod w=100u l=10u
m48 32 5 8 8 pmod w=100u l=10u
m49 32 4 8 8 pmod w=100u l=10u
m50 31 27 32 8 pmod w=100u l=10u
m51 31 4 30 0 nmod w=100u l=10u
m52 30 13 29 0 nmod w=100u l=10u
m53 29 5 0 0 nmod w=100u l=10u
m54 31 27 0 0 nmod w=100u l=10u
.tran 0.01ms 200ms
.control
run
plot V(1)
plot V(3)
```

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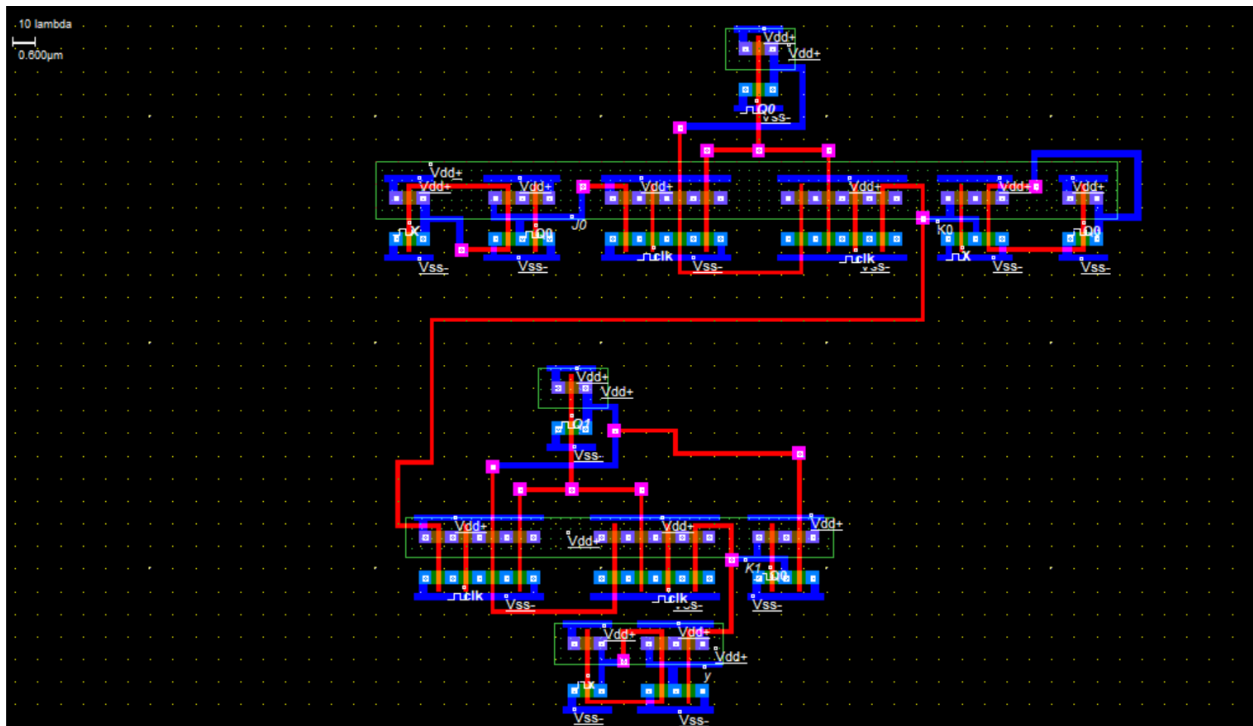
m30 19 23 0 0 nmod w=100u l=10u |
m31 24 5 8 8 pmod w=100u l=10u
m32 24 11 8 8 pmod w=100u l=10u
m33 24 3 8 8 pmod w=100u l=10u
m34 23 19 24 8 pmod w=100u l=10u
m35 23 19 0 0 nmod w=100u l=10u
m36 23 3 22 0 nmod w=100u l=10u
m37 22 11 21 0 nmod w=100u l=10u
m38 21 5 0 0 nmod w=100u l=10u
m39 28 7 8 8 pmod w=100u l=10u
m40 28 11 8 8 pmod w=100u l=10u
m41 28 5 8 8 pmod w=100u l=10u
m42 27 31 28 8 pmod w=100u l=10u
m43 27 7 26 0 nmod w=100u l=10u
m44 26 11 25 0 nmod w=100u l=10u
m45 25 5 0 0 nmod w=100u l=10u
m46 27 31 0 0 nmod w=100u l=10u
m47 32 13 8 8 pmod w=100u l=10u
m48 32 5 8 8 pmod w=100u l=10u
m49 32 4 8 8 pmod w=100u l=10u
m50 31 27 32 8 pmod w=100u l=10u
m51 31 4 30 0 nmod w=100u l=10u
m52 30 13 29 0 nmod w=100u l=10u
m53 29 5 0 0 nmod w=100u l=10u
m54 31 27 0 0 nmod w=100u l=10u
.tran 0.01ms 200ms
.control
run
plot V(1)
plot V(3)
plot V(4)
plot V(15)
.endc
.end

```

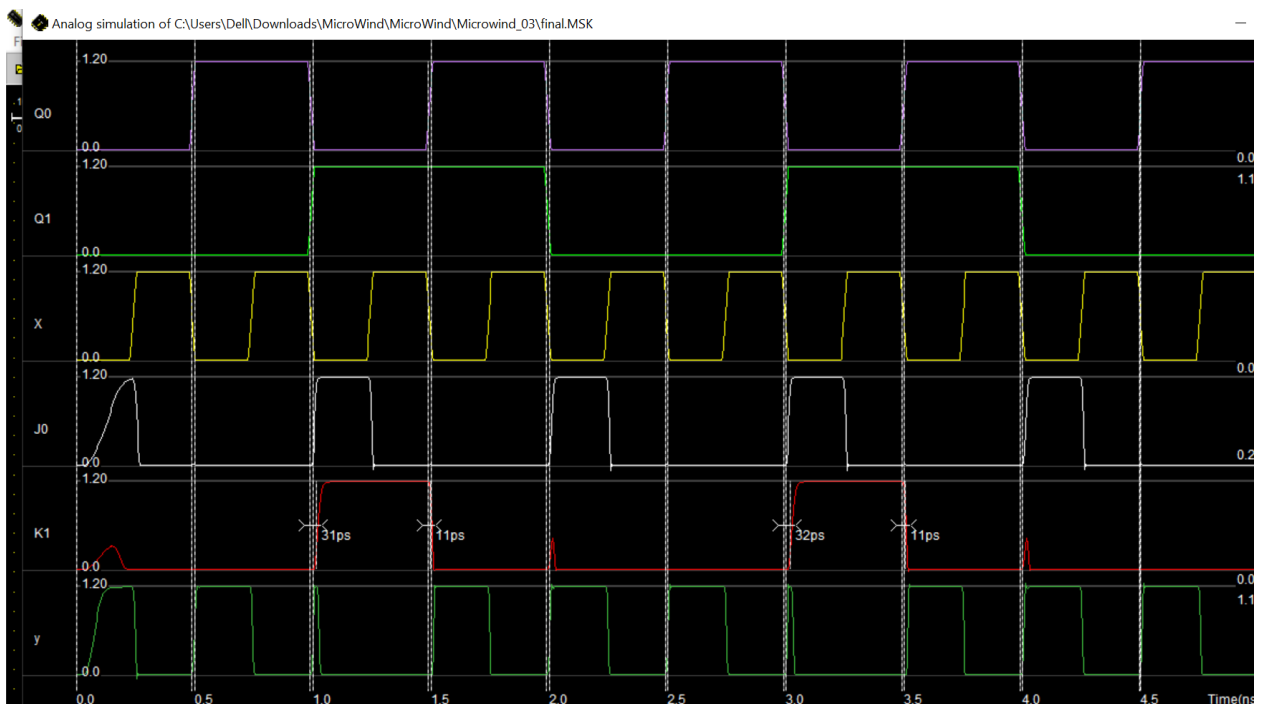
Input and Output in ngspice :



Layout in Microwind :



Microwind Output :



V(15) is the output waveform which I got from ngspice and Y is the output graph using microwind.

Power dissipation (microwind) = 0.371 mW.