**Pre Layout Simulations Report**

**Moshe Saban**

**CMOS OSC Clk 33MHz to ZYNC**

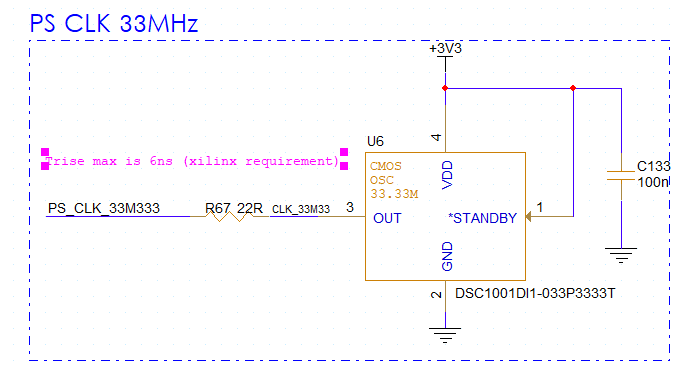
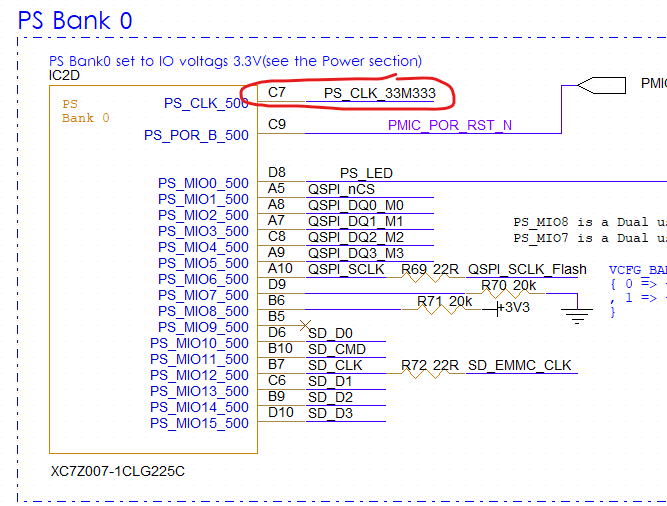
IBIS files dsc1001dl.IBIS and Zynq

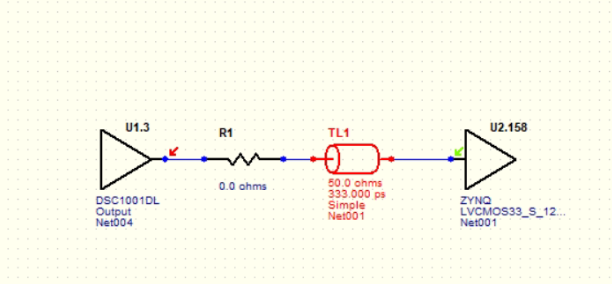
Course assumptions (FR4 average) - V=15cm/1ns

Assuming placing the OSCclk close as possible to the Zync and up to 333ps( 5cm)

I need review on selecting the Zync RX model(LVCMOS33\_S? \_F?)

Also need review on the Tr/Tf max time of 6ns and I get faster even with the 22ohm

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**With no clk output termination:**

**A screen shot of a graph

Description automatically generated**

**And With clk output termination=22ohm**

A diagram of a cable

Description automatically generated

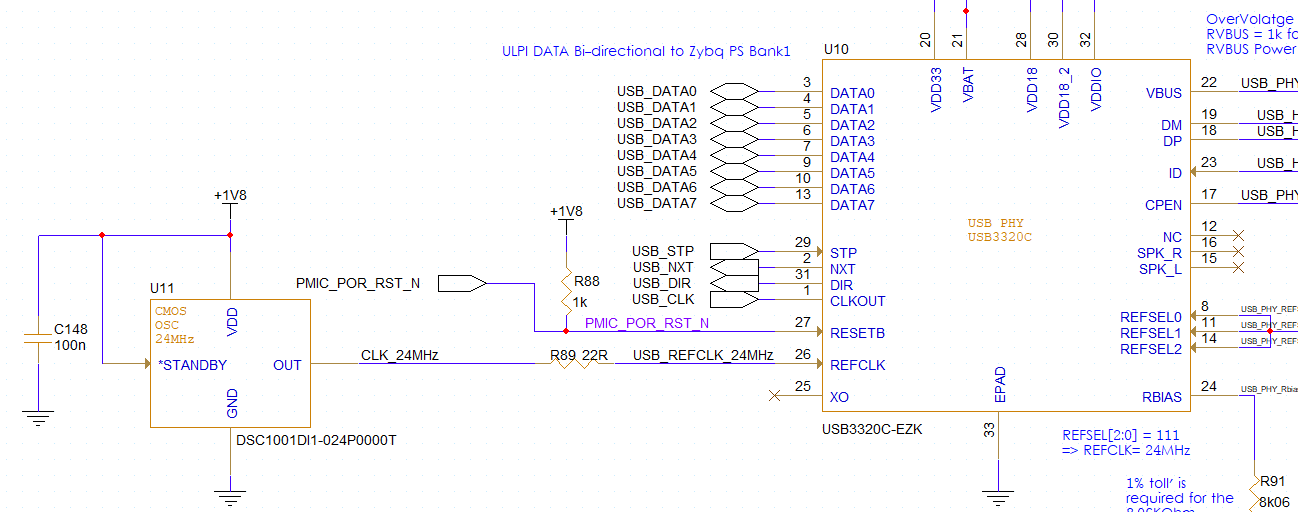
A screen shot of a graph

Description automatically generated

Much smoother RX die input with 22 ohm clk output termination.

**So 22ohm is recommended.**

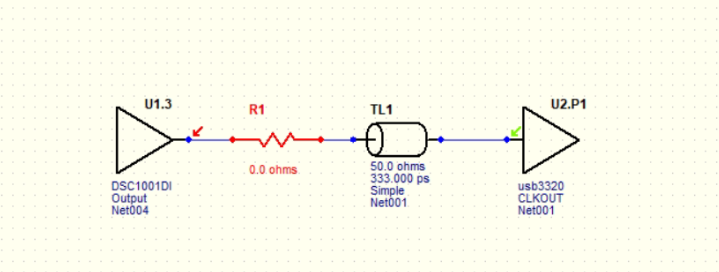
**CMOS OSC Clk 24MHz to USB PHY**

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IBIS files: **dsc1001dl.IBIS** (change to 1.8v CMOS) and **usb3320.IBIS**

Course assumptions (FR4 average) - V=15cm/1ns

Assuming placing the OSCclk close as possible to the FTDI and up to 333ps(5cm)



Results(ringing)

A screen shot of a computer

Description automatically generated

Will add 22 ohm tx output termination:

A diagram of a circuit

Description automatically generated

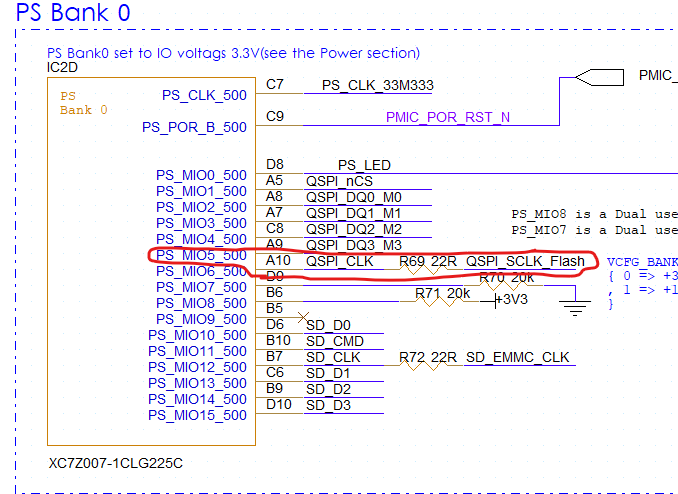
And results are now better:

A screen shot of a computer

Description automatically generated

**So 22ohm is recommended here as well.**

**QSPI Clk (from Zync to QSPI)**

A diagram of a flash memory

Description automatically generated

With no 22ohm resistor

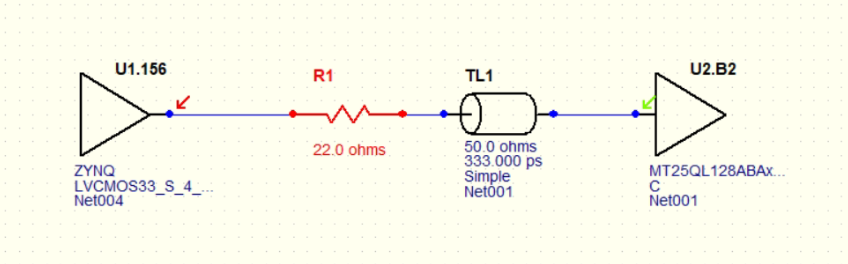
A diagram of a cable

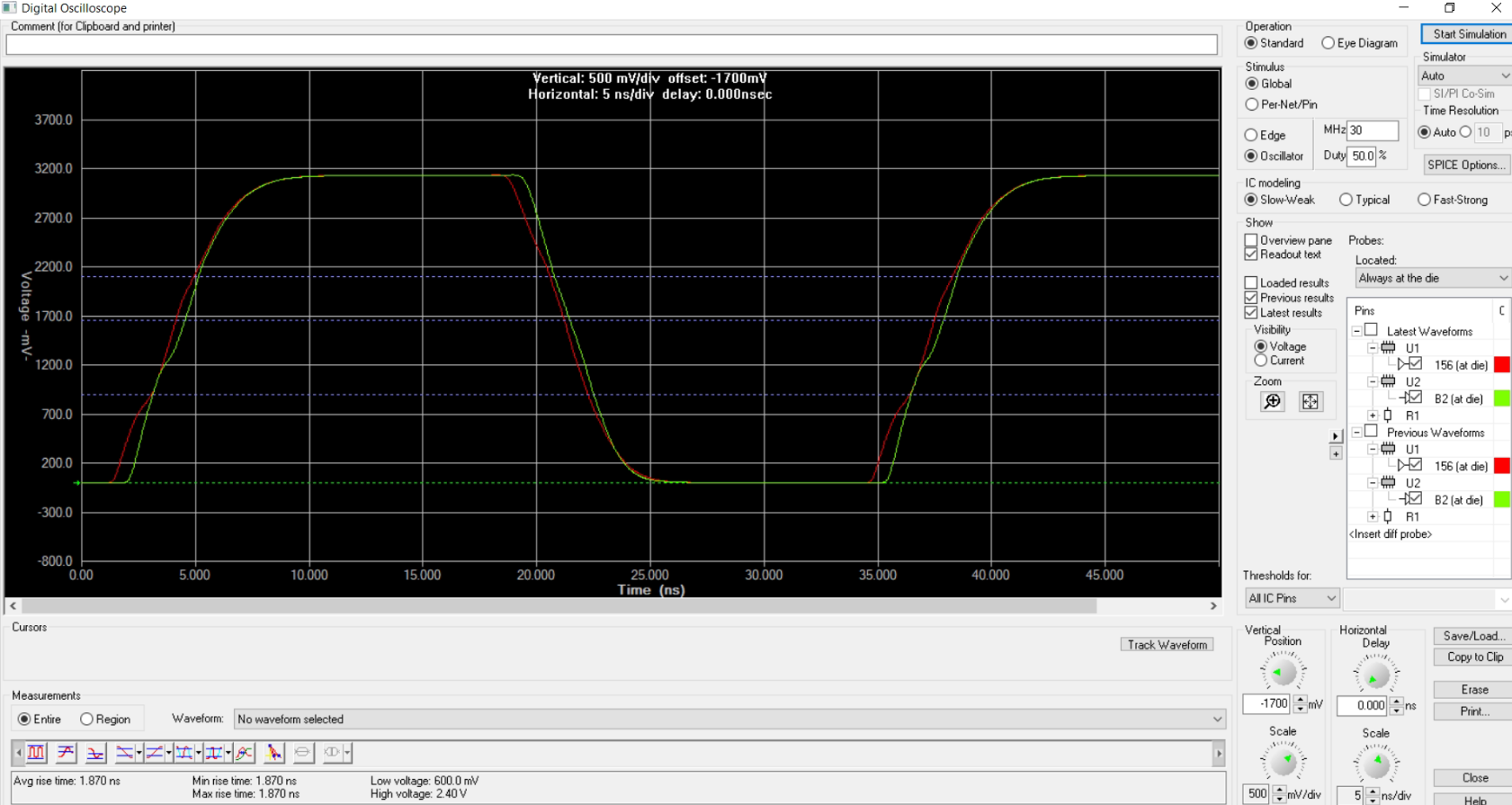
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A screen shot of a graph

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And with 22 ohm resistor:





Conclusion – an output resistor is not a must but recommended to keep it for good practice and debug.

**DDR3L**

DDR micron IBIS:

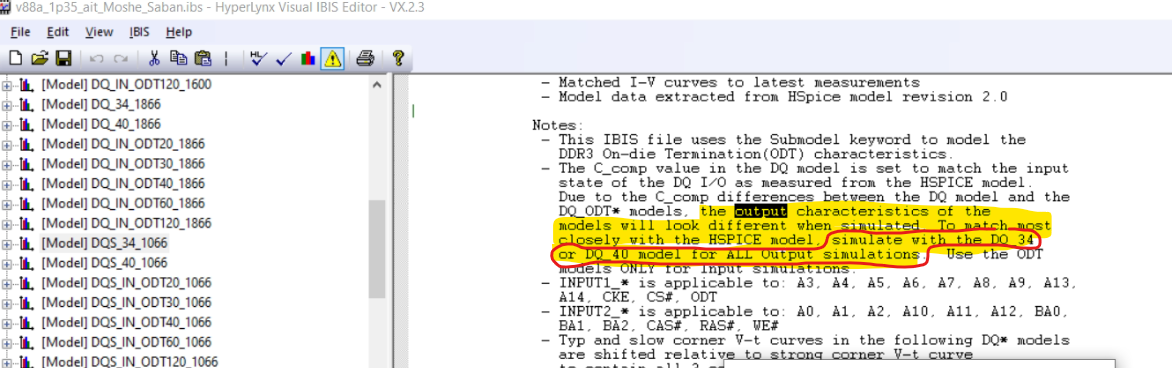
This IBIS model includes On Die Termination (ODT) characteristics

**v88a\_1p35\_ait.ibs** is valid for 1.283V-1.425V, Automotive Industrial Temperature Range -40C<=Tc<=95C

**ZYNC CLK to DDR CLK(800MHz)**

**Considering up to 15 cm DDR traces(1ns)**

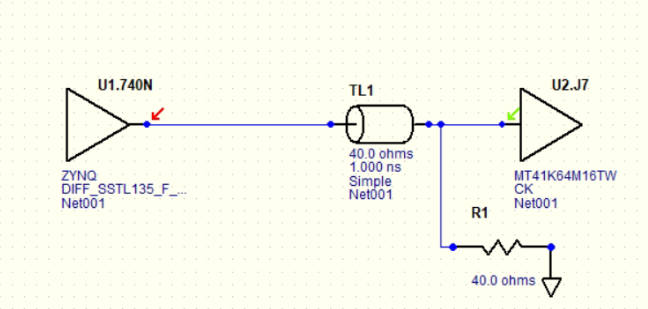
Should be differential clk but I get only SE model in the DDR IBIS so placing here SE simulation with SE termination instead of the 80 ohm differential termination

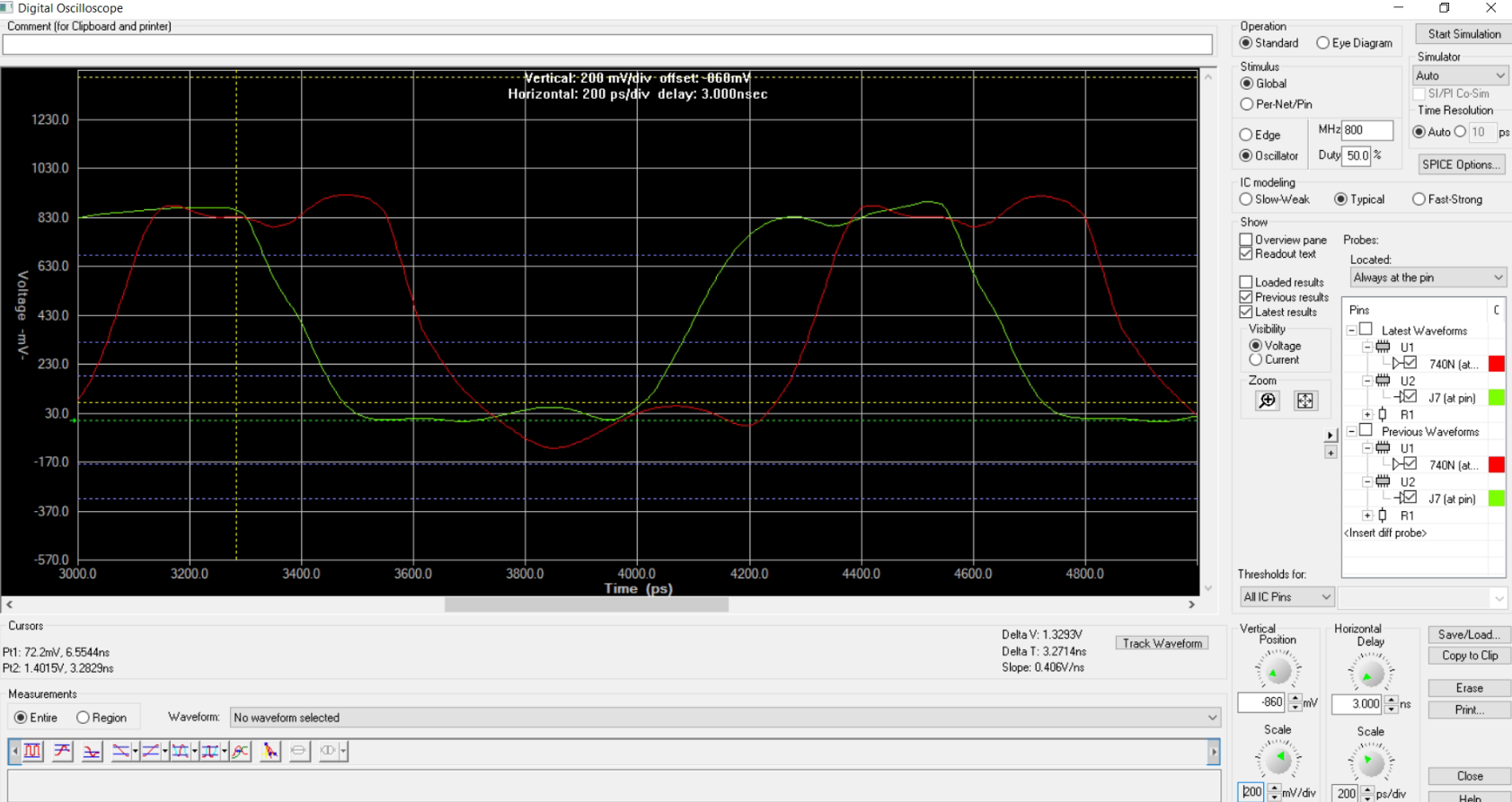


A screenshot of a computer

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**DDR to Zync simulations**

As specified in the IBIS file, all the output simulation from the DDR model should be taken from same model DQ34(Or DQ40). So this apply to DDR transmit address and DDR transmit DQ

Assuming ODT in Zync but not sure I selected the correct model for zync

A diagram of a simple network

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A screen shot of a computer

Description automatically generated

**Zync to DDR address A0 line with VTT termination**

A diagram of a circuit

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A screen shot of a computer

Description automatically generated

Zync to DDR DQ0 with ODT

Selected model with 40 ohm ODT:

A screenshot of a computer

Description automatically generated

A diagram of a circuit

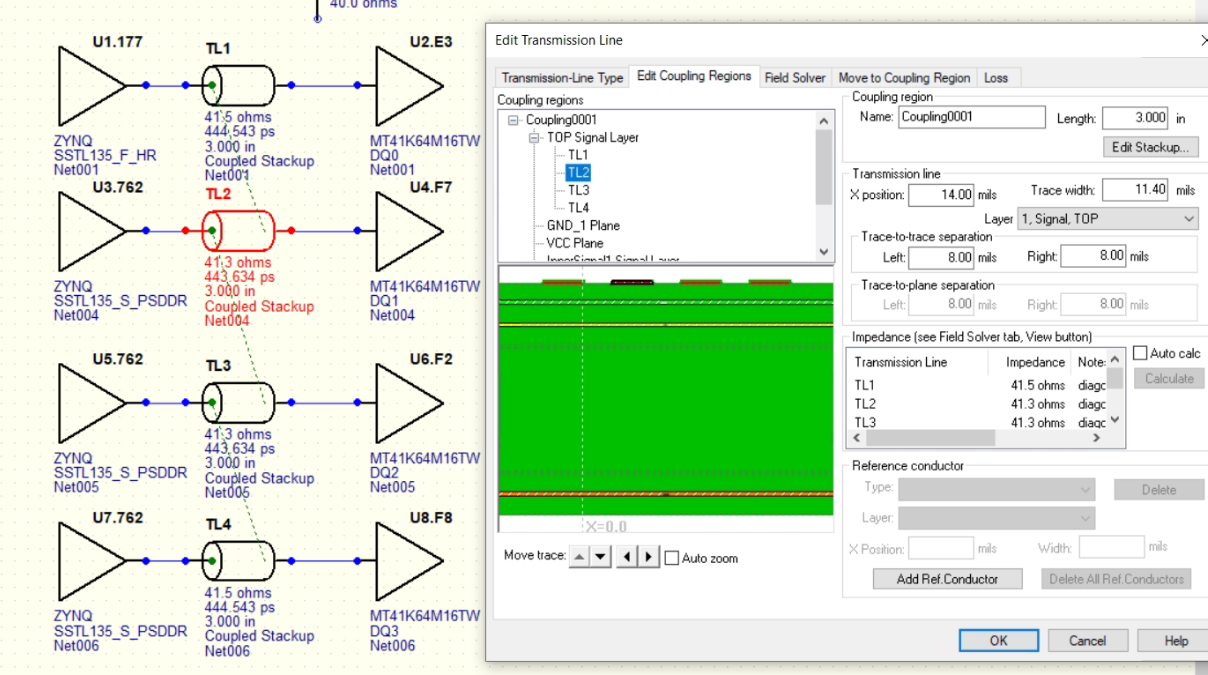
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A screen shot of a computer

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**Zync transmit 4 lames DQ0-DQ3 to DR with internal ODT and coupled TL to 40 ohms:**

**(Xtalk verification)**



Results:

A screen shot of a computer

Description automatically generated

