General Design Guidelines

General

- Trace to trace spacing digital to digital – 5H and at least 3H if you get space issues.
- Trace to Trace spacing – digital to RF – use 20H separation between RF and digital signals and at least 10H if you get space issues.
- Do not split RF and digital grounds to avoid EMI issues, just keep the 20H separation rule above.
- Output resistor terminations length from TX – keep as close as possible to the TX source and do not exceed the lumped length

Power and Decupling

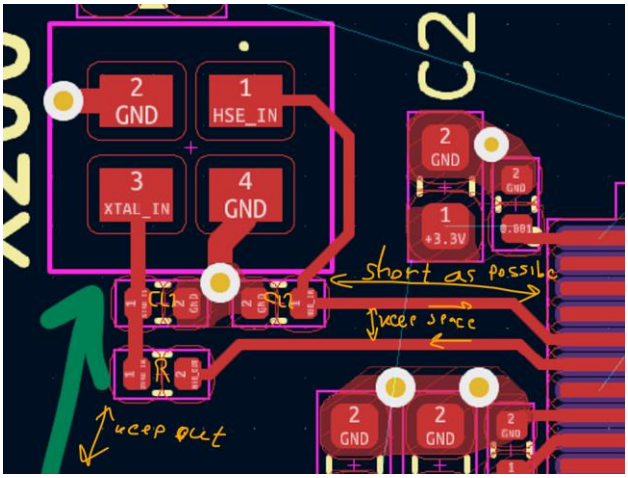
- Place small decupling first close to the power pin, then medium size and then bulk capacitors.
- **Power traces/polygons** – Route the power pins with polygons to the capacitors as wide as possible and min power trace width of **0.3mm trace** –> 1.7[mOhm/mm] –> 1A (PCB Trace width Calculator)
- **LDO Power traces** should be able to provide 2A bursts so keep power traces from the LDO with wide polygons and minimum power trace of **1mm trace** –> 0.8[mOhm/mm] –> 2A (PCB Trace width Calculator)
- PIMIC/LDO input/output caps with small loops and close to the BUCK
- Use reference/stitching vias close to the POWER VIAS
- Keep small loops connection (vias placement tight)
- Keep feedback lines of the buck and the PIMIC away from circuitry.
- Add as many GND vias as possible for better EMI and heat dissipation.
- Switch note only as large as needed for current – (Keep the connection from the buck to the inductor wide enough for the current requirement but not more than that)**. (max width calculation needed here)**
- Place ESD TVS diods as close as possible to the USB connectors.
- **PowerGood and Enable signals are less critical and route it last(before stitching vias)**
- **Power vias**: vias comes in pairs, move vias closer to reduce inductance for smaller loops.
- Split the power plane 4 to the zync voltages.
- Use L8 power polygons for the GSM Power
- Use chassis capacitor and connect all external connectors to the chassis capacitor.
- Decup capacitors priority Analog input(with ferriteBID in PI filter) Vs Digital voltage inputs – place the decup for digital voltage first and after that the Analog voltages(analog voltages are less speed dependent)

Zync Routing

Use "dog-bone" method and fit the trace width dog bone as required for the controlled impedance traces (use the width from the controlled impedance table)

XTAL – critical line

- Placement with no stubs of CL1/2 and R – see example below.
- Keep away from other High speed or PWM signals.
- Keep space large as possible from the consumer input and outputs.
- Keep out from other high speed or critical lines.
- Note this design guide document: XTAL Design guidelines by ABARCON
- Example for XTAL layout and routing:

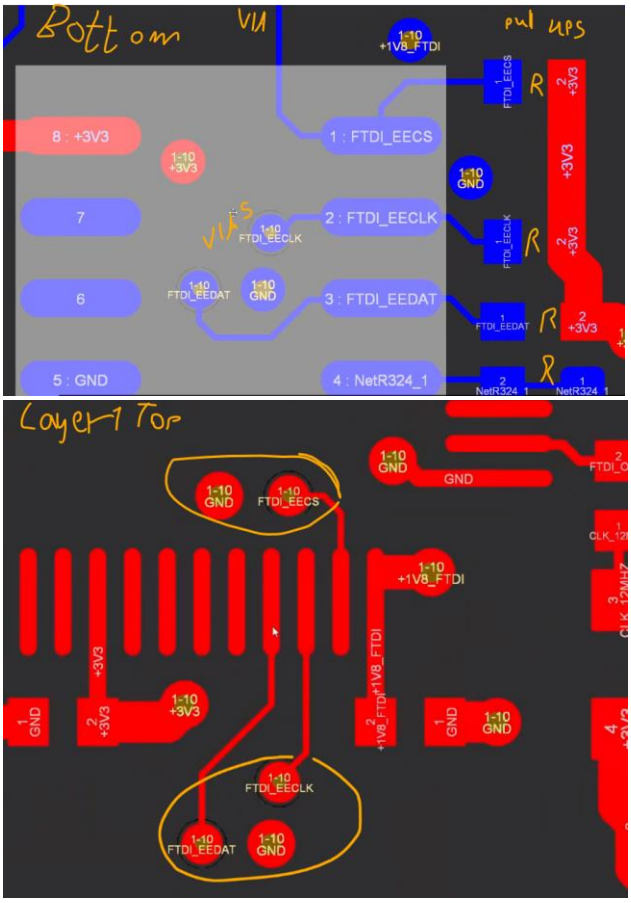


CMOS Oscillator Layout and Routing – Critical line

- Place OSC as close as possible to its consumer and in the resistor.
- Resistor right after and then short trace to the consumer
- Place it in a way that with his resistor there are no stubs.
- Decup oscillator below with short loops
- Oscillator Layout Layout example:

EEPROM Layout and Routing

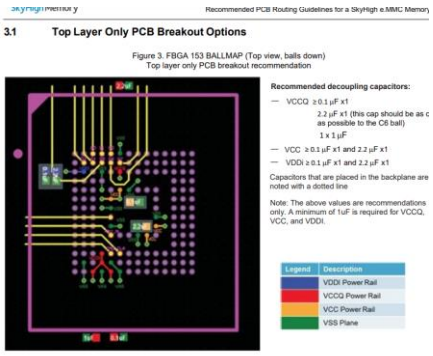
- The EEPROM is not very fast but still try to keep traces short.
- Option to place it in the bottom Layer and then:
  - Decupling close with short loops
  - Pull ups close.
- Example from previous project:



EMMC layout and routing (0.5mm pitch)

- See the attached document "Recommended PCB Routing Guidelines for SHM e.MMC.pdf"
- EMMC is with 0.5mm pitch but most of the pins are NC so can "de-populate" unused pins
- Placement close, up-right to the Zynq(SDIO pins there in upper-left)
- Terminations (pull ups) at the top layer near the EMMC
- Route SDIO traces:
    - to Layer 6 (good for high speed)
    - 50 ohm controlled impedance
    - Traces lengths as short as possible (about 30ps??)
    - Keep spacing between traces – more than the manufacturer limit(as possible)

      For example:



Boot parts guidelines:

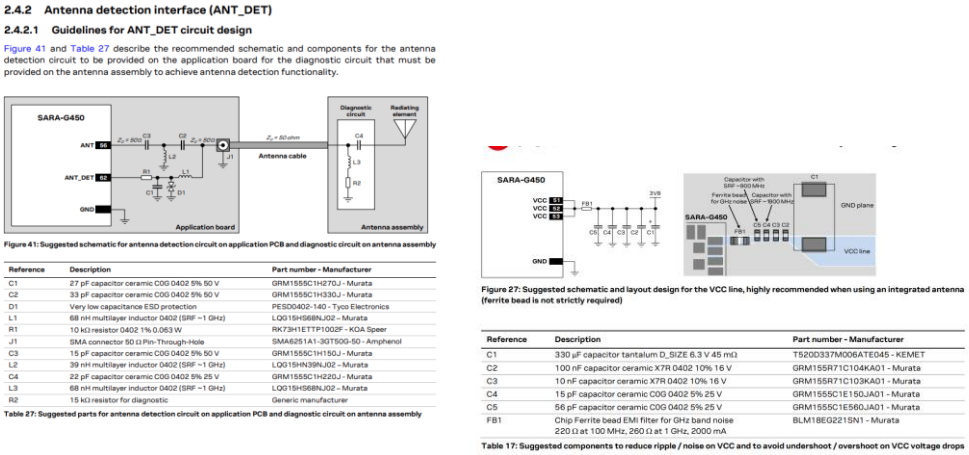
- QSPI Routing:
  - Data lines delay matching
  - QSPI CLK, a bit longer then the QSPI Data lines(and not shorter)
- JTAG Pins as 50 ohms (optional at layer 6 if there is enough space)
- Placement:
  - Place dip switch on the bottom (trough hole VIA) to avoid stubs
  - Place dip switch resistors (3 pull ups and 3 pull downs) near the dip switch on the bottom
  - Place the JTAG header(not used in this project) above the DIP switch on the TOP(avoid stubs)

Differential lines

- More important so first – Intra – pair skew – P to N matching (same diff channel)
- Then – Inter pair skew matching (diff to diff)

GSM part

- Placement on the bottom and route to the power planes on layer
- Keep spacing of 20H of RF signals(GSM and muRata) to digital signals
- Use the placement recommendation drawing in the SARA-G450 - System integration manual for example:



2.4.2 Antenna detection interface (ANT_DET)

2.4.2.1 Guidelines for ANT_DET circuit design

Figure 41 and Table 27 describe the recommended schematic and components for the antenna detection circuit to be provided on the application board for the diagnostic circuit that must be provided on the antenna assembly to achieve antenna detection functionality.

Figure 41: Suggested schematic for antenna detection circuit on application PCB and diagnostic circuit on antenna assembly

Reference	Description	Part number - Manufacturer
C1	27 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H270J - Murata
C2	33 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H330J - Murata
D1	Very low capacitance ESD protection	PESD0402-140 - Tyco Electronics
L1	68 nH multilayer inductor 0402 (SRF ~1 GHz)	LQG15HS68NJ02 – Murata
R1	10 kΩ resistor 0402 1% 0.063 W	RK73H1ETTP1002F - KOA Speer
J1	SMA connector 50 Ω Pin-Through-Hole	SMA6251A1-3GT500-50 - Amphenol
C3	15 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H150J - Murata
L2	39 nH multilayer inductor 0402 (SRF ~1 GHz)	LQG15HN39NJ02 – Murata
C4	22 pF capacitor ceramic C0G 0402 5% 25 V	GRM1555C1H220J - Murata
L3	68 nH multilayer inductor 0402 (SRF ~1 GHz)	LQG15HS68NJ02 – Murata
R2	15 kΩ resistor for diagnostic	Generic manufacturer

Table 27: Suggested parts for antenna detection circuit on application PCB and diagnostic circuit on antenna assembly

Figure 27: Suggested schematic and layout design for the VCC line, highly recommended when using an integrated antenna (ferrite bead is not strictly required)

Reference	Description	Part number - Manufacturer
C1	330 µF capacitor tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
C2	100 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
C3	10 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C4	15 pF capacitor ceramic C0G 0402 5% 25 V	GRM1555C1E150JA01 - Murata
C5	56 pF capacitor ceramic C0G 0402 5% 25 V	GRM1555C1E560JA01 - Murata
FB1	Chip Ferrite bead EMI filter for GHz band noise 220 Ω at 100 MHz, 260 Ω at 1 GHz, 2000 mA	BLM18EG221SN1 - Murata

Table 17: Suggested components to reduce ripple / noise on VCC and to avoid undershoot / overshoot on VCC voltage drops

2.4.2.2 Guidelines for ANT_DET layout design

Figure 42 describes the recommended layout for the antenna detection circuit to be provided on the application board to achieve antenna detection functionality, implementing the recommended schematic described in the previous Figure 41 and Table 27.

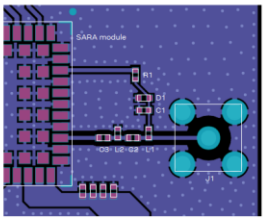


Figure 42: Suggested layout for antenna detection circuit on application board

DDR3L Memory:

- DDR Routing – Zync – > DDR3L –> VTT Resistors –> bypass capacitors
- Route clock signals first
- DDR3 DQ/DM to DQS_P/N skew limit is **50ps** maximum but keep as low as possible.
- DDR3 Address to Clock Skew Limit is **103ps** Maximum but keep as low as possible.
- DDR Traces Length – as short as possible and **8.55" (22cm)** Maximum(UG933)
- VTT resistor **slightly after** the DDR3L RX (and less than a TL length)
- Trace to Trace– spread above the manufacturer limit when space allows.
- DDR differential traces guidelines for **80[ohm]±10%** controlled diff Impedance:
    - See controlled impedance table
- Length matching/Delay matching +–10ps (UG988 table–5–9)
- Via stub Spacing
- Suggested routing layer – layers 6 and 8(8 is preferred due to less stub):

Layer	Type
L1	Signal
L2	GND
L3	POWER
L4	Signal (low speed, PMODS) + Power
L5	GND
L6	Signal (High speed)
L7	GND
L8 DDR	Signal (High speed, less Stub) + Power
L9	GND
L10	Signal

- Layout the following groups with same routing/layout/layer/vias:
    - **ACC_Group:**
        - Address lines [0–14]
        - BA[0–2]
        - CK_P, CK_N, CLKE
        - NCS, RAS,
        - CAS
    - **Data_Group0 – DDR BL0:**
        - DQ[0–7]
        - DDR_DM0
        - DDR_DQS0_N
        - DDR_DQS0_P

- **Data_Group1 – DDR BL1:**
  - DQ[8–15]
  - DDR_DM1
  - DDR_DQS1_N
  - DDR_DQS1_P
- Note 1 – DQ Only – Bytes groups swapping is optional on the Memory device size.
- Note 2 – DQ Only – bits in Bytes groups swapping is optional on the Memory device size.

USB and USB PHY

Route USB to impedance 0f 90 ohm

Impedance calculators

https://www.pcbway.com/pcb_prototype/impedance_calculator.html

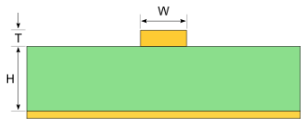
https://www.eeweb.com/tools/microstrip/

Controlled impedance table

Controlled impedance all units in [mm]	Trace Thickness T	substrate height H	trace width W	Spacing S	Substrate Dielectric Er
50 ohm SE **microstrip**	0.035	0.11	0.2	-	4
50 ohm SE **stripline**	0.035	0.11	TBD	-	4.29
40 ohm SE microstrip	0.035	0.11	0.29	-	4
40 ohm SE stripline	0.035	0.11	TBD	-	4.29
80 ohm diff microstrip	0.035	0.11	0.13	0.2	4.9
80 ohm diff Stripline	0.035	0.11	0.3	0.2	4
90 ohm diff(USB) - microstrip	0.035	0.11	0.3	0.2	4.9
90 ohm diff(USB) - stripline	0.035	0.11	TBD	TBD	4.29
100 ohm diff microstrip	0.035	0.11	0.21	0.2	4.29
100 ohm diff stripline	0.035	0.11	TBD	TBD	4.29

microstrip trace to SE 50ohm:

MICROSTRIP IMPEDANCE CALCULATOR



INPUTS

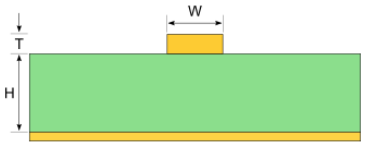
Trace Thickness	T	0.035	mm
Substrate Height	H	0.11	mm
Trace Width	W	0.2	mm
Substrate Dielectric	Er	4	

OUTPUT

Impedance (Z): 50.1 Ohms

Top trace to SE 40ohm:

MICROSTRIP IMPEDANCE CALCULATOR



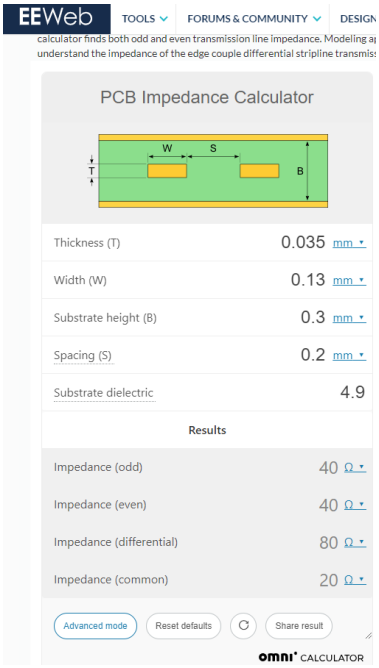
INPUTS

Trace Thickness	T	0.035	mm
Substrate Height	H	0.11	mm
Trace Width	W	0.29	mm
Substrate Dielectric	Er	4	

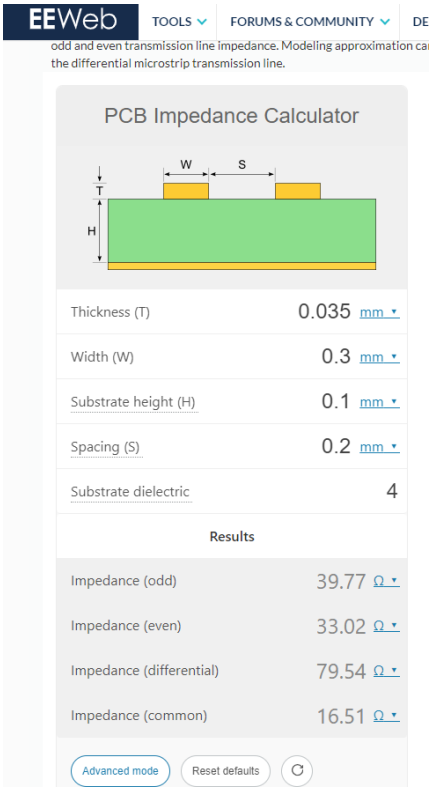
OUTPUT

Impedance (Z): 40.2 Ohms

Internal strip line dimensions diff 80 ohms (DDR)



microstrip dimensions diff 80 ohms (DDR)

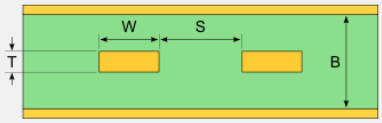


Internal strip line dimensions diff 90 ohms (USB)

EEWeb TOOLS FORUMS & COMMUNITY DESIGN & C

calculator finds both odd and even transmission line impedance. Modeling approx
understand the impedance of the edge couple differential stripline transmission li

PCB Impedance Calculator



Thickness (T)	0.035 mm
Width (W)	0.1 mm
Substrate height (B)	0.3 mm
Spacing (S)	0.2 mm
Substrate dielectric	4.9

Results

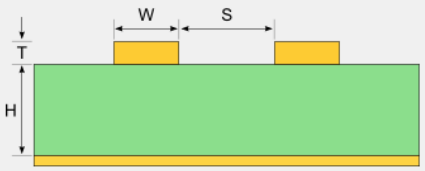
Impedance (odd)	45 Ω
Impedance (even)	45 Ω
Impedance (differential)	90 Ω
Impedance (common)	22.5 Ω

Differential 100 ohm

EEWeb TOOLS FORUMS & COMMUNITY DI

odd and even transmission line impedance. Modeling approximation ca
the differential microstrip transmission line.

PCB Impedance Calculator



Thickness (T)	0.035 mm
Width (W)	0.21 mm
Substrate height (H)	0.1 mm
Spacing (S)	0.2 mm
Substrate dielectric	4

Results

Impedance (odd)	50.44 Ω
Impedance (even)	41.696 Ω
Impedance (differential)	100.89 Ω
Impedance (common)	20.848 Ω

Advanced mode | Reset defaults