

# **CDR – Smart Helmet**

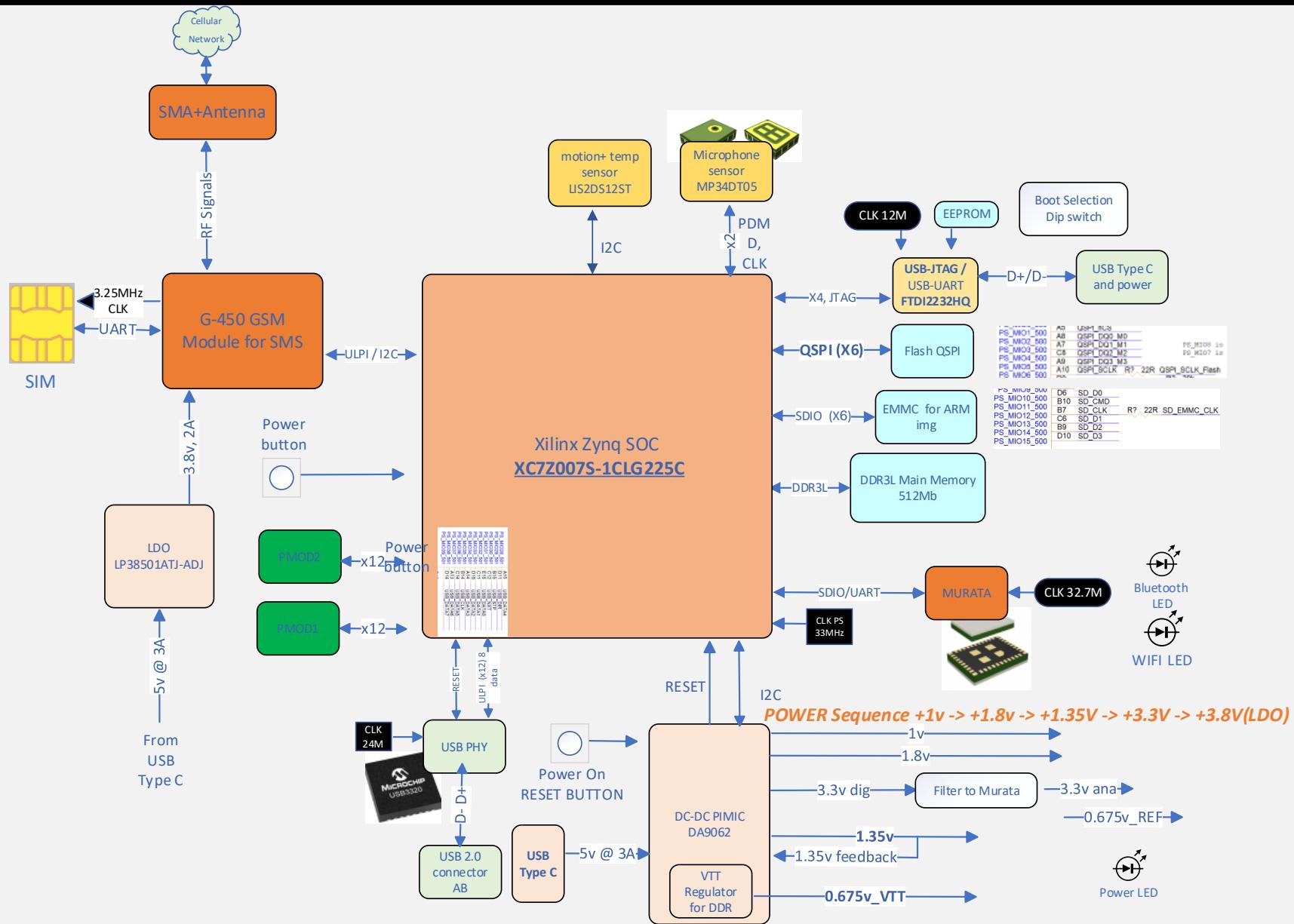
Moshe Saban

# OBJECTIVE

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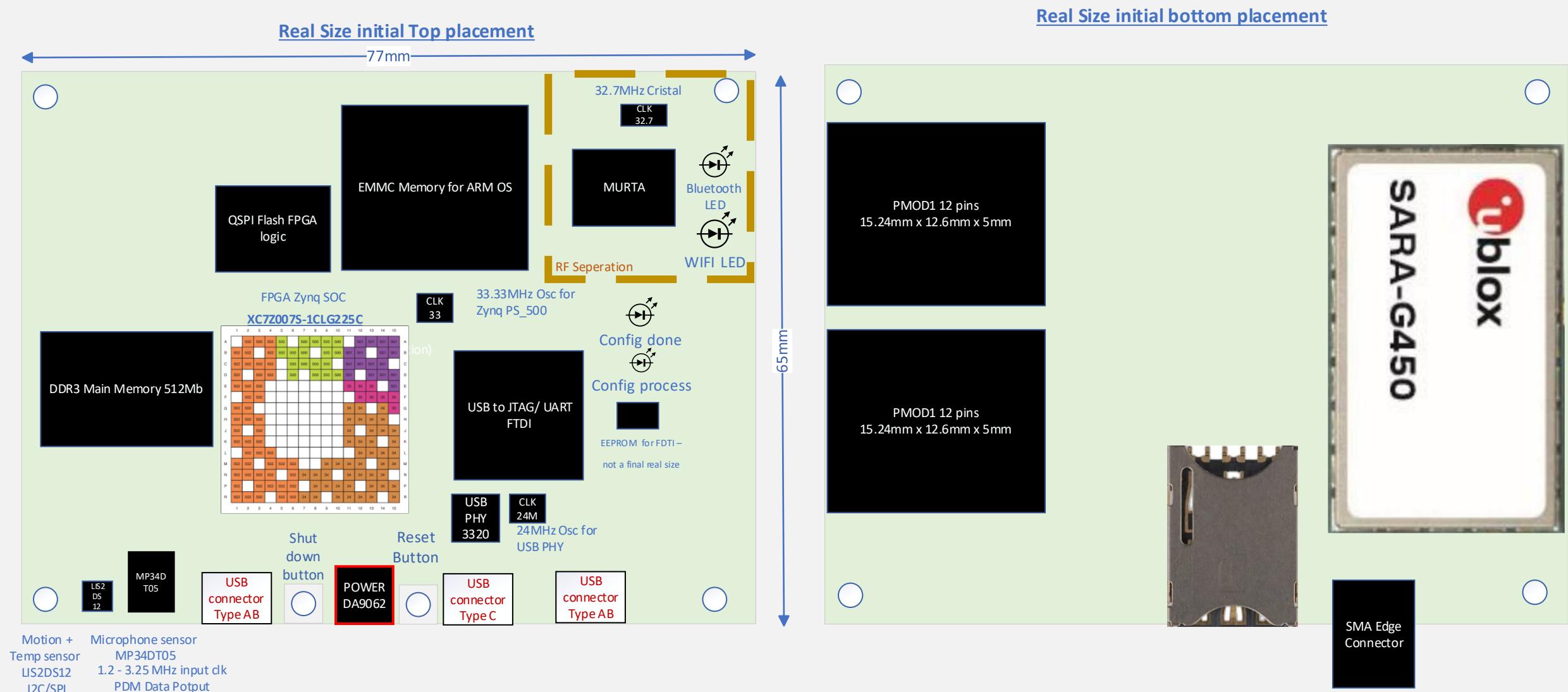
- Providing Smart helmet solution to the growing market of scoot and cycling
  - Drop sensor
  - Microphone
  - Bluetooth
  - PMODs for external peripherals like camera
  - Spec requirement – **EMI – TBD**
  - Spec requirement – **TBD**
  - Added SOS SMS messaging
- Competitors:
  - [Livall EVO21 Smart Helmet](#) – with fall detection and SOS texting with location to a selected and Rear and front lights
  - [KRACESS Bike Helmet](#) – with Bluetooth, video camera recorder, built in microphone and stereo speakers
- Optional – Add Rear and front lights
- Optional – Add **built in** Dash came
- Optional – Add build in stereo speakers for phone calls – consider the safety risk

# Updated Block Diagram



# PLACEMENT suggestion- Real Size

- Note – can extend the PCB sizes to 77mm x 71mm if required



# Build UP from PCB Way Manufacturer

10-layer PCB standard stackup

			1.6mm	2mm	2.4mm	
Thickness	Copper thick (outer/inner)	Layer No.	StackUp			Laminated chart Thickness
2.0mm±10%	1/1oz	L1				Copper 18 um--plating to 35um
		L2				PP 0.12 mm(2116) dielectric constant 4.29 ± (The DK value is not absolute and will vary depending on the base material's models and thickness.)
		L3				Core 0.3mm with 1/1 oz Cu
		L4				PP 0.19 mm(7628) dielectric constant 4.29 ± (The DK value is not absolute and will vary depending on the base material's models and thickness.)
		L5				Core 0.3mm with 1/1 oz Cu
		L6				PP 0.19 mm(7628) dielectric constant 4.29 ± (The DK value is not absolute and will vary depending on the base material's models and thickness.)
		L7				Core 0.3mm with 1/1 oz Cu
		L8				PP 0.19 mm(7628) dielectric constant 4.29 ± (The DK value is not absolute and will vary depending on the base material's models and thickness.)
		L9				Core 0.3mm with 1/1 oz Cu
		L10				PP 0.12 mm(2116) dielectric constant 4.29 ± (The DK value is not absolute and will vary depending on the base material's models and thickness.)

# STUCK UP update – edit to 10 layers

Layer	Type
L1	Signal
L2	GND
L3	POWER
L4	Signal + Power ( Low speed only, PMODs)
L5	GND
L6	Signal (High speed, less Stub)
L7	GND
L8	Signal + Power



Layer	Type
L1	Signal
L2	GND
L3	POWER
L4	Signal (low speed, PMODS) + Power
L5	GND
L6	Signal (High speed)
L7	GND
L8	Signal (High speed, less Stub) + Power
L9	GND
L10	Signal

# STUCK UP and Buildup

Layer	Type	Weight	Thikness	dk
	solder mask		0.2054mm	4
L1	Signal	1oz	0.035mm	
	Prepreg		0.07mm	4
L2	GND	1oz	0.035mm	
	Core		0.15mm	4.7
L3	POWER	1oz	0.035mm	
prepreg	Prepreg		0.133mm	4.7
L4	Signal (low speed, PMODS) + Power	1oz	0.035mm	
	Core		0.15mm	4.7
L5	GND	1oz	0.035mm	
prepreg	Prepreg		0.134mm	4.7
L6	Signal (High speed)	1oz	0.035mm	
	Core		0.15mm	4.7
L7	GND	1oz	0.035mm	
prepreg	Prepreg		0.134nn	4.7
L8	Signal (High speed, less Stub) + Power	1oz	0.035mm	
	Core		0.15mm	4.7
L9	GND	1oz	0.035mm	
	Prepreg		0.07mm	4.7
L10	Signal	1oz	0.035mm	
	solder mask		0.2054mm	4

# Circuits

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- Reset Circuits:
  - PIMIC Hard Reset:
    - Push button to Low -> PIMIC GPIO -> PIMIC RESET\_N output signal to:
      - To FTDI2232
      - To USB PHY
      - To Zync ( PS Bank0)
    - GSM and muRata need to get reset by Software
  - Zync Reset:
    - Push button to Low -> PS\_SRST\_B\_501
- I2C Circuit
  - PS to PIMIC
  - PS to Motion Sensor (pull ups near the sensor)
- JTAG Circuit and boot
  - QSPI to bank0 for initial boot (Boot option 1)
  - FTDI USB to JTAG for debug from external PC (Boot option2)
  - Optional JTAG header, DNP (Boot option3)
  - DIP Switch to switch between the modes Default boot from QSPI:
    - MIO3 '0' (DQ1\_M1) sw1-6 Close
    - MIO4 '0' (DQ2\_M2) sw2-5 Close
    - MIO5 '1' (DQ3\_M3) sw3-4 Open

# Pin Assignment “MIO-At-A-Glance” Table

**Peripheral I/O Pins** Summary Report

**Search:**  !

Bank 0 LVCMS 3.3V | Bank 1 LVCMS 1.8V

**Peripherals**

- Quad SPI Flash
- SRAM/NOR Flash
- NAND Flash
- Ethernet 0
- Ethernet 1
- USB 0
- USB 1
- SD 0
- SD 1
- SPI 0
- SPI 1
- UART 0
- UART 1
- I2C 0
- I2C 1
- CAN 0
- CAN 1
- TTC0
- TTC1
- SWDT
- PJTAG
- TPIU

Pin	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	EMIO
Quad SPI Flash	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	EMIO
SRAM/NOR Flash	SRAM/NOR Flash, addr[0-24]															EMIO																																						
NAND Flash	NAND Flash															EMIO																																						
Enet0	Enet0															EMIO																																						
Enet1	Enet1															EMIO																																						
USB0	USB0 <b>USB PHY</b>															USB1																																						
SD0	SD0															SD0																																						
SD1	SD1															SD1																																						
SPI0	SPI0 mos															SPI0 mos															SPI0 mos																							
SPI1	SPI1															SPI1															SPI1																							
UART0	UART0															UART0															UART0																							
UART1	UART1															UART1															UART1																							
I2C0	I2C0															I2C0															I2C0																							
I2C1	I2C1															I2C1															I2C1																							
CAN0	CAN0															CAN0															CAN0																							
CAN1	CAN1															CAN1															CAN1																							
TTC0	TTC0															TTC0															TTC0																							
TTC1	TTC1															TTC1															TTC1																							
SWDT	SWDT															SWDT															SWDT																							
PJTAG	PJTAG															PJTAG															PJTAG																							
Trace	Trace															Trace															Trace																							

*Handwritten annotations:*

- “BOOT QSPI” is written over the Quad SPI Flash row.
- “BOOT EMMC” is written over the SD1 row.
- “USB PHY” is written over the USB0 row.
- “I2C0” is circled in blue and labeled “PMOD”.
- “I2C1” is circled in blue and labeled “PMOD”.
- “I2C1” is circled in blue and labeled “PMOD”.
- “CAN1” is circled in blue and labeled “PMOD”.
- “TTC0” is circled in blue and labeled “PMOD”.
- “TTC1” is circled in blue and labeled “PMOD”.
- “SWDT” is circled in blue and labeled “PMOD”.
- “Pjtag” is circled in blue and labeled “PMOD”.
- “Trace” is circled in blue and labeled “PMOD”.
- A blue circle highlights pins 48 and 49, with the label “To PMODs” above them.

# **End CDR**

More slides for review below

Draft

# DDR3L Memory considerations

- Maximum clock 933MHz => DDR max speed is 1866Mb/s (Double Rate rise+fall sampling) which is more than our FPGA can handle(max is 1600 based on ViVado “memory part – custom” selection)
- According to the Memory data sheet – the DDR is backwards compatible to 1600Mb/s

Table 1: Key Timing Parameters					
Speed Grade	Data Rate (MT/s)	Target tRCD-tRP-CL	tRCD (ns)	tRP (ns)	CL (ns)
-093 <sup>1,2</sup>	2133	14-14-14	13.09	13.09	13.09
-107 <sup>1</sup>	1866	13-13-13	13.91	13.91	13.91
-125	1600	11-11-11	13.75	13.75	13.75

Notes: 1. Backward compatible to 1600, CL = 11 (-125)  
2. Backward compatible to 1866, CL = 13 (-107).

- My Zync DDR controller **clock** speed bin is up to 533MHz (**DDR3-1066Msamples/s**)
- DDR3 DQ/DM to DQS skew limit is 50ps maximum
- DDR3 Address to Clock Skew Limit is 103ps Maximum

Name	Selected	Description
Memory Type	DDR 3 (Low Voltage)	Type of memory interface. Refer to UG5
Memory Part	Custom	Memory component part number. For u
Effective DRAM Bus Width	32 Bit	Data width of DDR interface, not includ
ECC	Disabled	Enables error correction code support.
Burst Length	8	Minimum number of data beats the co
DDR	533.333333	Memory clock frequency. The allowed fr
Internal Vref	□	Enables internal voltage reference sou
Junction Temperature (C)	Normal (0-85)	Intended operating temperature range.
Memory Part Configuration		
DRAM IC Bus Width	8 Bits	Width of individual DRAM components.
DRAM Device Capacity	2048 MBits	Storage capacity of individual DRAM co
Speed Bin	DDR3 1066F	Speed bin of the individual DRAM comp
Bank Address Count (Bits)	DDR3 1056F	Number of bank address pins.
Row Address Count (Bits)	DDR3 1056G	Number of row address pins.
Col Address Count (Bits)	DDR3 1333F	Number of column address bits.
	DDR3 1333G	
	DDR3 1333H	
	DDR3 1333J	
	DDR3 1600G	
	DDR3 1600H	
	DDR3 1600J	

XILINX® Appendix A: Processing System Memory Derating Tables							
Table A-3: DDR3 DQ/DM to DQS Skew Limit		Memory Component Rating					
SoC Rating	Actual	2,133	1,866	1,600	1,333	1,066	800
1,333	1,333	69	56	15	10	N/A	N/A
	1,066	150	150	109	104	69	N/A
	800	150	150	150	150	150	150
1,066	1,066	104	91	50	45	10	N/A
	800	150	150	150	150	150	150
800	800	150	150	113	107	72	10

Table A-4: DDR3 Address to Clock Skew Limit							
SoC Rating	Actual	2,133	1,866	1,600	1,333	1,066	800
1,333	1,333	60	50	30	10	N/A	N/A
	1,066	150	150	150	150	125	N/A
	800	150	150	150	150	150	150
1,066	1,066	133	123	103	83	10	N/A
	800	150	150	150	150	150	150
800	800	150	150	150	150	85	10

# DDR3L Memory considerations

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- DDR3 DQ/DM to DQS\_P/N skew limit is **50ps** maximum but keep as low as possible
  - DDR3 Address to Clock Skew Limit is **103ps** Maximum but keep as low as possible
  - DDR Traces Length – place as close as possible and **8.55" (22cm)** Maximum
- 
- Place VTT Termination resistors close to the RX
  - Trace to Trace– spread above the manufacturer limit when space allows

# DDR3L Memory Routing and Layout

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- DDR Routing – Zync -> DDR3L -> VTT Resistors -> bypass capacitors
- Suggested routing layer – layer 6 since has both upper and bottom GND reference
- VTT resistor **slightly after** the DDR3L RX (less than a TL length)
- VTT Pull up resistors size 0201
- DDR ACC/DQ SE traces guidelines for  $40[\text{ohm}]\pm10\%$  SE – controlled SE Impedance:
  - Space from GND is (**see sizes table for 40ohm SE**)
  - Trace width – (**see sizes table for 40ohm SE**)
- DDR differential traces guidelines for  $80[\text{ohm}]\pm10\%$  controlled diff Impedance:
  - Space from GND is
  - Trace width – (**see sizes table for 80ohm differential**)
  - Differential Spacing S – (**see sizes table for 80ohm differential**)
- Length matching
- Via stub Spacing

# Boot

- Default boot from QSPI dip switch:**
  - MIO3 '0' (DQ1\_M1) sw1-6 Close
  - MIO4 '0' (DQ2\_M2) sw2-5 Close
  - MIO5 '1' (DQ3\_M3) sw3-4 Open
- Additional JTAG Boot 1 for debug:**
  - From USB trough FTDI JTAG output:
  - MIO3 '0' (DQ1\_M1) sw1-6 Close
  - MIO4 '0' (DQ2\_M2) sw2-5 Close
  - MIO5 '0' (DQ3\_M3) sw3-4 Close
- Additional JTAG Boot 2 for debug:**
  - From JTAG Header trough Xilinx red BOX("Xilinx Platform Cable")
  - or "Digilent JTAG Cable":
  - Place the DNP 22 ohm resistors near the JTAG Header, and:
  - MIO3 '0' (DQ1\_M1) sw1-6 Close
  - MIO4 '0' (DQ2\_M2) sw2-5 Close
  - MIO5 '0' (DQ3\_M3) sw3-4 Close

Table 6-4: Boot Mode MIO Strapping Pins

Pin-signal / Mode	MIO[8] VMODE[4]	MIO[7] VMODE[0]	MIO[6] BOOT_MODE[4]	MIO[5] BOOT_MODE[0]	MIO[4] BOOT_MODE[2]	MIO[3] BOOT_MODE[1]	MIO[2] BOOT_MODE[3]				
Boot Devices											
JTAG Boot Mode; cascaded is most common <sup>(1)</sup>			0	0	0						
NOR Boot <sup>(3)</sup>			0	0	1						
NAND			0	1	0						
Quad-SPI <sup>(3)</sup>			1	0	0						
SD Card			1	1	0						
Mode for all 3 PLLs											
PLL Enabled			0	Hardware waits for PLL to lock, then executes BootROM.							
PLL Bypassed			1	Allows for a wide PS_CLK frequency range.							
MIO Bank Voltage <sup>(4)</sup>											
	Bank 1	Bank 0	Voltage Bank 0 includes MIO pins 0 thru 15. Voltage Bank 1 includes MIO pins 16 thru 53.								
2.5 V, 3.3 V	0	0									
1.8 V	1	1									

Notes:

1. JTAG cascaded mode is most common and is the assumed mode in all the references to JTAG mode except where noted.

# Boot design

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- QSPI Routing:
  - Data lines delay matching
  - QSPI CLK, a bit longer then the QSPI Data lines(and not shorter)
- JTAG Pins as 50 ohms ( optional at layer 6 if there is enough space)
- Placement :
  - Place dip switch on the bottom(trough hole VIA) to avoid stubs
  - Place dip switch resistors (3 pull ups and 3 pull downs) near the dip switch on the bottom
  - Place the JTAG header above the DIP switch on the TOP(avoid stubs)

# DDR3L Memory Routing and Layout

Layers to route – L6 is the best option, then bottom or top. Avoid placing DDR traces in L4

Layout the following groups with same routing/layout/layer/vias:

- ACC\_Group:

- Address lines[0-14]
- BA[0-2]
- CK\_P, CK\_N, CLKE
- NCS, RAS,
- CAS

- Data\_Group0 – DDR BL0:

- DQ[0-7]
- DDR\_DM0
- DDR\_DQS0\_N
- DDR\_DQS0\_P

- Data\_Group1 – DDR BL1:

- DQ[8-15]
- DDR\_DM1
- DDR\_DQS1\_N
- DDR\_DQS1\_P

Layer	Type
L1	Signal
L2	GND
L3	POWER
L4	Signal + Power ( Low speed signals)
L5	GND
L6	Signal (High speed, less Stub)
L7	GND
L8	Signal

- Note 1 – DQ Only – Bytes groups swapping is optional on the Memory device size

- Note 2 – DQ Only – bits in Bytes groups swapping is optional on the Memory device size

# Power bypass caps for DDR controller

- ByPass Ztarget is 100KHz-1000MHz according to UG933

## Recommended PCB Capacitors per Device

A simple PCB-decoupling network for the Zynq-7000 SoC devices is listed in [Table 3-1](#) and [Table 3-2](#). The optimized quantities of PCB decoupling capacitors assumes that the voltage regulators have stable output voltages and meet the regulator manufacturer's minimum output capacitance requirement.

Decoupling methods other than those presented in these tables can be used, but the decoupling network should be designed to meet or exceed the performance of the simple decoupling networks presented here. The impedance of the alternate network must be less than or equal to that of the recommended network across frequencies from 100 KHz to 100 MHz.

Because device capacitance requirements vary with CLB and I/O utilization, PCB decoupling guidelines are provided on a per-device basis.  $V_{CCINT}$ ,  $V_{CCAUX}$ ,  $V_{CCAUX\_IO}$ ,  $V_{CCBRAM}$ , and PS supply capacitors are listed as the quantity per device, while  $V_{CCO}$  capacitors are listed as

**Table 3-2: Required PCB Capacitor Quantities per Device (PS)**

Zync PL

# Zync PL

- Banks 34 and 35
- Connection with the GSM module
- Connection with the user PMOD extension pins
- Knowledge complete:
  - PMOD Pins configurations?
  - PMOD Power to supply form the Zync
  - PMOD Clk to supply from the ZYNC?(I have refence for that in lesson7)

**FPGA Zynq SOC**  
**XC7Z007S-1CLG225C**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A		502	502	502	500		500	500	500	500		501	501	501	501	A
B	502	502		502	500	500	500		500	500	501	501		501	501	B
C	502	502	502	502		500	500	500	500		501	501	501	501		C
D	502		502	502		500	500	500	500	501		501	501	501	501	D
E	502	502	502								35	35	35		501	E
F		502	502								35	35	35	35		F
G	502	502									34	34		34	35	G
H	502	502	502								34	34	34	34		H
J	502		502								34		34	34	34	J
K	502	502	502								34	34	34		34	K
L		502	502	502							34	34	34	34	34	L
M	502	502		502	502	502				34	34	34	34		34	M
N	502	502	502	502		502	34	34	34		34	34	34	34		N
P	502		502	502	502	502		34	34	34	34		34	34	34	P
R	502	502	502		502	502	34	34		34	34	34	34		34	R

# FTDI

[https://www.youtube.com/watch?v=NkD\\_FACLgpQ](https://www.youtube.com/watch?v=NkD_FACLgpQ)

# FT2232 (FTDI) key points

- USB High Speed to Dual Interface. The FT2232H is a USB 2.0 High Speed (480Mbit/s) to dual independent flexible and configurable parallel/ interfaces.
- I will use FT2232H pins used in an MPSSEa (Multi-Protocol Synchronous Serial Engine) with
  - Channel A for JTAG programming
  - Channel B for UART communication
- USB < D-D+> USB to serial interface(FTDI) <JTAG or UART or I2C or SPI or RS232> CPU
- The FT2232H also includes :
  - an integrated +1.8V @150mA Low Drop-Out (LDO) regulator
  - A 12MHz to 480MHz PLL
  - 4kbytes Tx and Rx data buffers per interface
  - The FT2232H effectively integrates the entire USB protocol on a chip with no firmware required.
  - UTMI PHY to handle the USB high speed Serdes – up to USB2.0 480Mbit/s (**no USB PHY is required here**)
  - EEPROM interface – without EEPROM, the FTDI defaults to a USB to dual asynchronous serial port device(**we want JTAG which is synchronous so we must use the EEPROM**)
  - **EEPROM 9356 by microchip was selected**
  - Voltage levels(all TYP, IO Strength =12mA):
    - **V<sub>OH</sub>=3.22v**
    - **V<sub>IL</sub>=0.08v**

**EEPROM Interface.** When used without an external EEPROM the FT2232H defaults to a USB to dual asynchronous serial port device. Adding an external 93C46 (93C56 or 93C66) EEPROM allows each of the chip's channels to be independently configured as a serial UART (RS232 mode), parallel FIFO (245) mode or fast serial (opto isolation). The external EEPROM can also be used to customise the USB VID, PID, Serial Number, Product Description Strings and Power Descriptor value of the FT2232H for OEM applications. Other parameters controlled by the EEPROM include Remote Wake Up, Soft Pull Down on Power-Off and I/O pin drive strength.

The EEPROM should be a 16 bit wide configuration such as a Microchip 93LC46B or equivalent capable of a 1Mbit/s clock rate at VCC = +3.0V to 3.6V. The EEPROM is programmable in-circuit over USB using a utility program called [FT PROG](#). This allows a blank part to be soldered onto the PCB and programmed as part of the manufacturing and test process.

Parameter	Description	Minimum	Typical	Maximum	Units
Voh	Output Voltage High	2.40	3.14		v
			3.20		v
			3.22		v
			3.22		v
Vol	Output Voltage Low	0.12	0.18	0.40	v
			0.08		v
			0.07		v
Channel A Pin No.					
24,23,22, 21, 19,18,17, 16	4	Vil	Input low Switching Threshold	-	0.80 v
26		Vih	Input High Switching Threshold	2.00	- v
27		Vt	Switching Threshold	1.50	v

when Synchronous channel B is then configuration is sw transfer before con default mode (D7: WR# are inputs a configure the chan channel B pins driv any switching of c set\_data\_bits cor

The MPSSE car D2XX\_Programmer MPSSE.

# FTDI EEPROM and drivers

- EEPROM Layout:
  - No layout specific requests for the DS
  - Decoup first and as close as possible
  - Clk far from other high speed and far from the XTAL 12MHz for the FTDI
- EEPROM Programming:
  - The EEPROM is programmable in-circuit over USB using a utility program called FT\_PROG.
- Install FTDI Drivers in the connected PC (VCP drivers section in the FTDI website)

Operating System	Release Date	X86 (32-Bit)	X64 (64-Bit)	PPC	ARM	MIPSII	MIPSIV	SH4	Comments
Windows*	2017-08-30	<a href="#">2.12.28</a>	<a href="#">2.12.28</a>	-	-	-	-	-	WHQL Certified. Includes VCP and D2XX. Available as a <a href="#">setup executable</a> . Please read the <a href="#">Release Notes</a> and <a href="#">Installation Guides</a> .
Linux	-	-	-	-	-	-	-	-	All FTDI devices now supported in Ubuntu 11.10, kernel 3.0.0-19 Refer to <a href="#">TN-101</a> if you need a custom VCP VID/PID in Linux VCP drivers are integrated into the <a href="#">kernel</a> .

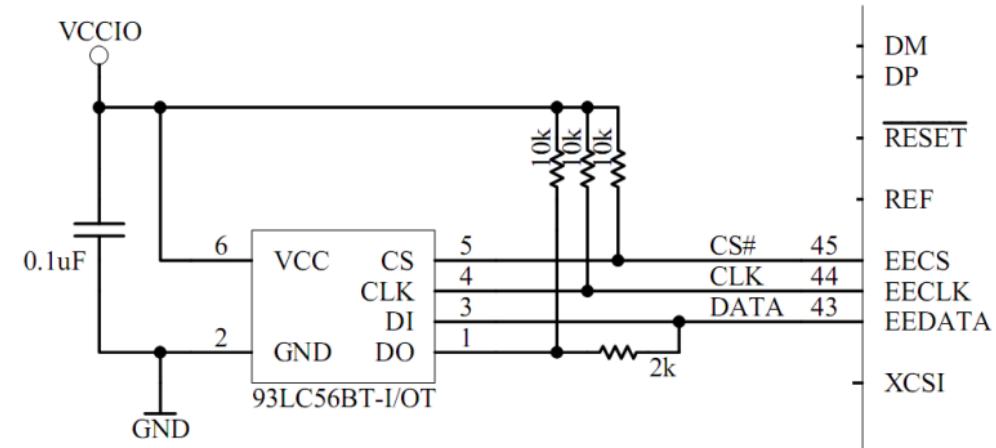
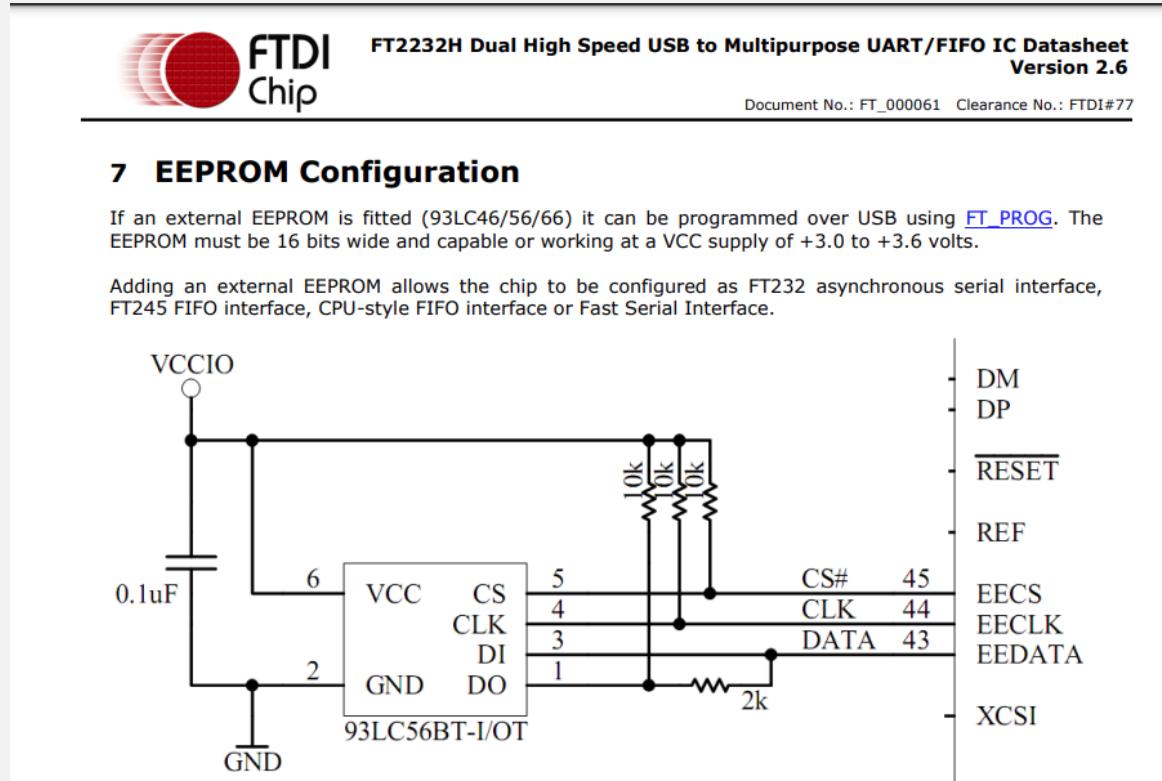


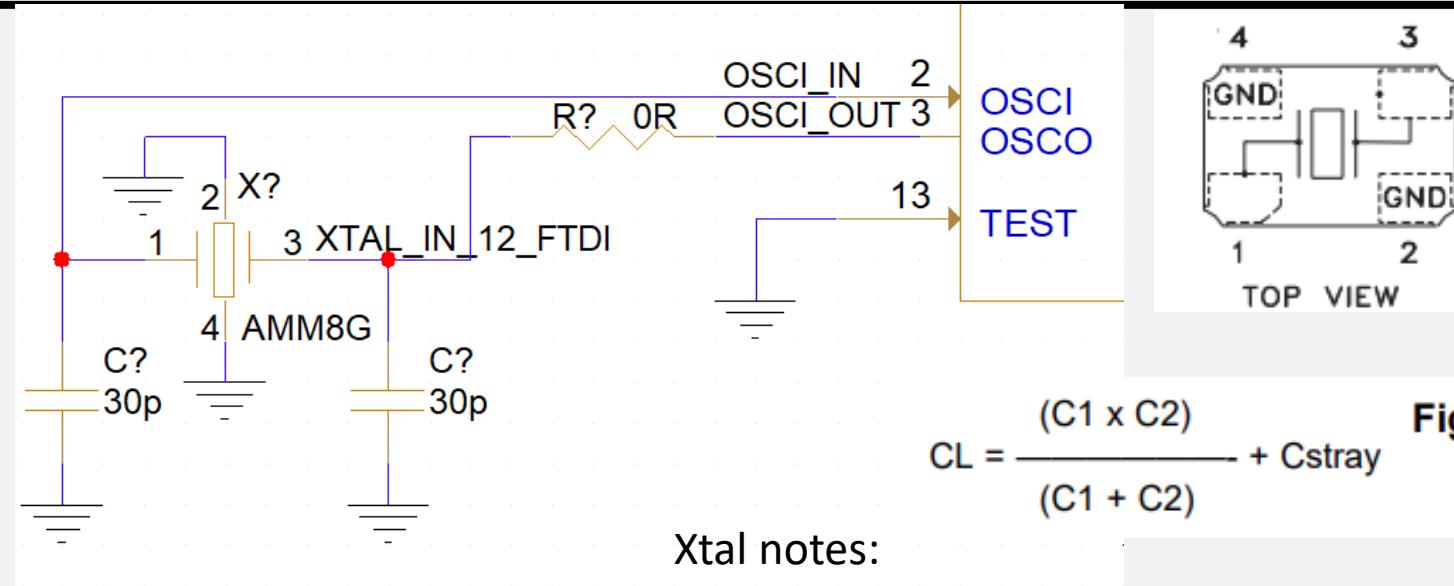
Figure 7.1 EEPROM Interface

The external EEPROM can also be used to customise the USB VID, PID, Serial Number, Product Description Strings and Power Descriptor value of the FT2232H for OEM applications. Other parameters controlled by the EEPROM include Remote Wake Up, Soft Pull Down on Power-Off and I/O pin drive strength.

If the FT2232H is used without an external EEPROM the chip defaults to a USB to FT232 asynchronous serial interface port device. If no EEPROM is connected (or the EEPROM is blank), the FT2232H uses its built-in default VID (0403), PID (6010) Product Description and Power Descriptor Value. In this case, the device will not have a serial number as part of the USB descriptor.

# FTDI XTAL

- [ABRACON manufacturer](#)
- [XTAL Design guidelines by ABARCON](#)
- XTAL – Design Guidelines – [Link](#)
- CL\_1\_2 XTAL rule of thumb:
  - $CL_{1/2} = (CL\_Data\_Sheet - Cstarw/C0) * 2$
  - $CL_{1/2} = (10\text{pF} - 5\text{ps}) * 2 = 10\text{PF}$
- Will use 30PF because of
  - DC voltage derating
  - Capacitance Tolerance
  - XTAL Manufacturer recommendations
- Will place series resistance to:
  - reduce unwanted harmonies
  - Reduce rise/fall time
  - Value 0 ohm for now



Xtal notes:

$$F_0 = 12\text{MHz}$$

$$C_0 = 5\text{pF}$$

$$ESR = 120\text{ohm}$$

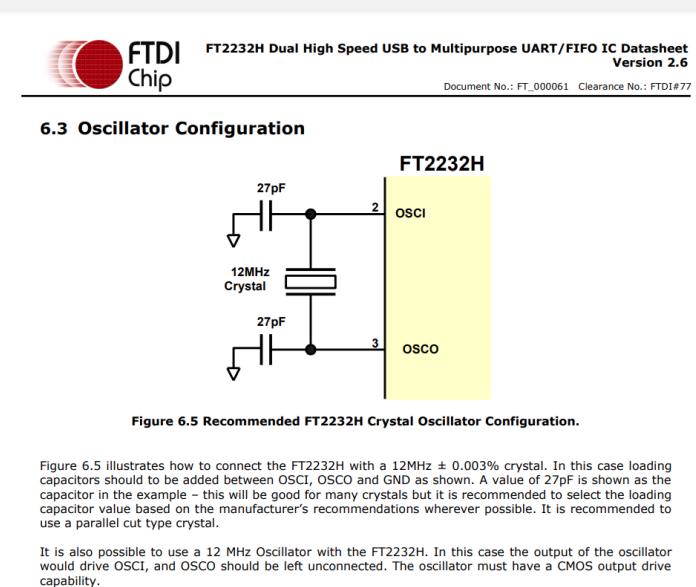
$$R_{ext} = 10\% \text{ from:}$$

$$1/(2*\pi*F_0*C_0) = 1326$$

$$R_{ext} = 130\text{ohm} \text{ (can use 100ohm)}$$

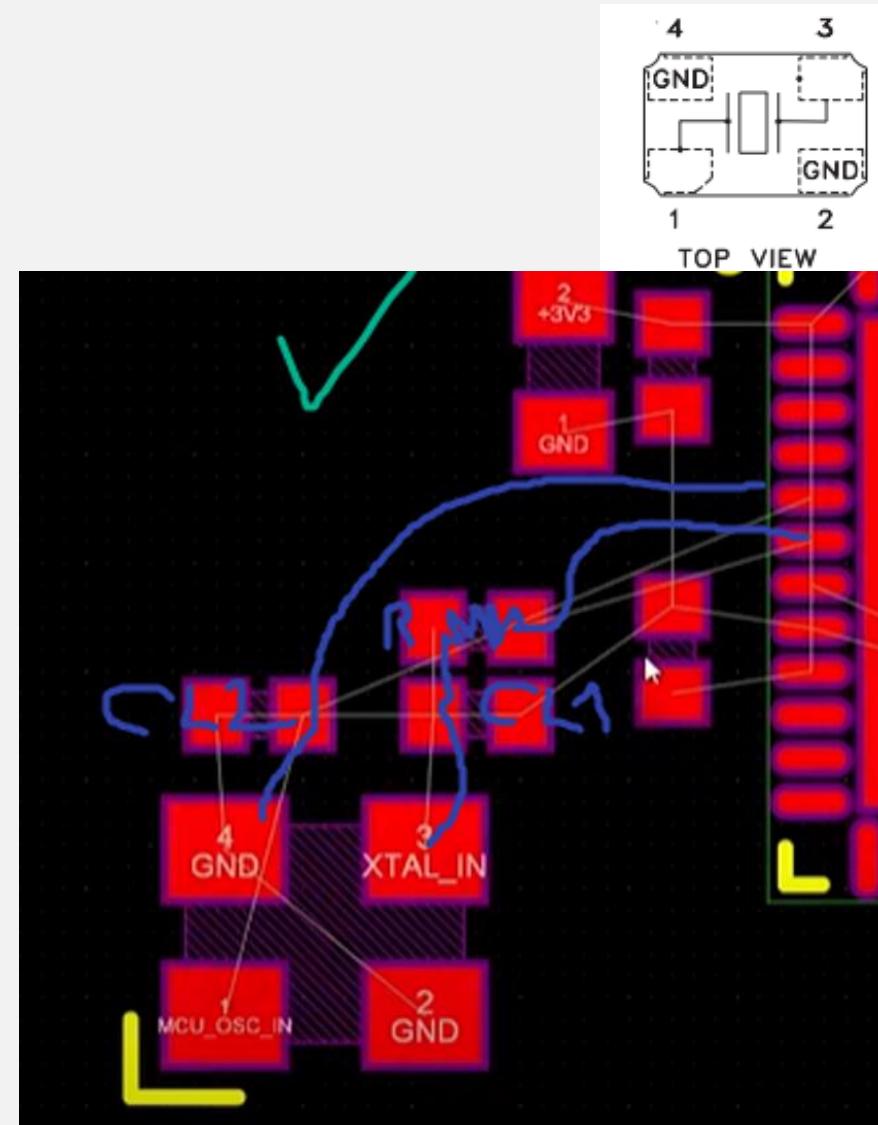
CS is the straw capacitance and it's 3-5PF

$$CL = CL_1 = CL_2 = 2*(C_0 - CS) = 10-14\text{pF}$$



# FTDI XTAL Design guidelines

- Place as close as possible to the FT2232 with short traces
- Place capacitors with short loops but with no stubs



# USB

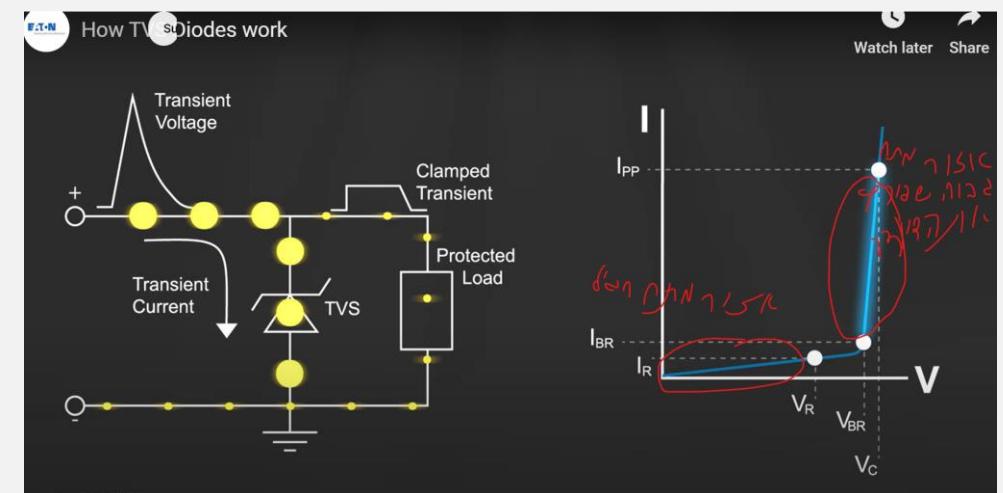
- USB typeC Application note [TA0357](#)

	<p><b>Mfr. Part No.</b> <a href="#">GSB1C41111DS1HR</a></p> <p><b>ouser Part No</b> 523-GSB1C41111DS1HR</p> <p> New Product</p>	<p>Amphenol Canada</p>	<p>USB Connectors USB2.0 TYPE C</p> <p><a href="#">Learn More</a></p>	 <a href="#">Datasheet</a>	<p>9,838 In Stock</p>	<p>Cut Tape 1: \$0.86 10: \$0.702 25: \$0.687 100: \$0.627 Reel 1,000: \$0.478 2,000: <a href="#">View</a></p>	<input type="button" value="Buy"/> <p>Min.: 1 Mult.: 1 Reel: 1,000</p>	 <a href="#">3D Model</a>
---	--	----------------------------	---	---	---------------------------	--	---	--

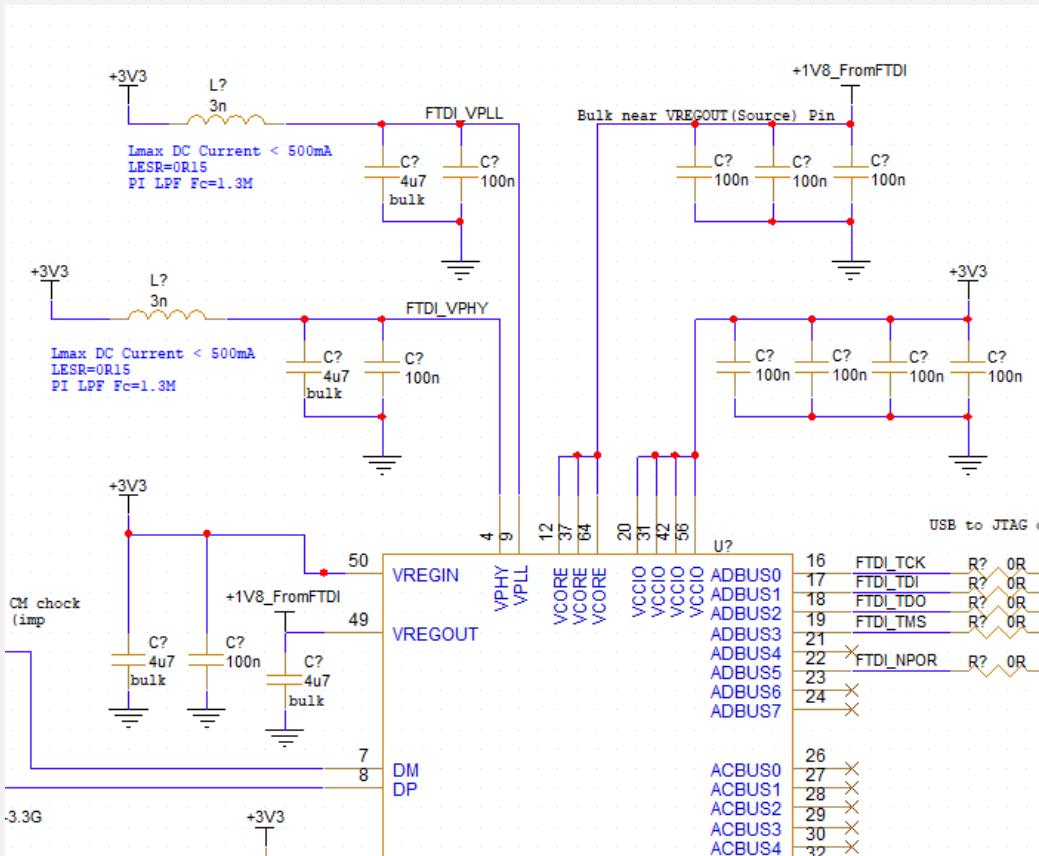
# TVS Diodes

TVS Diode considerations:	<u>option 1 Bourns</u>	option 2
• Low capacitance to minimize line delay	0.05pF	101pF(for 3.3V)
• Bi-directional	yes	yes
• Minimum power consumption (Leakage current, Power loss)	<5nA	IRM < 0.09uA
• Low Clamping voltage	25v	26v
• How much ESD voltage are they good for?	<15kV	<23kV

- TVS Diodes layout and routing
  - Place the diode as close as possible to the connector
  - Place it in a way that there are no subs



# FTDI VPHY VPLL Power filtering



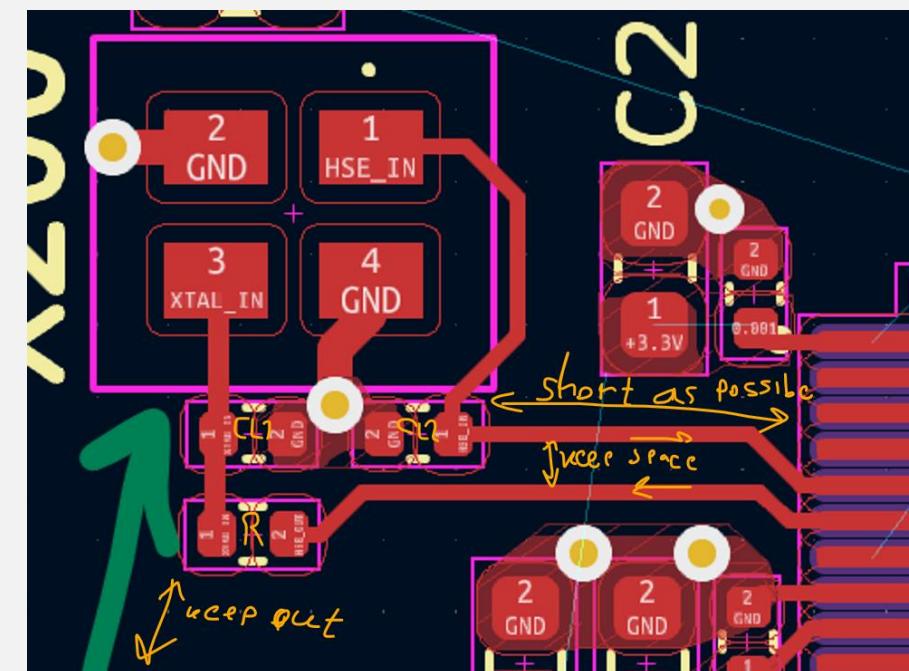
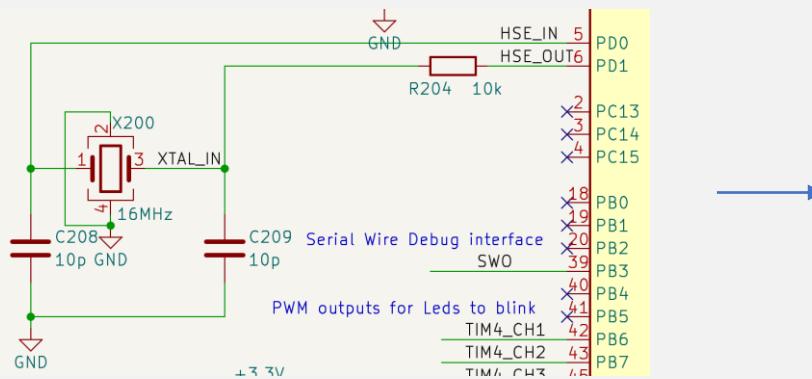
# OSCILATOR Layout and Routing

- Oscillator Layout and Routing
  - Place OSC as close as possible to its consumer and in the resistor.
  - Resistor right after and then short trace to the consumer
  - Place it in a way that with his resistor there are no stubs.
  - Dec up oscillator below with short loops
  - Oscillator Layout Layout example:



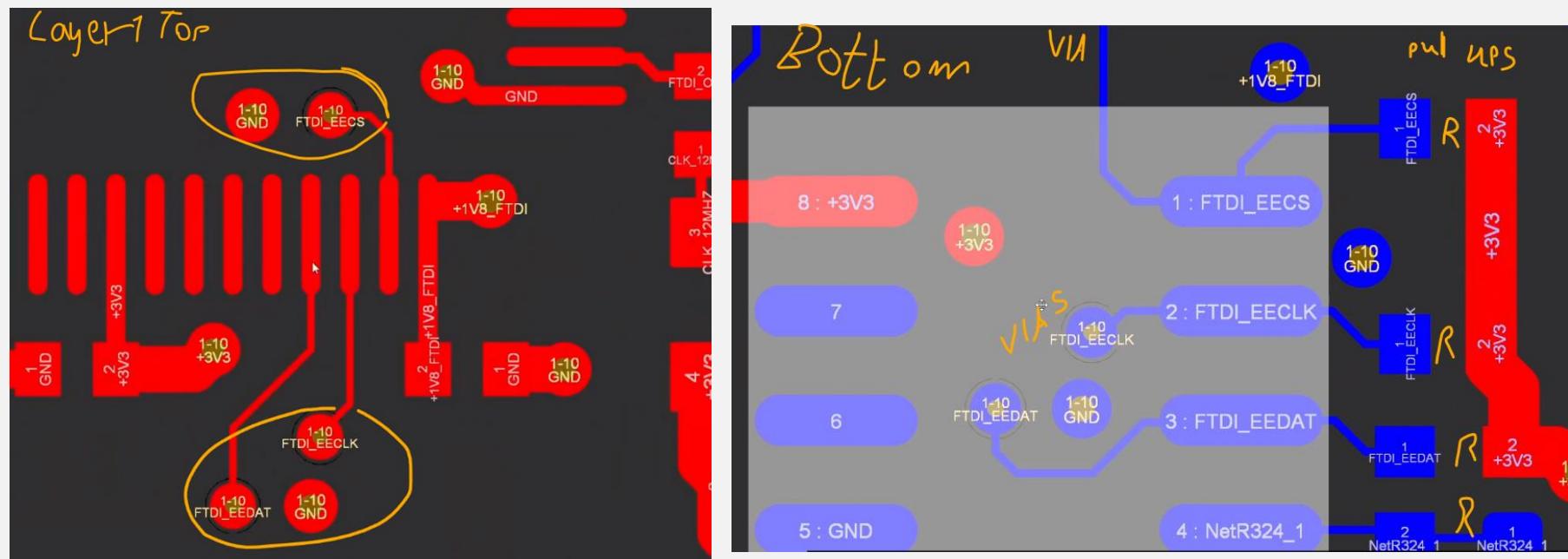
# XTAL Layout And Routing

- XTAL is a critical line
- Placement with no stubs of CL1/2 and R – see example from previous projects
- Keep away from other High speed or PWM signals
- Keep space as possible from the consumer input and outputs
- Keep out from other high speed or critical lines
- Example:

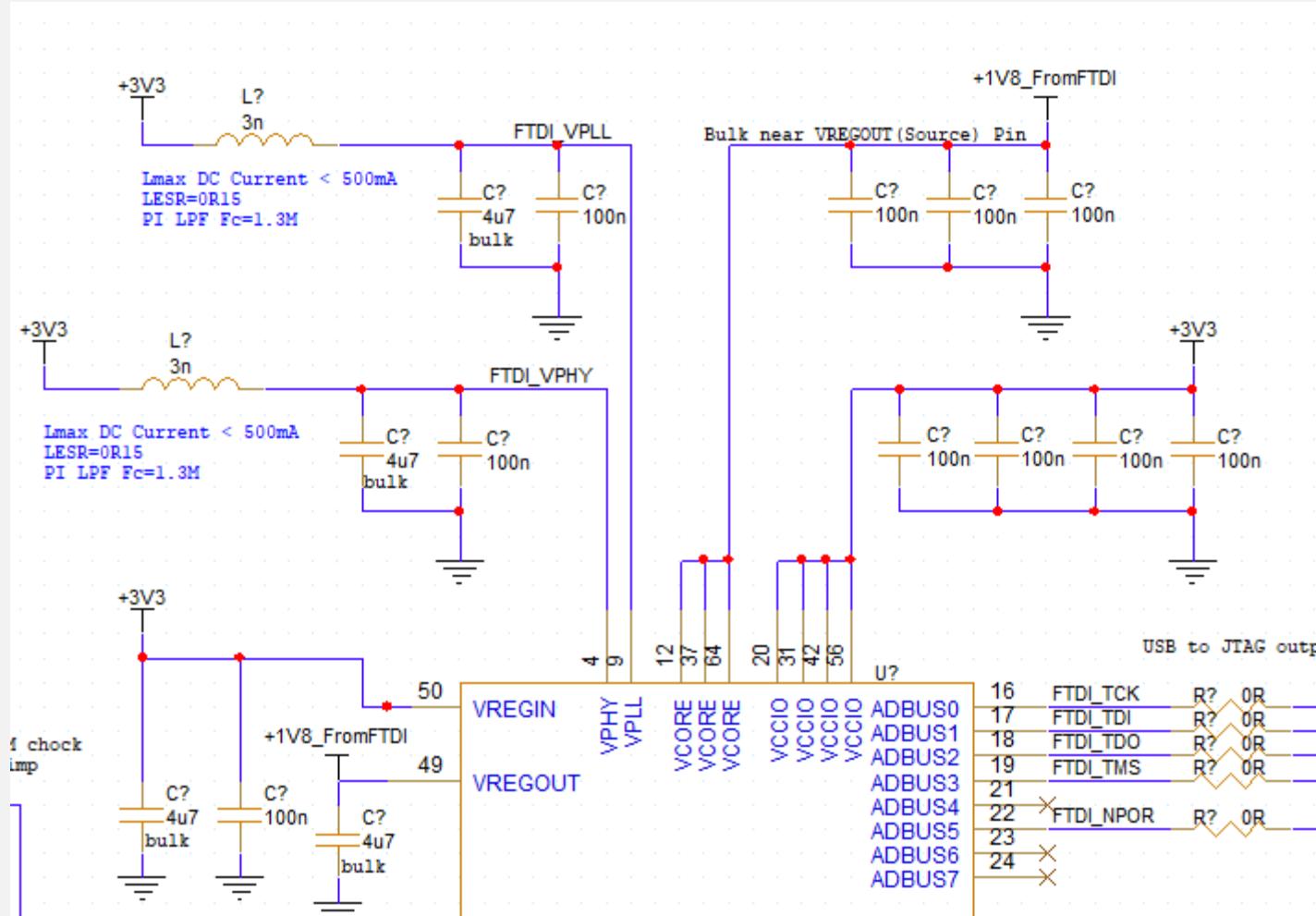


# EEPROM Layout And Routing

- The EEPROM is not very fast but still try to keep traces short
- Option to go down to the bottom Layer with Via and then:
  - Decoupling close with short loops
  - Pull ups close
- Example from previous project:



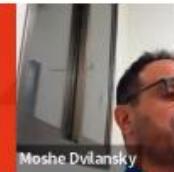
# FTDI POWER



# OPENS ISSUES FROM PDR

זה שקי מתיק מציג CDR שומרה מה לא נסגר ב PDR וטוגר אותו ב CDR

## Open Issues from PDR



Moshe Dvilansky

- ZYNQ storage FLASH – micro SD / eMMC -> Verimatrix -> eMMC
- DDR3 density
  - ZYNQ -> **2 x 2Gbits(mian stream)**
- Audio decoding in ST7105 – Assembly DSP
- USB – Do we need it ? – **No USB**
- Board to board connectors - **Done**
- Q-tone input - **No**
- ST7105 FLASH/FRAM – **NOR FLASH No FRAM (DDR standby)**

# Zynq PL

---

- Will be directed to the PMOD extensions
- Differential lines
  - More important so first – Intra – pair skew – P to N matching (same diff channel)
  - Then – Inter pair skew matching (diff to diff)

זכיר חשוב לדיק באורךים בתוך הקי הדיפרנציאלי  
בין P ל N של אותו טרייס(**intra - pair skew**) יותר  
מאשר התאום אורךים בין הטריסים הדיפרנציאליים  
**השוניים** (**inter pair skew**)

# General

---

- Terminations
  - TX 22ohm Series terminations, use 0402 but place with space so it can get replaced in the lab

# POR Circuit

- Certainly! In PCB (Printed Circuit Board) design, a Power-On Reset (POR) circuit is commonly used to ensure that the system starts in a known and reliable state when power is applied. The POR circuit monitors the power supply voltage and generates a reset signal to initialize or reset other components in the system until the power supply stabilizes within a specified range.
- Let's go through a typical POR circuit using an example of a PIMIC (Power Management Integrated Circuit) that generates and distributes the POR signal to other parts of the circuit:

## 1. POR Circuit Components:

1. **Voltage Detector/Comparator:** This is a key component in the POR circuit. It monitors the input voltage and compares it against a reference voltage.
2. **Reference Voltage Source:** A stable reference voltage is required to compare against the incoming power supply voltage. This could be generated internally within the PIMIC or provided externally.
3. **Delay Circuit:** To prevent false resets due to brief fluctuations in the power supply, a delay circuit may be included. It ensures that the POR signal is not asserted until the power supply voltage remains stable within the specified range for a certain duration.
4. **Output Driver:** Once the POR condition is met, the output driver is responsible for generating the POR signal that resets or initializes other components in the system.

## 2. Example PIMIC POR Circuit:

Let's assume we have a PIMIC with an integrated POR circuit. The PIMIC may have the following connections:

1. **VDD (Power Supply Input):** Connected to the main power supply of the system.
2. **GND (Ground):** Connected to the ground reference of the system.
3. **POR Output:** This is the POR signal generated by the PIMIC.

## 3. Operation:

1. When power is applied to the system, the voltage detector in the PIMIC monitors the VDD voltage.
2. If the VDD voltage is below a certain threshold, indicating that the power supply is not yet stable, the POR circuit remains inactive.
3. Once the VDD voltage rises and stabilizes within the acceptable range, the voltage detector triggers the POR circuit.
4. The delay circuit may introduce a brief delay to filter out short transients.
5. The output driver then asserts the POR signal, indicating that the system is now in a stable and reliable state.

## 4. Connecting POR Signal to Other Components:

1. The POR signal generated by the PIMIC is typically connected to the reset pins of other components on the PCB.
2. Microcontrollers, FPGAs, or other critical digital circuits often have reset pins that can be connected to the POR signal. When POR is asserted, these components are reset to a known state.

# USB PHY

---

- From the 3320 Data Sheet:
  - Includes full support for the optional On-The-Go (OTG) protocol detailed in the On-The-Go Supplement Revision 2.0 specification

# Reference Designs

[digilent.com/reference/programmable-logic/cora-z7/start](https://digilent.com/reference/programmable-logic/cora-z7/start)

FREE US shipping on orders \$35+  1

You are here: [Digilent Reference](#) / [Programmable Logic](#) / Cora Z7

## Cora Z7

 The Cora Z7-10 variant is now retired in our store. The Cora Z7-07S is not affected and will remain in production.

The Cora Z7 is a ready-to-use, low-cost, and easily embeddable development platform designed around the powerful Zynq-7000 All-Programmable System-on-Chip (APSoC) from Xilinx. The Zynq-7000 architecture tightly integrates a single or dual core 667MHz ARM Cortex-A9 processor with a Xilinx 7-series FPGA. This pairing grants the ability to surround the processor with a unique set of software defined peripherals and controllers, tailored for the target application.

The Cora Z7's wide array of hardware interfaces, from a 1Gbps Ethernet PHY to analog-to-digital converters and general-purpose input/output pins, make it an ideal platform for the development of a vast variety of embedded applications. The small form factor and mounting holes make the Cora Z7 ready to be used as one component of a larger solution. The on-board SD Card slot, Ethernet, and Power solution allow the Cora Z7 to operate independently of a host computer.



**Buy**

[Reference Manual](#) [Technical Support](#)

**Cora Z7**  
Zynq for Hobbyists and Makers

**Features**

- Full support for Vivado and Petalinux design environments
- 667 MHz Cortex-A9 processor with tightly integrated Xilinx FPGA
- 512 MB DDR3 memory
- Arduino shield and Pmod connectors for add-on hardware devices
- USB and Ethernet connectivity
- Large array of general purpose input/output ports for any number of different custom solutions
- Small form factor and mounting holes
- Programmable from JTAG and microSD card

**Key FPGA Specifications**

Part Number	XC7Z007S-1CLG400 (XC7Z010-1CLG400*)
Logic Slices	3,600 (4,400*)
6-input LUTs	14,400 (17,600*)
Flip-Flops	28,800 (35,200*)
Block RAM	225 KB (270 KB*)
DSP Slices	66 (80*)
Clock Resources	Zynq PLL with 4 outputs 2 PLLs 2 MMCMs 125 MHz external clock

# EMMC

- Probably needs weak pull ups ( according to SDIO specification)
- VDDI is the internal Core regulator output to the internal Core Logic – So it needs decoupling capacitors
- EMMC Guidelines
  - See the attached document "[Recommended PCB Routing Guidelines for SHM e.MMC.pdf](#)"
  - EMMC is with 0.5mm pitch but most of the pins are NC so can “de-populate” unused pins
  - Placement close, up-right to the Zynq(SDIO pins there in upper-left)
  - Terminations (pull ups) at the top layer near the EMMC
  - Route SDIO traces:
    - to Layer 6 (good for high speed)
    - 50 ohm controlled impedance
    - Traces lengths as short as possible (about 30ps??)
    - Keep spacing between traces – more than the manufacturer limit(as possible)

## Decoupling Capacitor Recommendations

- X7R or X5R capacitors are recommended with a rated voltage > 6.3V.
- 0603 or a smaller size is recommended.
- Pick capacitors with low ESL and ESR.
- It is important to place decoupling caps as close to the target supply balls while maintaining > 20 mil trace width for supply connections to capacitor SMT pads.
- Recommended Value and Quantity:

$$V_{CCQ} \geq 0.1 \mu F \times 1$$

2.2  $\mu F \times 1$  (for BGA153, this cap should be as close as possible to C6 ball)

$$1 \times 1 \mu F$$

1  $\mu F$  (additional cap only for BGA100 package)

$$V_{CC} \geq 0.1 \mu F \times 1 \text{ and } 2.2 \mu F \times 1$$

$$V_{DDI} \geq 0.1 \mu F \times 1 \text{ and } 2.2 \mu F \times 1$$

Customer is requested to place all of the caps shown above. For  $V_{CCQ}$  caps, they should be located as close as possible to the  $V_{CCQ}/V_{SSQ}$  balls near the DAT0-7 signals.

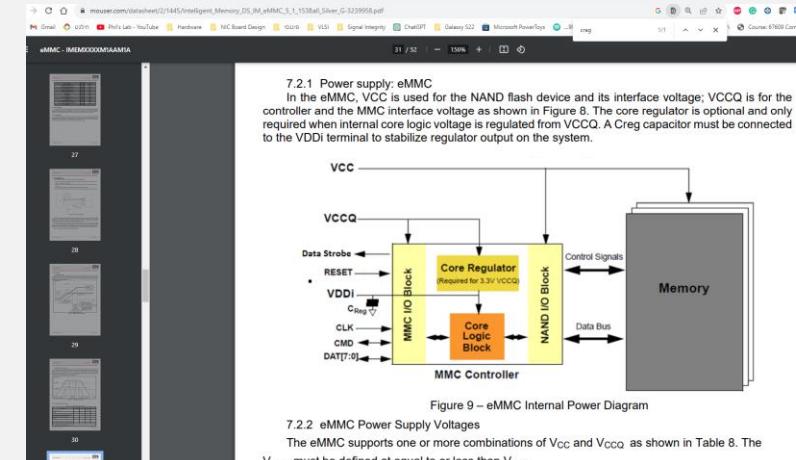
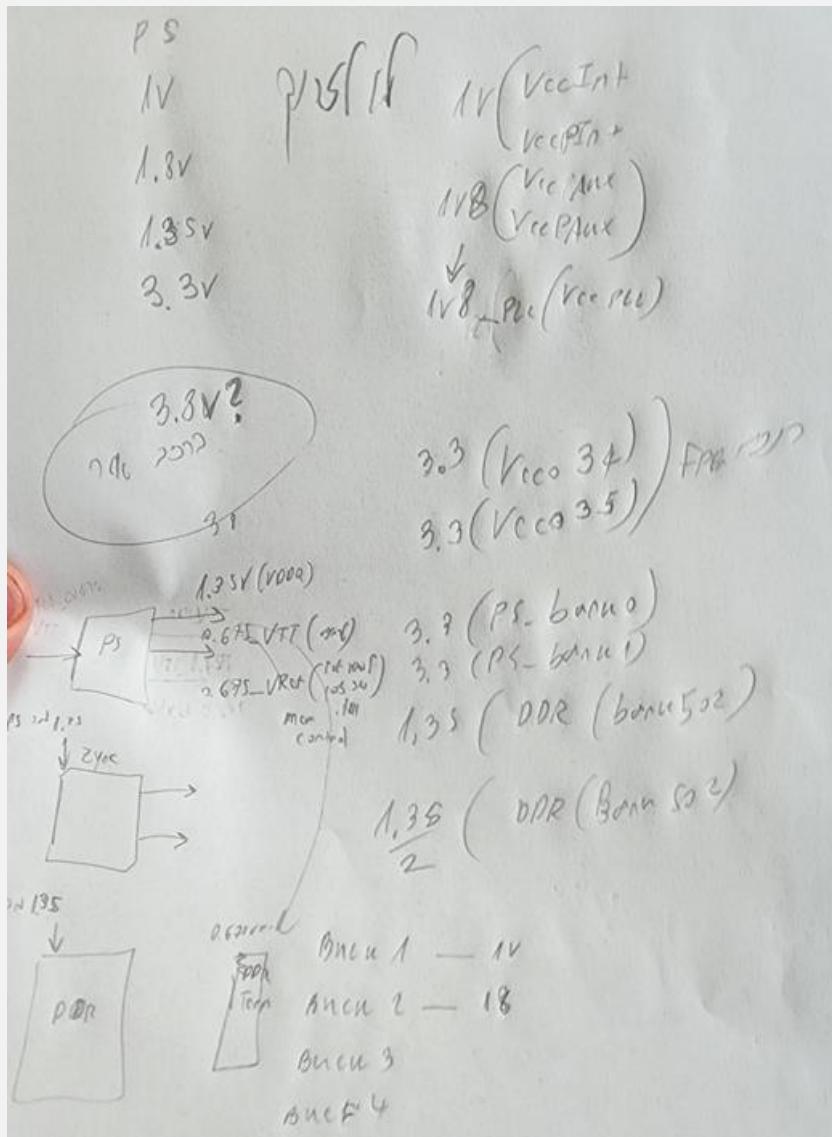


Figure 9 – eMMC Internal Power Diagram

7.2.2 eMMC Power Supply Voltages

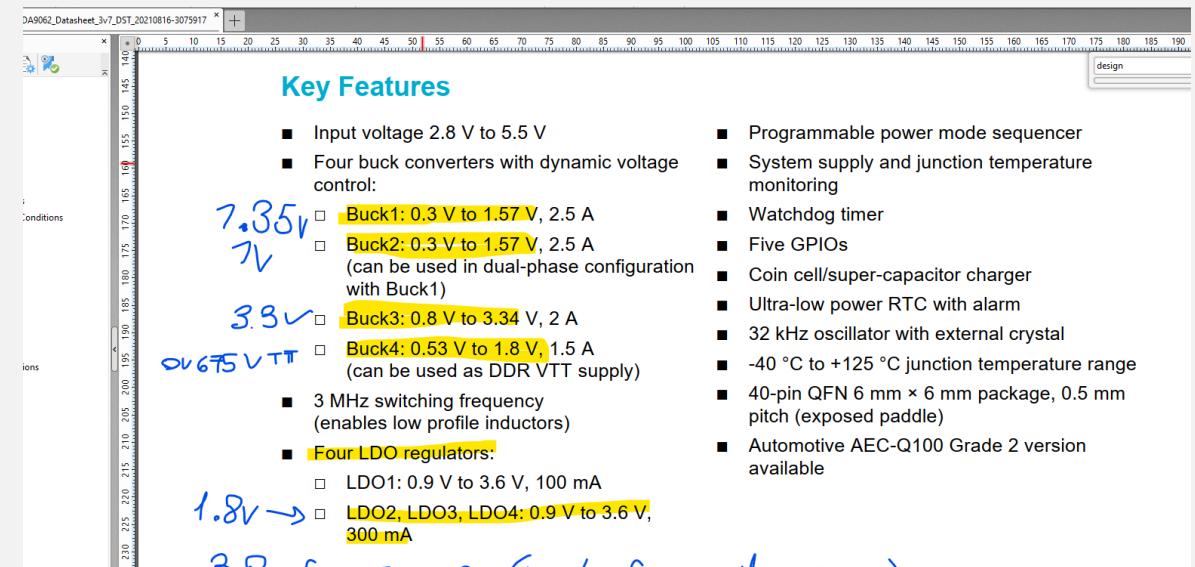
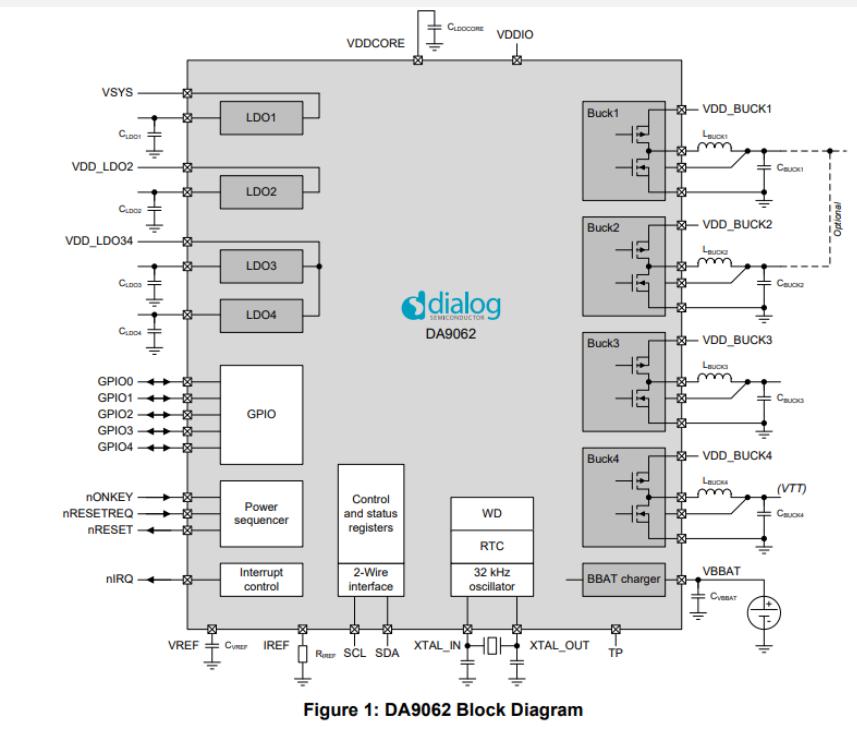
The eMMC supports one or more combinations of  $V_{CC}$  and  $V_{CCQ}$  as shown in Table 8. The  $V_{CCQ}$  must be defined at equal to or less than  $V_{CC}$ .

# My power notes DRAFT



# POWER

- DA9062 PIMIC Notes:
  - four buck converters providing a total current of 8.5 A.
  - four LDO regulators with programmable output voltage provide up to 300 mA.
  - one of the bucks can be used as a DDR VTT supply
  - Dynamic voltage control (DVC) with I<sup>2</sup>C access
  - Power/shutdown sequence can be triggered by software control, GPIOs, or with the “on-key”



# PIMIC recommended capacitors

Table 34: Recommended Capacitors

Pin	Value	Tol.	Size (mm)	Height (mm)	Temp. Char.	Rating (V)	Part
VLDO1	1 $\mu$ F	$\pm 10\%$	1005	0.55	X5R	10	GRM155R61A105KE15
VLDOx	2.2 $\mu$ F	$\pm 20\%$	1005	0.55	X5R	10	GRM155R60J225ME95#
VBUCK3 $I_{OUT} \leq 1.5$ A	2 x 22 $\mu$ F	$\pm 20\%$	2012	0.95	X5R	6.3	GRM219R60J226M***
		$\pm 20\%$	1005	0.5	X5R	4.0	CL05A226MR5NZNC
VBUCK3 $I_{OUT} > 1.5$ A	2 x 47 $\mu$ F	$\pm 20\%$	2012	0.95	X5R	4.0	GRM219R60G476M***
		$\pm 20\%$	1608	0.8	X5R	4.0	CL10A476MR8NZN
VBUCK4	2 x 22 $\mu$ F	$\pm 20\%$	1608	1	X5R	6.3	GRM188R60J226MEA0
		$\pm 20\%$	1005	0.5	X5R	4.0	CL05A226MR5NZNC
VBUCK4 (VTT mode)	2 x 47 $\mu$ F	$\pm 20\%$	2012	0.95	X5R	4.0	GRM219R60G476M***61
		$\pm 20\%$	1608	0.8	X5R	4.0	CL10A476MR8NZN
VBUCK1, VBUCK2 (half-current mode)	2 x 22 $\mu$ F	$\pm 20\%$	1608	1	X5R	6.3	GRM188R60J226MEA0
		$\pm 20\%$	1005	0.5	X5R	4.0	CL05A226MR5NZNC
VBUCK1, VBUCK2 (full-current mode)	2 x 47 $\mu$ F	$\pm 20\%$	2012	0.95	X5R	4.0	GRM219R60G476M***61
		$\pm 20\%$	1608	0.8	X5R	4.0	CL10A476MR8NZN
VSYS	1 x 1 $\mu$ F	$\pm 10\%$	1005	0.5	X5R	10	GRM155R61A105KE15D
VDD_BUCKx	2 x 22 $\mu$ F	$\pm 20\%$	2012	1.25	X5R	10	LMK212BJ226MG-T

DA9062



PMIC for Applications Requiring up to 8.5 A

Pin	Value	Tol.	Size (mm)	Height (mm)	Temp. Char.	Rating (V)	Part
	4 x 10 $\mu$ F	$\pm 20\%$	1005	0.5	X5R	10	GRM155R61A106ME21
VDD_LDO2	1 x 1 $\mu$ F	$\pm 10\%$	1005	0.5	X5R	10	GRM155R61A105KE15D
VDD_LDO34	1 x 1 $\mu$ F	$\pm 10\%$	1005	0.5	X5R	10	GRM155R61A105KE15D
VBBAT	470 nF	$\pm 10\%$	1005	0.55	X5R	10	GRM155R61A474KE15#
VDDCORE	2.2 $\mu$ F	$\pm 20\%$	1005	0.55	X5R	6.3	GRM155R60J225ME95#
VREF	220 nF	$\pm 15\%$	1005	0.5	X5R	16	GRM155R71C224KA12
XTAL_IN, XTAL_OUT	12 pF	$\pm 5\%$	1005	0.55	U2J	50	GRM1557U1H120JZ01#

# Zync POWER Impedance range

- From Design Guide 933:
  - The impedance of the alternate network must be less than or equal to that of the recommended network across frequencies from **100 KHz to 100 MHz**
  - recommended capacitors amount, value, size, ESR are taken from DG933(in case I did not have it, I would use 10uF for bulk, and 100uF per pin)

Table 3-2 lists the decoupling requirements for the Processing System (PS).

Table 3-2: Required PCB Capacitor Quantities per Device (PS)

Package	Device	V <sub>CCPINT</sub>			V <sub>CCPAUX</sub> <sup>(1)</sup>			V <sub>CCO_DDR</sub>			V <sub>CCO_MIO0</sub>			V <sub>CCO_MIO1</sub>			V <sub>CCPLL</sub> <sup>(2)(3)</sup>	
		100 μF	4.7 μF	0.47 μF	100 μF	4.7 μF	0.47 μF	100 μF	4.7 μF	0.47 μF	100 μF	4.7 μF	0.47 μF	100 μF	4.7 μF	0.47 μF		
CLG225	Z-7007S	1	1	3	1	1	1	1	1	4	1	1	1	1	1	1		

## Required PCB Capacitor Quantities

Table 3-1 lists the PCB decoupling capacitor guidelines per V<sub>CC</sub> supply rail for Zynq-7000 SoC devices.

Table 3-1: Required PCB Capacitor Quantities per Device (PL)

Package	Device	V <sub>CCINT</sub>				V <sub>CCBRAM</sub>				V <sub>CCAUX</sub>			V <sub>CCAUX_IO</sub>			V <sub>CCO</sub> per Bank <sup>(3)(4)</sup>		Bank 0		
		680 μF	330 μF	100 μF	4.7 μF	0.47 μF	100 μF	47 μF	4.7 μF	0.47 μF	47 μF	4.7 μF	0.47 μF	47 μF or 100 μF	4.7 μF	0.47 μF	47 μF	Bank 0		
CLG225	Z-7007S	0	0	1	1	2	NA	NA	NA	NA	1	1	1	NA	NA	NA	1	2	4	1

Table 3-3: PCB Capacitor Specifications

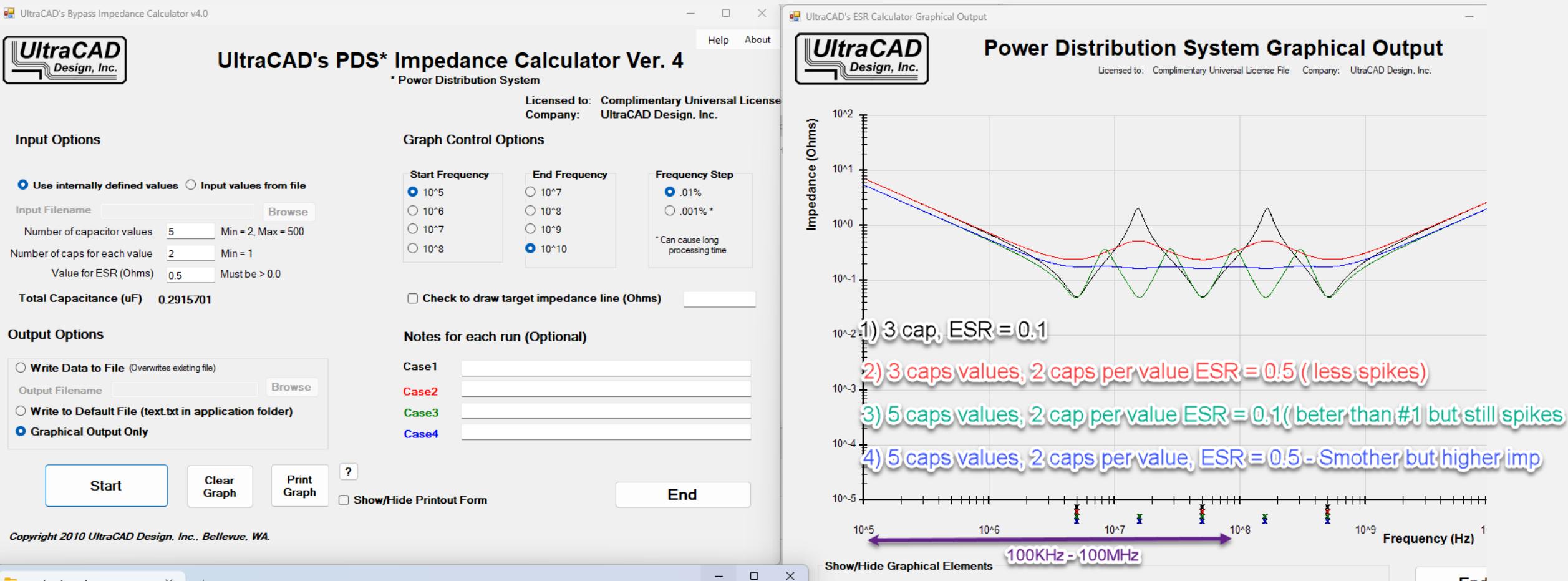
Ideal Value	Value Range <sup>(1)</sup>	Body Size <sup>(2)</sup>	Type	ESL Maximum	ESR Range <sup>(3)</sup>	Voltage Rating <sup>(4)</sup>	Suggested Part Number
680 μF	C > 680 μF	2917/D /7343	2-Terminal Tantalum	2.1 nH	5 mΩ < ESR < 40 mΩ	2.5V	T530X687M006ATE018
330 μF	C > 330 μF	2917/D /7343	2-Terminal Tantalum	2.0 nH	5 mΩ < ESR < 40 mΩ	2.5V	T525D337M006ATE025
330 μF	C > 330 μF	2917/D /7343	2-Terminal Niobium Oxide	2.0 nH	5 mΩ < ESR < 40 mΩ	2.5V	NOSD337M002#0035
100 μF	C > 100 μF	1210	2-Terminal Tantalum, Ceramic X7R, X7U, or X5R	1 nH	1 mΩ < ESR < 40 mΩ	2.5V	GRM32EE70G107ME19
47 μF	C > 47 μF	1210	2-Terminal Ceramic X7R or X5R	1 nH	1 mΩ < ESR < 40 mΩ	6.3V	GRM32ER70J476ME20L
10 μF	C = 10 μF	0603	2-Terminal Ceramic X7R or X5R	0.25 nH	5 mΩ	4.0V	GRM188R60G106ME47
4.7 μF	C > 4.7 μF	0805	2-Terminal Ceramic X7R or X5R	0.5 nH	1 mΩ < ESR < 20 mΩ	6.3V	GRM21BR71A475KA73
0.47 μF	C > 0.47 μF	0603	2-Terminal Ceramic X7R or X5R	0.5 nH	1 mΩ < ESR < 20 mΩ	6.3V	GRM188R70J474KA01

## Notes:

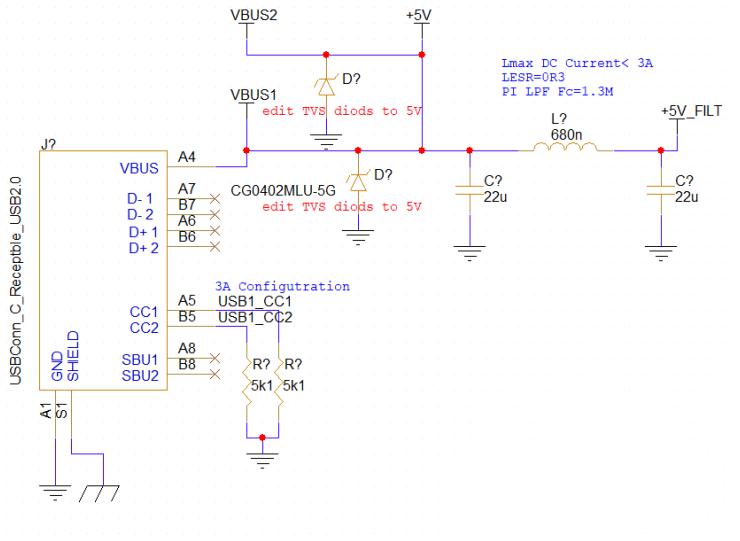
- Values can be larger than specified.
- Body size can be smaller than specified.
- ESR must be within the specified range.
- Voltage rating can be higher than specified.

# Zync POWER Impedance

- The impedance of the alternate network must be less than or equal to that of the recommended network across frequencies from **100 KHz to 100 MHz**
- recommended capacitors amount, value, size, ESR are taken from DG933(in case I did not have it, I would use 10uF for bulk, and 100uF per pin)



# Power Filters



[OKAWA Electric Design](#)

[Top > Tools > Filter > RLC Low-pass Filter Design Tool > Result](#)

### RLC Low-pass Filter Design Tool - Result -

Calculated the transfer function for the RLC Low-pass filter, displayed on graphs, showing Bode diagram, Nyquist diagram, Impulse response and Step response

#### RLC Filter

R=0.3  $\Omega$  L=680n  $H$   
C=22u  $F$   
p: pico, n:nano, u:micro, k:kilo, M:mega

Frequency analysis  
 Bode diagram  
 Phase  Group delay  
 Nyquist diagram  
 Pole, zero  
 Phase margin  
 Oscillation analysis  
 Analysis on frequency range:  
 $f_1 = \text{~} f_2 = \text{[Hz]}$  (optional)

Transfer Function:  
 $G(s) = \frac{66844919786.096}{s^2 + 441176.47058824 + 66844919786.096}$

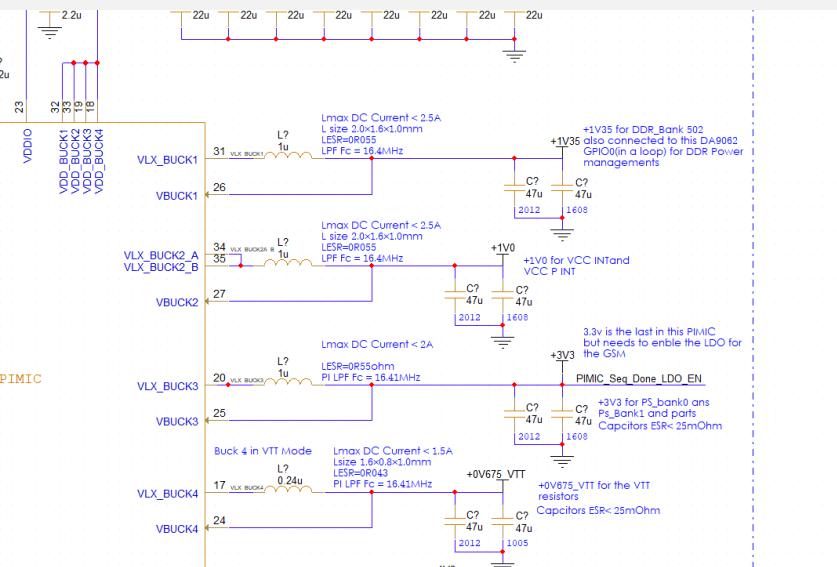
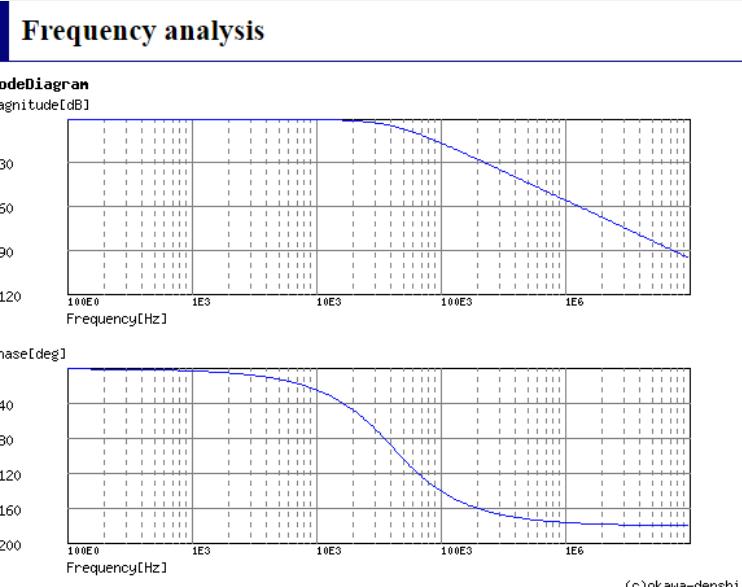
Cut-off frequency  
 $f_c = 41148.530937338 \text{ [Hz]}$

Quality factor  
 $Q = 0.59603271532769$

Damping ratio  
 $\zeta = 0.85319468849178$

Pole(s)  
 $p = -35107.708034977 + 21462.768573321 \text{ [Hz]}$   
 $p = 41148.530937338 \text{ [Hz]}$   
 $p = -35107.708034977 - 21462.768573321 \text{ [Hz]}$   
 $p = 41148.530937338 \text{ [Hz]}$

**Calculate**



[OKAWA Electric Design](#)

[Top > Tools > Filter > RLC Low-pass Filter Design Tool > Result](#)

### RLC Low-pass Filter Design Tool - Result -

Calculated the transfer function for the RLC Low-pass filter, displayed on graphs, showing Bode diagram, Nyquist diagram, Impulse response and Step response

#### RLC Filter

R=0.055  $\Omega$  L=1u  $H$   
C=94u  $F$   
p: pico, n:nano, u:micro, k:kilo, M:mega

Frequency analysis  
 Bode diagram  
 Phase  Group delay  
 Nyquist diagram  
 Pole, zero  
 Phase margin  
 Oscillation analysis  
 Analysis on frequency range:  
 $f_1 = \text{~} f_2 = \text{[Hz]}$  (optional)

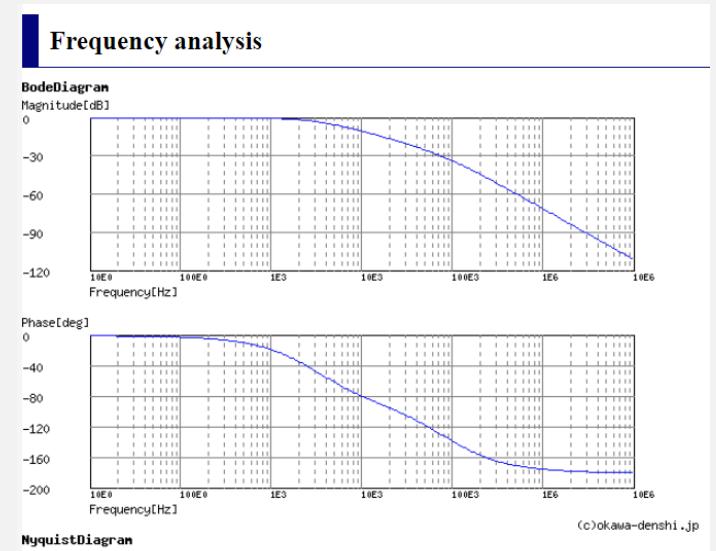
Transfer Function:  
 $G(s) = \frac{10638297872.34}{s^2 + 55000s + 10638297872.34}$

Cut-off frequency  
 $f_c = 16415.578975209 \text{ [Hz]}$

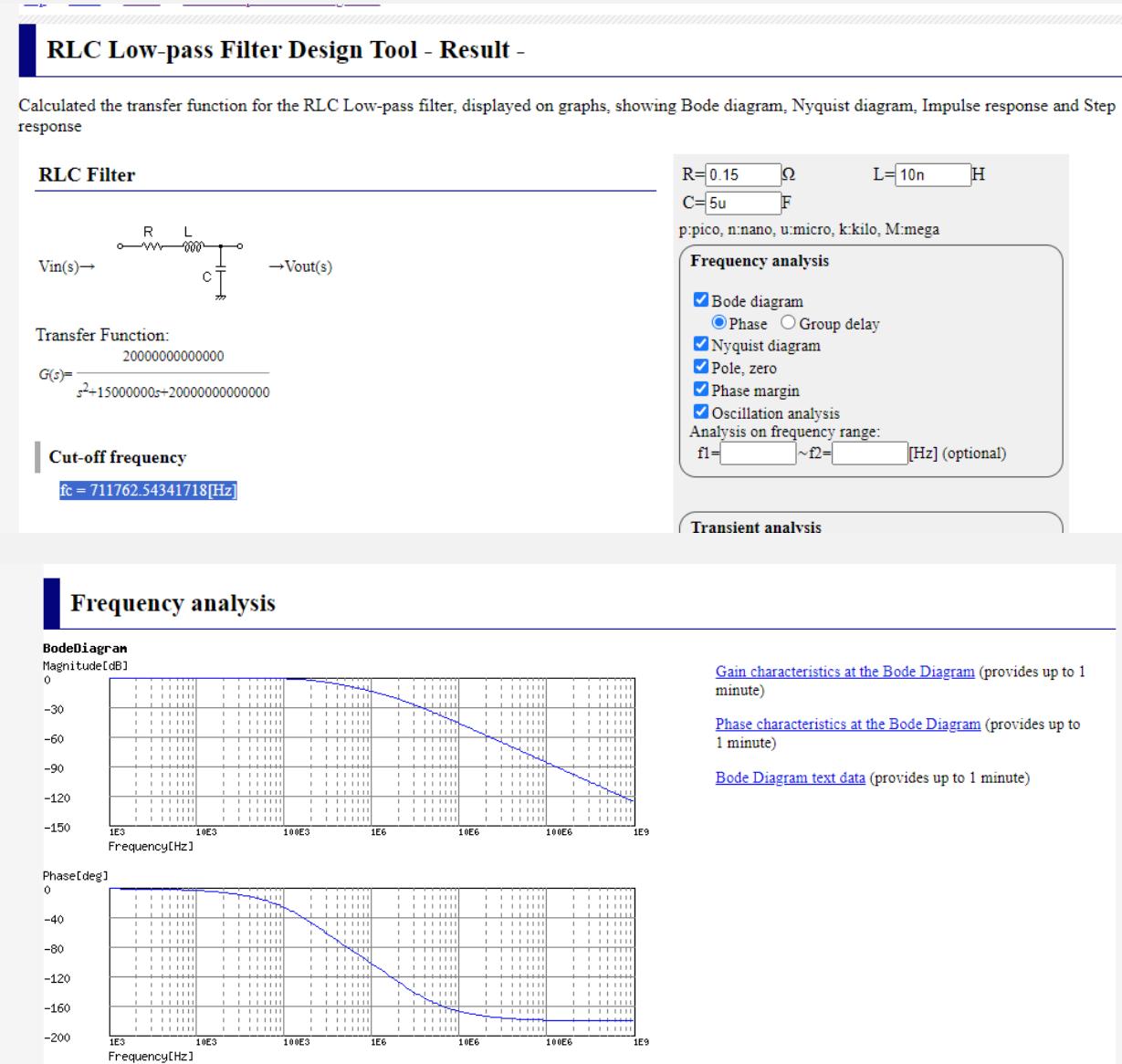
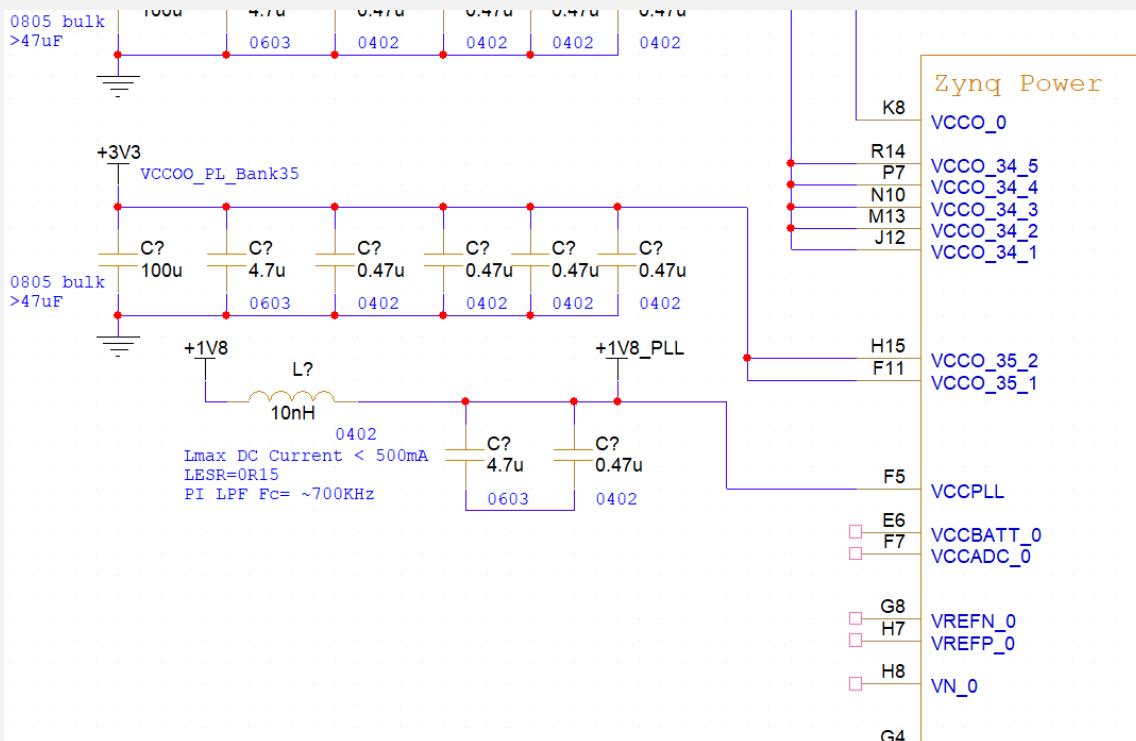
Quality factor  
 $Q = 1.8753113568342$

Damping ratio  
 $\zeta = 0.2666223921579$

**Transient analysis**  
 Step response  
 Impulse response  
 Overshoot  
 Final value of the step response  
 Analysis on time range:  
 $0 \text{~} 10 \text{ sec}$  (optional)

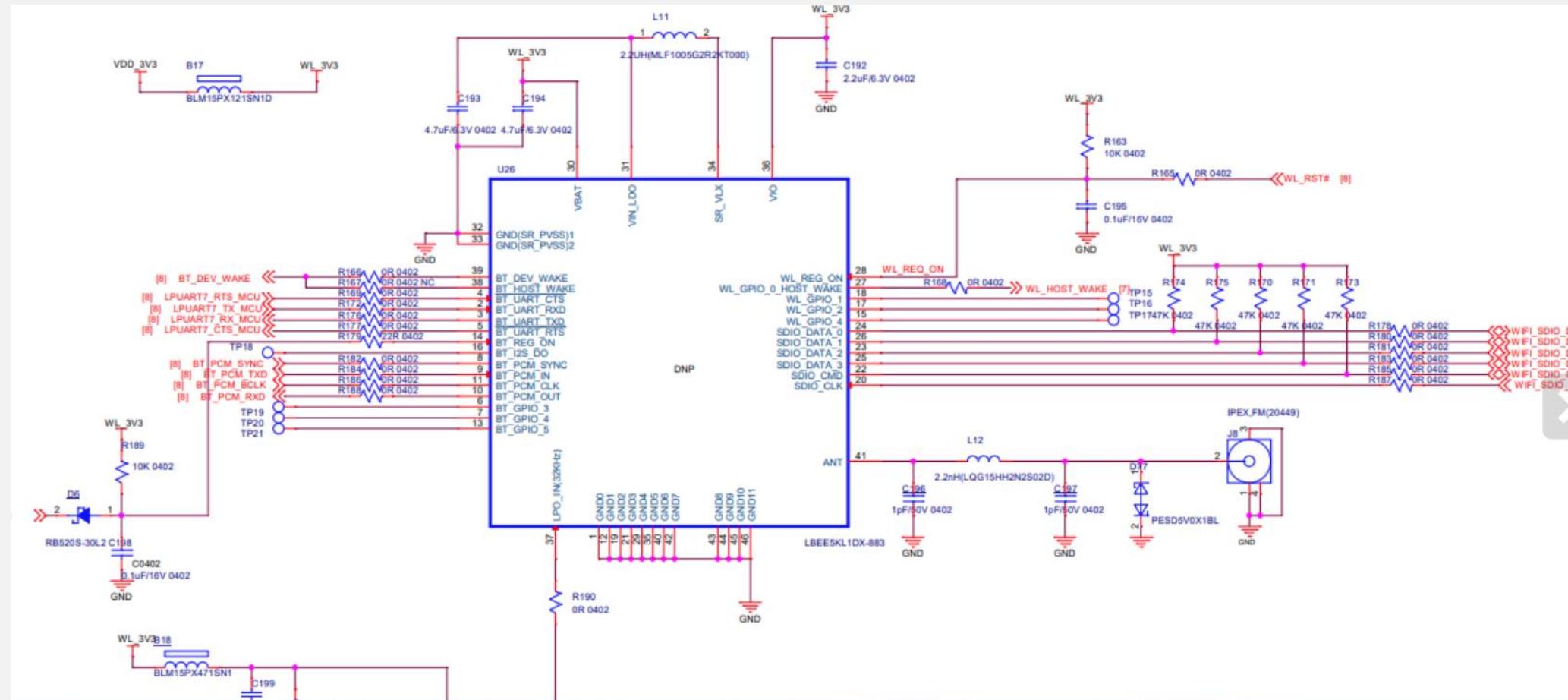


# Zync PLL Power Filter



# IPEX Antenna reference for review

- <https://www.mouser.co.il/c/passive-components/?antenna%20connector%20type=IPEX%20MHF4&minimum%20frequency=2.4%20GHz>



# GSM specific parts recommendations

- From the [design guideline](https://content.u-blox.com/sites/default/files/SARA-G450_SysIntegrManual_UBX-18046432.pdf) : [https://content.u-blox.com/sites/default/files/SARA-G450\\_SysIntegrManual\\_UBX-18046432.pdf](https://content.u-blox.com/sites/default/files/SARA-G450_SysIntegrManual_UBX-18046432.pdf)

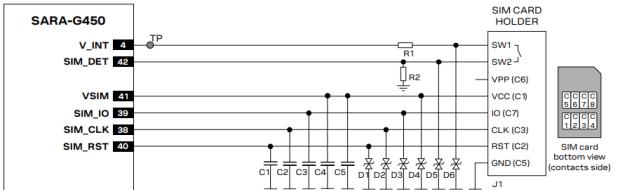


Figure 45: Application circuit for the connection to a single removable SIM card, with SIM detection implemented

Reference	Description	Part number - Manufacturer
C1, C2, C3, C4	33 pF capacitor ceramic COG 0402 5% 50 V	GRM1555C1H330JA01 - Murata
C5	1 µF capacitor ceramic X7R 0402 10% 16 V	GRM155R70J105KA12 - Murata
D1 – D6	Very low capacitance ESD protection	PESD0402-140 - Tyco Electronics
R1	1 kΩ resistor 0402 5% 0.1 W	RC0402JR-071KL - Yageo Phycomp
R2	470 kΩ resistor 0402 5% 0.1 W	RC0402JR-07470KL - Yageo Phycomp
J1	SIM card holder 6 + 2 positions, with card presence switch	Generic manufacturer, CCM03-3013LFT R102 - C&K Components

Table 30: Examples of components for the connection to a single removable SIM card, with SIM detection implemented

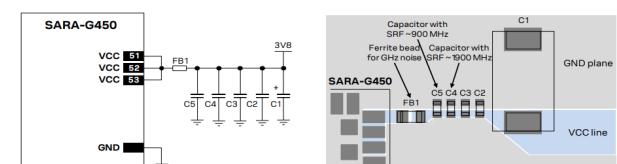


Figure 27: Suggested schematic and layout design for the VCC line, highly recommended when using an integrated antenna (ferrite bead is not strictly required)

Reference	Description	Part number - Manufacturer
C1	330 µF capacitor tantalum D_SIZE 6.3 V 45 mΩ	T520D37M006ATE045 - KEMET
C2	100 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
C3	10 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C4	15 pF capacitor ceramic COG 0402 5% 25 V	GRM1555C1E150JA01 - Murata
C5	56 pF capacitor ceramic COG 0402 5% 25 V	GRM1555C1E560JA01 - Murata
FB1	Chip Ferrite bead EMI filter for GHz band noise 220 Ω at 100 MHz, 260 Ω at 1 GHz, 2000 mA	BLM18EG221SN1 - Murata

Table 17: Suggested components to reduce ripple / noise on VCC and to avoid undershoot / overshoot on VCC voltage drops

## 2.4.2 Antenna detection interface (ANT\_DET)

### 2.4.2.1 Guidelines for ANT\_DET circuit design

Figure 41 and Table 27 describe the recommended schematic and components for the antenna detection circuit to be provided on the application board for the diagnostic circuit that must be provided on the antenna assembly to achieve antenna detection functionality.

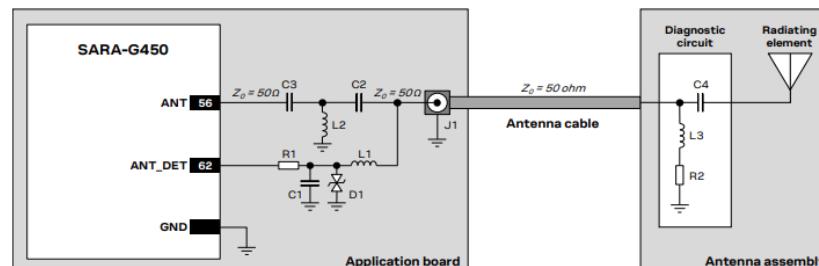


Figure 41: Suggested schematic for antenna detection circuit on application PCB and diagnostic circuit on antenna assembly

Reference	Description	Part number - Manufacturer
C1	27 pF capacitor ceramic COG 0402 5% 50 V	GRM1555C1H270J - Murata
C2	33 pF capacitor ceramic COG 0402 5% 50 V	GRM1555C1H330J - Murata
D1	Very low capacitance ESD protection	PESD0402-140 - Tyco Electronics
L1	68 nH multilayer inductor 0402 (SRF ~1 GHz)	LQG15HS68NJ02 - Murata
R1	10 kΩ resistor 0402 1% 0.063 W	RK73H1ETTP1002F - KOA Speer
J1	SMA connector 50 Ω Pin-Through-Hole	SMA6251A1-3GT50G-50 - Amphenol
C3	15 pF capacitor ceramic COG 0402 5% 50 V	GRM1555C1H150J - Murata
L2	39 nH multilayer inductor 0402 (SRF ~1 GHz)	LQG15HN39NJ02 - Murata
C4	22 pF capacitor ceramic COG 0402 5% 25 V	GRM1555C1H220J - Murata
L3	68 nH multilayer inductor 0402 (SRF ~1 GHz)	LQG15HS68NJ02 - Murata
R2	15 kΩ resistor for diagnostic	Generic manufacturer

Table 27: Suggested parts for antenna detection circuit on application PCB and diagnostic circuit on antenna assembly

# From GSM user manual

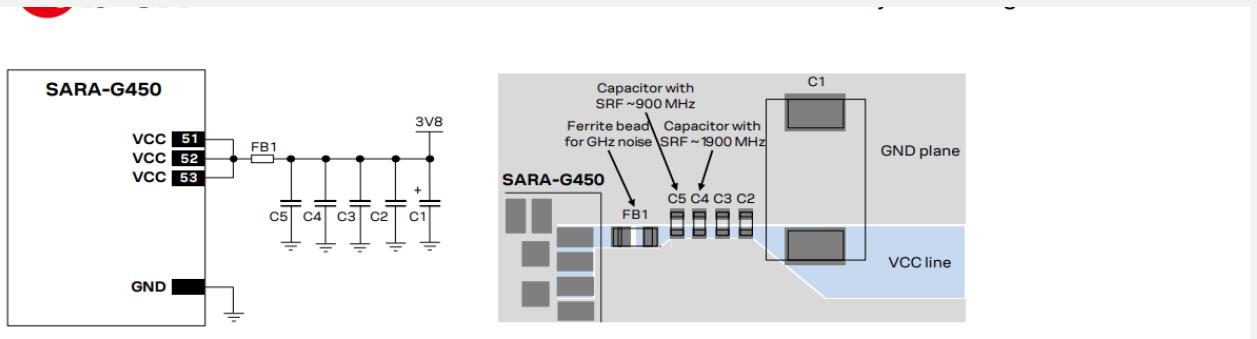


Figure 27: Suggested schematic and layout design for the VCC line, highly recommended when using an integrated antenna (ferrite bead is not strictly required)

Reference	Description	Part number - Manufacturer
C1	330 $\mu$ F capacitor tantalum D_SIZE 6.3 V 45 m $\Omega$	T520D337M006ATE045 - KEMET
C2	100 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
C3	10 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C4	15 pF capacitor ceramic C0G 0402 5% 25 V	GRM1555C1E150JA01 - Murata
C5	56 pF capacitor ceramic C0G 0402 5% 25 V	GRM1555C1E560JA01 - Murata
FB1	Chip Ferrite bead EMI filter for GHz band noise 220 $\Omega$ at 100 MHz, 260 $\Omega$ at 1 GHz, 2000 mA	BLM18EG221SN1 - Murata

Table 17: Suggested components to reduce ripple / noise on VCC and to avoid undershoot / overshoot on VCC voltage drops

## 1.2 Architecture

Figure 1 summarizes the architecture of SARA-G450 modules, illustrating the internal blocks modules, consisting of the RF, baseband and power management main sections, and the available interfaces.

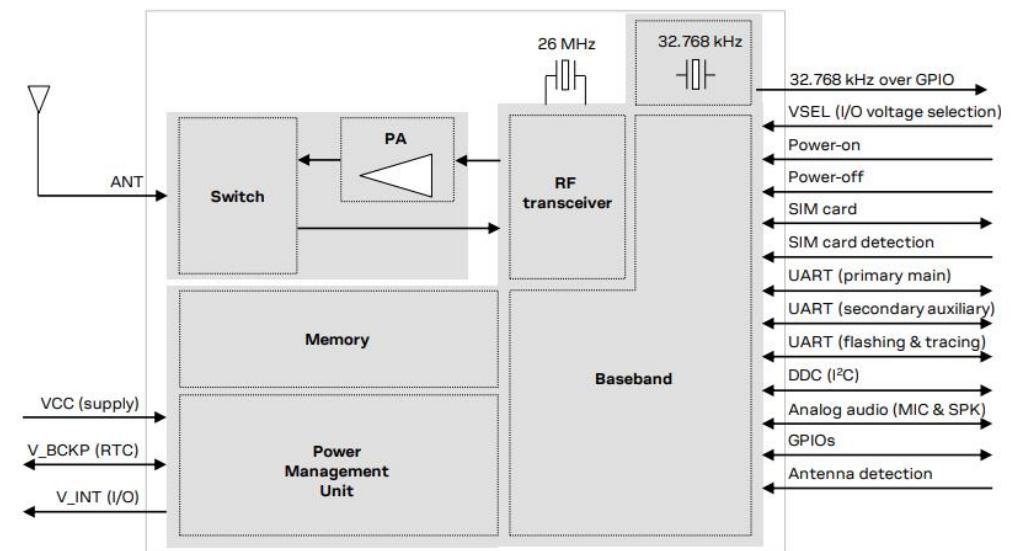


Figure 1: SARA-G450 modules block diagram

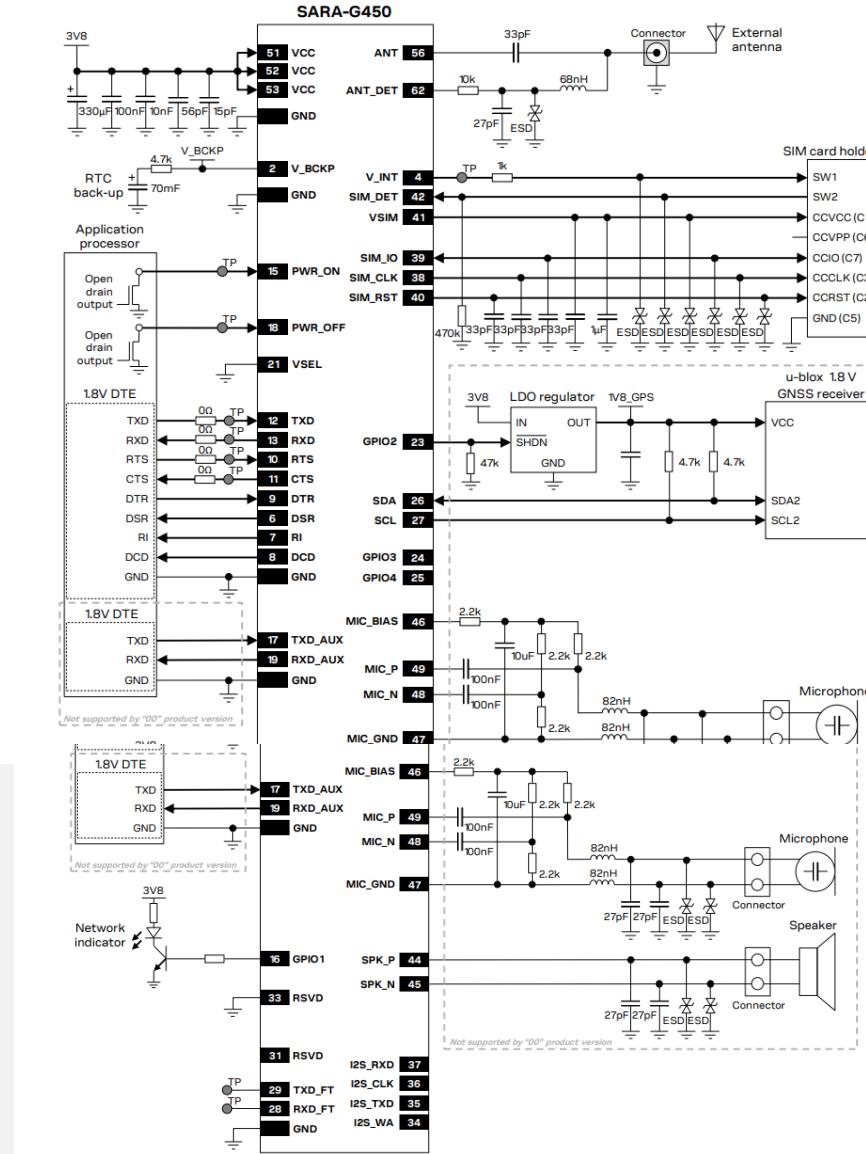
<sup>1</sup> Device can be attached to both GPRS and GSM services (i.e. Packet Switch and Circuit Switch mode) using one service at a time. For example, if an incoming call occurs during data transmission, the data connection is suspended to allow the voice communication. Once the voice call has terminated, the data service is resumed.

<sup>2</sup> GPRS multi-slot class 12 implies a maximum of 4 slots in Down-Link (reception) and 4 slots in Up-Link (transmission) with 5 slots in total. The SARA-G450 modules can be configured as GPRS multi-slot class 10 by means of AT command.

<sup>3</sup> The maximum bit rate of the module depends on the current network settings.

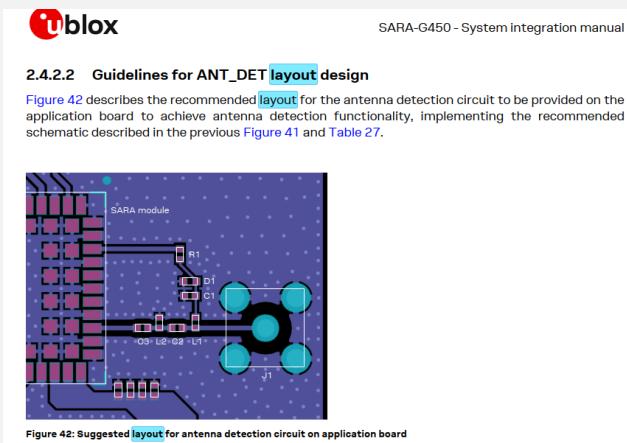
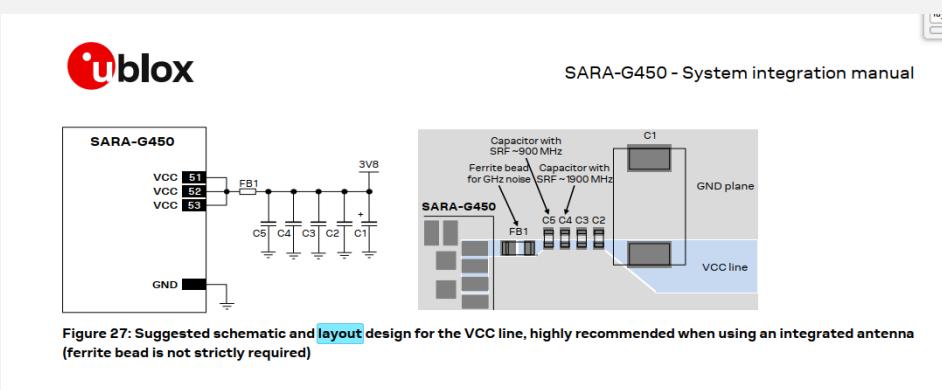
# From GSM user manual

application board, using all the available interfaces and functions of the module.



# LAYOUT Guidelines GSM

- All in the [SARA-450 System integration Manual](#)
- Some of the relevant:

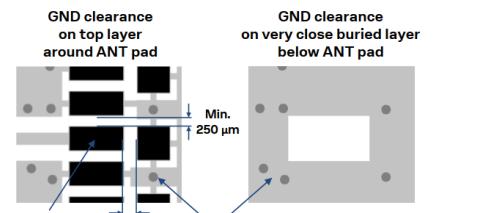


## 2.4.1.2 Guidelines for antenna RF interface design

### Guidelines for ANT pin RF connection design

Correct transition between the **ANT** pin and the application board PCB must be provided, implementing the following design-in guidelines for the [layout](#) of the application PCB close to the pad designed for the **ANT** pin:

- On a multi-layer board, the whole layer stack below the RF connection should be free of digital lines
- Increase ground keep-out (i.e. clearance, a void area) around the **ANT** pad, on the top layer of the application PCB, to at least 250  $\mu\text{m}$  up to adjacent pads metal definition and up to 400  $\mu\text{m}$  on the area below the module, to reduce parasitic capacitance to ground, as described in the left picture in [Figure 37](#)
- Add ground keep-out (i.e. clearance, a void area) on the buried metal layer below the **ANT** pad if the top-layer to buried layer dielectric thickness is below 200  $\mu\text{m}$ , to reduce parasitic capacitance to ground, as described in the right picture in [Figure 37](#)



SARA-G450 - System integration manual

### Guidelines for RF transmission line design

The transmission line from the **ANT** pad up to the antenna connector or up to the internal antenna pad must be designed so that the characteristic impedance is as close as possible to 50  $\Omega$ .

The transmission line can be designed as a micro strip (consists of a conducting strip separated from a ground plane by a dielectric material) or a strip line (consists of a flat strip of metal which is sandwiched between two parallel ground planes within a dielectric material). The micro strip, implemented as a coplanar waveguide, is the most common configuration for printed circuit board.

[Figure 38](#) and [Figure 39](#) provide two examples of suitable 50  $\Omega$  coplanar waveguide designs. The first transmission line can be implemented for a 4-layer PCB stack-up herein described, the second transmission line can be implemented for a 2-layer PCB stack-up herein described.

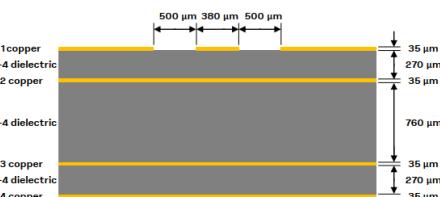


Figure 38: Example of 50  $\Omega$  coplanar waveguide transmission line design for the described 4-layer board layup

## 2.5.2 Guidelines for SIM [layout](#) design

The [layout](#) of the SIM card interface lines (**VSIM**, **SIM\_CLK**, **SIM\_IO**, **SIM\_RST**) may be critical if the SIM card is placed far away from the SARA-G450 modules or in close proximity to the RF antenna. In these two cases should be avoided or at least mitigated as described below.

In the first case, a too-long connection can cause the radiation of some harmonics of the digital frequency as any other digital interface: keep the traces short and avoid coupling with RF lines sensitive analog inputs.

In the second case, the same harmonics can be picked up and create self-interference that can reduce the sensitivity of GSM receiver channels whose carrier frequency is coincidental with the harmonics frequencies: placing the RF bypass capacitors suggested in [2.5.1](#) near the SIM connector will mitigate the problem.

In addition, since the SIM card is typically accessed by the end user, it can be subjected to ESD discharges: add adequate ESD protection as suggested in [2.5.1](#) to protect the module SIM pins that are close to the SIM connector.

Limit the capacitance and series resistance on each SIM signal to match the SIM specification. Connections should always be kept as short as possible.

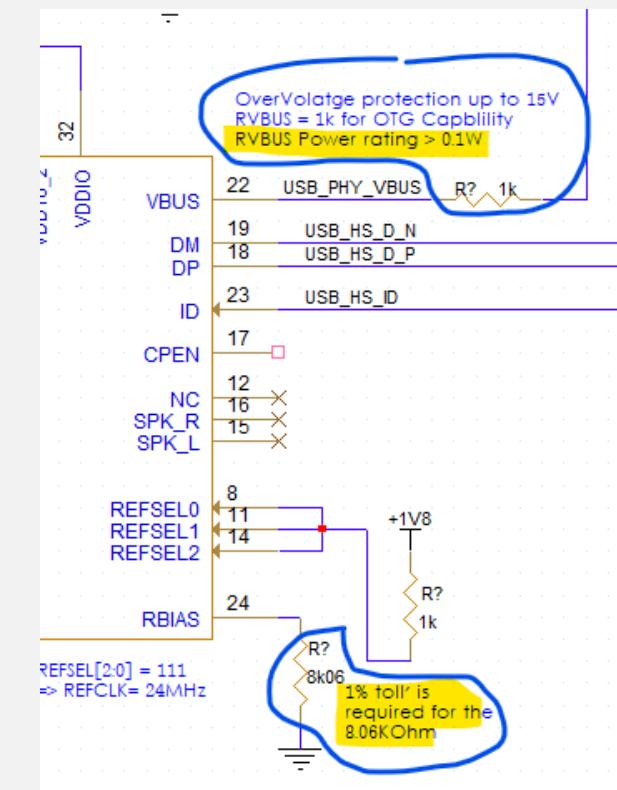
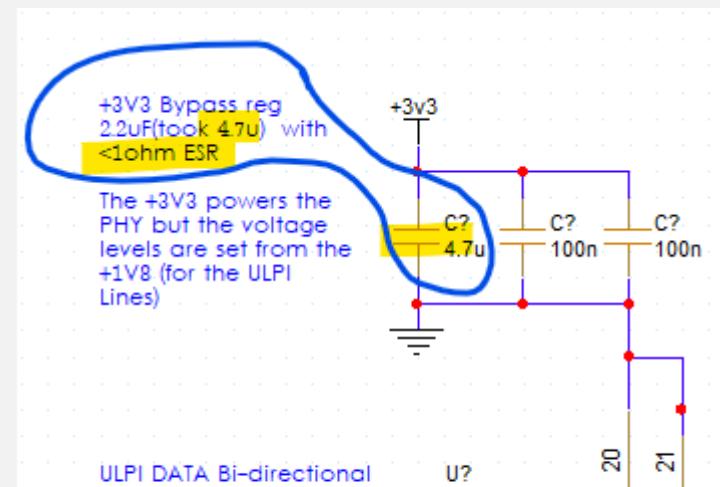
Avoid coupling with any sensitive analog circuit, since the SIM signals can cause the radiation of harmonics of the digital data frequency.

## 2.13.2 Layout checklist

The following are the most important points for a simple [layout](#) check:

- Check 50  $\Omega$  nominal characteristic impedance of the RF transmission line connected to the **ANT** pad (antenna RF input/output interface).
- Follow the recommendations of the antenna producer for correct antenna installation and deployment (PCB [layout](#) and matching circuitry).
- Ensure no coupling occurs between the RF interface and noisy or sensitive signals (like audio input/output signals, SIM signals, high-speed digital lines).
- The **VCC** line should be wide and short.
- Provide the suggested bypass capacitors close to the **VCC** pins implementing the recommended [layout](#) and placement, especially if the device integrates an internal antenna.
- Route the **VCC** supply line away from sensitive analog signals.
- Ensure clean grounding.
- Optimize placement for minimum length of RF line and closer path from DC source for **VCC**.
- Route analog audio signals away from noisy sources (like RF interface, **VCC**, switching supplies).
- The audio output lines on the application board must be wide enough to minimize series resistance.
- Keep routing short and minimize parasitic capacitance on the SIM lines to preserve signal integrity.
- Ensure optimal thermal dissipation from the module to the ambient.

# BOM points to manufacturer



# PDR – Smart Helmet

Moshe Saban

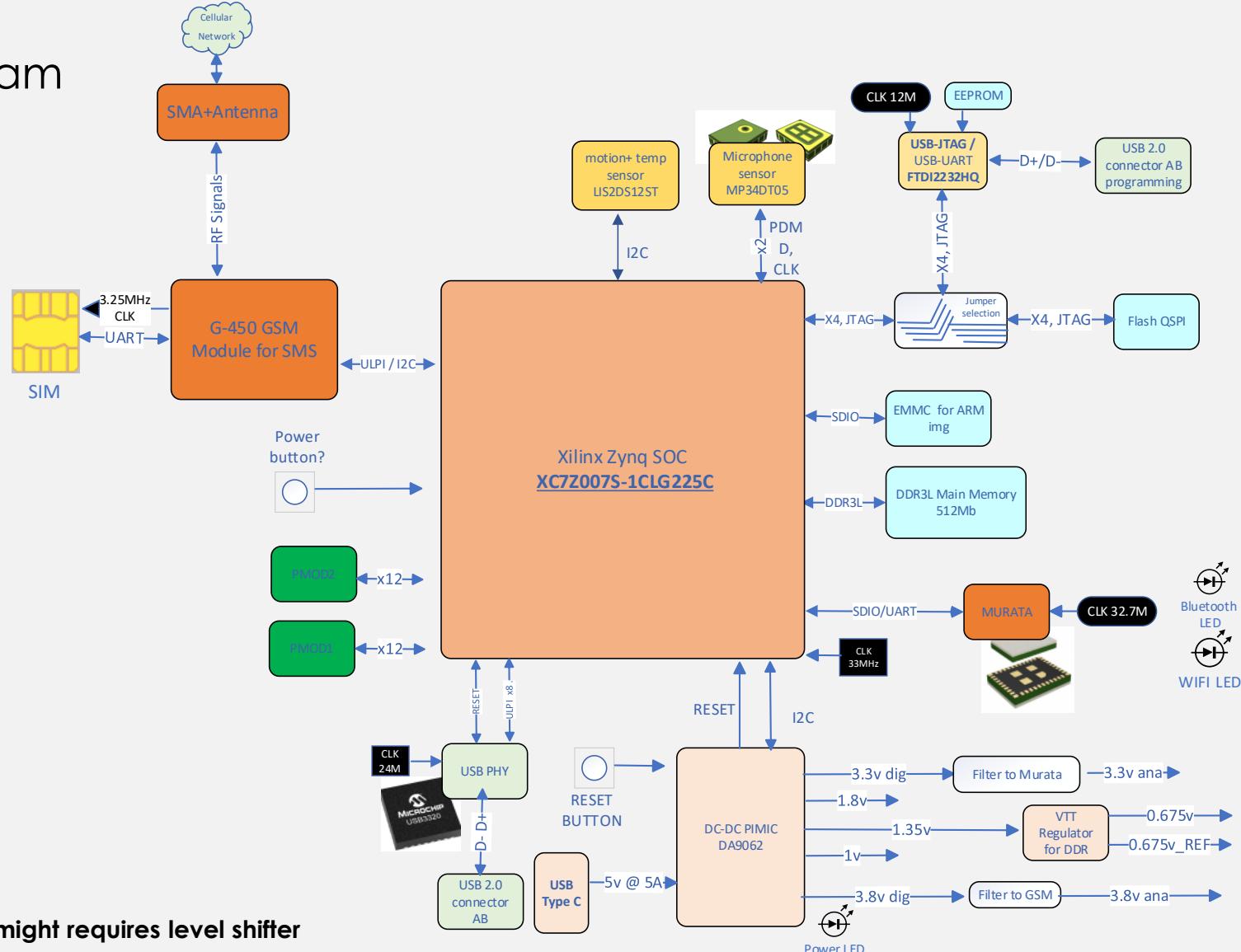
# OBJECTIVE

---

- Providing Smart helmet solution to the growing market of scoot and cycling
  - Drop sensor
  - Microphone
  - Bluetooth
  - PMODs for external peripherals like camera
  - Spec requirement – **EMI – TBD**
  - Spec requirement – **TBD**
  - Added SOS SMS messaging
- Competitors:
  - [Livall EVO21 Smart Helmet](#) – with fall detection and SOS texting with location to a selected and Rear and front lights
  - [KRACESS Bike Helmet](#) – with Bluetooth, video camera recorder, built in microphone and stereo speakers
- Optional – Add Rear and front lights
- Optional – Add **built in** Dash came
- Optional – Add build in stereo speakers for phone calls – consider the safety risk

# BLOCK DIAGRAM

## Block Diagram



# MAIN COMPONENTS

Component	P/N
Zynq single-core System-on-Chip	XC7Z007S-1CLG225C
Micron DDR3L memory	MT41K256M16TW-107
Micron QSPI flash memory	MT25QL128ABA8E12-0SIT
Micron on-board eMMC memory	MTFC8GAKAJCN-4M
Wireless Radio Module	Murata LBEE5KL1DX
USB Host Interface (mouse, keyboard or USB camera )	Microchip USB3320C USB 2.0 A USB Type A USB0 connector
<b>“On Board JTAG and UART FTDI Device”</b>	<b>FT2232HQ</b>
Pmod connectors	Two 12-pin Pmod connectors

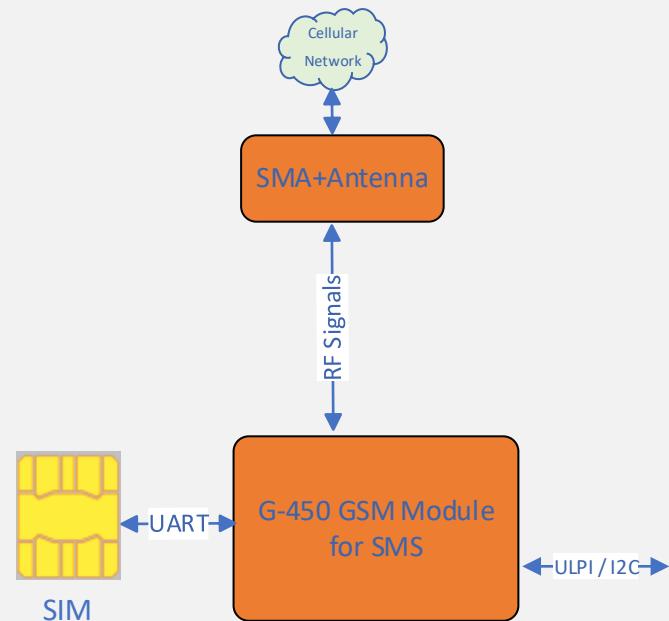
\* Taken after review from the architecture requirement document

# MAIN COMPONENTS – CONT'

Component	P/N
Microphone Input	MP34DT05
Motion & Temperature sensor	LIS2DS12
Push Buttons <ol style="list-style-type: none"><li>1. A pushbutton switch feeds into the power supply, where it is de-bounced and used to trigger a hard power-on reset.</li><li>2. Another pushbutton switch is connect to the PS and can be used as a MIO input.</li></ol>	TBD
<b>Optional – Camera, Rear and front lights, Stereo speakers</b>	TBD

# SMS COMPONENTS

Component	P/N
SARA-G450 Quad-band GSM/GPRS module for SMS SOS texting	SARA-G450-01C-01
Nano SIM Card Holder	0786463001
SMA straight female for 1.2mm PCB Edge	526-5791



\* **GSM is Typ 3.8v so might requires level shifter**

# CLK

CLK Component	P/N
Zynq PS clock – 33.33 MHz Microchip	DSC1001DI1-033.3333T Oscillator
USB OTG PHY – 24 MHz Microchip	DSC1001DI1-024.0000T Oscillator
USB-to-serial FTDI device – 12 MHz Abracon LLC	ABM8G-12.000MHZ-B4Y-T Crystal
Murata 1DX wireless module LPO (low power oscillator) – 32768 Hz Abracon LLC	ABS07AIG-32.768KHZ-1-T Crystal
<b>Microphone sensor – 1.2–3.25MHz Clk</b>	<b>TBD ( option to get it from Zync)3.25</b>
<b>3.25MHz SIM_CLK is generated by the GSM Module</b>	

# FPGA PROGRAMMING

- Default Boot from Quad SPI
- Option to external connection for programming – requires split – mind the stubs, **consider jumpers or dip switch.**
- From the requirements document:

● Boot mode:

Table 15 – Boot Mode Switch Selections

Boot Mode	Default Setting	Function
SW1	PS_MIO[5]	J (VCC) PS-PL JTAG Cascaded
SW1	F (GND)	QSPI Boot Mode

- From the block diagram:

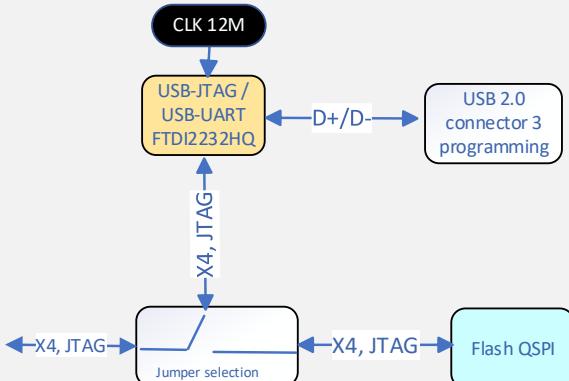


Table 6-4: Boot Mode MIO Strapping Pins

Pin-signal / Mode	MIO[8]	MIO[7]	MIO[6]	MIO[5]	MIO[4]	MIO[3]	MIO[2]
VMODE[1]	VMODE[1]	VMODE[0]	BOOT_MODE[4]	BOOT_MODE[0]	BOOT_MODE[2]	BOOT_MODE[1]	BOOT_MODE[3]
<b>Boot Devices</b>							
JTAG Boot Mode; cascaded is most common <sup>(1)</sup>	0	0	0				
NOR Boot <sup>(3)</sup>	0	0	1				
NAND	0	1	0				
Quad-SPI <sup>(3)</sup>	1	0	0				
SD Card	1	1	0				
<b>Mode for all 3 PLLs</b>							
PLL Enabled		0	Hardware waits for PLL to lock, then executes BootROM.				
PLL Bypassed		1	Allows for a wide PS_CLK frequency range.				
<b>MIO Bank Voltage<sup>(4)</sup></b>							
	<b>Bank 1</b>	<b>Bank 0</b>	Voltage Bank 0 includes MIO pins 0 thru 15. Voltage Bank 1 includes MIO pins 16 thru 53.				
<b>2.5 V, 3.3 V</b>	0	0					
<b>1.8 V</b>	1	1					

**Notes:**

1. JTAG cascaded mode is most common and is the assumed mode in all the references to JTAG mode except where noted.
2. For secure mode, JTAG is not enabled and MIO[2] is ignored.
3. The Quad-SPI and NOR boot modes support execute-in-place (this support is always non-secure)
4. Voltage Banks 0 and 1 must be set to the same value when an interface spans across these voltage banks. Examples include NOR, 16-bit NAND, and a wide TPIU test port. Other interface configuration may also span the two banks.

# POWER

- USB2 input power, 5V and up to 0.5A – not sufficient
- For More power, I will use USB Type C for 5V At 5A
- **PIMIC DA9062**, optimized for mobile devices, 4 Bucks, 4 LDOs, up to 8.5A
  - ESD protection
  - Low switching frequency of 3MHz – high buck freq => small circuits around it.
  - We will operate the following FPGA power sequence controlled by the PIMIC :
    - **1v -> 1.8v -> 1.35V -> 3.3V**
  - This power sequence is recommended in the Zync data Sheet DS18
- Will consider **VTT voltage regulator BD3539FVM-TR** for DDR terminations stable voltage with sinking and sourcing capabilities
- Will consider **Additional buck converter** for the GSM 3.8V

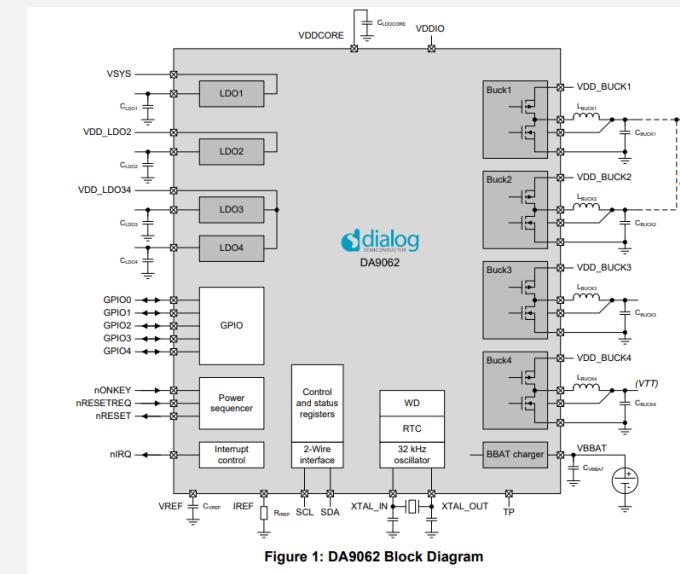


Figure 1: DA9062 Block Diagram

# BOM + POWER CALC

Note – the BOM here does not include passive component ( R L C)

my note	Part	Manufacturer PN	Description	Qty	unit price(usd)	voltage[v]	Max current[A]
FPGA+ARM	Zync	XC7Z007S-1CLG225C	SoC FPGA XC7Z007S-1CLG225C Zynq 7000 series	1	60	3.3v, 1.8V, 1V, 2.5V	? TBD
memories	DDR3L	MT41K256M16TW-107	Micron DDR3L memory (DRAM or SDRAM) 32 Meg x 16 x 8 banks TW = 96-ball (8mm x 14mm) <b>Rev. P</b> Timing – cycle time – 1.07ns @ CL = 13 (DDR3-1866) -107	1	7.41	1.35v	0.16
memories	QSPI Flash	MT25QL128ABA8E12-0SIT	Micron QSPI flash memory (for Zync FPGA Logic) NOR Flash SPI FLASH NOR SLC 32MX4 TBGA	1	3.97	3.3v	0.05
memories	OUT OF STOCK	MTFC8GAKAJCN-4M	Micron on-board eMMC flash memory (for the embedded CPU - OS)	0	OUT OF STOCK		
memories	emmc	SFEM064GB2ED1TO-I-6F-111-STD	on-board eMMC flash memory (for the embedded CPU - OS)	1	30.5	3.3v	0.1
Power management	PIMIC POWER	DA9062	power management integrated circuit (PMIC) (4LDO and 4Bucks), <b>5V input and up to 8A Output</b>	1	5	5v	
USB To JTAG	USB To JTAG	FT2232HQ-REEL	USB Interface IC USB HS to Dual UART/FIFO/SPI/JTAG/I2C	1	5.3	1.8V	0.07
clk - osc	clk for the Zync	DSC1001DI1-033.3333T	Standard Clock Oscillators MEMS Oscillator, Low Power, -40C-85C, 25ppm	1	1.22	1.8 or 2.5 or 3.3	0.01
clk - osc	clk for USB PHY ( CMOS OSC)	DSC1001DI1-024.0000T	DSC1001DI1-024.0000T Oscillator	1	1.38	1.8 or 2.5 or 3.3	0.05
clk - Crystal	clk for FDTI (crystal)		ABM8G-12.000MHZ-B4Y-T crystal	1	0.58		
clk - Crystal	clk for Murata ( crystal)		ABS07AIG-32.768KHZ-1-T crystal	1	0.67		0.05
RF WIFI+Bluetooth	Murata	LBEE5KL1DX	Murate Wireless Radio Module	1	11.24	3.3v	0.37
USB data to FPGA	USB PHY	USB3320C	USB 2.0 ULPI Transceiver	1	1.92	1.8v or 3.3v	0.03
PMOSs	external peripherals	PMOD Header 12 female	12 pin pmod connector	2	1		
sensors	motion sensor	LIS2DS12	motion and temp sensor	1	3	1.8V	0.015
sensors	microphone sensor	MP34DT05	microphone input	1	1.5		
SMS part	GSM Module for SMS	SARA-G450-01C-01	<b>SARA-G450</b> Quad-band GSM/GPRS module	1	14.71	3.8v	2
SMS part	SMA conn for Antenna connection	526-5791	SMA straight female for 1.2mm PCB Edge	1	8.9		
SMS part	nano sim card holder	786463001	6 Position Card Connector NANO SIM Surface Mount, Right Angle Gold		0.5		
				Total Price[\$]	134.69	Current SUM without FPGA [A]	2.905

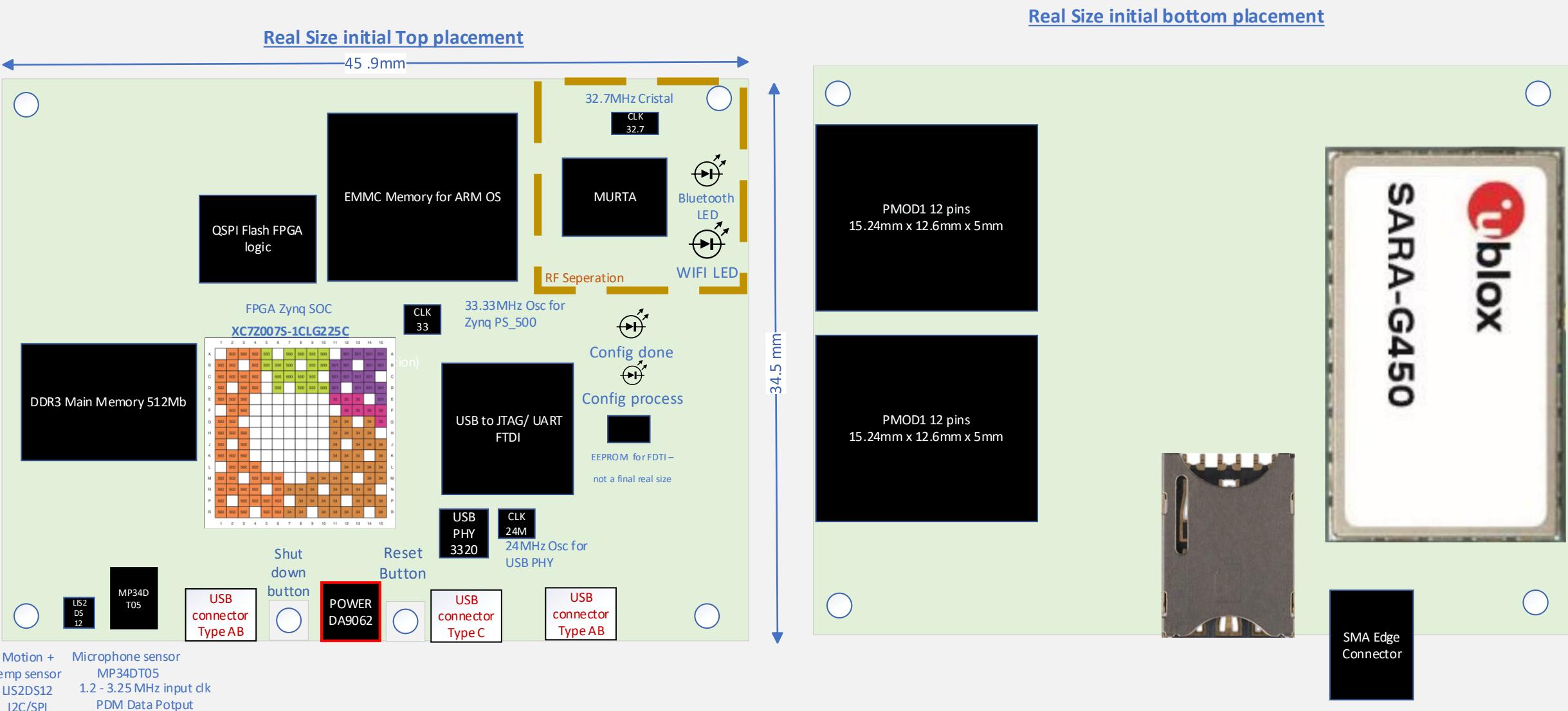
## distributions)

device	Part number	1.2v[mA]	1.8v[mA]	2.5v[mA]	3.3v[mA]	P[mW]	Cost[\$]
xilinx 4vfx20ff672-10	XC4VFX20-10FFG672C	241		210	100	1144.2	72
serial prom	XCF32PVOG48		10		15	67.5	25
ds3150	DS3150T				95	313.5	18.5
ds3170 ds3-framer	DS3170				120	396	25
88e111-gbit * 2		500		762		2505	12
e1 liu	DS21348T+				66	217.8	7.5
2*ddr	MT46V64M16P			250		625	10
flash	S29GL128N				10	33	6.5
osc-44m					25	82.5	5
osc25m					25	82.5	8
ASI	CYP15G0101DXB-BBC				330	1089	14
sram X 2	K6R4016V1D-UL10				65	214.5	10
Ix971 fast phy					142	468.6	3.5
pi3807						0	0.4
clk synt-In25 O 27,2.048,100	CY22393FC				37	122.1	2
I/O Expender	MCP23017-E/SS / MCP23S17-E/SS				47	155.1	0.9
Connectors -Hi speed 100pin	QTS-050-01-L-D-RA-WT					0	
RS232						0	1
HotLink					330	1089	12
Temp sensor						0	
Misc						0	30
Total		741	10	1222	1407	8605.3	263.3
watt		0.8892	0.018	3.055	4.6431	8.6053	

8.6 Watt 263 \$

# INITIAL PLACEMENT- Real Size

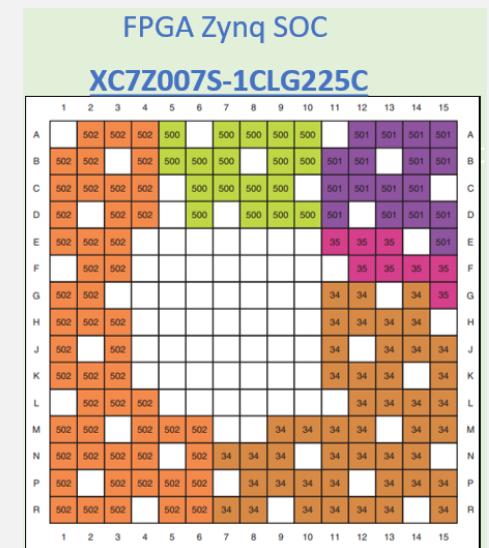
- Note – can extend the PCB sizes to 71mm x 71mm according to the requests



# STUCK UP

- Stuck Up Considerations:
  - Hard estimation, due to ~3 internal FPGA “Rings”, the PCB will require 3 signal layers
  - 1 power plane + power planes in one of the slow signal layer should be enough **but additional power plane will be considered**
  - Power plane close to above main FPGA for quick power supply
  - Signal fields and Power fields are contained to avoid EMI and SI interference
- Due to above, the following 8 layers stuck up is proposed

Layer	Type
L1	Signal
L2	GND
L3	POWER
L4	Signal + Power ( Low speed signals)
L5	GND
L6	Signal (High speed, less Stub)
L7	GND
L8	Signal



# BUILD UP

- From PCBWay manufacturer
- Materials listed are not final
- Controlled impedance will be calculated for 50ohm SE and differential according to requirements

8-layer PCB standard stackup

Thickness	Copper thick (outer/inner)	Layer No.	StackUp	Laminated chart Thickness
1.2mm±10%	1/1oz	L1		Copper 18 um--plating to 35um
		L2		PP 0.11 mm(2116) dielectric constant 4.29 ± (The DK value is not absolute and will vary depending on the base material's models and thickness.)
		L3		Core 0.2mm with 1/1 oz Cu
		L4		PP 0.11 mm(2116) dielectric constant 4.29 ± (The DK value is not absolute and will vary depending on the base material's models and thickness.)
		L5		Core 0.2mm with 1/1 oz Cu
		L6		PP 0.11 mm(2116) dielectric constant 4.29 ± (The DK value is not absolute and will vary depending on the base material's models and thickness.)
		L7		Core 0.2mm with 1/1 oz Cu
		L8		PP 0.11 mm(2116) dielectric constant 4.29 ± (The DK value is not absolute and will vary depending on the base material's models and thickness.)

# MECHANICS

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- Highest Part is the PMOD – 5.2mm
- Mounting holes
- PCB Thickness: 1.2mm
- Initial PCB Size 45.9cm x 34.5cm – smaller than the requirements so might consider to enlarge

# Open issues

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- PCB layer amount(8) will be considered to raise to 10 due to the:
  - large number of voltages
  - small package BGA and close voltage pins
  - GSM device will need 2A bursts so might consider getting a Power plane closer to its bottom location
- Check if the FTDI requires EEPROM
- Check how to connect the PIMIC to the FPGA
- PIMIC – verify the power sequence works well with the FPGA and the other circuits
- GSM is 3.8v so might require level shifter

# SCHEDULE

- Timeline
- Note – Moshe reference timeline is too long according to Ziv – to reduce all the 10W lines.
- Good timeline is about 6-7 months according to Ziv

Tasks	Weeks	data
PDR	2	10-Jan-24
CDR Schematic View	3	29-Jan-24
Complete Layout + simulations	10	1-Apr-24
Complete PCB Layout	2	15-Apr-24
Completed Assembly	2	29-Apr-24
First integration	6	27-Jun-24
full integration	10	29-Aug-24

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First integration	6 <del>3</del>	27-Jun-24
full integration	10 <del>3</del>	29-Aug-24

# RISKS

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- EMC radiation
- Cellular radiation – need to check Specs
- RF parts – keep good separation
- Bottom parts, will have long path access to Power plane L4 which is far from the bottom

**End**

Draft

# FPGA PROGRAMMING

- How do we load to FPGA – QSPI Flash
- JTAG connection option 1:
  - 6 pin header connecting to Xilinx Platform Cable(red box)
  - Editing the VHDL Code,
  - signal monitoring
  - programing.
  - 100EURO
  - currently preferred option
- JTAG connection option 2:
  - JTAG-USB Cable by Diligent
  - 60 USD



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USB JTAG-Kabel HW-US...

