Smart Helemet Prototype Schematic

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Size: B	Document Number: 1	Rev: RevA0
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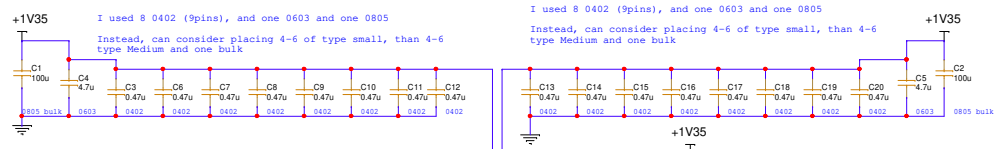
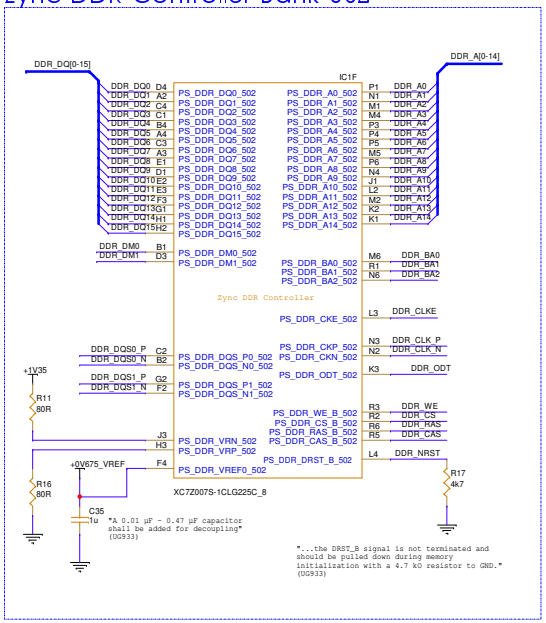
Zync DDR Interface

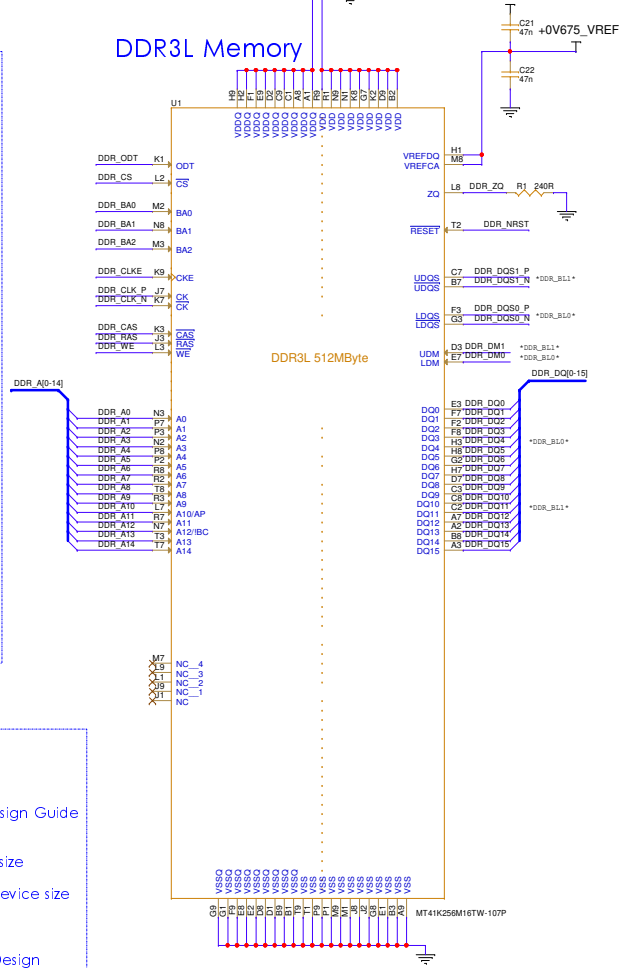
DDR Routing - Zync -> DDR3L -> VTT Resistors -> bypass capcitors



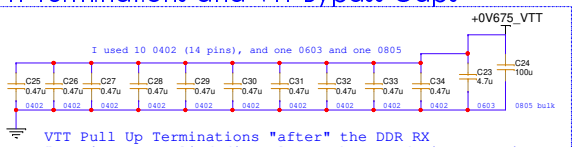
Zync DDR Controller Bank 502



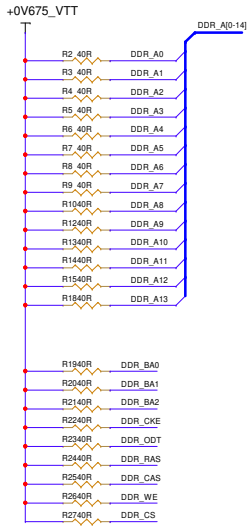
DDR3L Memory



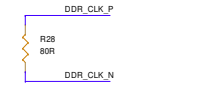
VTT Terminations and VTT Bypass Caps



VTT Pull Up Terminations "after" the DDR RX
"VTT is not applied directly to the DDR device. VTT is a system supply for signal termination resistors"(DDR data sheet)



DDR CLK differential Termination



Notes

DDR_Part:

1. DDR ZQ calibration resistor value of 240[ohms] acoording to Zync Design Guide (UG933) table 5-11
2. DQ Only - Bytes groups swapping is optional on the Memory device size
3. DQ Only - bits in Bytes groups swapping is optional on the Memory device size

Zync_DDR_Part:

1. Zync VRN VRP pull up/down values of 80[ohms] acoording to Zync Design Guide (UG933) table 5-2 (double the DDR SE trace and voltage of VCCO_DDR)

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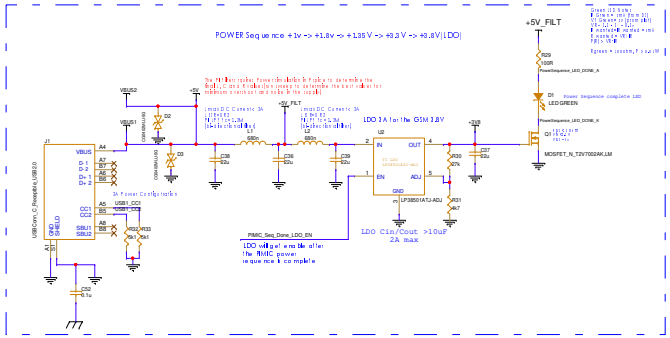
Power

USB TypeC 3A Power input and LDO for the GSM



Zync PL/PS Power and Decupling

Zync PS Decupling capacitors notes:

recommended capacitors amount, value, size, ESR are taken from DesignGuide933(in case I did not have it, I would use 10uF as bulk, and 100uF per pin)

with the following notes:
1. Values can be larger than specified (DC Voltage derating)
2. Body size can be smaller than specified.
3. ESR must be within the specified range.
4. Voltage rating can be higher than specified(due to voltage derating

Rule of thumb used when moving to bigger capacitor – increasing the value times 10 (at least)

according to the 933, can consolidate the bulk caps for:
VCCINT and VVCPINT
VCCAUX and VCCPAXUX

cannot consolidate the bulk for VCCIO_MIO0 and VCC_MIO1

Bank34 and 35 decupling notes:
can consolidate the 100uF bulk into 1 shared bulk for both
tThe 100uF bulk can be also 47uF

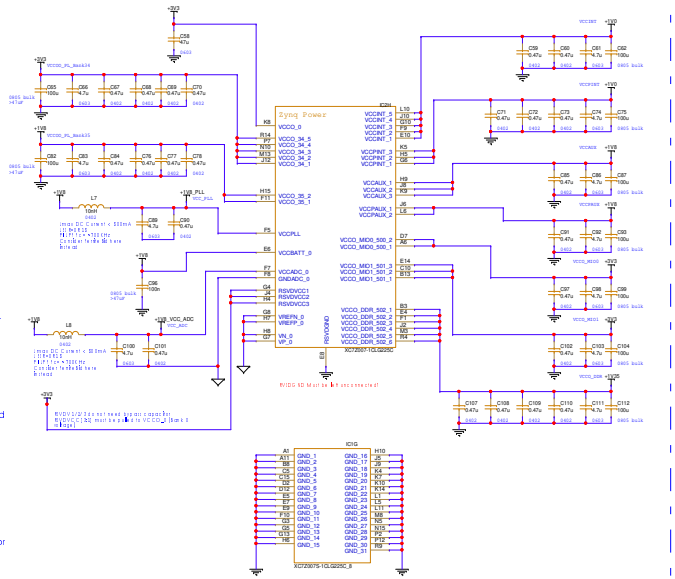
for bank 35 can consider using less decups since it has only 2 pins for this ZYNC7007

VCCBAT
for use with battery in case we need "bitstream encryption! – not used in this project so just connected to the bank 0 voltage of 1.8V

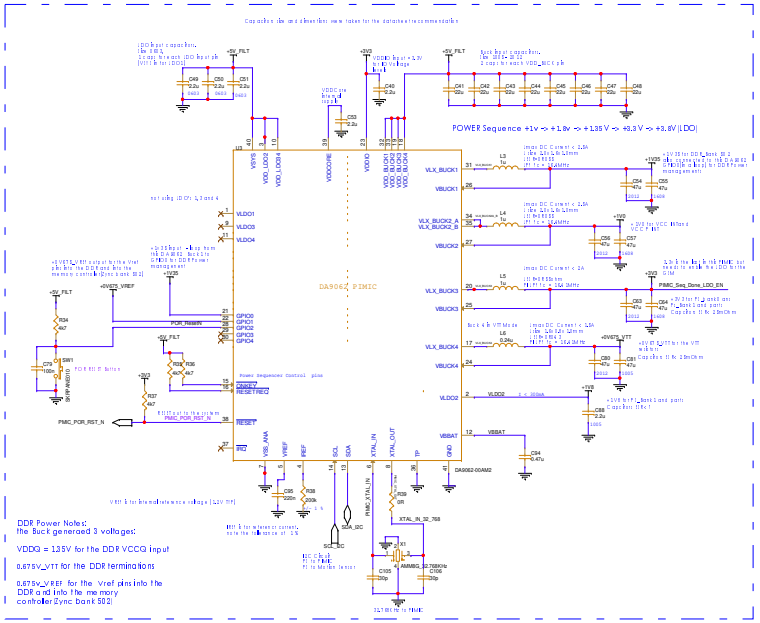
VCCADC_0
This pin s of internal ADC of 12 bits also called "XADC" and it reuired filtering the lines with inductors or Ferrite bids

VP, VN
This is the possitive and negative analog inputs that make up the 17th input to the XADC.

VREFN_0 VREFP_0 This is the input threshold voltage for Bank 0.



PIMIC Power Management, DDR Power management and POR Button



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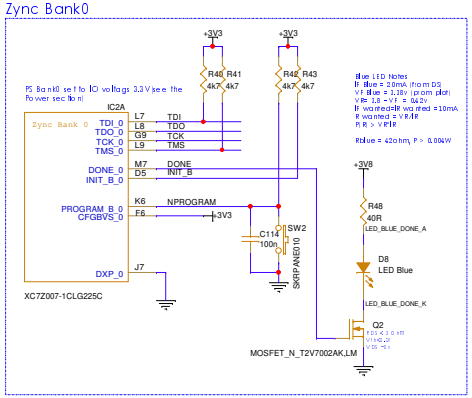
Zync Programming

Zync Bank0



Zync Bank 0 notes:

see UG470 configuration pins

DONE_0:
indicate the completion of the configuration sequence
OPEN-DRAIN Output(there is internal resistor so the 4k7 is optional addition)

INIT_B_0
Active Low FPGA init or configuration error pin – connected to 4k7 pull up to VCC_O

PROGRAM_B:
ProgramB_0 is Active Low Reset to the FPGA(FPGA Reset Button)

CFGBVG_0(config bank voltage select):
VCCO_0 (vcc bank0) is +3V3 => CFGBVG_0 = 1 (connecccted to VCCO_0)

VN_0/VP_0 = 0 (internal ADC inpputs) – not used
DXP_0/DXN_0 – temp meas pins(old option, not recommended) – not used
VREFP/VREFN – reference inputs for the internal ADC – not used(different symbol here)

Xtal notes:

F0 = 12MHz
C0 = 5pF
ESR = 120ohm

Rext = 10% from:
1/(2*pi*F0*C0) = 1326
Rext = 130ohm (can use 100ohm)

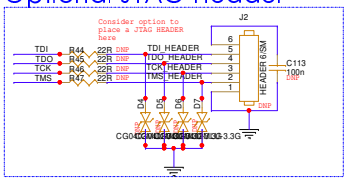
CS is the straw capacitace and it's 3-5PF
CL= CL1 = CL2 = 2*(C0 - CS) = 10-14pF
Will use CL1=CL2 = 30PF because of:
* DC voltage derating
* Capacitance Tolerance
* XTAL Manufacturer recommendations

EEPROM

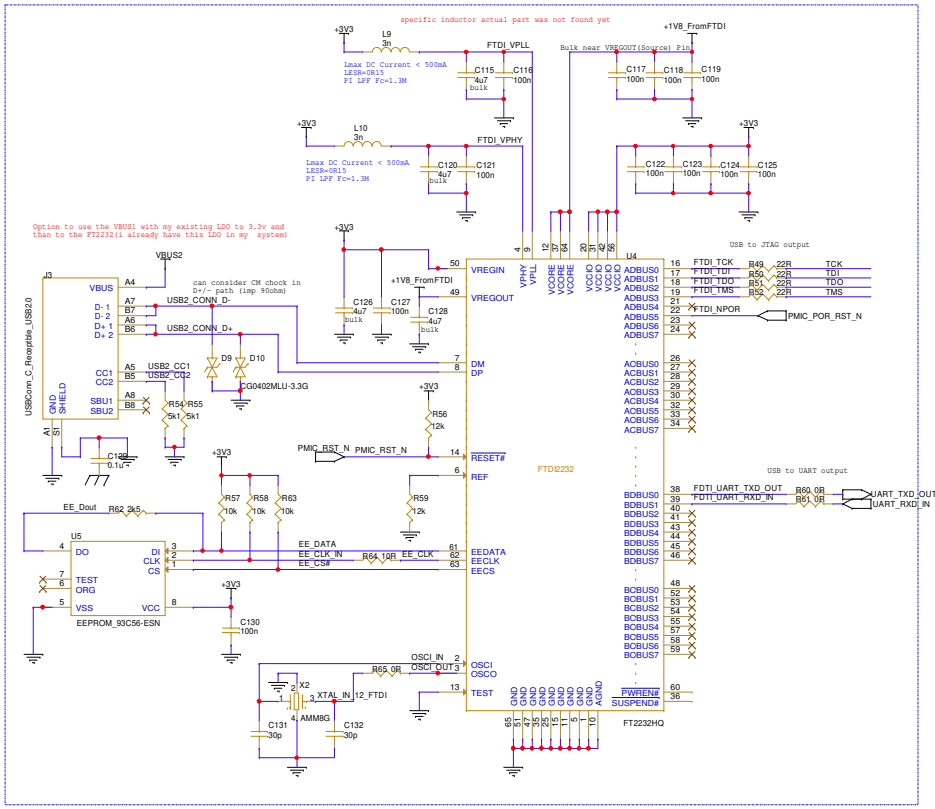
EECLK R value could be edites later

The EEPROM is programmable in-circuit over USB using a utility program called FT_PROG.

Optional JTAG Header

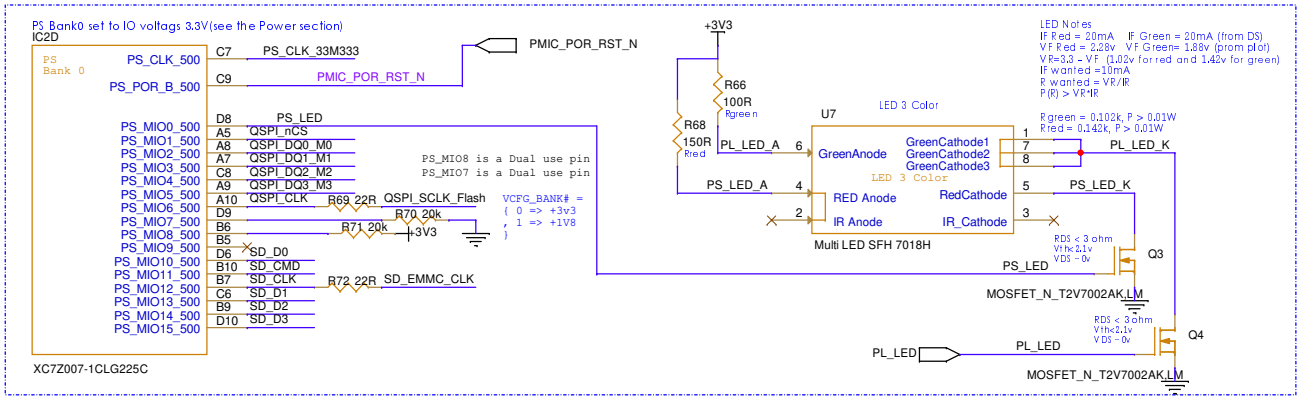


FTDI JTAG Programmer USB to JTAG and USB To UART



Zync PS Banks & Boot

PS Bank 0



PS Bank0 notes:

Pins MIO 3–8 are configuration Boot pins
MIO3–5 set the boot mode

Default boot from QSPI:
MIO3 '0' (DQ1_M1) sw1–6 Close
MIO4 '0' (DQ2_M2) sw2–5 Close
MIO5 '1' (DQ3_M3) sw3–4 Open

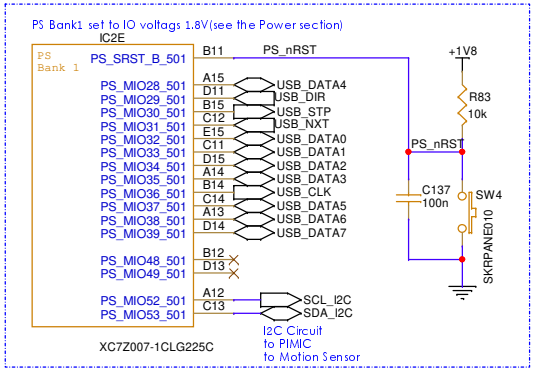
Additional JTAG Boot 1 for debug:
From USB trough FTDI JTAG output:
MIO3 '0' (DQ1_M1) sw1–6 Close
MIO4 '0' (DQ2_M2) sw2–5 Close
MIO5 '0' (DQ3_M3) sw3–4 Close

Additional JTAG Boot 2 for debug:
From JTAG Header trough Xilinx red BOX("Xilinx Platform Cable) or "Digilent JTAG Cable":
Place DNP 22 ohm resistors near the JTAG Header, and:
MIO3 '0' (DQ1_M1) sw1–6 Close
MIO4 '0' (DQ2_M2) sw2–5 Close
MIO5 '0' (DQ3_M3) sw3–4 Close

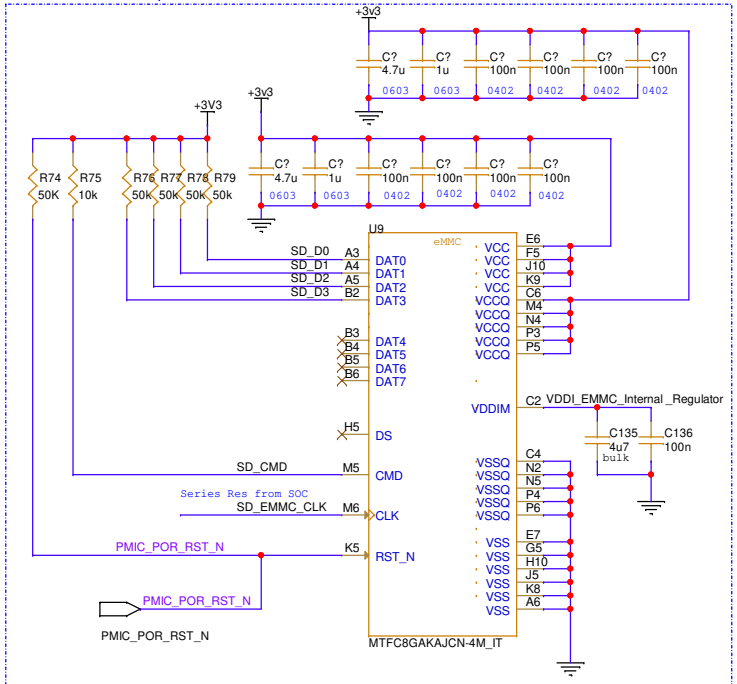
MIO7 and MIO8 are Dual use pins that are shared with the highspeed QSPI/NAND/SRAM
MIO7_500 Pull down with 20K => set MIO_BANK0 VCCO_MIO0 to +3V3

MIO8_500 Pull up with 20K to 3+3.3V => set MIO_BANK1 to +1V8

PS Bank 1

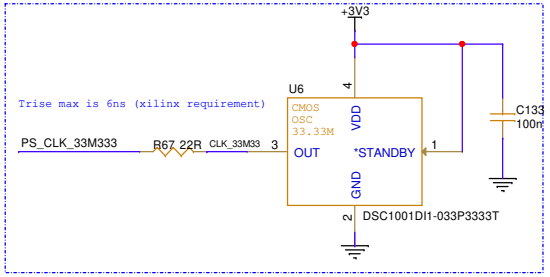


EMMC Memory

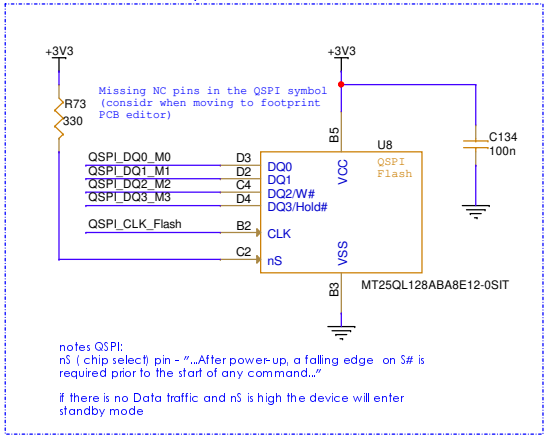


EMMC Notes
SD_EMMC_CLK arriving after serin 22ohm series termination from the Zynq
EMMC Pull ups values from: "Recommended PCB Routing Guidelines for SHM_e.MMC.pdf"

PS CLK 33MHz



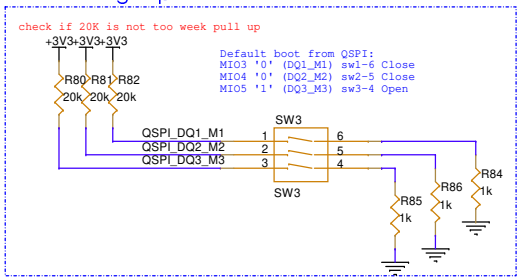
QSPI Flash Memory



notes QSPI:
nS (chip select) pin - "...After power-up, a falling edge on S# is required prior to the start of any command..."

if there is no Data traffic and nS is high the device will enter standby mode

Boot Config Dip Switch



Title: Zync PS Banks & Boot Circuits		
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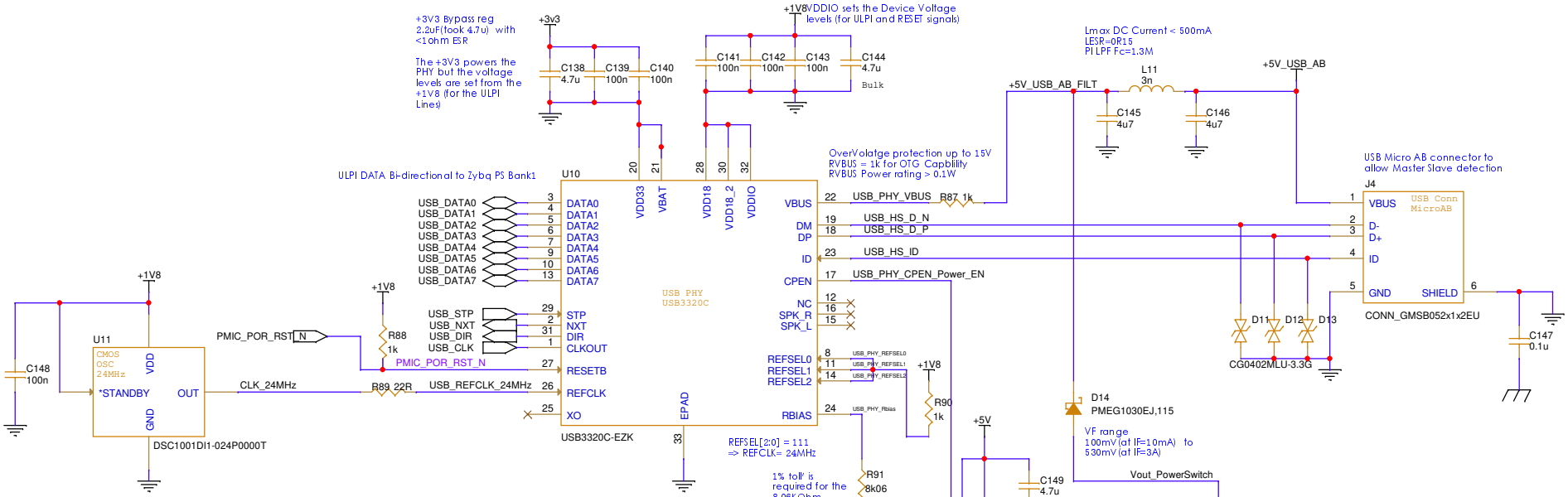
USB High-Speed OTG Circuit



USB3320 PHY Notes: need to check USB PHY CLK Rise time requirements

USB OTG("On The Go") is implemeted with USB Connector micro AB

Ths U3320 boot from the 3.3V but gets it's ULPI/RESET voltage levels from VDDIO voltage pin(1.8V) - to work with Zynq bank1=1.8V.

CLKOUT Pin:
Following POR or hardware reset, the voltage at CLKOUT must not exceed VIH_ED of 0.4* VDDIO (0.72V)

REFSEL 2 1 0 = 1 1 1 => 24MHz input clk

CPEN Pin
External 5V supply enable. Controls the external VBUS power switch. CPEN is low on POR. this pin enables the Power switch when the connected USB is Slave and needs Power.

VDDIO Pin
External 1.8V to 3.3V ULPI supply input pin. This voltage sets the value of VOH for the ULPI signals.

VBAT Pin
Regulator input

RESETB Pin
When high, the USB3320 will operate as a normal ULPI

VOH > 1.4v
VIH > 1.224V
VIL < 0.72v
VOL < 0.4v

P_RVBUS = (Vprotect - 5)^2 / RVBUS=
(15v - 5) ^2 / 1k = 0.1W

CLKOUT Pin:
ULPI Input Clock Mode (60MHz from the Zynq)

OTG probebly requires the 24MHz CLK (that we have in the system) - need to verify.

Supply-Or-Draw-Current-Table

USB Connected PCB

Device/Slave Host/Master => host supply current, CPEN enables the Power switch. current comming for our PCB Main 5V supply(USB TypeC in our case) trough the Power switch(5V -> Vin -> VOUT - > zenerDiode -> Filter -> USB VBUS Pin)

USB Connected PCB

Host/Master Device/Slave => connected USB is the Host and it does not need current. we(PCB) also does not need current so the Power switch is of and also a zener diode is preventing current from arriving to the Poer switch

RLimit
connected to ILIMIT to determine the max current
Table 2 in the data sheet provides the resistor values and theie current limits.
RLimit= 500ohm to provide ~0.45A current limit

FAULT
Fault is an open drain circuit that should be pulld high in order to operate. did not use it here with LED indication for now

Title: USB High-Speed OTG Circuit			
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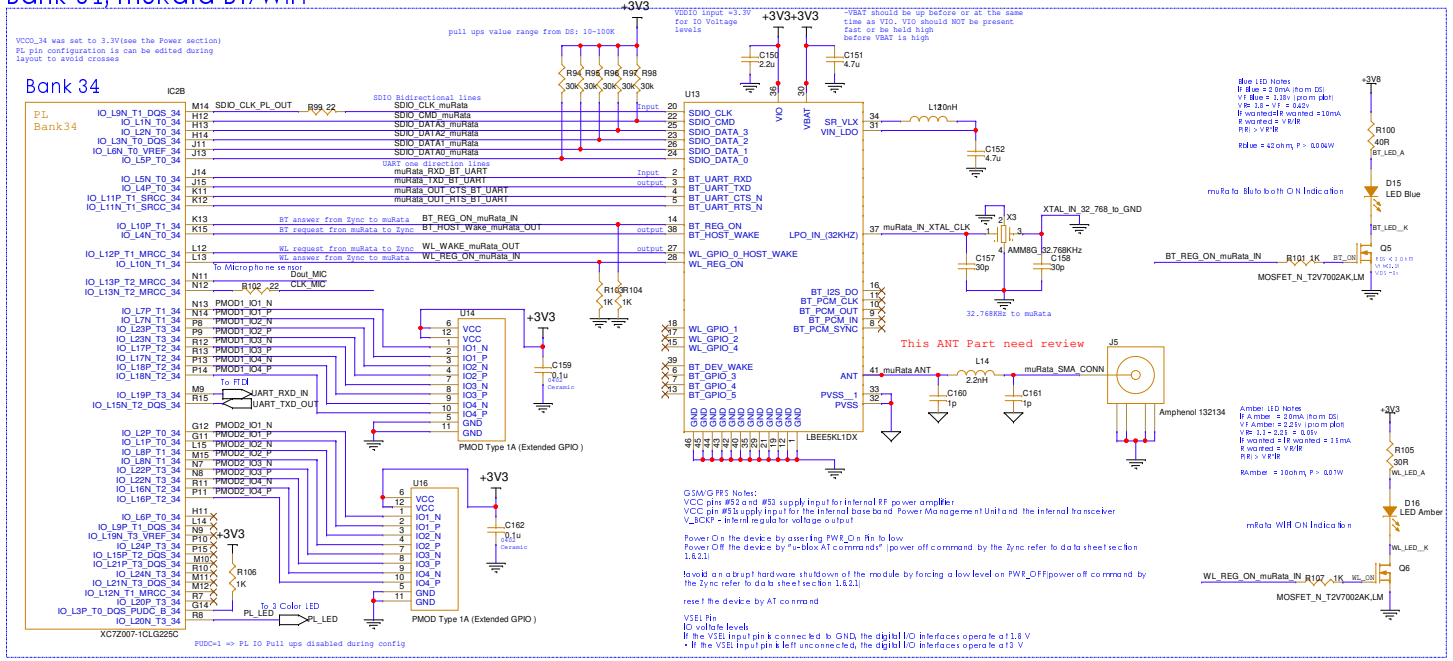
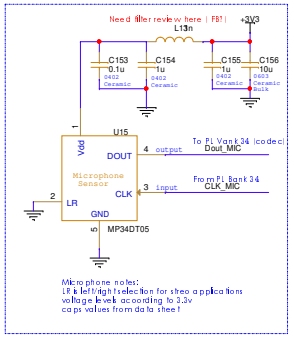
Zync PL, GSM, muRata & Sensors

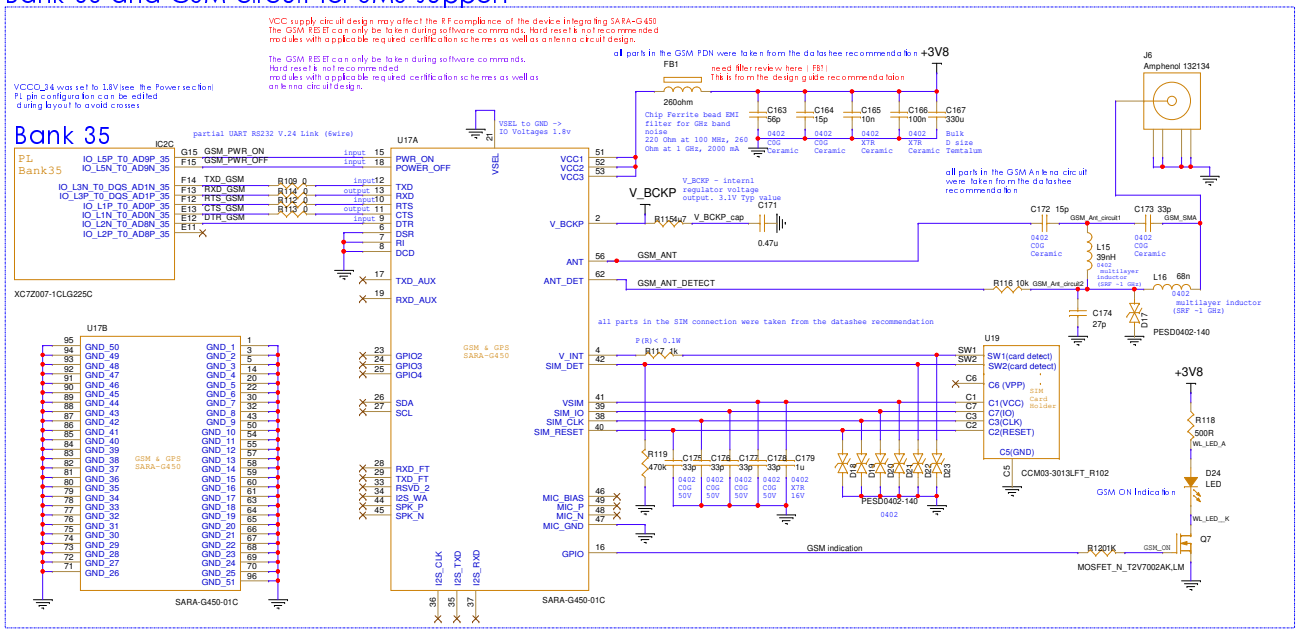
Bank 34, muRata BT/WiFi



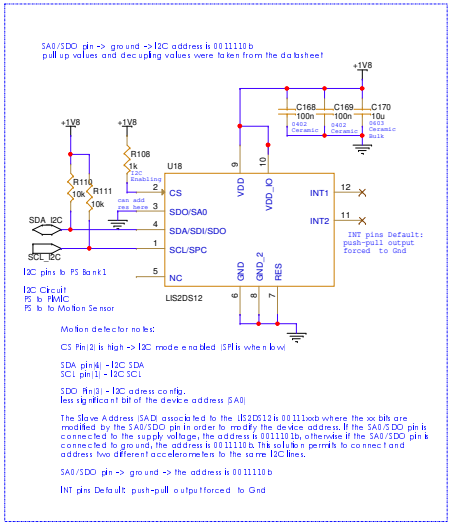
Microphone sensor



Bank 35 and GSM circuit for SMS support



Motion sensor



Title	Zync PL, GSM, muRata & Sensors		
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