PDN Pre layout Simulation with LTspice and UltraCAD by Moshe Saban

Notes:

Not including VIAs(0.7mm pad VIA with 1.2mm VIA length gives 0.495nH)

Not including GND Bounce conductor inductance (shown as ideal but they are not Ideal)

Ohmic Resistance – for 1Oz copper, 10 degC max temp rise:

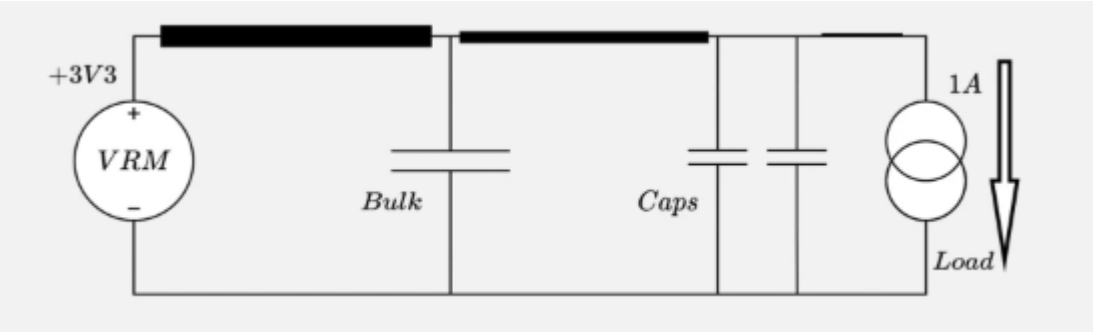
- W=0.3mm power trace width – 1.7mOhms/mm -> 1A (will use this power trace)
- W=0.6mm power trace width – 0.8mOhms/mm ->1.6A (will use this power trace)

Inductance – for 1Oz copper:

- W=0.3mm power trace width, H (dielectric)= 0.21mm -> 0.95nH/mm
- W=0.6mm power trace width, H (dielectric)= 0.21mm -> 0.48nH/mm
- W=0.3mm power trace width, H (dielectric)= 0.12mm -> 0.58nH/mm – (will use this power trace)
- W=0.6mm power trace width, H (dielectric)= 0.12mm -> 0.29nH/mm – (will use this power trace)

Capacitor ESL and ESR were taken from the muRata online tool – "SimSurfing"

General diagram:

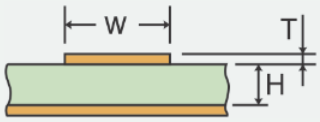


Inductance formula:

Trace Inductance Calculator

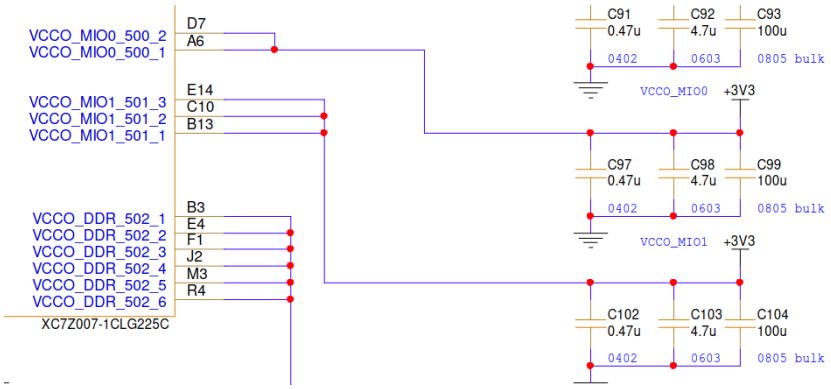
Trace Inductance calculator for wide traces over a ground plane with trace width (W) much larger than substrate thickness (T). Relative Permeability is assumed to be 1. Low frequency, perfect conductor: no skin effect.

Conditions: W>>H, H>T

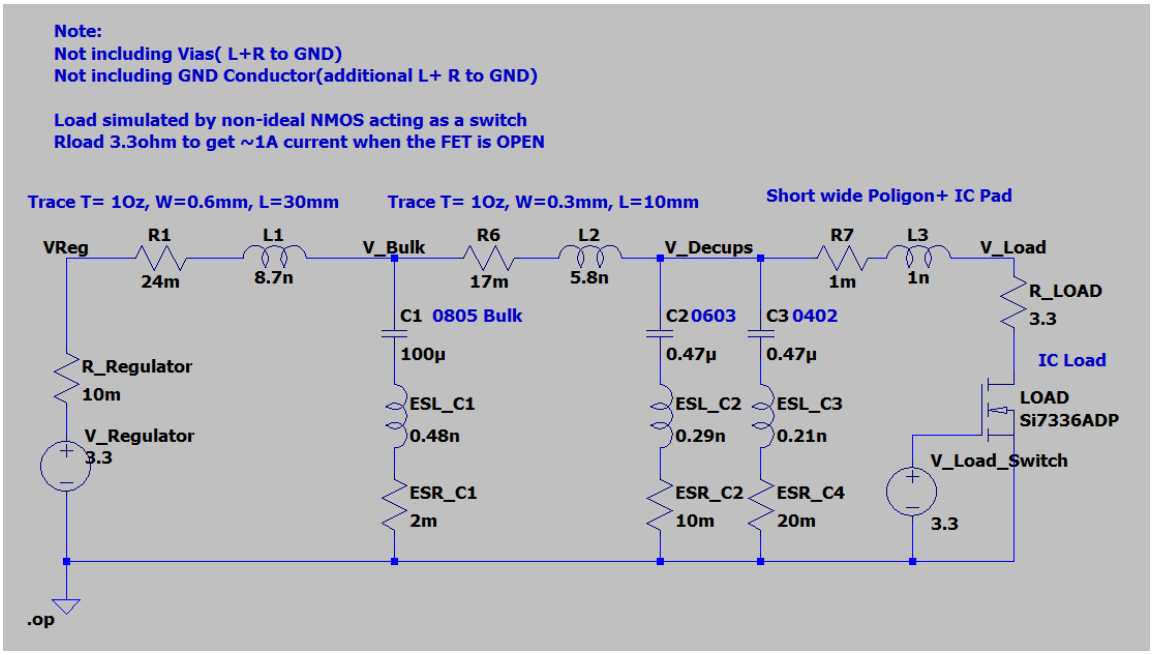


$$L \approx \frac{\mu_0 \cdot \mu_r \cdot (H + T/2) \cdot L}{W}$$

VCC_MIO0 Circuit from schematic:

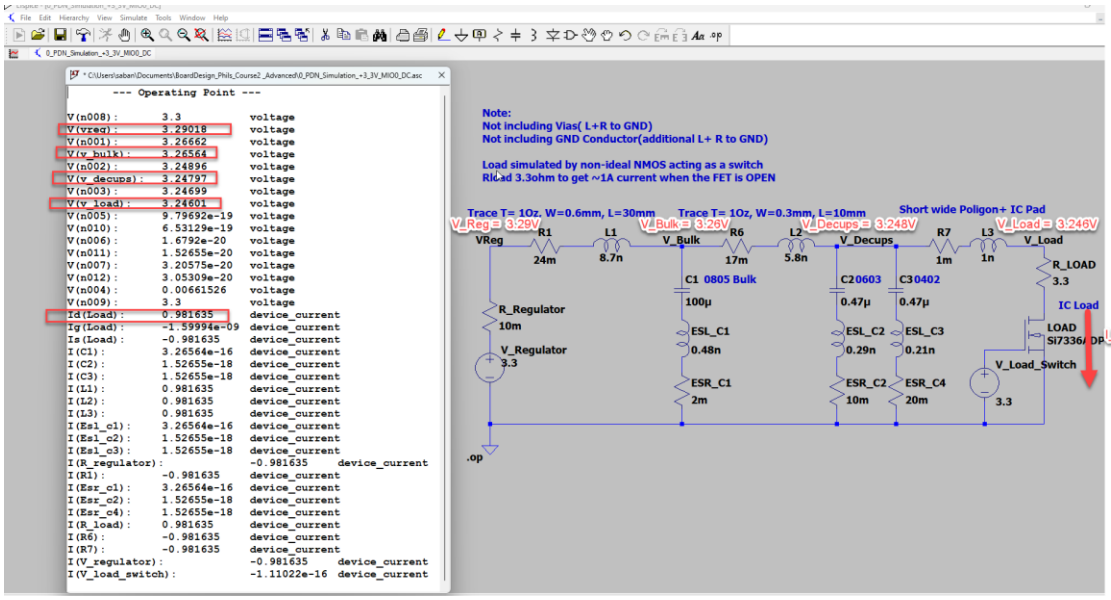


VCC_MIO0 Circuit in LTspice:



VCC_MIO0 DC voltage drop (Ohmic resistors only):

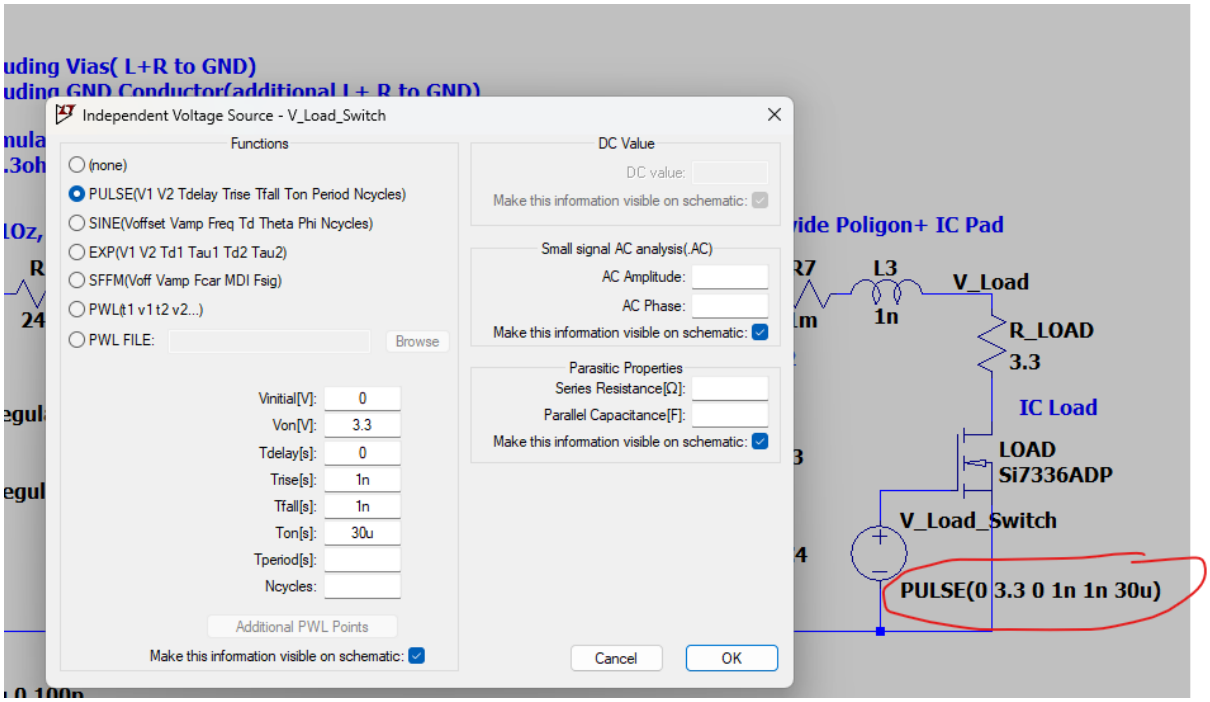
54mV Ohmic voltage drop (resistors only)



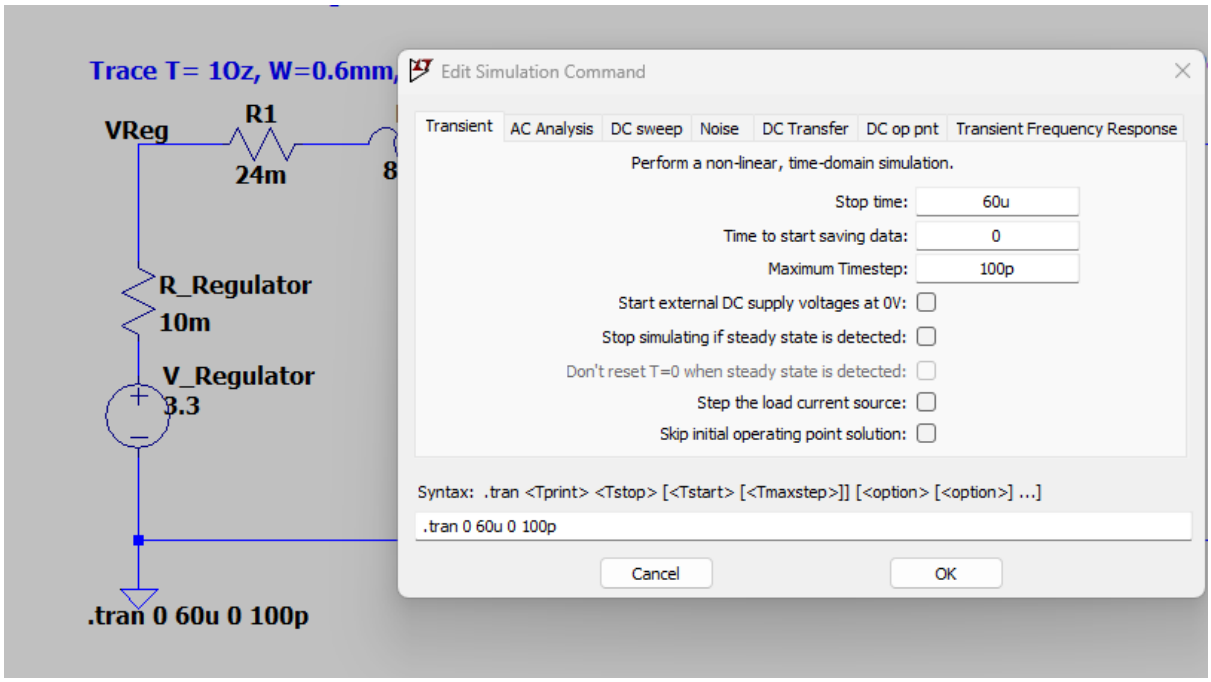
AC and switching characteristics.

Trise= Tfall = 1ns (0.001uSec)

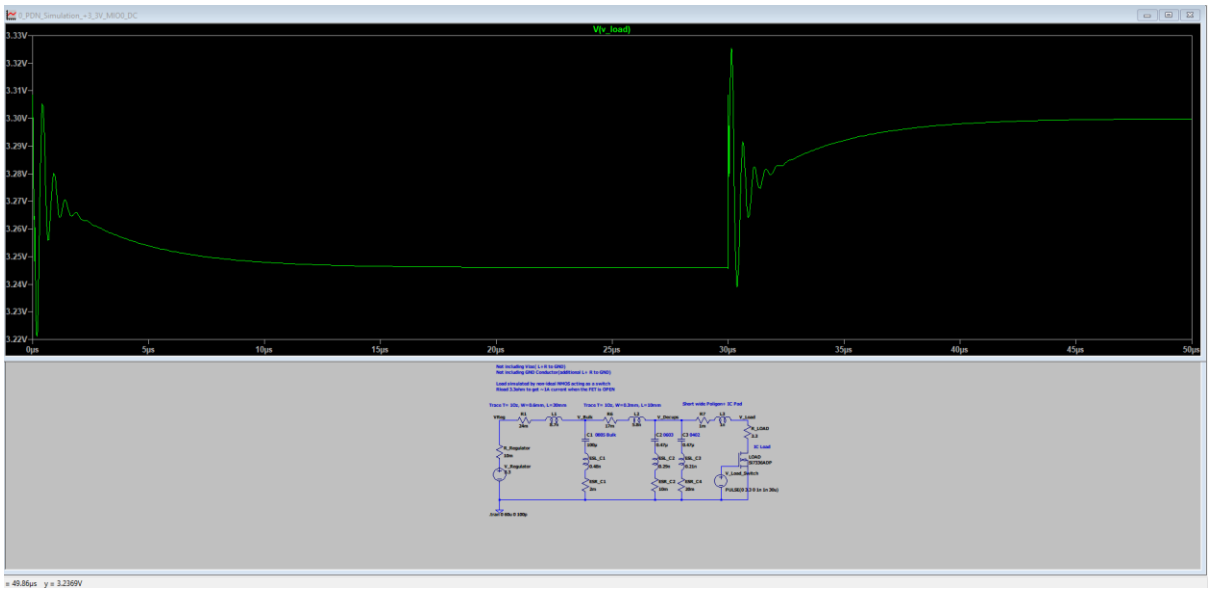
Pulse width = 30usec



Defining running time of 60uSec and measurement step(resolution) of 100psec



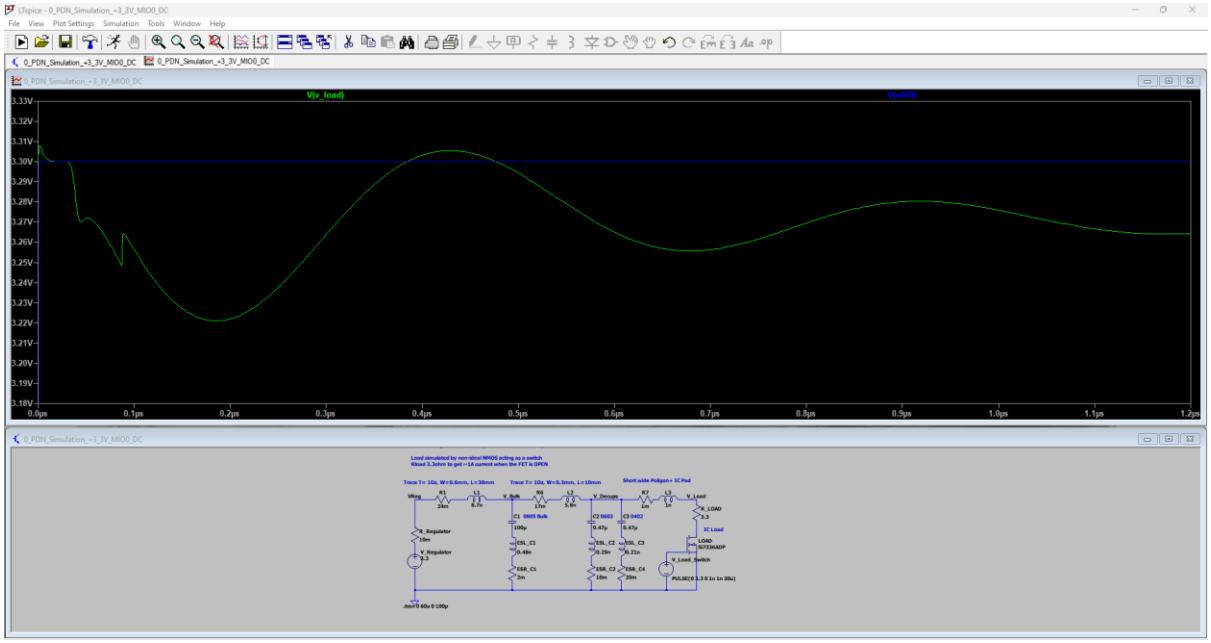
Results:



Vload Result:

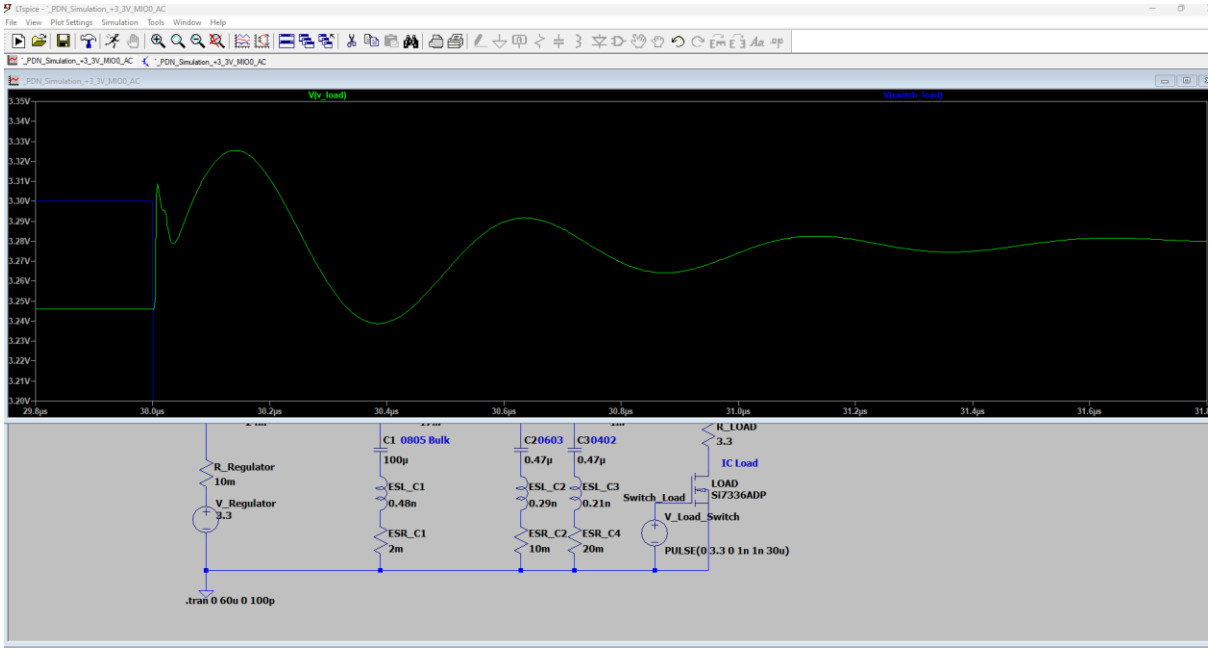
After Load pulse rising edge:

10mV over shoot on rising edge, following by additional resonance that eventually settled to 3.246v (not arriving to 3.3V due to the Ohmic resistance)

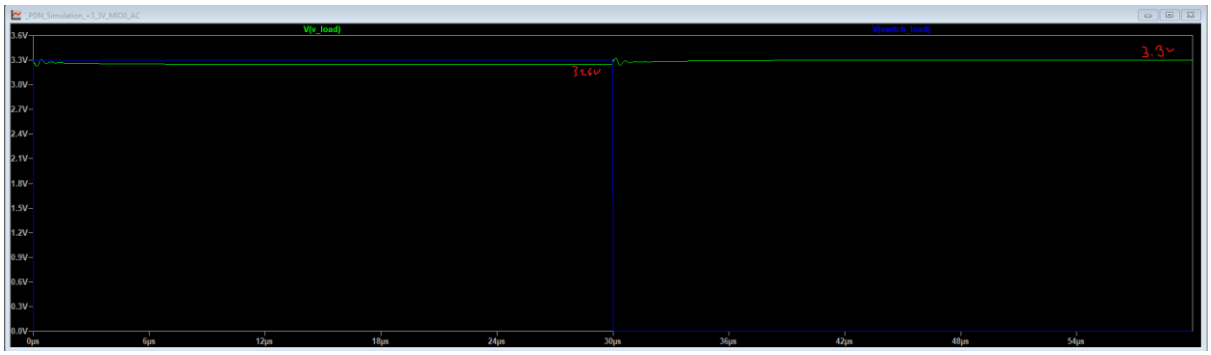


After Load pulse falling edge:

25mV over shoot on falling edge, following by additional resonance that eventually settled to 3.3v (arriving to 3.3V since to no current drawn by the Load)



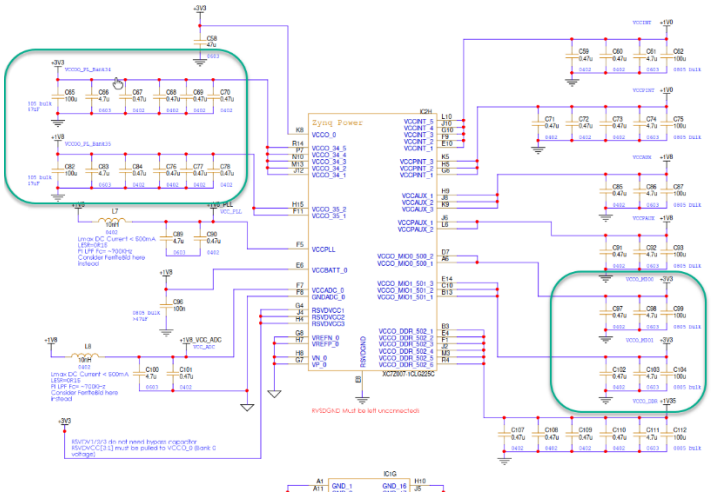
Zoom Out for reference:



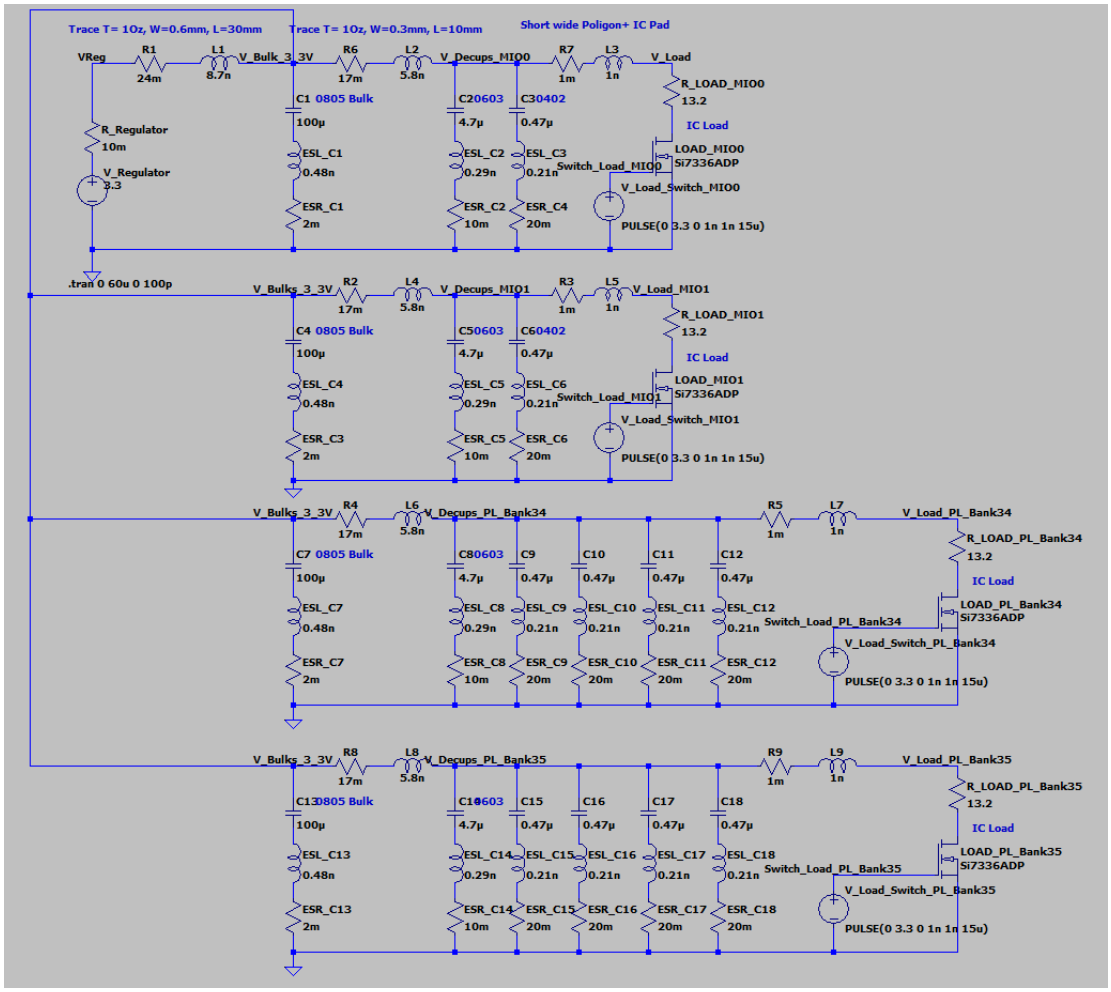
Zynq all 3.3v banks PDN Simulation

Assumption: max current of 1A total, 0.25A per bank consumer. All consumers toggle together.

Schematic view:

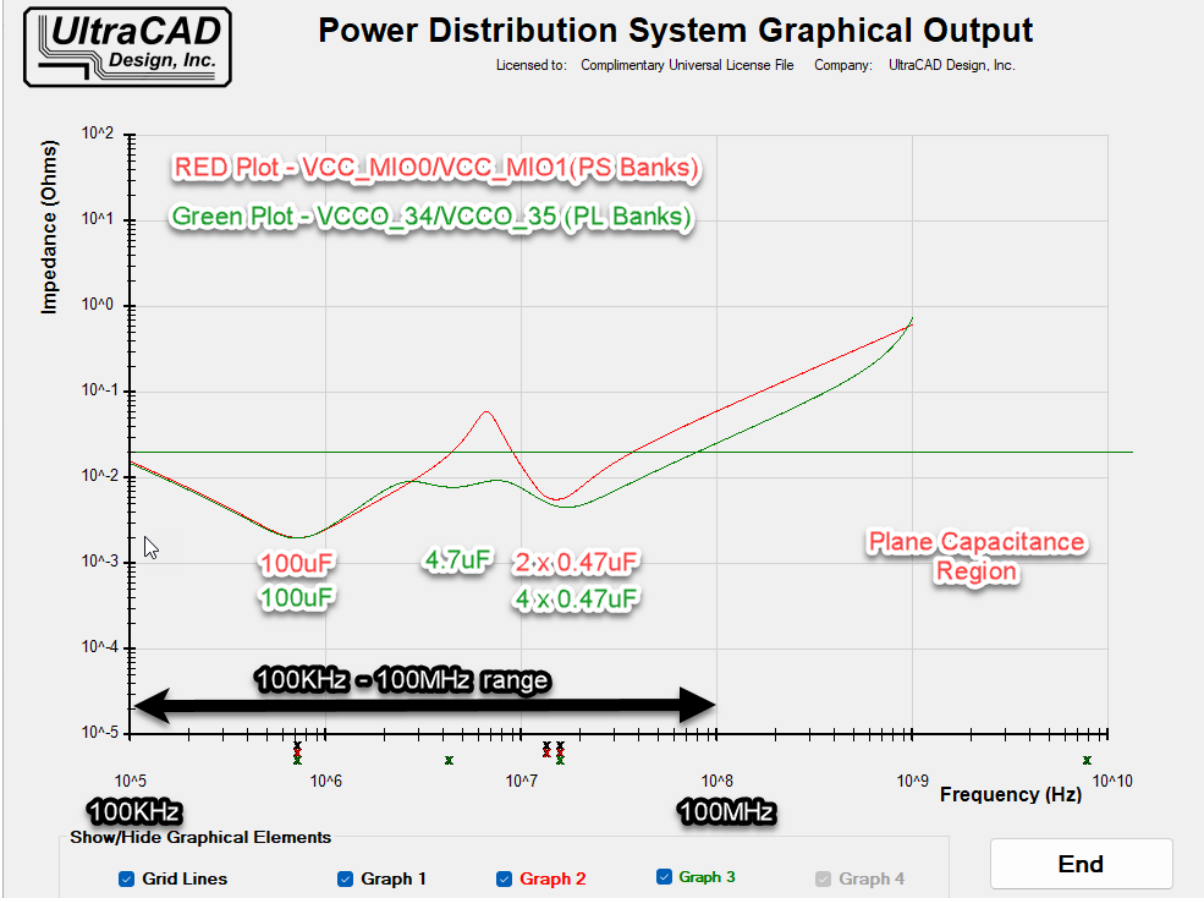


LTspice circuit:



PDN impedance Simulation for all 3.3v Zynq banks according to capacitors C, ESL and ESR:

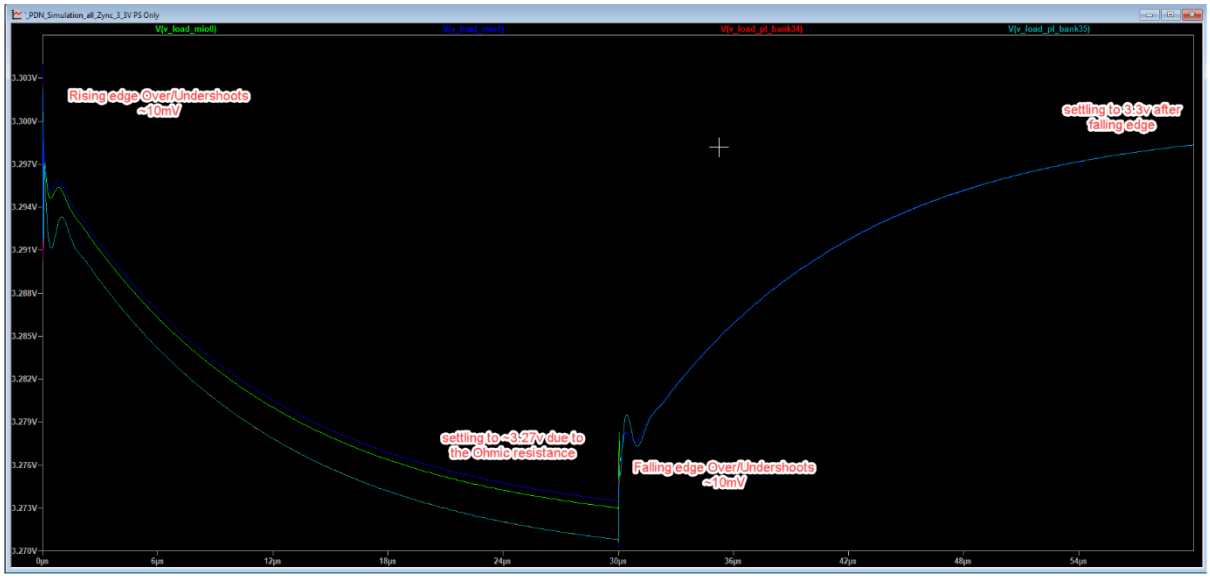
- From Design Guide 933:
  - The impedance of the alternate network must be less than or equal to that of the recommended network across frequencies from **100 KHz to 100 MHz**



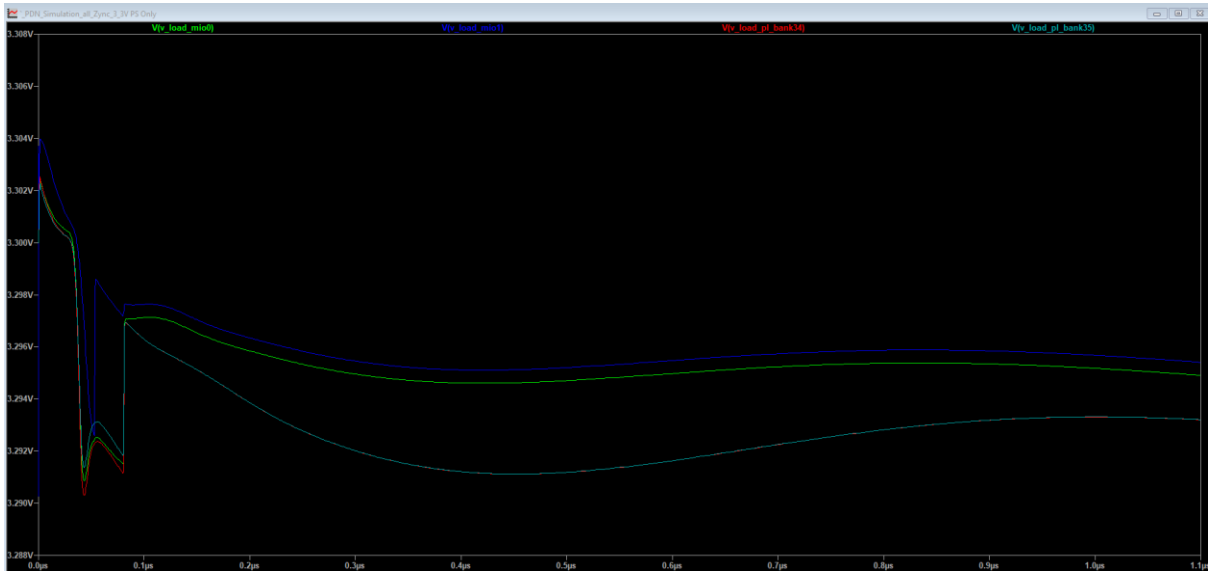
AC+DC Ohmic Results:

AC Overshoot and under shoot max absolute voltage is ~10mV

Ohmic resistance takes ~30mV so final voltage after rising edge settling is ~3.27V



Rising Edge Zoom:



Falling edge zoom: