UCS1502- Microprocessors and Interfacing

CAT-1

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PART-A

1(a) The different type of addressing modes are:

(1.) Intermediate addressing mode:-

In this mode, the operand is specified in the instruction itself. Instructions are longer but the operands are easily identified.

Ex: MOV CL, 12 H

instruction 12 moves imedialely into CL register. CL ← 12H

(2.) Register addresing mode:

In this mode, oprands are mentioned in the registers. Registers may be used as source operands, destination operands or both.

Ex;

MOV AX, BX.

instruction copies the contents of BX to AX.

(3.) Direct addressing mode:

In this mode, the memory location is writen directly in the instruction.

Ex: MOX AX, [5000]

Physical address calculation for above instructions is

10H × DS + 5000H

Eg: if DS = 1000, DS: Offset = 1000 : 5000

Physical address = 10H × 1000 + 5000 = 10000 + 5000 = 15000 H.

(4.) Register indirect addressing mode:

This addressing mode allows data to be addressed at any memory location through an offset address held in any of the following registers. BP, BX, DI and SI

Ex. MOV AX, [BX]

Physical address calculation, = 10H × DS + BX

if DS = 1000, BX = 2000

Physical address = 10H × 1000 + 2000 = 10000 + 2000

= 12000 H

(5.) Indexd addressing mode;

In this mode, offset of the operand is stored in one of the index registers. DS is the default segment for SI, and ES is the default segment for DI.

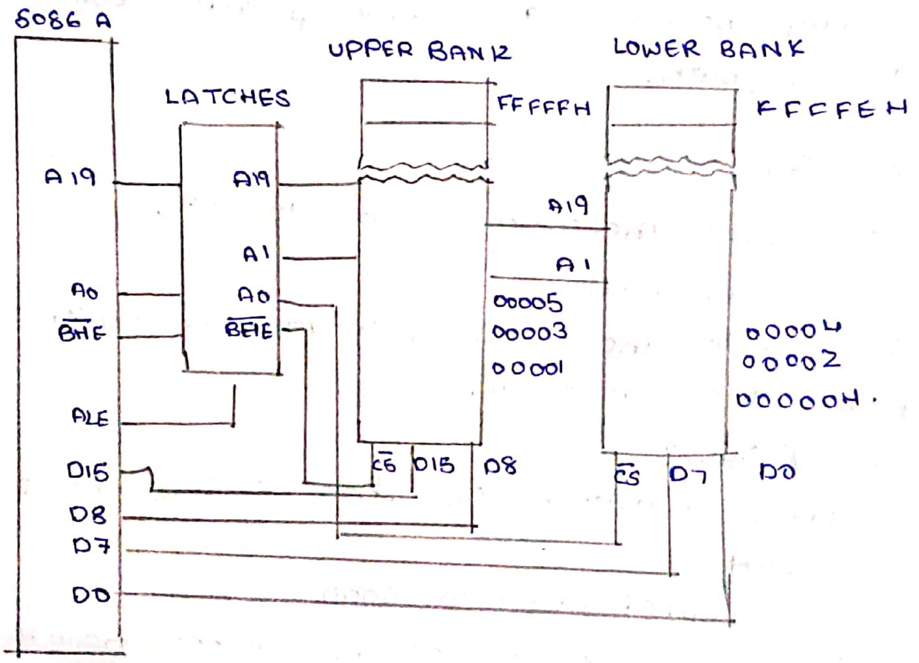
Ex: MOV AX, [SI]

physical address: 10H × DS + SI

22(b) Memory organization of 8086:

To make it possible to read or write a word (16 bits) with one machine cycle, the memory of 8086 is set up as two banks.

- odd bank (512 K)
- Even bank (512k)



Operation.	$\overline{BHE}$	A0	Bus Cycle	Data lines used
R/W word from/to even address	0	0	one	D0 -D15
R/W byte from/to odd address	0	1	one	D8 -D15
R/W byte from/to even address	1	0	one	D0 - D7.
R/words from/to odd address	0	1	First	D8 - D15
	1	0	second	D0 -D7.

(23) Program for subtracting 2 32 bit

```
assume cs: code , ds: data
data segment
 result H dw 0000 H.
  opr AH dw 1123 H
  opr AL dw 2311 H.
  opr BH dw 1012 H.
  opr BL dw 2111 H.
  result dw 0000 H.
data ends
code segment
        org 0100h
        mov ax ,data
        mov ds ,ax
        mov ax, opr AL
        mov ax ,0000 H ;cx
        mox bx ,opr BL
        cmp ax , bx
        jnc here
         mov cx , 0001 H
         ~~mov dx, 1~~
         mov dx , F000 H
         sub dx , bx
         add ax , dx
         mov dx , 0000 H.
 here : mov result L , ax
        mov ax , opr AH
        mov bx , opr BH
        sub ax , cx
        sub ax , bx
        jnc here1
         neg ax
         add dx , 0001 H.
 here1 : mov result H , ax
          mov ah, 4ch
          int 21 h
          code ends
 end start
```