Sri Sivasubramaniya Nadar College of Engineering, Kalavakkam – 603 110

(An Autonomous Institution, Affiliated to Anna University, Chennai)
Department of Information Technology
Continuous Assessment Test – II
Question Paper

Degree & Branch	B.Tech. Information Technology	Semester	IV
Subject Code & Name	**UIT1403 – Microprocessors and Microcontrollers**		
Time: 90 Minutes **Date: 10.05.2022**	**Answer All Questions**	**Maximum: 50 Marks**	

(K1 – Remembering, K2- Understanding, K3- Applying, K4- Analyzing, K5- Evaluating, K6 – Creating)

CO1	Write programs to run on 8086 microprocessor based systems.
CO2	Design the system using memory chips and peripheral chips for microprocessor and Microcontroller.
CO3	Analyse, Specify. Design , write and test assembly language programs.

Part – A (6 × 2 = 12 Marks)

Q. No.	Questions	KL	CO	PI
1	What is the assembler directive statement that used to reserve an array of 100 words in memory but leave the 100 words uninitialized and give it a name TEMP?	K2	CO1	2.1.3
2	Let us consider an assembly statement as INT 10H. What will be the starting and ending addresses for the respective interrupt service routine stored in the interrupt vector table?	K2	CO3	2.1.3
3	What will be the contents of A_0, A_1, and $\overline{CS}$ signals when the output (write) operation is done on Port A (i.e. data bus to Port A) of 8255 PPI.	K2	CO3	2.1.3
4	Determine the mode of operation and the selected counter based on the control word format of 8253/8254 programmable interval timer. D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0 1 0 0 0 X 1 1 1	K2	CO2	2.1.3
5	How many number of vectored priority interrupts are handled by the Intel 8259A Programmable Interrupt Controller when it is connected to the 8086 microprocessor in cascade configuration?	K2	CO2	2.1.3
6	If 8251 USART is programmed in asynchronous mode, how many stop bits the receiver requires?	K2	CO2	2.1.3

Part – B (3 × 6 = 18 Marks)

7	Explain the following assembler directives with an example.
	   a) ASSUME
	   b) SEGMENT
	   c) EQU
		K2	CO2	1.3.1, 1.4.1

8	Briefly describe the conditions which cause the 8086 microprocessor to perform each of the following types of interrupts: Type 0, Type 1, Type 2, Type 3 and Type 4.	K2	CO2	1.3.1, 1.4.1

| 9 | Compare I/O mapped and memory mapped I/O Techniques. | K2 | CO2 | 1.3.1, 1.4.1 |

Part – C (2 × 10 = 20 Marks)

10	**a)** Write a program to initialize 8255 in the configuration given below. • Port A: Output with handshake • Port B: Input with handshake • Port C_L: Output • Port C_U: Input Assume address of the control word register of 8255 as 83H. Also find the control word for the register arrangement of the ports of Intel 8255. (**5 Marks**) **b)** Write a program to blink Port C bit 0 (i.e., D_0) of the 8255. Assume address of the control word register of 8255 is 23H. Use Bit Set/Reset mode. (**5 Marks**)	K3	CO3	1.3.1, 1.4.1, 2.1.3
	OR			
11	**a)** Assume that GATE1 = 1 and CLK1 =1 MHz and the clock count N= 5000. Show the output if 8253/8254 PIT is programmed in mode 0 and mode 2. (**5 Marks**) **b)** Write an ALP to generate a delay of 100 msec using an 8086 system that runs on 10 MHz frequency (Hint: Use procedure in ALP to write a delay routine). (**5 Marks**)	K3	CO3	1.3.1, 1.4.1, 2.1.3
12	Design and explain a peripheral device which handles multiple interrupt requests from external devices.	K3	CO2	3.1.1, 4.1.3, 5.1.1
	OR			
13	Design and explain a peripheral device which translates serial to parallel and parallel to serial data for synchronous mode of data transmission.	K3	CO2	3.1.1, 4.1.3, 5.1.1