Register Number | | | | | | | | | |

Sri Sivasubramaniya Nadar College of Engineering, Kalavakkam – 603 110

(An Autonomous Institution, Affiliated to Anna University, Chennai)

Department of Computer Science and Engineering

Continuous Assessment Test – I

Question Paper

Degree & Branch	B.E. Computer Science and Engineering				**Semester**	V
Subject Code & Name	UCS1502 -Microprocessors and Interfacing				**Regulation: 2018**	
Academic Year	2020-2021	**Batch**	2018-2022	**Date**	**01.09.2020**	**10:30am – 12:00noon**
Time: 90 Minutes	**Answer All Questions**				**Maximum: 50 Marks**	

Part – A Answer all the questions (10×2 = 20 Marks)
(MCQ type –Randomly post 10 questions to the student)

K3	1.What is the physical address of the operand in the following instruction? MOV AX, [BX+SI+5000], if DS = 1000, BX= 2000 and SI = 3000 a) 20000 b) 1A000 c) 10000 d) 5000 Ans: b) 1A000	CO1
K3	2.If AL=B3, what will be the content of AL after the execution of following instructions? MOV CL, 04 ROR AL, CL a) B3 b) 3B c) 33 d) BB Ans: b) 3B	CO1
K3	3. If AL=95, What will be the content of AL and carry flag after the execution of following instructions? MOV CL, 01 SAR AL, CL a) 4A, 1 b) 4A, 0 c) CA, 0 d) CA, 1 Ans: d) CA, 1	CO1
K3	4.During the execution of instruction MOV AL, [0001], the status of A0 and data lines used are a) 1, D8-D15 b) 0, D8-D15 c) 1, D0-D7	CO2

	d) 0, D0-D7 e) Ans: a) 1, D8-D15	
K3	5. What is the physical address of the operand in the following instruction? MOV AX, [BX], if DS=1000, BX=2000, [2000] =3000 a) 15000 b) 12000 c) 10000 d) 2000 Ans: b) 12000	CO1
K3	6.If CX=FFFE, BX=FFFF, what will be the status of CF,ZF and SF after the execution of the instruction CMP CX, BX? a) 1, 0, 1 b) 0, 1, 0 c) 0, 0, 0 d) None of these Ans: a) 1,0,1	CO1
K3	7. If AX=0FFC and flag register content is FF0F, the content of flag register after the execution of SAHF will be a) 0FFF b) FFFC c) FCFF d) No change Ans d) No change	CO1
K3	8. What are the invalid instructions in the list 1. MOV AX, AL 2. MOV AL, BL 3. ADD [5000], [3000] 4. PUSH AL a) 2 and 4 b) 1, 3 and 4 c) 3 d) 1 and 3 Ans : b) 1, 3 and 4	CO1
K3	9.Assume SP=1236, AX=24B6, DI=85C2 and DX=5F93. After the execution of following instructions, what will be the contents of SP and stack top PUSH AX PUSH DI PUSH DX	CO1

	a) 123C, 5F b) 1230, 93 c) 123B,93 d) 1231, 5F Ans: b) 1230, 93	
K3	10. If SS= 3500H, what is the upper range of stack segment a) 35000 b) 35FFF c) 44FFE d) 44FFF Ans d) 44FFF	CO1
K2	11. Why do we need memory segmentation in 8086? a) Because 20-bit addresses are too big to fit in 16-bit registers b) Because we have segment registers c) Because segmenting will increase storage size d) Because 8086 is capable of accessing 2^{20} memory locations Ans a) Because 20-bit addresses are too big to fit in 16-bit registers	CO1
K1	12. What is the instruction used for loading lower byte of flag registers into AH? a) LAHF b) LAFH c) LDHF d) LOHF Ans a) LAHF	CO1
K2	13.Please select the flags that are affected on executing DAA instruction. a) Auxiliary carry flag b) Parity flag c) Carry Flag d) Overflow Flag Ans a) Auxiliary carry flag, b) Parity flag and c) Carry Flag	CO1
K1	14. Which of the following assembler directive is used for reserving one memory location for 8-bit signed displacement in jump instructions? a) Far b) Near c) Long d) Short Ans d) Short	CO1
K2	15. What is the role of QS0 and QS1 signal in 8086 maximum mode of operation? a) It is used by the coprocessor to keep track of the host processor's queue status b) It is used by host processor to keep track of its processing status c) It is used by host processor to keep track of its queue status d) It is used by the coprocessor to keep track its queue status Ans a) It is used by the coprocessor to keep track of the host processor's queue status	CO2
K2	16. How is the TEST pin of 8086 processor examined? a) By executing 'TEST' instruction b) By executing 'ESC' instruction	CO1

	c) By examining the 'WAIT' signal d) By executing 'WAIT' instruction Ans d) By executing 'WAIT' instruction	
K2	17. During the maximum mode of operation, when the status signal S2 is active high and both S1 and S0 are active low, what is being done? a) Data is read from memory b) Data is written to memory c) Code is accessed from memory d) Data is read from input port Ans c) Code is accessed from memory	CO2
K2	18.What does bus interface unit of 8086 contain? a) Instruction queue b) Address summer c) Instruction Decoder d) Flag Register Ans a) Instruction queue and b) Address summer	CO1
K2	19. Which of the following statements are correct? a) Instruction pointer is under the direct control of programmer b) Instruction pointer is not under the direct control of programmer c) Instruction pointer is always incremented by two d) Instruction pointer points to the next instruction to be executed by the processor Ans b) Instruction pointer is not under the direct control of programmer and d) Instruction pointer points to the next instruction to be executed by the processor	CO1
K1	20. Select the control flags of 8086. a) Carry Flag b) Direction Flag c) Sign Flag d) Trap Flag Ans b) Direction Flag and d) Trap Flag	CO1

Part – B Answer all the questions (2×5 = 10 Marks)

K2	1. Explain the memory organization of 8086 microprocessor.	CO1
K3	2. Write an 8086 ALP snippet to set the trap flag in flag register. Ans: PUSHF POP AX OR AX,0100H PUSH AX POPF	CO1

Part – C Answer any TWO questions (2×10 = 20 Marks)

K1	3. Draw and explain the architecture of 8086.	CO1
K3	4. Write an 8086 MASM ALP to perform 32-bit subtraction along with its algorithm. (Input: two 32-bit numbers; Output: Difference in absolute form and sign indicator; All inputs and outputs should be in memory locations)	CO1
K3	5. Write an 8086 MASM ALP to create an array that shows the count of one's present in each element of an array of 8-bit numbers. (Input: set of n 8-bit numbers; Output: set of n 8-bit numbers; All inputs and outputs should be in memory locations)	CO1

Prepared By	Reviewed By	Approved By
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