UCS1502 - MICROPROCESSORS AND INTERFACING

PPI – 8255

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Learning Objective

- To understand the architecture of 8255
- To understand 8255 operation

Overview

- Pin diagram of 8255
- Architecture
- Control word
- Modes of operation

Introduction

- PPI – Programmable Peripheral Interface
- It is an I/O port chip used for interfacing I/O devices with microprocessor
- Very commonly used peripheral chip
- Knowledge of 8255 essential for students in the Microprocessors lab for Interfacing experiments

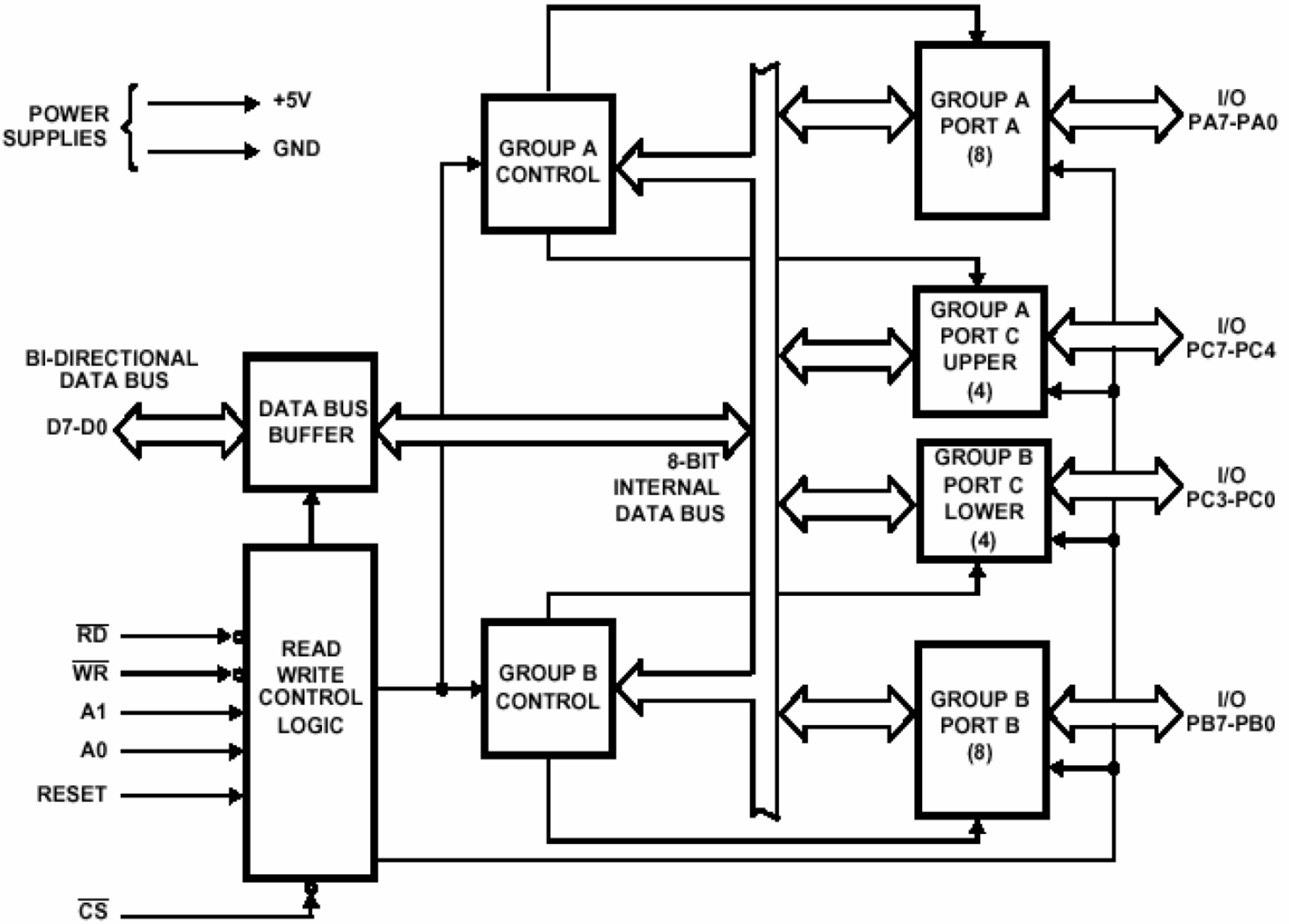
8255 Ports

- 8255 PPI has three 8-bit ports.
  - Port A (PA)
  - Port B (PB)
  - Port C (PC)

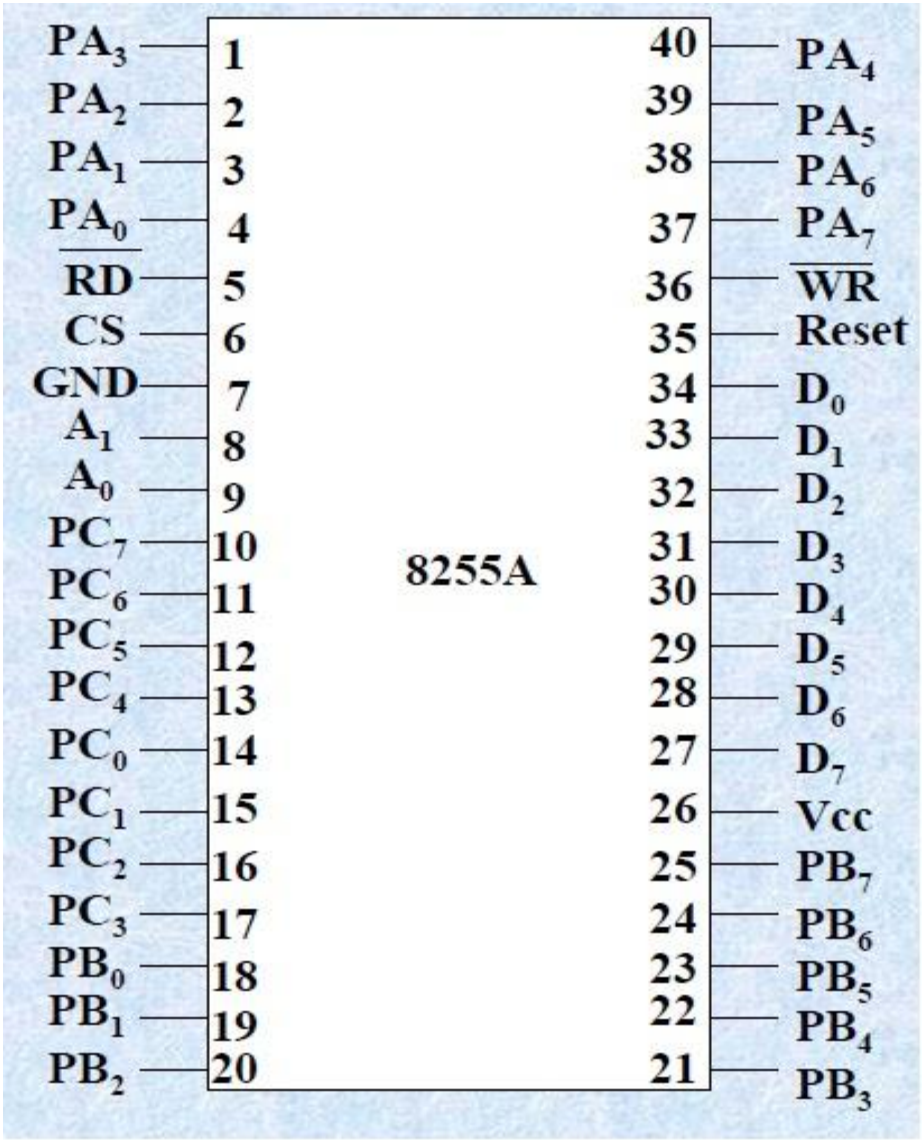
A1	A0	Selected port
0	0	Port A
0	1	Port B
1	0	Port C
1	1	Control port

- Port C composed of two independent 4-bit ports: PC7-4 (PC Upper) and PC3-0 (PC Lower)

- Port A, Port B, Port C and Control port will have the addresses as 7CH, 7DH, 7EH, and 7FH respectively.


POWER SUPPLIES
+5V
GND
GROUP A CONTROL
GROUP A PORT A (8)
I/O PA7-PA0
GROUP A PORT C UPPER (4)
I/O PC7-PC4
BI-DIRECTIONAL DATA BUS
D7-D0
DATA BUS BUFFER
8-BIT INTERNAL DATA BUS
GROUP B PORT C LOWER (4)
I/O PC3-PC0
RD
WR
A1
A0
RESET
READ WRITE CONTROL LOGIC
GROUP B CONTROL
GROUP B PORT B (8)
I/O PB7-PB0
CS

Pin Diagram


PA3 1
PA2 2
PA1 3
PA0 4
RD 5
CS 6
GND 7
A1 8
A0 9
PC7 10
PC6 11
PC5 12
PC4 13
PC0 14
PC1 15
PC2 16
PC3 17
PB0 18
PB1 19
PB2 20
8255A
40 PA4
39 PA5
38 PA6
37 PA7
36 WR
35 Reset
34 D0
33 D1
32 D2
31 D3
30 D4
29 D5
28 D6
27 D7
26 Vcc
25 PB7
24 PB6
23 PB5
22 PB4
21 PB3

Pin Description

- **PA7-PA0** : These are eight port A lines that acts as either latched output or buffered input lines depending upon the control word loaded into the control word register.

- **PC7-PC4** **:** Upper nibble of port C lines. They may act as either output latches or input buffers lines. *This port also can be used for generation of handshake lines in mode 1 or mode 2.*
- **PC3-PC0** : These are the lower port C lines, other details are the same as PC7-PC4 lines.

- **PB0-PB7** : These are the eight port B lines which are used as latched output lines or buffered input lines in the same way as port A.

Pin Description

- **RD** **:** This is the input line driven by the microprocessor and should be low to indicate read operation to 8255.
- **WR** **:** This is an input line driven by the microprocessor. A low on this line indicates write operation.
- **CS** **:** This is a chip select line. If this line goes low, it ables the 8255 to respond to RD and WR signals, otherwise RD and WR signal are neglected.
- **A1-A0** : These are the address input lines and are driven by the microprocessor.
- **RESET** : The 8255 is placed into its reset state if this input line is a logical 1. All peripheral ports are set to the input mode.

$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	A_1	A_0	Input (Read) cycle
0	1	0	0	0	Port A to Data bus
0	1	0	0	1	Port B to Data bus
0	1	0	1	0	Port C to Data bus
0	1	0	1	1	CWR to Data bus

$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	A_1	A_0	Output (Write) cycle
1	0	0	0	0	Data bus to Port A
1	0	0	0	1	Data bus to Port B
1	0	0	1	0	Data bus to Port C
1	0	0	1	1	Data bus to CWR

$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	A_1	A_0	Function
X	X	1	X	X	Data bus tristated
1	1	0	X	X	Data bus tristated

Control Word Register

Programming 8255

- 8255 has three operation modes: mode 0, mode 1, and mode 2

Mode 0 - Simple Input or Output mode

Mode 1 - Input or Output with Handshake mode

Mode 2 - Bidirectional Data Transfer mode

Mode 0 - Simple Input or Output

- In this mode, ports A, B are used as two simple 8-bit I/O ports & port C as two independent 4-bit ports.
- Each port can be programmed to function as simply an input port or an output port.
- The input/output features in Mode 0 are as follows.

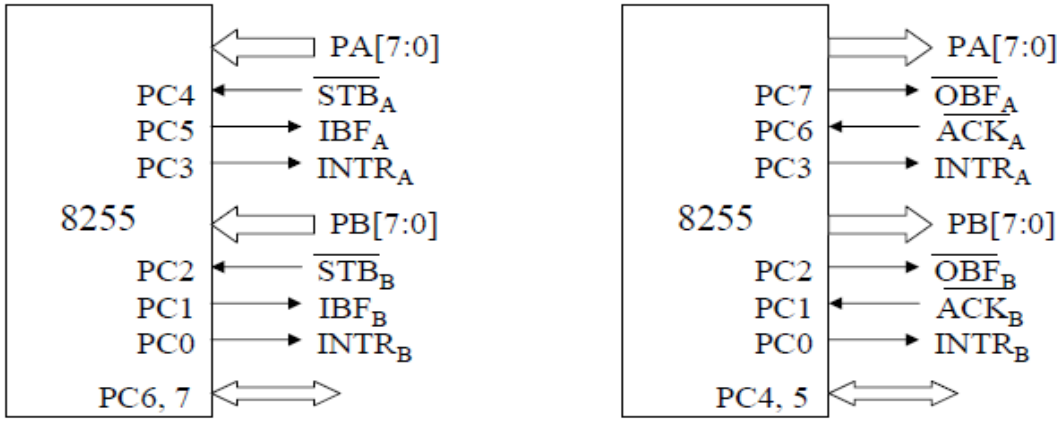
  1. Outputs are latched.
  2. Inputs are not latched.
  3. Ports don't have handshake or interrupt capability.

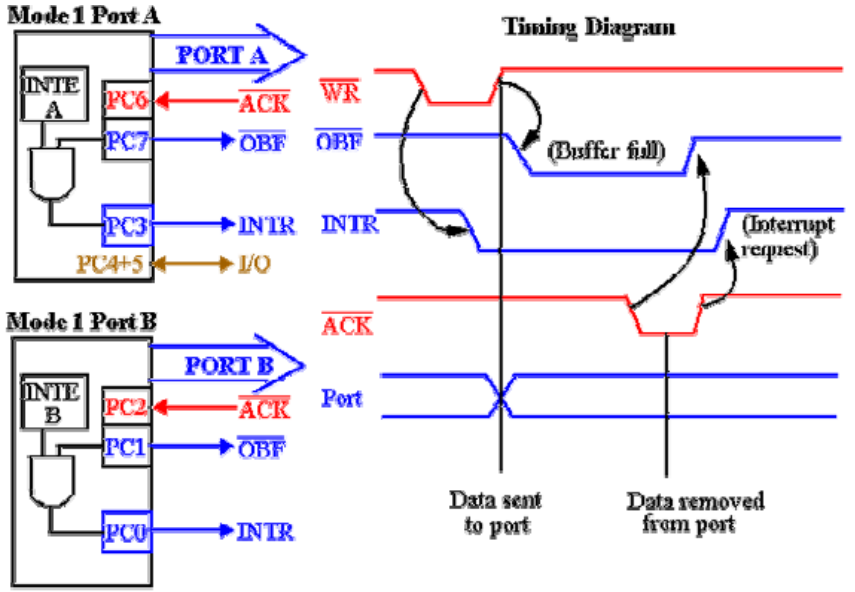
Mode 1 - Input or Output with Handshake

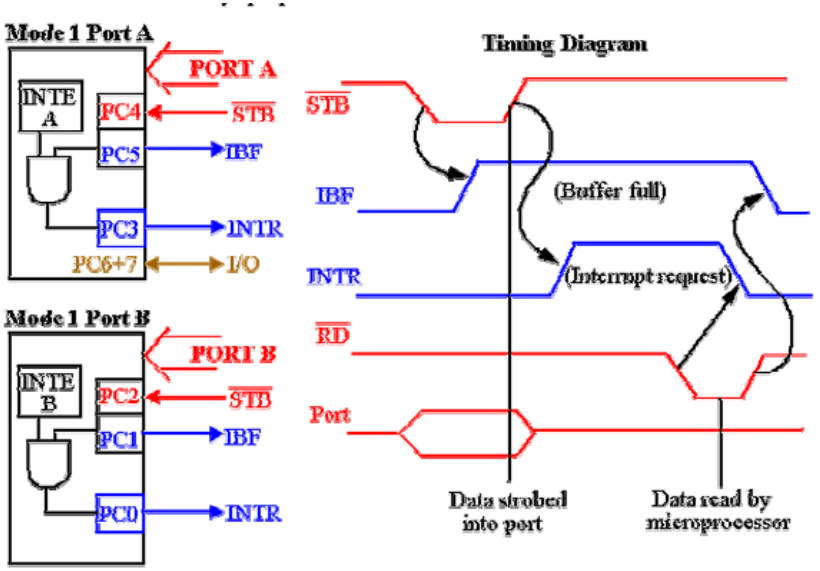
- In this mode, handshake signals are exchanged between the MPU and peripherals prior to data transfer.
- The features of the mode include the following:

1. Two ports (A and B) function as 8-bit I/O ports.
   They can be configured as either as input or output ports.
2. Each port uses three lines from port C as handshake signals.
   The remaining two lines of Port C can be used for simple I/O operations.
3. Input and Output data are latched.
4. Interrupt logic is supported.

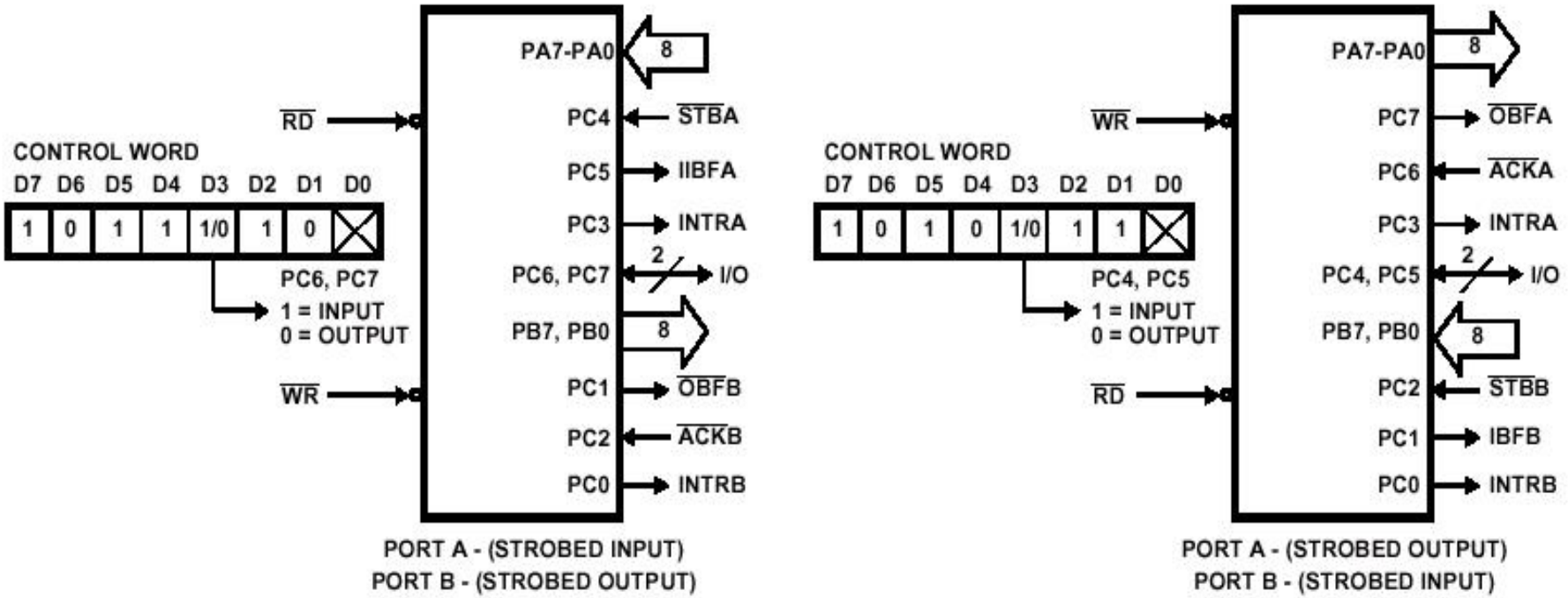
Mode 1 - Input or Output with Handshake







Mode 1 - Input or Output with Handshake



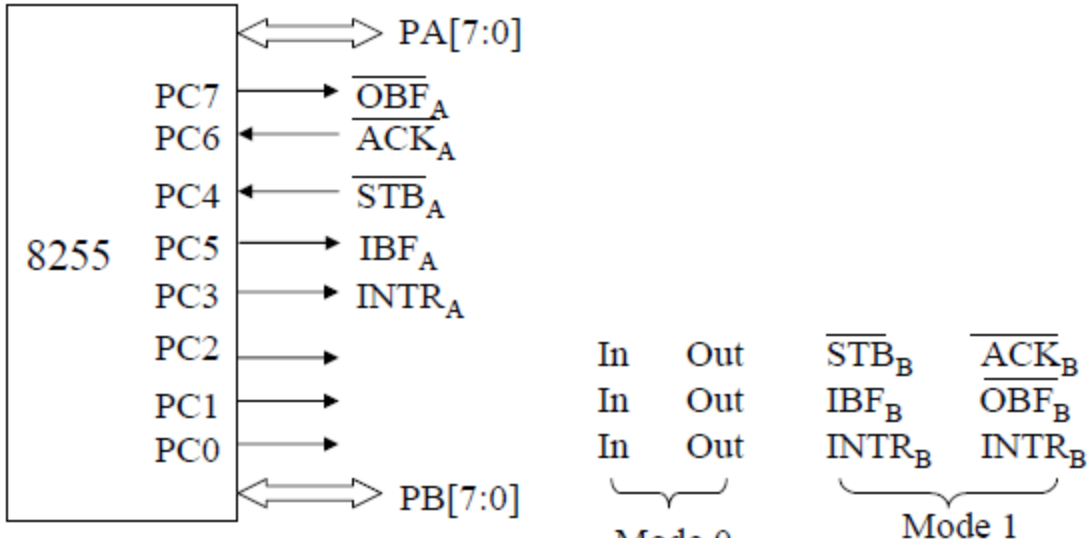
Combinations of Mode 1: Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

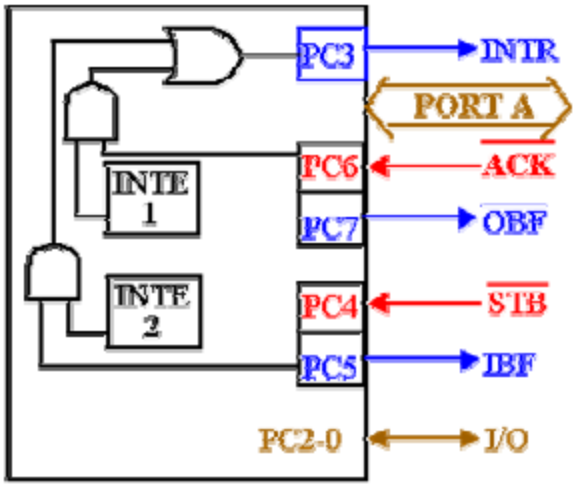
FIGURE 10. COMBINATIONS OF MODE 1

Mode 2 - Bidirectional Data Transfer

- This mode is used primarily in applications such as data transfer between two computers.
- In this mode, Port A can be configured as the bidirectional port, Port B either in Mode 0 or Mode 1.
- Port A uses five signals from Port C as handshake signals for data transfer.
- The remaining three signals from Port C can be used either as simple I/O or as handshake for port B.

Mode 2 - Bidirectional Data Transfer





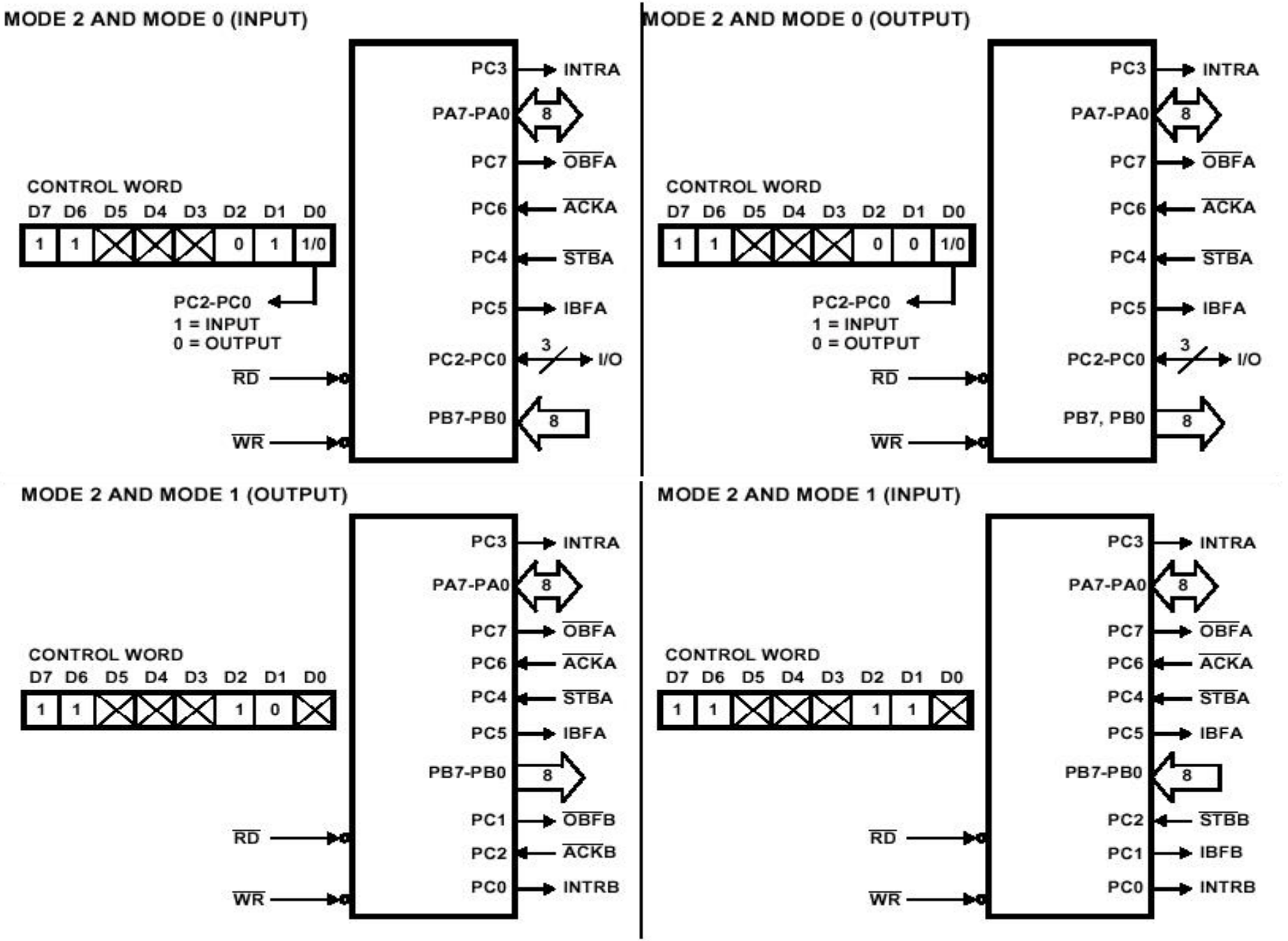


FIGURE 14. MODE 2 COMBINATIONS

8255 Modes Summary

- Port A can work in Mode 0, Mode 1, or Mode 2
- Port B can work in Mode 0, or Mode 1
- Port C can work in Mode 0 only, if at all

- Port A, Port B and Port C can work in Mode 0
- Port A and Port B can work in Mode 1
- Only Port A can work in Mode 2

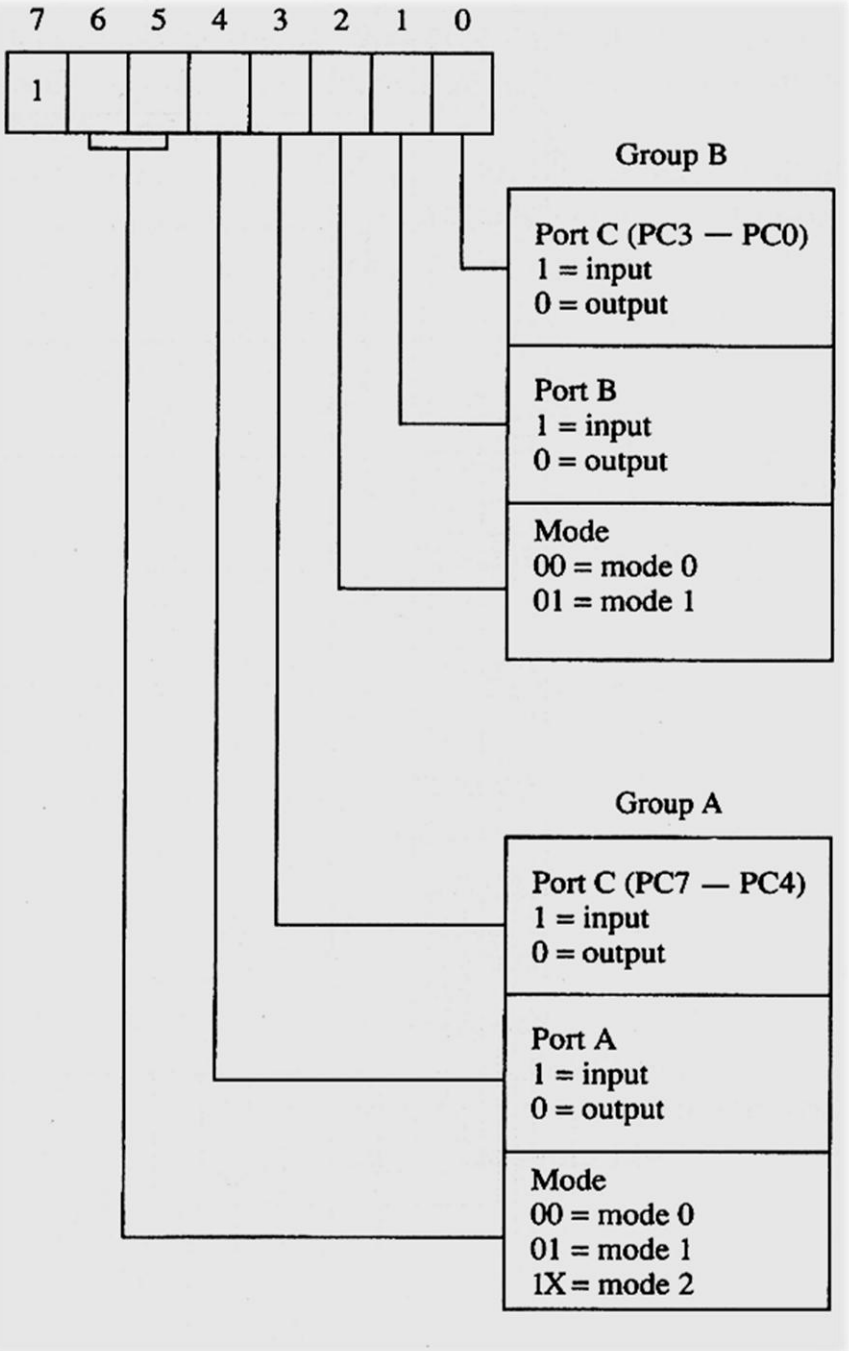
8255 Control Words

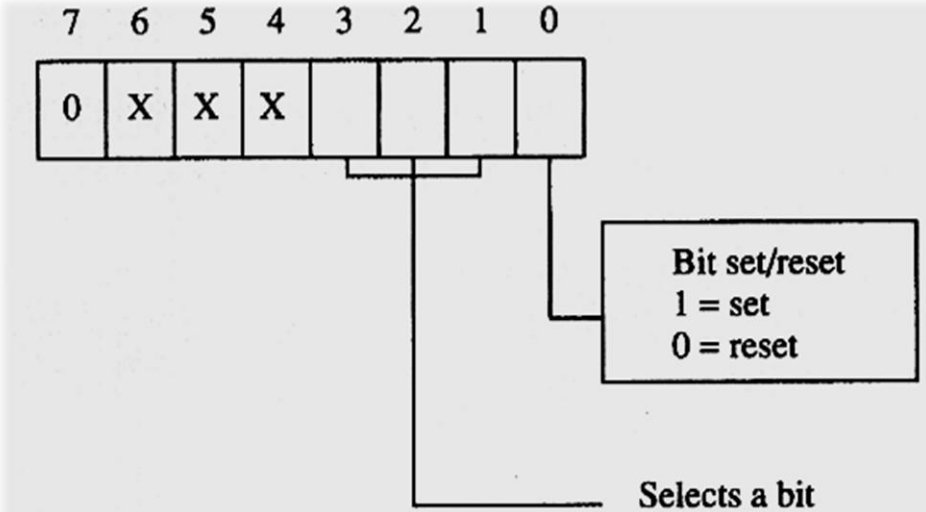
- There are 2 control words in 8255.
    1. Mode Definition (MD) Control word and
    2. Bit Set / Reset (BSR) Control Word

- MD control word configures the ports of 8255 as input or output in Mode 0, 1, or 2.

- PCBSR control word is used to set to 1 or reset to 0 any one selected bit of Port C

8255 Control words





A_1	A_0	*Function*
0	0	Port A
0	1	Port B
1	0	Port C
1	1	Command Register

Summary

- Pin diagram of 8255
- Architecture
- Control word
- Modes of operation

Check your understanding

- What are the different modes of operation of PPI?

Thank you