Sri Sivasubramaniya Nadar College of Engineering, Kalavakkam – 603 110

(An Autonomous Institution, Affiliated to Anna University, Chennai)

Department of Information Technology

Continuous Assessment Test – 3

Question Paper

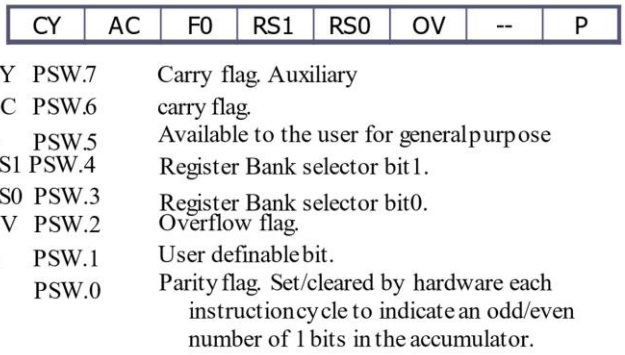
Degree & Branch	B.Tech. Information Technology	**Semester**	IV
Subject Code & Name	UIT1403 - MICROPROCESSORS AND MICROCONTROLLERS		
Time: 90 Minutes **Date: 06-06-2022**	**Answer Key**	**Maximum: 50 Marks**	

Part – A (6 × 2 = 12 Marks)

<table>
<tr><th>Q.no</th><th>Questions</th></tr>
<tr><td>1</td><td>Name four major differences between a Microprocessor and Microcontroller.
<table>
<tr><td>Microprocessor</td><td>Microcontroller</td></tr>
<tr><td>Microprocessor assimilates the function of a central processing unit (CPU) on to a single integrated circuit (IC).</td><td>Microcontroller can be considered as a small computer which has a processor and some other components to make it a computer.</td></tr>
<tr><td>Computational capacity of microprocessor is very high. Hence can perform complex tasks.</td><td>Less computational capacity when compared to microprocessors. Usually used for simpler tasks.</td></tr>
<tr><td>The clock frequency is very high usually in the order of Giga Hertz.</td><td>Clock frequency is less usually in the order of Mega Hertz.</td></tr>
<tr><td>Have few bit manipulation instructions</td><td>Bit manipulation is powerful and widely used feature in microcontrollers. They have numerous bit manipulation instructions.</td></tr>
</table></td></tr>
<tr><td>2</td><td>Find the time taken to execute an ADD A, R1 one cycle Instruction if crystal frequency is 16 MHZ.

Number of Cycles = C = 1
Time to Execute the Instruction = (C * 12) / Cyrstal Frequency = 0.75 Microseconds.</td></tr>
<tr><td>3</td><td>Write an 8051 program to find 2’s complement of a Number.</td></tr>
</table>

	MOV A, #02H
	CPL A
	ADD A, #1

4	Name the 8051 Registers associated with Timer. TL0, TL1, TH0, TH1, TMOD, TCON 8 Bit Registers
5	Draw the diagram of Processor Status Word in 8051.  **RS1 RS0 RegisterBank Address** 0 0 0 00H – 07H 0 1 1 08H – 0FH 1 0 2 10H – 17H 1 1 3 18H – 1FH
6	Illustrate the DJNZ Instruction in 8051. DJNZ instruction (decrement and jump if not zero) is for loop control. MOV R7, #10 LOOP: (begin loop) (end loop) DJNZ R7, LOOP (continue)

Part – B (3 × 6 = 18 Marks)

7	Write an 8051 program to subtract (A – B) where A = EEEEH, B = FFFFH
	
	CLR C
	MOV DPTR, #8500H
	MOV R0, #00H
	MOV R1, #EEH

	MOV R2, #EEH
	MOV R3, #FFH
	MOV R4, #FFFH
	MOV A, R1
	SUBB A, R3
	MOV @DPTR, A
	INR DPTR
	MOV A, R2
	SUBB A, R4
	MOV @DPTR, A
	JNC L1
	INR R0
	L1: INR DPTR
	MOV A, R0
	MOV @DPTR, A
	L2: SJMP L2

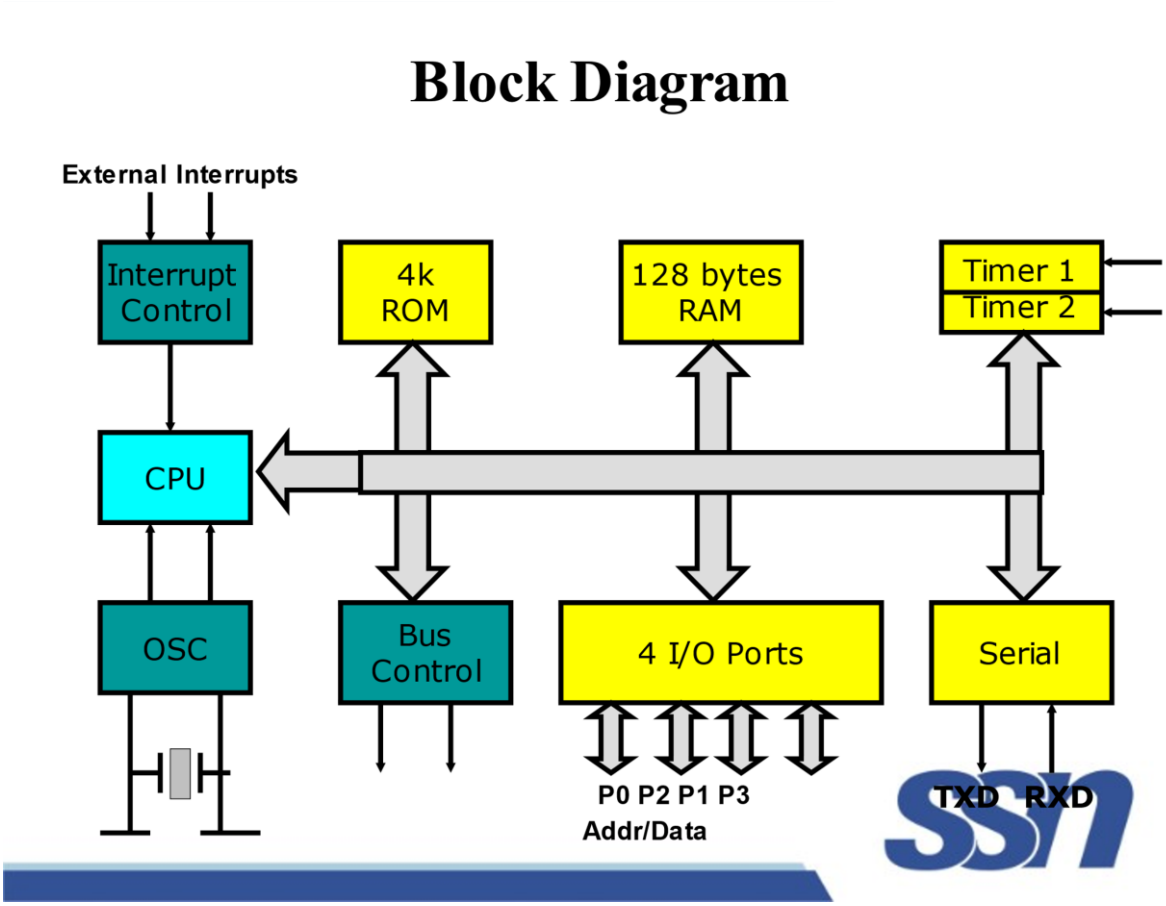
8	Explain about any 3 Bit addressable special function register other than Ports. Register: TCON, SCON, B , A , PSW, IP, IE Explain above reg in detail.
9	Explain about the 8051 Signals. RESET, PSEN, ALE, EA, XTAL1, INT0 **IMPORTANT PINS** • **PSEN** (out): Program Store Enable, the read signal for external program memory (active low). • **ALE** (out): Address Latch Enable, to latch address outputs at Port0 and Port2 • **EA** (in): External Access Enable, active low to access external program memory locations 0 to 4K • **RXD,TXD**: UART pins for serial I/O on Port 3 • **XTAL1** & **XTAL2**: Crystal inputs for internal oscillator.

Pins of 8051

- RST（pin 9）：reset
  - input pin and active high （normally low）.
    - The high pulse must be high at least 2 machine cycles.
  - power-on reset.
    - Upon applying a high pulse to RST, the microcontroller will reset and all values in registers will be lost.
    - Reset values of some 8051 registers
  - power-on reset circuit

INT0 – External Interrupt 0.

Part – C (2 × 10 = 20 Marks)

10	Explain the architecture of 8051 with a neat diagram  Diagram: 5 Marks Key features : 5 Marks	
	Or	

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Discuss on different addressing modes of 8051 with suitable Examples.

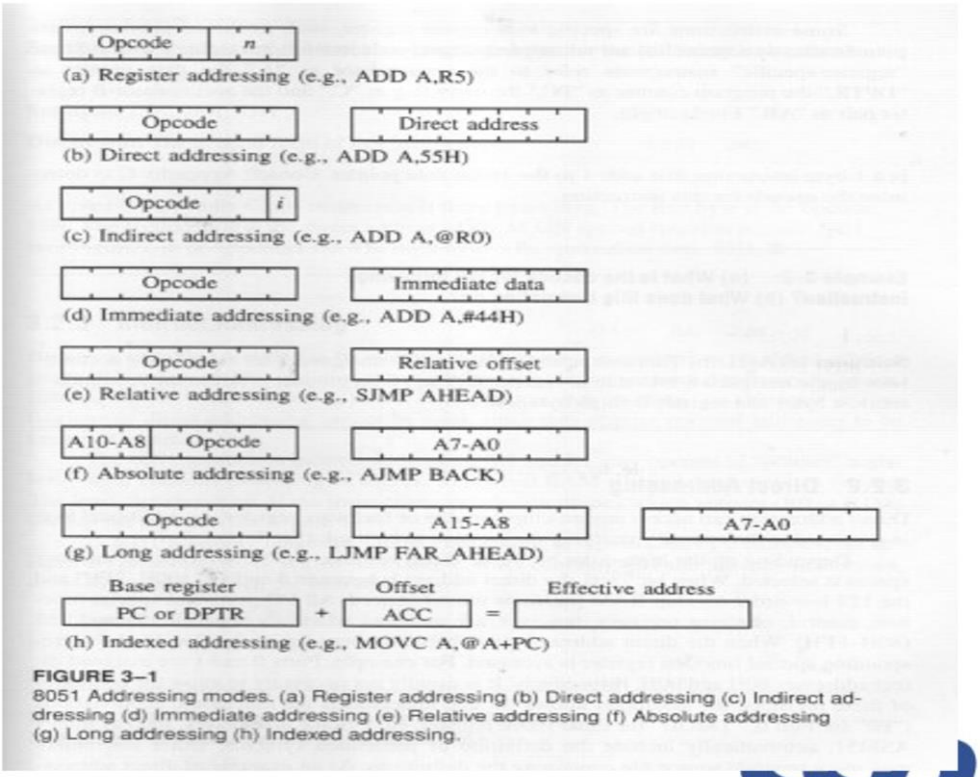

FIGURE 3–1
8051 Addressing modes. (a) Register addressing (b) Direct addressing (c) Indirect addressing (d) Immediate addressing (e) Relative addressing (f) Absolute addressing (g) Long addressing (h) Indexed addressing.

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Explain about the following Instructions
SJMP, AJMP, LJMP, CALL, CJNE

Marks: 5 * 2 = 10 Marks

- SJMP instruction specifies the destination address as a relative offset
- Two bytes long
- The jump distance is limited to -128 to +127 bytes relative to the address following the SJMP
- LJMP instruction specifies the destination address as a 16-bit constant
- Three bytes long
- AJMP instruction specifies the destination address as an 11-bit constant
- Two bytes long
- Destination must be within the same 2K block as the instruction following the AJMP
- Since there is 64K of code memory space. there are 32 such blocks, each beginning at a 2K address boundary
- Programmer specifies the destination address as a label or as a 16-bit constant.
- If the format required by the instruction will not support the distance to the specified destination address, a "destination out of range" message is given.

Subroutines and Interrupts

- Two variations of the CALL instruction: ACALL and LCALL, using absolute and long addressing, respectively.
- Generic CALL mnemonic may be used with Intel's assembler
- Either instruction pushes the content of the program counter on the stack and loads the program counter with the address specified in the instruction
- PC will contain the address of the instruction *following* the CALL instruction when it gets pushed on the stack
- PC is pushed on the stack low-byte first, high-byte second.
- LCALL and ACALL instructions have the same restrictions on the destination address as the LJMP and AJMP instructions just discussed.

- The CJNE instruction (compare and jump if not equal) is also used for loop control. Two bytes are specified in the operand field of the instruction, and the jump is executed only if the two bytes are not equal.

```
        CJNE A, #03H, SKIP
        SJMP TERMINATE
SKIP:   (continue)
```

Or

13 Explain about Internal and External Memory Organization of 8051 Microcontroller.

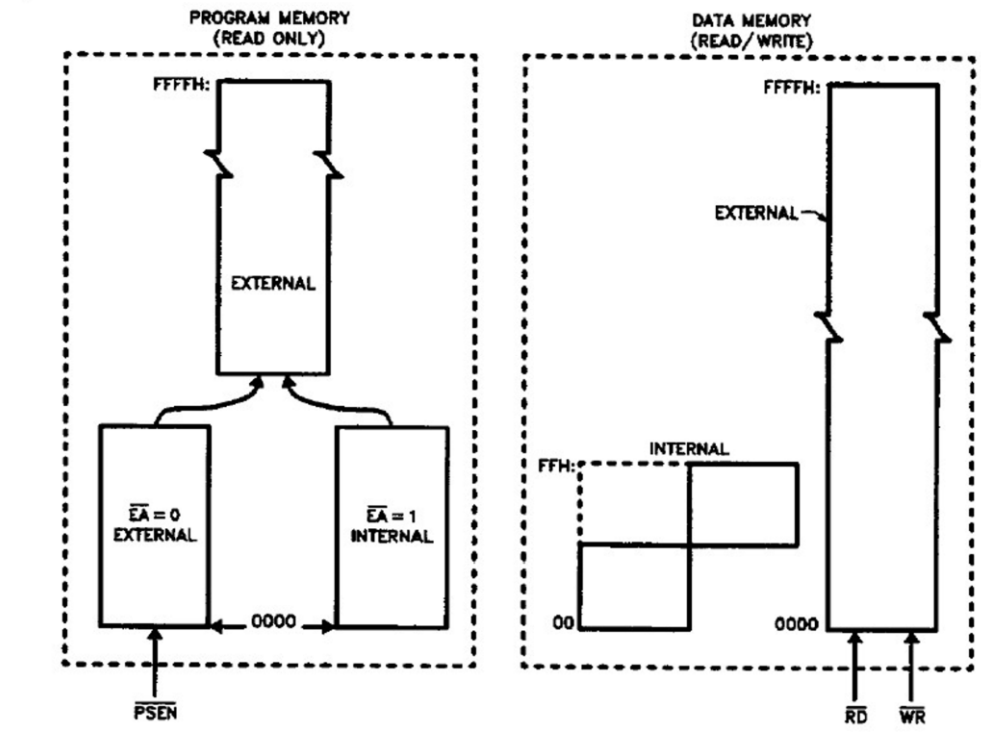

Figure 2. MCS®-51 Memory Structure

8051 memory-register map