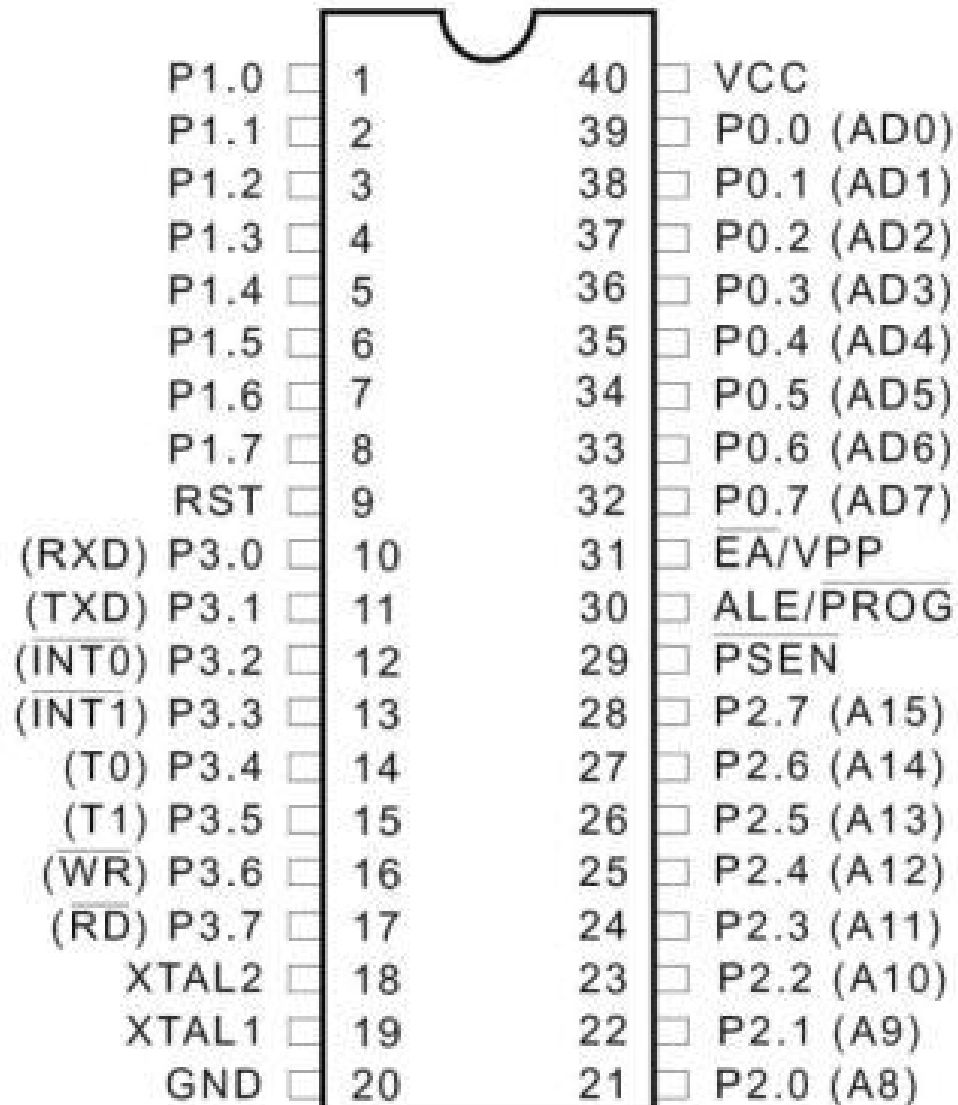


Pin Diagram of the 8051

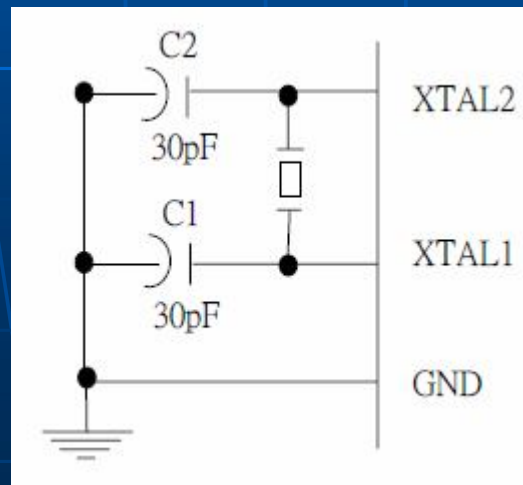
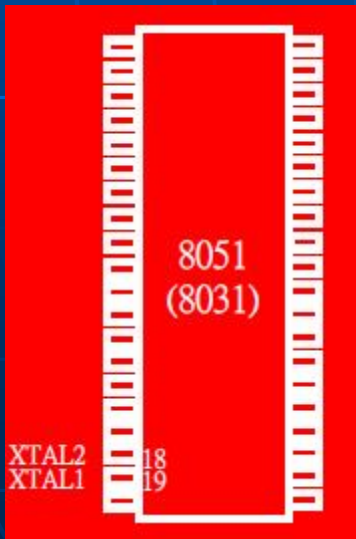


The diagram shows the pin configuration of the 8051 microcontroller. The chip is represented by a rectangle with a notch at the top. Pins are numbered 1 to 40. The functions for each pin are listed on either side of the chip.

P1.0	1	40	VCC
P1.1	2	39	P0.0 (AD0)
P1.2	3	38	P0.1 (AD1)
P1.3	4	37	P0.2 (AD2)
P1.4	5	36	P0.3 (AD3)
P1.5	6	35	P0.4 (AD4)
P1.6	7	34	P0.5 (AD5)
P1.7	8	33	P0.6 (AD6)
RST	9	32	P0.7 (AD7)
(RXD) P3.0	10	31	EA/VPP
(TXD) P3.1	11	30	ALE/PROG
(INT0) P3.2	12	29	PSEN
(INT1) P3.3	13	28	P2.7 (A15)
(T0) P3.4	14	27	P2.6 (A14)
(T1) P3.5	15	26	P2.5 (A13)
(WR) P3.6	16	25	P2.4 (A12)
(RD) P3.7	17	24	P2.3 (A11)
XTAL2	18	23	P2.2 (A10)
XTAL1	19	22	P2.1 (A9)
GND	20	21	P2.0 (A8)

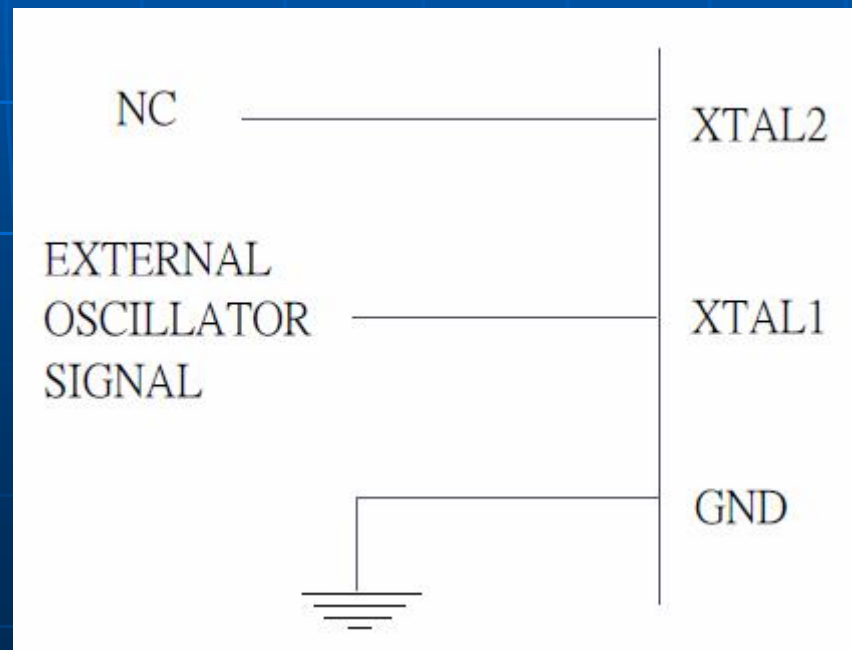
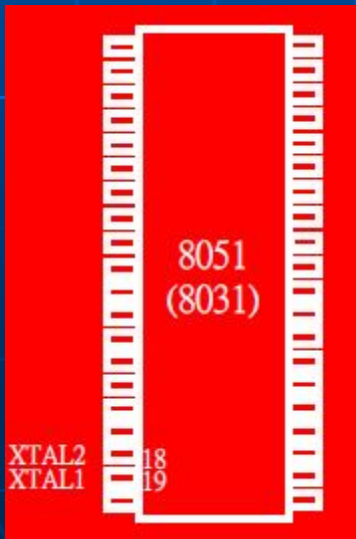
XTAL1 and XTAL2

- The 8051 has an on-chip oscillator but requires an external clock to run it
 - A quartz crystal oscillator is connected to inputs XTAL1 (pin19) and XTAL2 (pin18)
 - The quartz crystal oscillator also needs two capacitors of 30 pF value



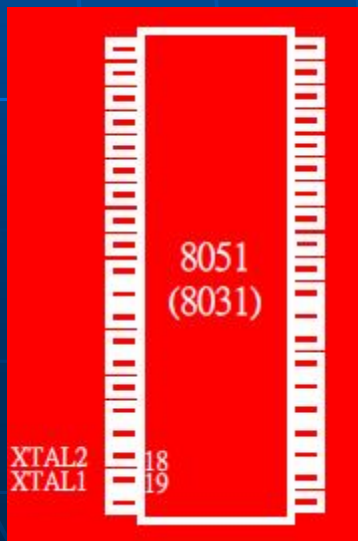
XTAL1 and XTAL2

- If you use a frequency source other than a crystal oscillator, such as a TTL oscillator:
 - It will be connected to XTAL1
 - XTAL2 is left unconnected



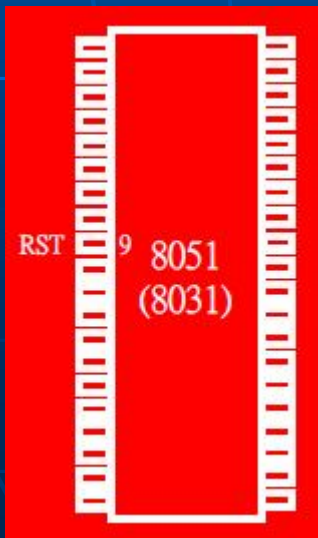
XTAL1 and XTAL2

- The **speed of 8051** refers to the maximum oscillator frequency connected to XTAL.
- We can observe the frequency on the XTAL2 pin using the oscilloscope.



RST

- RESET pin is an input and is active high (normally low)
- Upon applying a high pulse to this pin, the microcontroller will reset and terminate all activities
- This is often referred to as a power-on reset
- Activating a power-on reset will cause all values in the registers to be lost



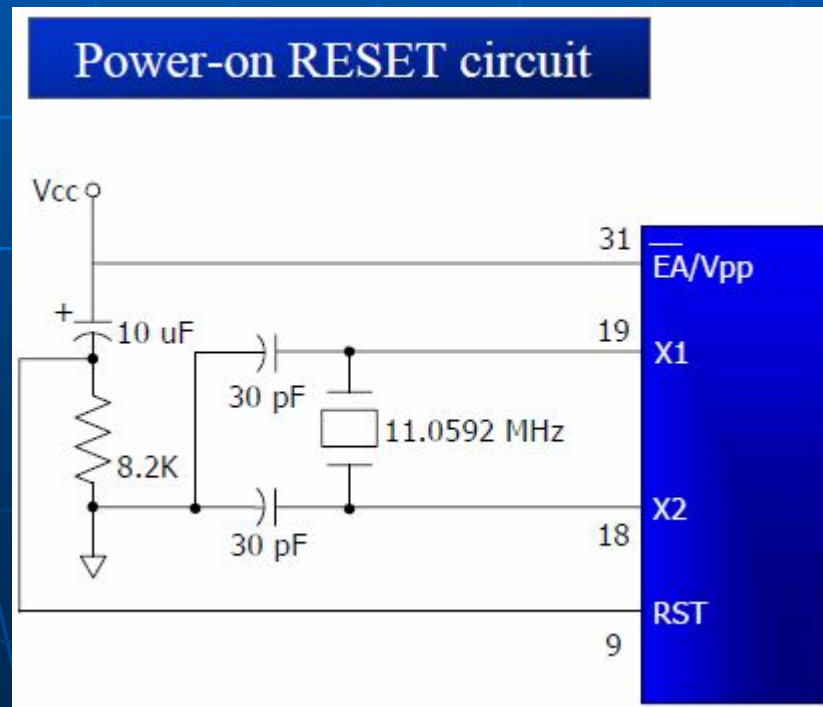
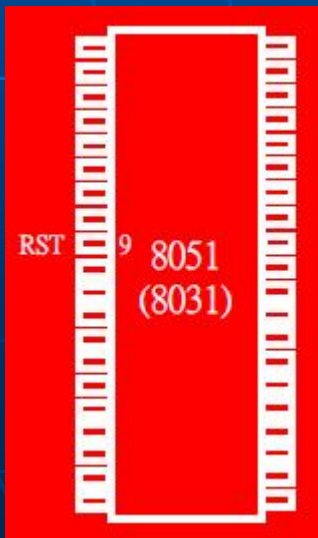
RESET value of some 8051 registers

we must place the first line of source code in ROM location 0

Register	Reset Value
PC	0000
DPTR	0000
ACC	00
PSW	00
SP	07
B	00
P0-P3	FF

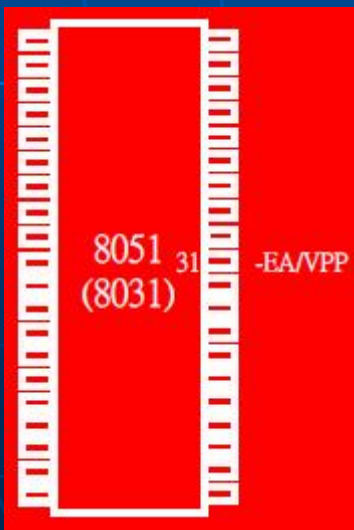
RST

- In order for the RESET input to be effective, it must have a minimum duration of 2 machine cycles.
- In other words, the high pulse must be high for a minimum of 2 machine cycles before it is allowed to go low.



EA'

- EA', "external access", is an input pin and must be connected to Vcc or GND
- The 8051 family members all come with on-chip ROM to store programs and also have an external code and data memory.
- Normally EA pin is connected to Vcc
- EA pin must be connected to GND to indicate that the code or data is stored externally.



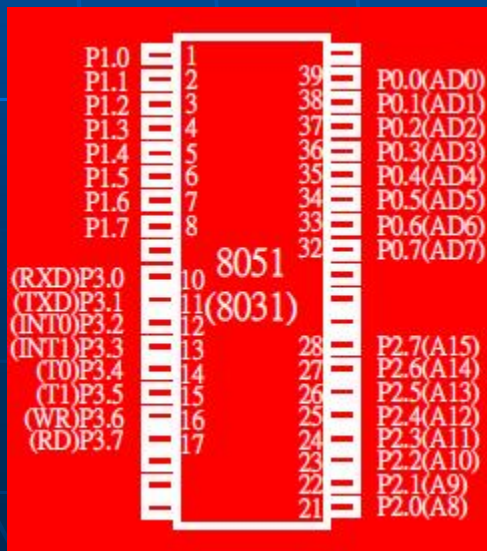
PSEN' and ALE

- PSEN, “program store enable”, is an output pin
- This pin is connected to the OE pin of the external memory.
- For External Code Memory, $PSEN' = 0$
- For External Data Memory, $PSEN' = 1$
- ALE pin is used for demultiplexing the address and data.



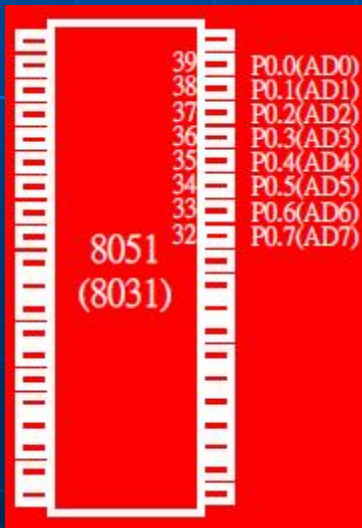
I/O Port Pins

- The four 8-bit I/O ports **P0, P1, P2 and P3** each uses 8 pins.
- All the ports upon RESET are configured as output, ready to be used as input ports by the external device.

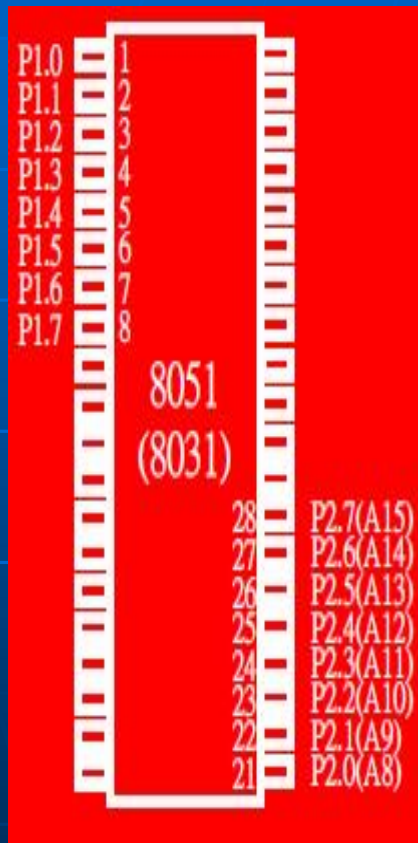


Port 0

- Port 0 is **also** designated as **AD0-AD7**.
- When connecting an 8051 to an external memory, port 0 provides both address and data.
- The 8051 multiplexes address and data through port 0 to save pins.
- **ALE** indicates if P0 has address or data.
 - When $ALE=0$, it provides data D0-D7
 - When $ALE=1$, it has address A0-A7



Port 1 and Port 2



- In 8051-based systems **with no external memory connection**:
 - Both P1 and P2 are used as simple I/O.
- In 8051-based systems **with external memory connections**:
 - Port 2 must be used along with P0 to provide the 16-bit address for the external memory.
 - P0 provides the lower 8 bits via A0 – A7.
 - P2 is used for the upper 8 bits of the 16-bit address, designated as A8 – A15, and it cannot be used for I/O.

Port 3

P3 Bit	Function	Pin
P3.0	RxD	10
P3.1	TxD	11
P3.2	<u>INT0</u>	12
P3.3	<u>INT1</u>	13
P3.4	T0	14
P3.5	T1	15
P3.6	<u>WR</u>	16
P3.7	<u>RD</u>	17

Serial
communications

External
interrupts

Timers

Read/Write signals
of external memories

Pin Description Summary

PIN	TYPE	NAME AND FUNCTION
Vss	I	Ground: 0 V reference.
Vcc	I	Power Supply: This is the power supply voltage for normal, idle, and power-down operation.
P0.0 - P0.7	I/O	Port 0: Port 0 is an open-drain, bi-directional I/O port. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory.
P1.0 - P1.7	I/O	Port 1: Port 1 is an 8-bit bi-directional I/O port.
P2.0 - P2.7	I/O	Port 2: Port 2 is an 8-bit bidirectional I/O. Port 2 emits the high order address byte during fetches from external program memory and during accesses to external data memory that use 16 bit addresses.
P3.0 - P3.7	I/O	Port 3: Port 3 is an 8 bit bidirectional I/O port. Port 3 also serves special features as explained.

Pin Description Summary

PIN	TYPE	NAME AND FUNCTION
RST	I	Reset: A high on this pin for two machine cycles while the oscillator is running, resets the device.
ALE	O	Address Latch Enable: Output pulse for latching the low byte of the address during an access to external memory.
PSEN*	O	Program Store Enable: The read strobe to external program memory. When executing code from the external program memory, PSEN* is activated twice each machine cycle, except that two PSEN* activations are skipped during each access to external data memory.
EA*/VPP	I	External Access Enable/Programming Supply Voltage: EA* must be externally held low to enable the device to fetch code from external program memory locations. If EA* is held high, the device executes from internal program memory. This pin also receives the programming supply voltage Vpp during Flash programming. (applies for 89c5x MCU's)