

UCS1502 - MICROPROCESSORS AND INTERFACING

Interrupt Controller – 8259

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Learning Objective

- To understand the architecture of 8259
- To understand 8259 operation

Overview

- Pin diagram of 8259
- Architecture
- Control word
- Modes of operation

8259 Features

- 8259 is **Programmable Interrupt Controller (PIC)**
- It is a tool **for managing the interrupt requests.**
- 8259 is a very **flexible** peripheral controller chip:
 - PIC can deal with **up to 64 interrupt inputs**
 - interrupts can be **masked individually.**
 - **various priority schemes** can also programmed.

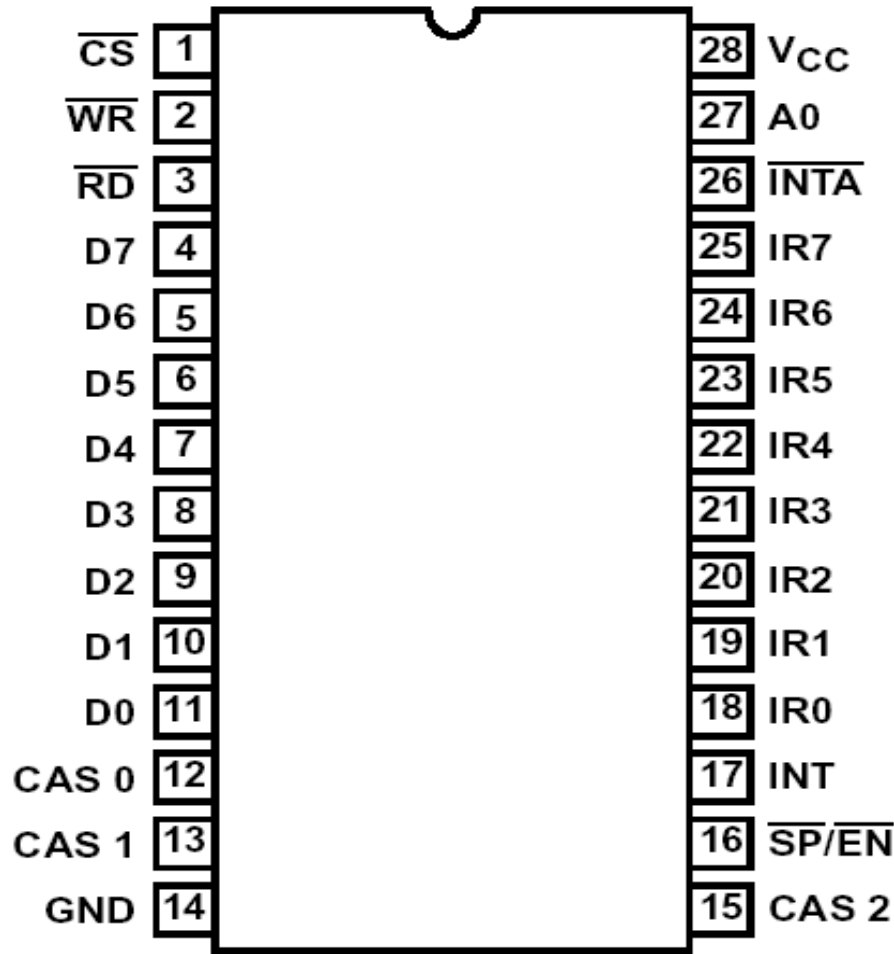


1. manage eight interrupts according to the instructions written into its control registers. This is equivalent to providing eight interrupt pins on the processor in place of one INTR (8085) pin.
2. vector an interrupt request anywhere in the memory map. However, all eight interrupts are spaced at the interval of either four or eight locations. This eliminates the major drawback of the 8085 interrupts in which all interrupts are vectored to memory locations on page 00H.
3. resolve eight levels of interrupt priorities in a variety of modes, such as fully nested mode, automatic rotation mode, and specific rotation mode (to be explained later).
4. mask each interrupt request individually.
5. read the status of pending interrupts, in-service interrupts, and masked interrupts.
6. be set up to accept either the level-triggered or the edge-triggered interrupt request.
7. be expanded to 64 priority levels by cascading additional 8259As.
8. be set up to work with either the 8085 microprocessor mode or the 8086/8088 microprocessor mode.



8259 Pin Diagram

82C59A (PDIP, Cerdip)
TOP VIEW



Pin Names

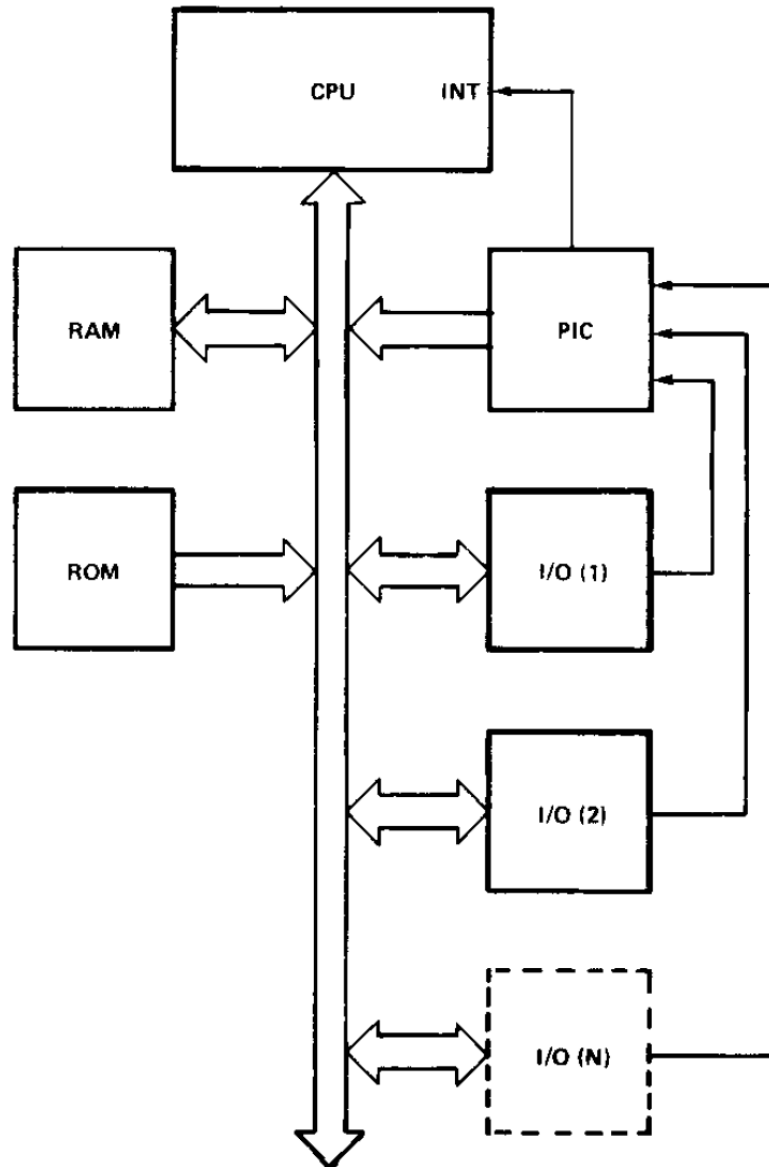
D ₇ -D ₀	Data Bus (Bidirectional)
\overline{RD}	Read Input
\overline{WR}	Write Input
A ₀	Command Select Address
\overline{CS}	Chip Select
CAS ₂ -CAS ₀	Cascade Lines
$\overline{SP/EN}$	Slave Program/Enable Buffer
INT	Interrupt Output
\overline{INTA}	Interrupt Acknowledge Input
IR ₀ -IR ₇	Interrupt Request Inputs

Pin Details

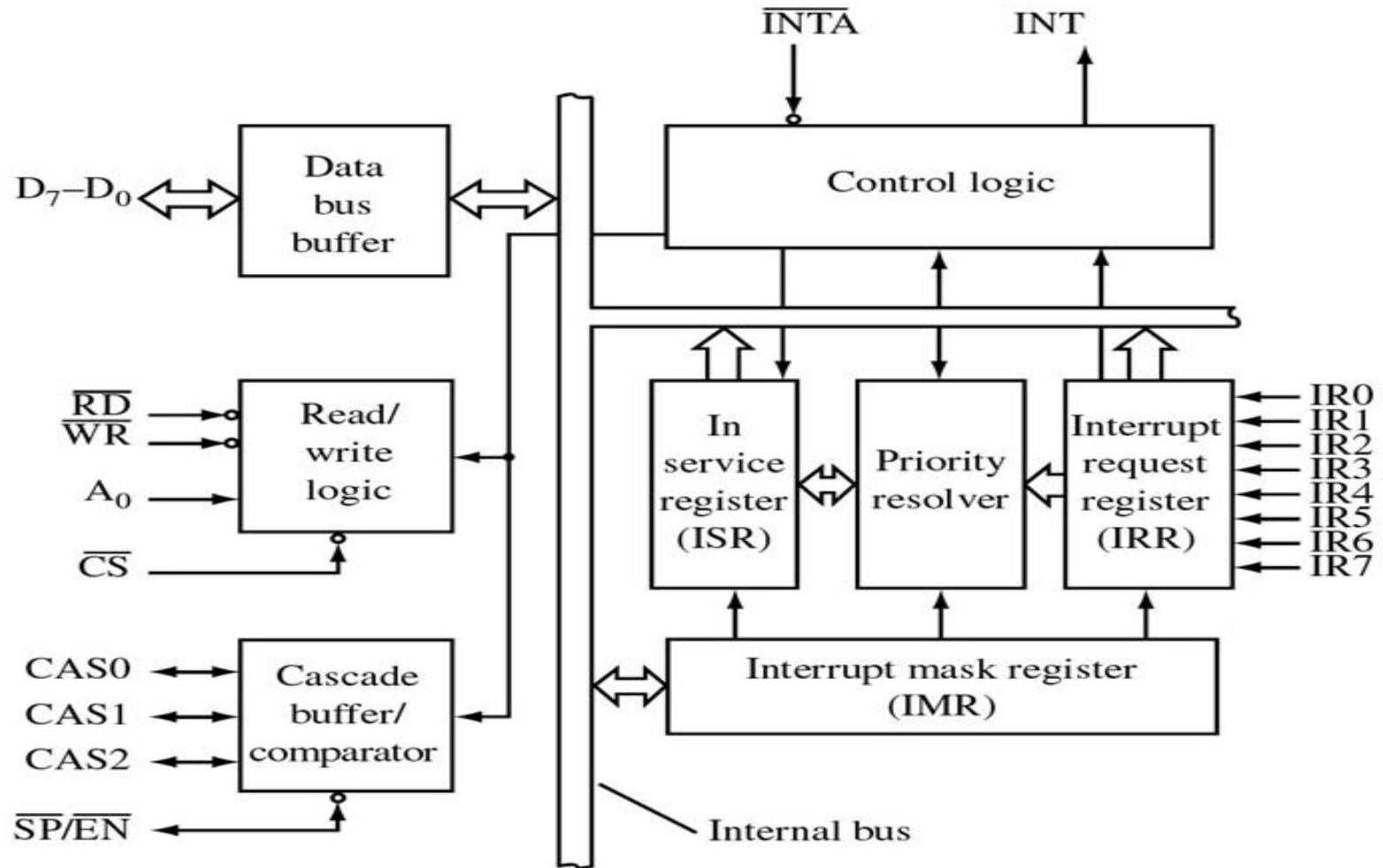
Symbol	Pin No.	Type	Name and Function
$\overline{SP}/\overline{EN}$	16	I/O	SLAVE PROGRAM/ENABLE BUFFER: This is a dual function pin. When in the Buffered Mode it can be used as an output to control buffer transceivers (EN). When not in the buffered mode it is used as an input to designate a master (SP = 1) or slave (SP = 0).
INT	17	O	INTERRUPT: This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to the CPU's interrupt pin.
IR ₀ –IR ₇	18–25	I	INTERRUPT REQUESTS: Asynchronous inputs. An interrupt request is executed by raising an IR input (low to high), and holding it high until it is acknowledged (Edge Triggered Mode), or just by a high level on an IR input (Level Triggered Mode).
\overline{INTA}	26	I	INTERRUPT ACKNOWLEDGE: This pin is used to enable 8259A interrupt-vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
A ₀	27	I	AO ADDRESS LINE: This pin acts in conjunction with the \overline{CS} , \overline{WR} , and \overline{RD} pins. It is used by the 8259A to decipher various Command Words the CPU writes and status the CPU wishes to read. It is typically connected to the CPU A0 address line (A1 for 8086, 8088).



Interfacing 8259



Block Diagram



Working of 8259

1. One or more of the **INTERRUPT REQUEST** lines (IR0 – IR7) are raised high, setting the corresponding IRR bit(s).
2. The 8259A evaluates these requests, and sends an **INT to the CPU**, if appropriate.
3. The CPU acknowledges the INT and responds with an **INTA*** pulse.
4. Upon receiving an INTA* from the CPU group, the **highest priority ISR bit is set and the corresponding IRR bit is reset**.



Working of 8259

5. Then 8086 will send **one more INTA** pulse to 8259.
 - On this second interrupt acknowledge cycle, 8259 will send an interrupt vector byte of data to the CPU, which is a pointer of the interrupt to be processed.

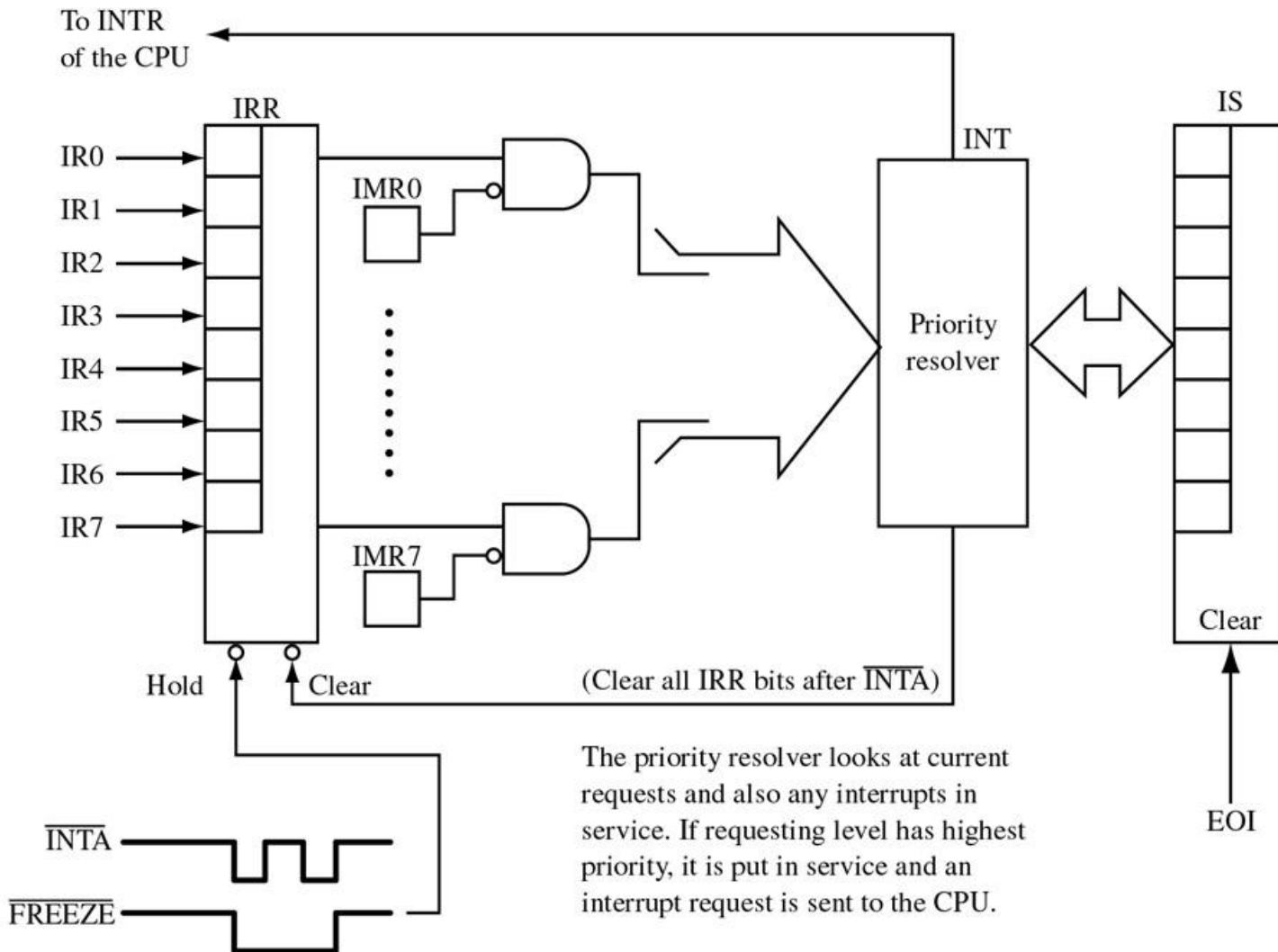
This **completes** the interrupt cycle.

6. The **ISR bit is reset** at the end of the **3rd** INTA pulse.

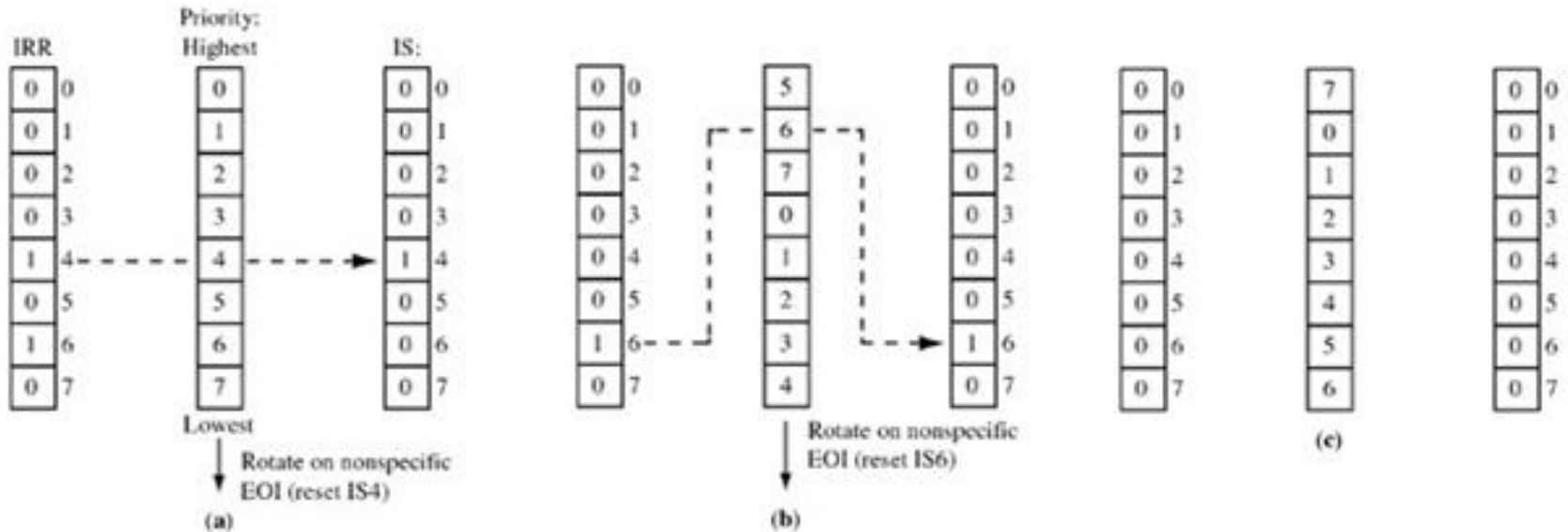
Interrupt vector byte

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	T7	T6	T5	T4	T3	1	1	1
IR6	T7	T6	T5	T4	T3	1	1	0
IR5	T7	T6	T5	T4	T3	1	0	1
IR4	T7	T6	T5	T4	T3	1	0	0
IR3	T7	T6	T5	T4	T3	0	1	1
IR2	T7	T6	T5	T4	T3	0	1	0
IR1	T7	T6	T5	T4	T3	0	0	1
IR0	T7	T6	T5	T4	T3	0	0	0

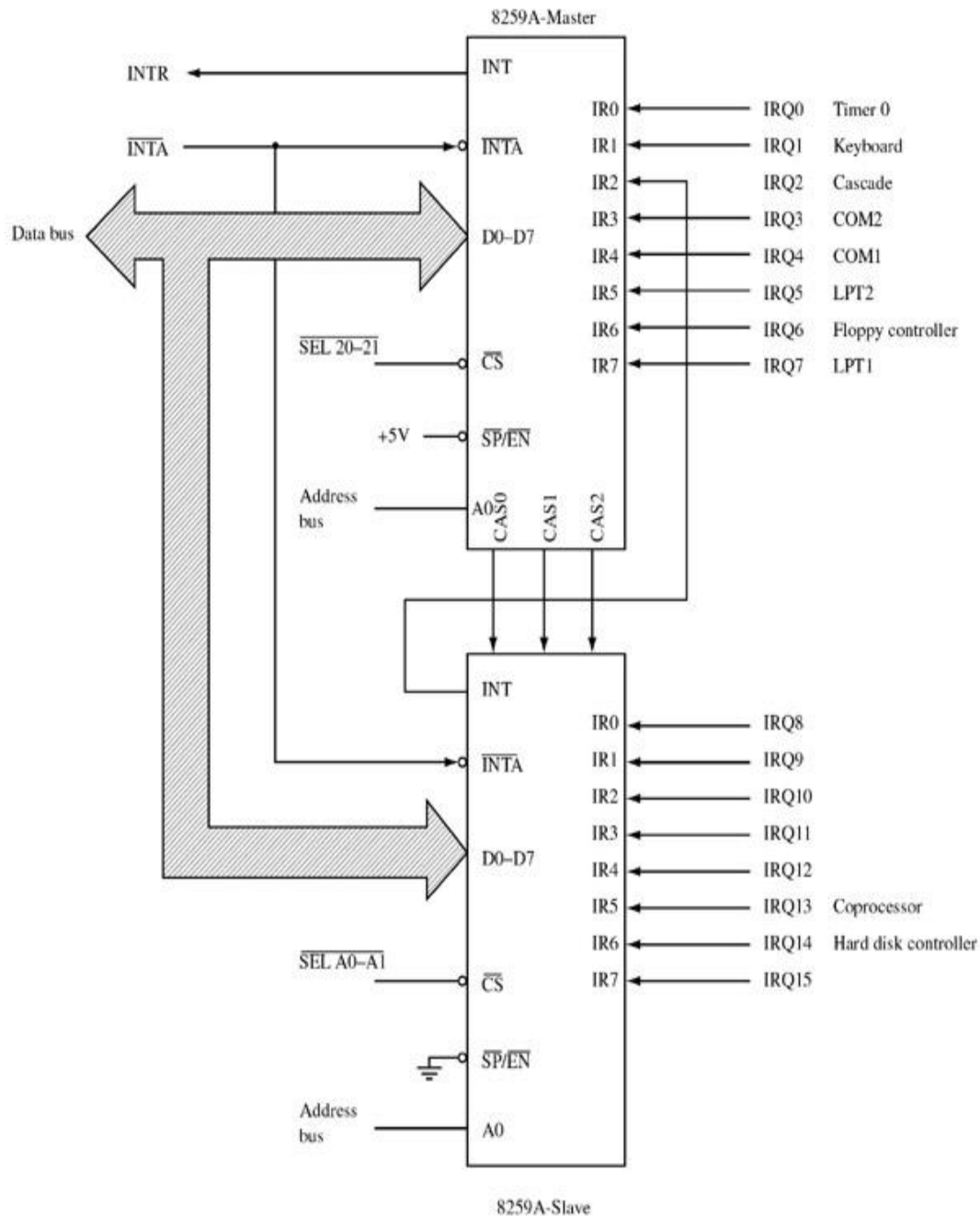
Work flow inside 8259



8259 Priority Resolver



- (a) Simultaneous interrupt requests arrive on IR4 and IR6. IR4 has highest priority and its IS bit is set as the IR4 service routine is put in service.
- (b) The IR4 service routine issues a rotate-on-nonspecific-EOI command, resetting IS4 and assigning it lowest priority. IR6 is now placed in service.
- (c) The IR6 service routine issues a rotate-on-nonspecific-EOI command, resetting IS6 and assigning it lowest priority.



8259 Command Words

- There are 2 Command Words in 8259.

1. Initialization Command Words (ICWs): Before normal operation can begin, each 82C59A in the system must be brought to a starting point using these command words.

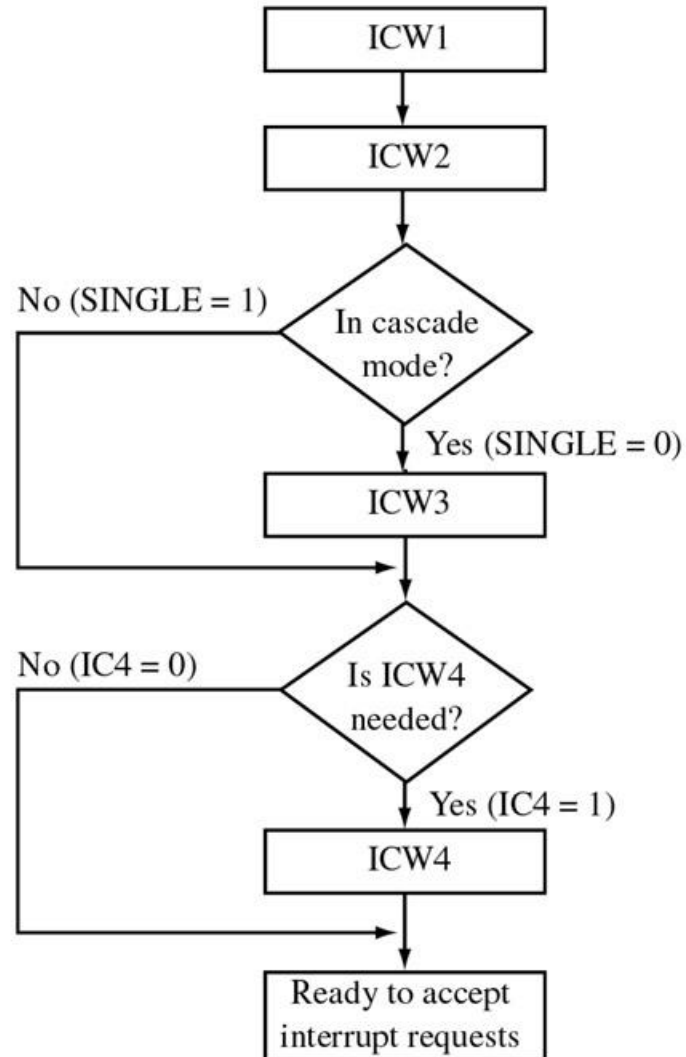
- There are **4 ICWs** in 8259.

2. Operation Command Words (OCWs): These are the command words which command the 82C59A to operate in various interrupt modes.

- There are **3 OCWs** in 8259



8259A initialization sequence



ICW1 Format

A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	A ₇	A ₆	A ₅	1	LTIM	ADI	SNGL	IC4

→ 1 = ICW4 needed
0 = No ICW4 needed

→ 1 = Single
0 = Cascade Mode

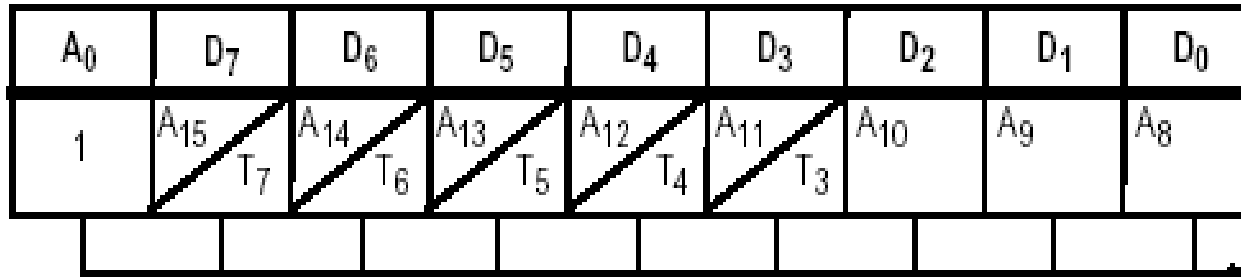
→ CALL address interval
1 = Interval of 4
0 = Interval of 8

→ 1 = Level triggered mode
0 = Edge triggered mode

→ A₇ - A₅ of Interrupt vector address
(MCS-80/85 mode only)



ICW2 Format



A₁₅ - A₈ of interrupt vector address
(MCS80/85 mode)

T₇ - T₃ of interrupt vector address
(8086/8088 mode)

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	T7	T6	T5	T4	T3	1	1	1
IR6	T7	T6	T5	T4	T3	1	1	0
IR5	T7	T6	T5	T4	T3	1	0	1
IR4	T7	T6	T5	T4	T3	1	0	0
IR3	T7	T6	T5	T4	T3	0	1	1
IR2	T7	T6	T5	T4	T3	0	1	0
IR1	T7	T6	T5	T4	T3	0	0	1
IR0	T7	T6	T5	T4	T3	0	0	0



ICW3 Format

- This word is read only when **there is more than one 8259** in the system and cascading is used, in which case **SNGL = 0** in **ICW1**.

ICW3 (Master device)

A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	S ₇	S ₆	S ₅	S ₄	S ₃	S ₂	S ₁	S ₀

This register is treated as a mask, with 1's indicating the IRQ channels connected to master/slave 8259As.

0 = IR Input has a slave
1 = IR Input does not have a slave

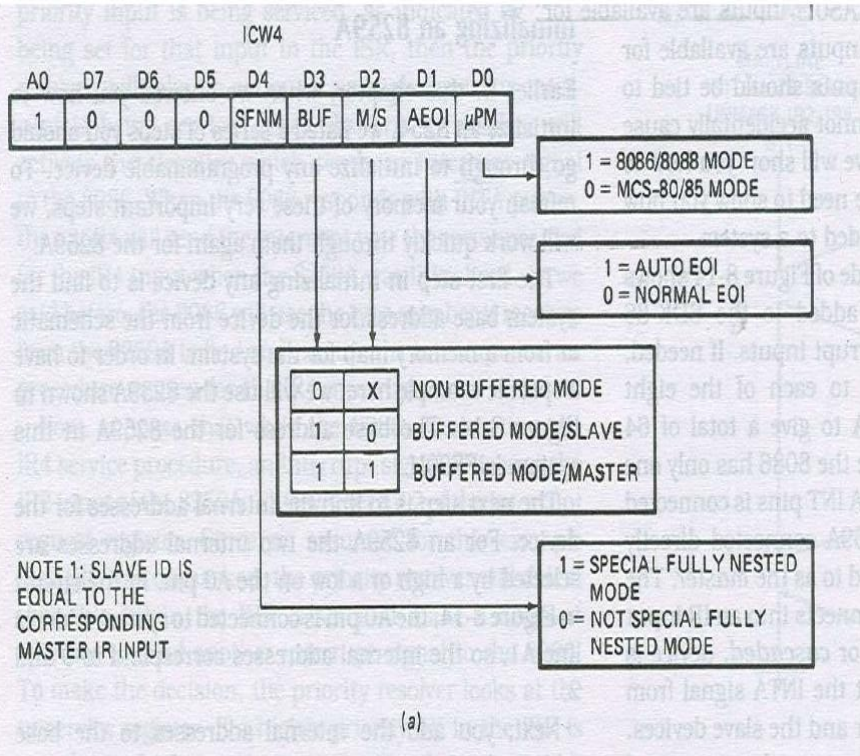
ICW3 (SLAVE DEVICE)

A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	0	0	ID ₂	ID ₁	ID ₀

SLAVE ID (NOTE)

0	1	2	3	4	5	6	7
0	1	0	1	0	1	0	1
0	0	1	1	0	0	1	1
0	0	0	0	1	1	1	1

ICW4 Format



SFNM: If SFNM = 1, the special fully nested mode is programmed.

BUF: If BUF = 1, the buffered mode is programmed. In buffered mode, $\overline{SP}/\overline{EN}$ becomes an enable output and the master/slave determination is by M/S.

M/S: If buffered mode is selected: M/S = 1 means the 82C59A is programmed to be a master, M/S = 0 means the 82C59A is programmed to be a slave. If BUF = 0, M/S has no function.

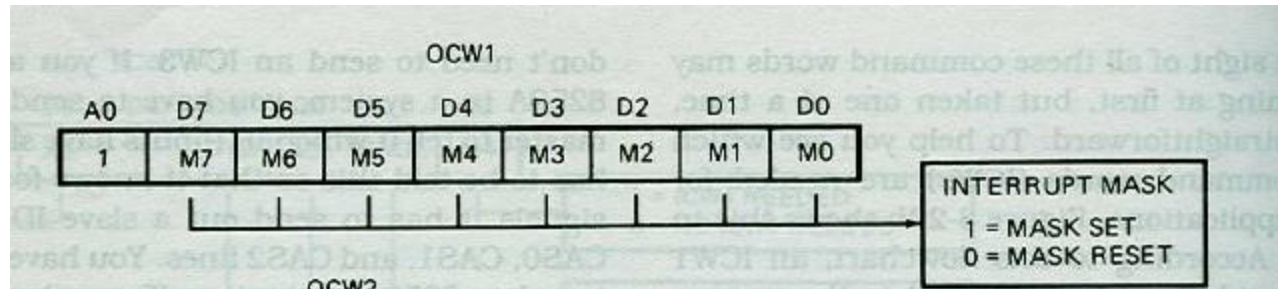
AEOI: If AEOI = 1, the automatic end of interrupt mode is programmed.

μ PM: Microprocessor mode: μ PM = 0 sets the 82C59A for 8080/85 system operation, μ PM = 1 sets the 82C59A for 80C86/88/286 system operation.

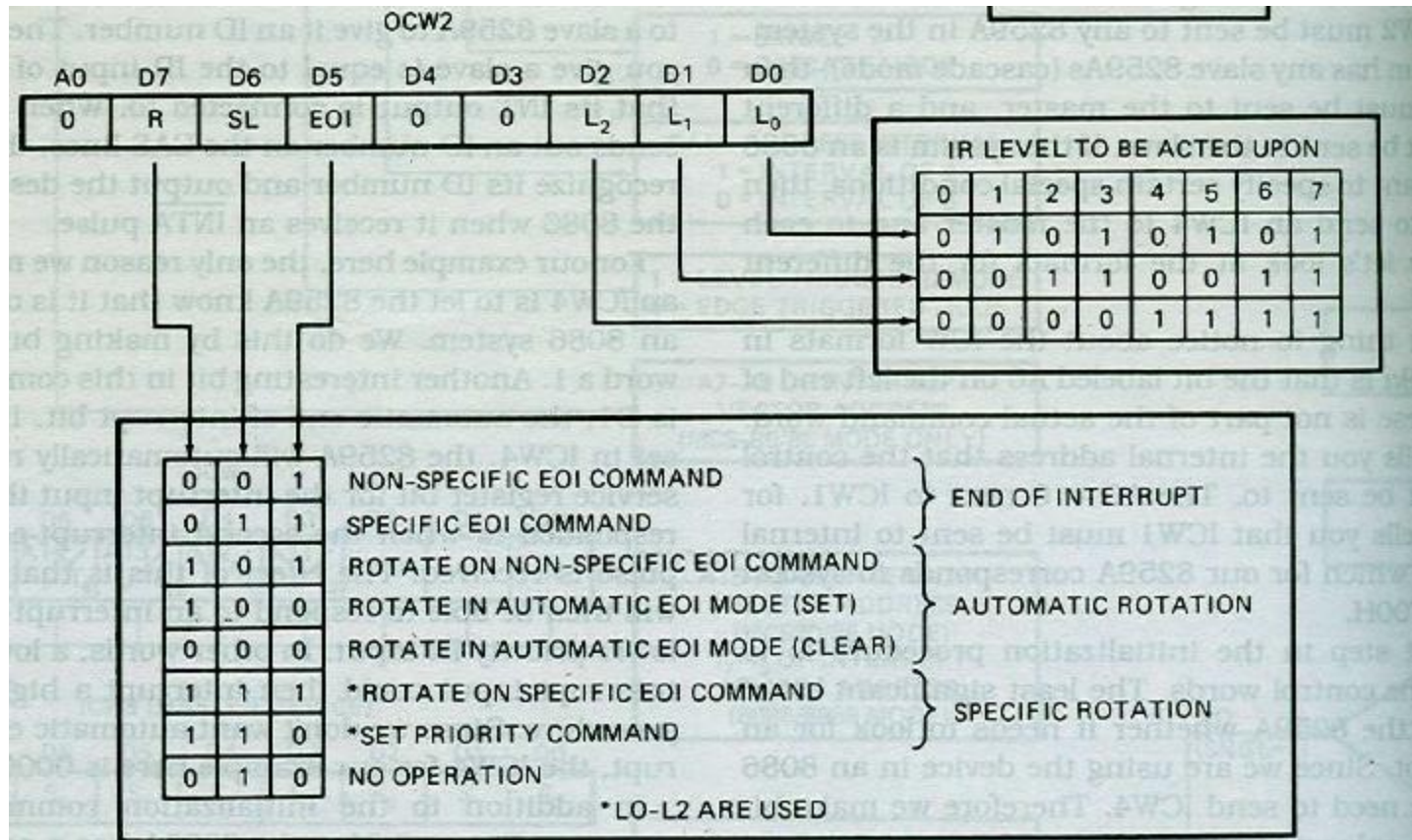
Operation Command Words (OCWs)

- After the **Initialization Command Words (ICWs)** are programmed into the 8259A, the chip is ready to accept interrupt requests at its input lines.
- However, during the 8259A operation, a selection of algorithms can command the **8259A to operate in various modes** through the Operation Command Words (OCWs).

OCW1 Format



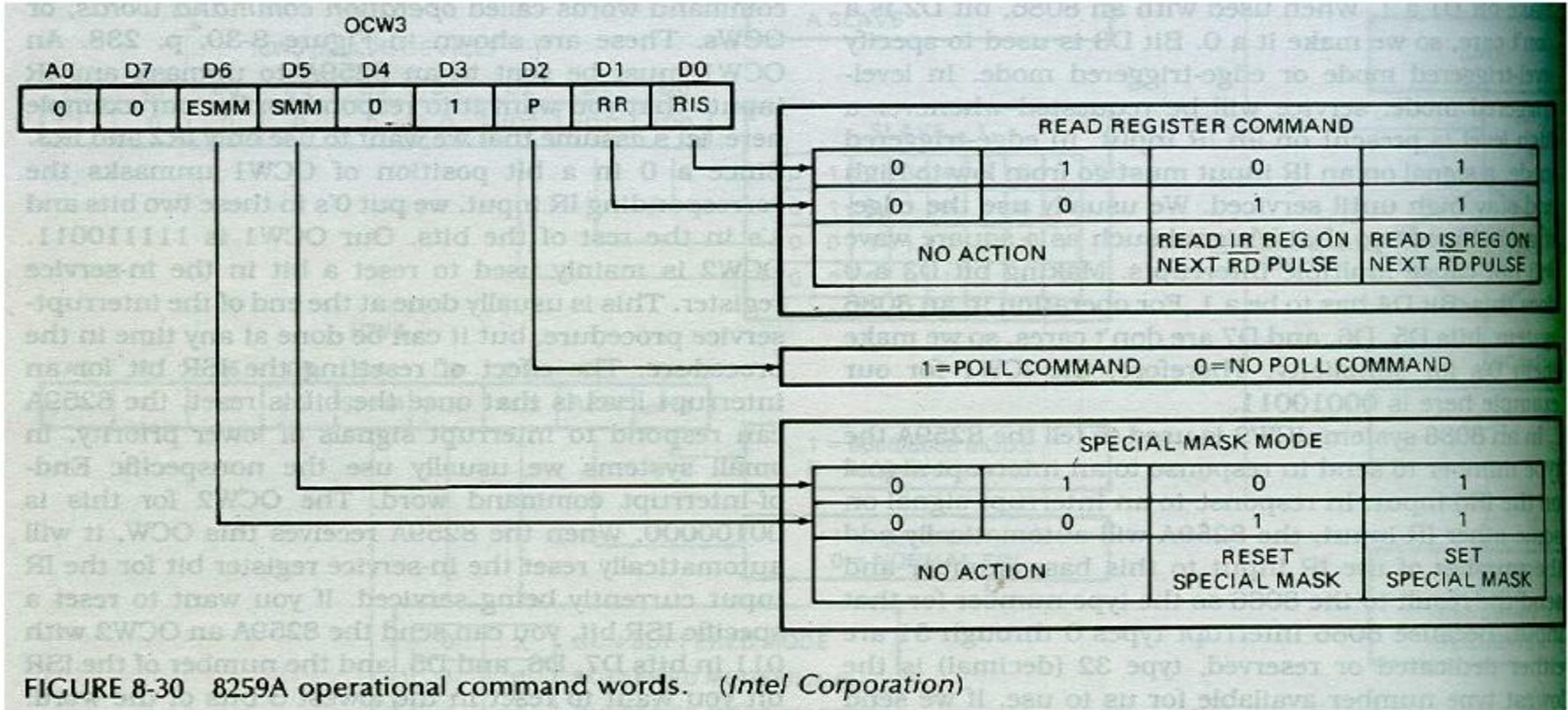
OCW2 Format



R, SL, EOI: These three bits control the Rotate and End of Interrupt modes and combinations of the two.

L2, L1, L0: These bits determine the interrupt level acted upon when the SL bit is active.

OCW3 Format



ESMM - Enable Special Mask Mode. When this bit is set to 1 it enables the SMM bit to set or reset the Special Mask Mode. When ESMM = 0, the SMM bit becomes a “don’t care”.

SMM - Special Mask Mode. If ESMM = 1 and SMM = 1, the 82C59A will enter Special Mask Mode. If ESMM = 1 and SMM = 0, the 82C59A will revert to normal mask mode. When ESMM = 0, SMM has no effect.



8259 Working Modes

- There are 4 different modes for 8259.
 1. Fully nested mode.
 2. Rotating priority mode.
 3. Special mask mode.
 4. Polled mode.

Fully nested mode

- This mode is entered after initialization unless another mode is programmed.
- The interrupt requests are ordered in priority from 0 through 7 (0 highest).
- When an interrupt is acknowledged the highest priority request is determined and its vector placed on the bus.
- Additionally, a bit of the Interrupt Service register (ISO-7) is set.
- This bit remains set until the microprocessor issues an End of Interrupt (EOI) command immediately before returning from the service routine
- If AEIO (Automatic End of Interrupt) bit is set, until the trailing edge of the last INTA.



After Rotate (IR4 was serviced, all other priorities rotated correspondingly)

IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
0	1	0	0	0	0	0	0

“IS” Status

231468–20

Highest Priority			Lowest Priority				
2	1	0	7	6	5	4	3

Priority Status

231468–21



Special mask mode

- Some applications may require an interrupt service routine to dynamically alter the system priority structure during its execution under software control.
- For example, the routine may wish to inhibit lower priority requests for a portion of its execution but enable some of them for another portion.
- That is where the Special Mask Mode comes in.
- In the special Mask Mode, when a mask bit is set in OCW1, it inhibits further interrupts at that level and enables interrupts from all other levels (lower as well as higher) that are not masked.
- Thus, any interrupts may be selectively enabled by loading the mask register.



Polled mode

- In Polled mode the INT output functions as it normally does.
- The microprocessor should ignore this output.
- This can be accomplished either by not connecting the INT output or by masking interrupts within the microprocessor, thereby disabling its interrupt input.
- Service to devices is achieved by software using a Poll command.
- The Poll command is issued by setting $P = 1$ in OCW3.



Summary

- Pin diagram of 8259
- Architecture
- Control word
- Modes of operation

Check your understanding

- What are the different modes of operation of 8259?

Thank you