Sri Sivasubramaniya Nadar College of Engineering, Kalavakkam – 603 110

(An Autonomous Institution, Affiliated to Anna University, Chennai)

Department of Information Technology

Continuous Assessment Test – II

Answer Key

Degree & Branch	B.Tech. Information Technology	**Semester**	IV
Subject Code & Name	**UIT1403 – Microprocessors and Microcontrollers**		
Time: 90 Minutes **Date: 10.05.2022**	**Answer All Questions**	**Maximum: 50 Marks**	

(K1 – Remembering, K2- Understanding, K3- Applying, K4- Analyzing, K5- Evaluating, K6 – Creating)

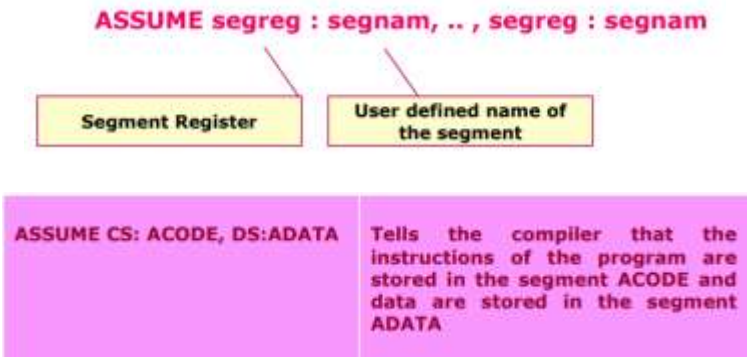
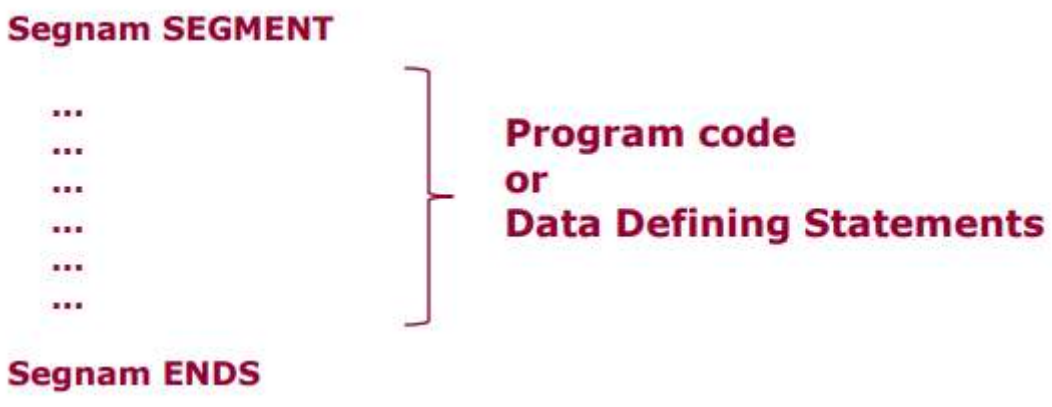
CO1	Write programs to run on 8086 microprocessor based systems.
CO2	Design the system using memory chips and peripheral chips for microprocessor and Microcontroller.
CO3	Analyse, Specify. Design , write and test assembly language programs.

Part – A (6 × 2 = 12 Marks)

<table>
<tr><th>Q. No.</th><th>Questions</th><th>KL</th><th>CO</th><th>PI</th></tr>
<tr><td>1</td><td>What is the assembler directive statement that used to reserve an array of 100 words in memory but leave the 100 words uninitialized and give it a name TEMP?
Answer:
TEMP DW 100 DUP (?)</td><td>K2</td><td>CO1</td><td>2.1.3</td></tr>
<tr><td>2</td><td>Let us consider an assembly statement as INT 10H. What will be the starting and ending addresses for the respective interrupt service routine stored in the interrupt vector table?
Answer:
10H = 16 (in decimal)
= 16 * 4 (Segment Size) = 64 = 0040H
Starting Address: 0040H
Ending Address: 0043H</td><td>K2</td><td>CO3</td><td>2.1.3</td></tr>
<tr><td>3</td><td>What will be the contents of A_0, A_1, and $\overline{CS}$ signals when the output (write) operation is done on Port A (i.e. data bus to Port A) of 8255 PPI.
Answer:
<table>
<tr><th>A_1</th><th>A_0</th><th>$\overline{RD}$</th><th>$\overline{WR}$</th><th>$\overline{CS}$</th><th>Operation</th></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Data bus to Port A</td></tr>
</table></td><td>K2</td><td>CO3</td><td>2.1.3</td></tr>
<tr><td>4</td><td>Determine the mode of operation and the selected counter based on the control word format of 8253/8254 programmable interval timer.
<table>
<tr><th>D_7</th><th>D_6</th><th>D_5</th><th>D_4</th><th>D_3</th><th>D_2</th><th>D_1</th><th>D_0</th></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>X</td><td>1</td><td>1</td><td>1</td></tr>
</table>
Answer:
Mode 3
Select Counter 2</td><td>K2</td><td>CO2</td><td>2.1.3</td></tr>
</table>

5	How many number of vectored priority interrupts are handled by the Intel 8259A Programmable Interrupt Controller when it is connected to the 8086 microprocessor in cascade configuration? **Answer:** 64	K2	CO2	2.1.3
6	If 8251 USART is programmed in asynchronous mode, how many stop bits the receiver requires? **Answer:** 1 or 1½ or 2 stop bits	K2	CO2	2.1.3

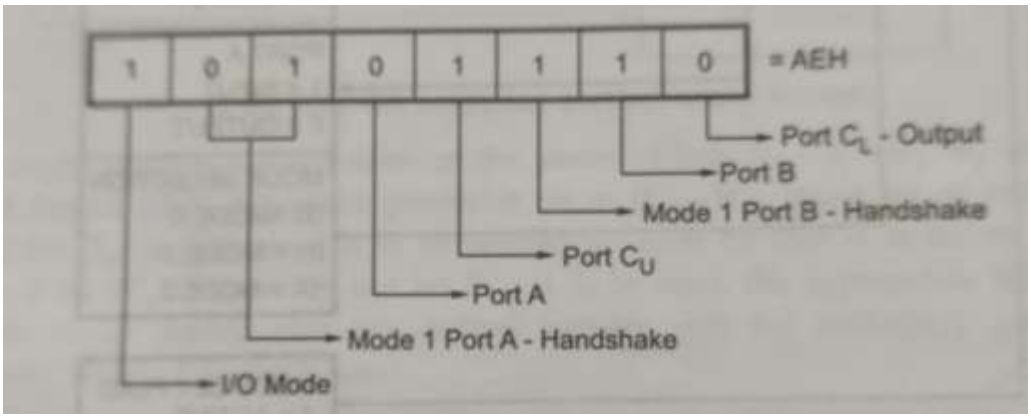
Part – B (3 × 6 = 18 Marks)

7	Explain the following assembler directives with an example. a) ASSUME b) SEGMENT c) EQU **Answer:** **a) ASSUME (2 Marks)** Informs the assembler the name of the program/ data segment that should be used for a specific segment. General form:  **b) SEGMENT (2 Marks)** SEGMENT : Used to indicate the beginning of a code/ data/ stack segment General form:  **c) EQU (2 Marks)** EQU (Equate) is used to attach a value to a variable	K2	CO2	1.3.1, 1.4.1

	Example: **LOOP EQU 10FEH** — **Value of variable LOOP is $10FE_H$**			
8	Briefly describe the conditions which cause the 8086 microprocessors to perform each of the following types of interrupts: Type 0, Type 1, Type 2, Type 3 and Type 4. **Answer:** • Type 0 interrupts: This interrupt is also known as the divide by zero interrupt. For cases where the quotient becomes particularly large to be placed / adjusted an error might occur. (2 marks) • Type 1 interrupts: This is also known as the single step interrupt. This type of interrupt is primarily used for debugging purposes in assembly language. (1 mark) • Type 2 interrupts: also known as the non-maskable NMI interrupts. These types of interrupts are used for emergency scenarios such as power failure. (1 mark) • Type 3 interrupts: These types of interrupts are also known as breakpoint interrupts. When this interrupt occurs, a program would execute up to its break point. (1 mark) • Type 4 interrupts: Also known as overflow interrupts is generally existent after an arithmetic operation was performed. (1 mark)	K2	CO2	1.3.1, 1.4.1
9	Compare I/O mapped and memory mapped I/O Techniques. **Answer: (Any two points - 2 marks)** **Memory Mapped IO** • IO is treated as memory. • 16-bit addressing. • More Decoder Hardware. • Can address 2^{16}=64k locations. • Less memory is available. **IO Mapped IO** • IO is treated IO. • 8- bit addressing. • Less Decoder Hardware. • Can address 2^{8}=256 locations. • Whole memory address space is available.	K2	CO2	1.3.1, 1.4.1

Part – C (2 × 10 = 20 Marks)

10	**a)** Write a program to initialize 8255 in the configuration given below. • Port A: Output with handshake • Port B: Input with handshake • Port C_L: Output • Port C_U: Input Assume address of the control word register of 8255 as 83H. Also find the control word for the register arrangement of the ports of Intel 8255. (**5 Marks**) **Answer:** **Control Word Register (3 marks)**	K3	CO3	1.3.1, 1.4.1, 2.1.3



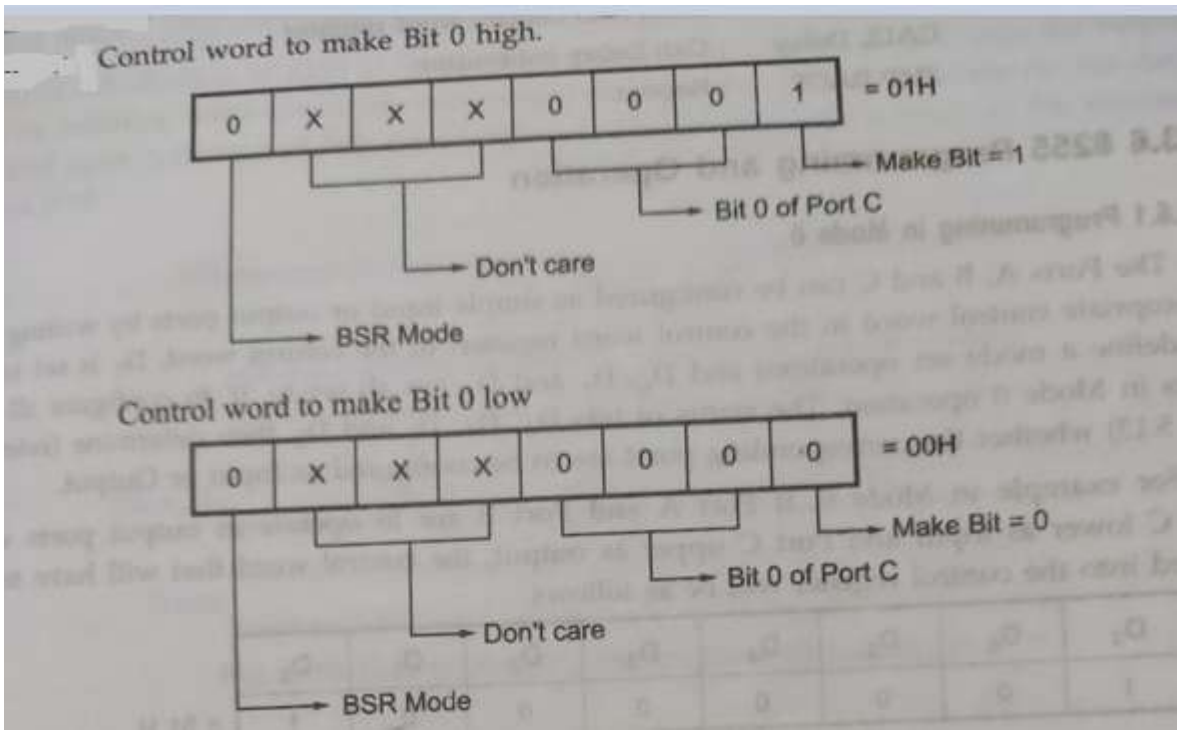
Source Program: (2 Marks)

```
MOV AL, 0AEH        ; Load control word
OUT 83H, AL ; Send Control Word
```

b) Write a program to blink Port C bit 0 (i.e., D_0) of the 8255. Assume address of the control word register of 8255 is 23H. Use Bit Set/Reset mode. (**5 Marks**)

Answer:

Control Word Register (2½ Marks)

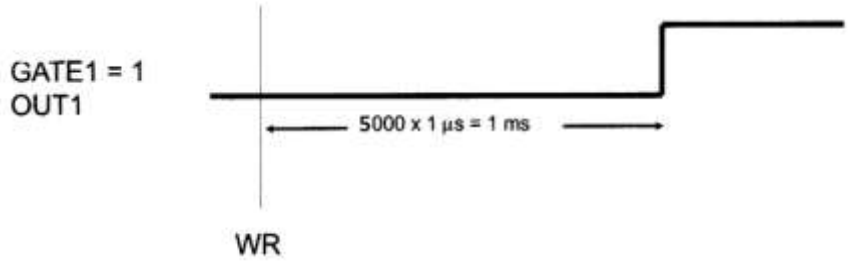
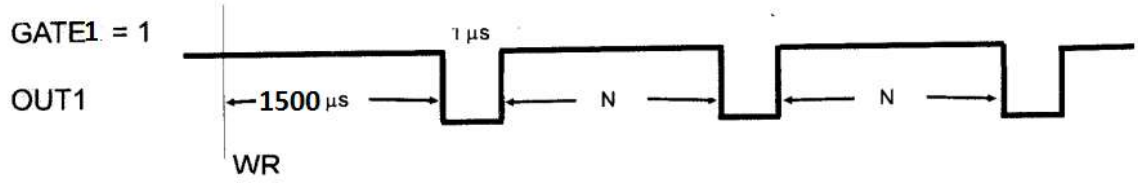


Source Program (2½ Marks)

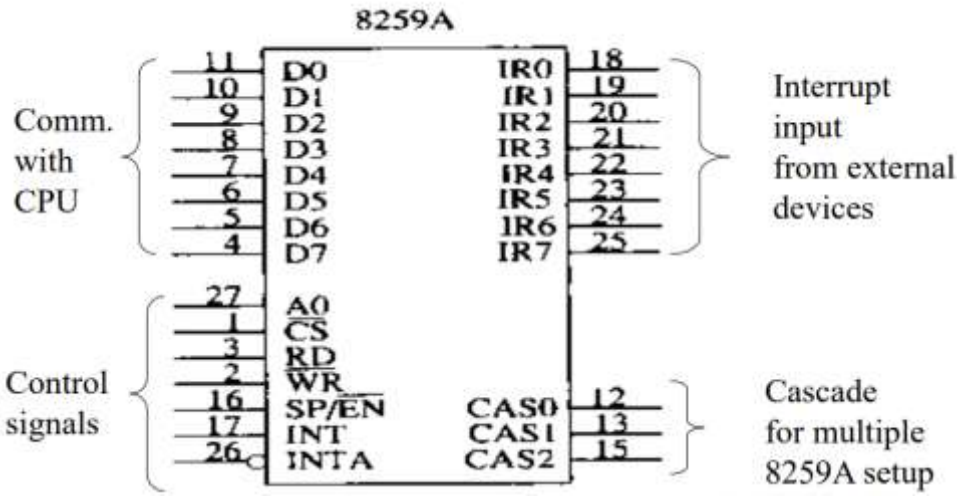
Source program :

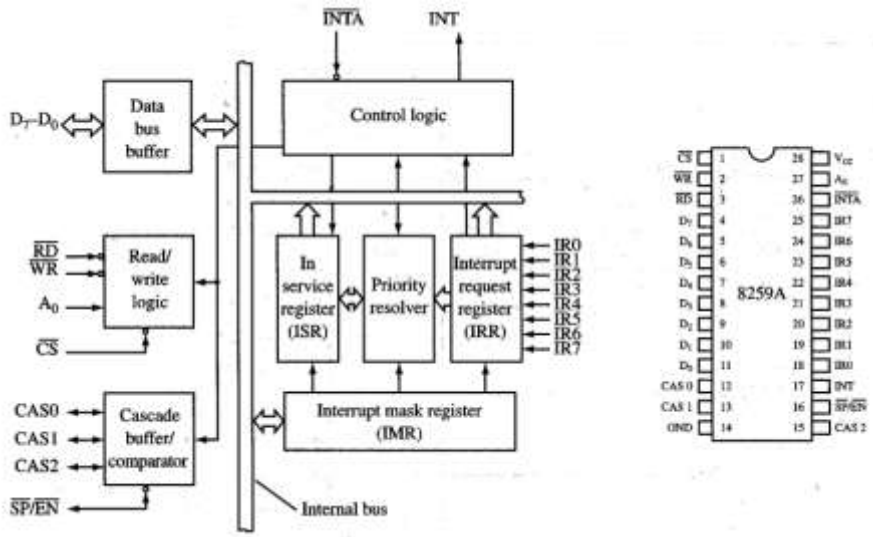
```
BACK :  MOV AL,01H   ; Load bit pattern to make PC0 high
        OUT 83H,AL   ; Send it to control word register
        CALL DELAY   ; Call Delay subroutine
        MOV AL,00H   ; Load bit pattern to make PC0 Low
        OUT 83H,AL   ; Send it to control word register
        CALL Delay   ; Call Delay subroutine
        JMP BACK     ; Repeat
```

OR

11	**a)** Assume that GATE1 = 1 and CLK1 =1 MHz and the clock count N= 5000. Show the output if 8253/8254 PIT is programmed in mode 0 and mode 2. (**5 Marks**) **Answer:** **Mode 0:(2½ Marks)** The clock period of CLK1 is 1 µs; therefore, OUT1 is low for 5000 *x* 1 µs = 1 ms, before it goes high, as shown in the following diagram.  **Mode 2:(2½ Marks)** Notice that the count is reloaded automatically and the counter countinues to produce OUT1.  **b)** Write an ALP to generate a delay of 100 msec using an 8086 system that runs on 10 MHz frequency (Hint: Use procedure in ALP to write a delay routine). (**5 Marks**) **Answer:** **ALP for Delay Routine(5 Marks)**	K3	CO3	1.3.1, 1.4.1, 2.1.3

```
PROC      DELAY LOCAL
ASSUME    CS: CODEP
CODEP     SEGMENT
          MOV CX, BA03H
WAIT:     DEC CX
          NOP
          JNZ  WAIT
          RET
          DELAY ENDP
```

12	Design and explain a peripheral device which handles multiple interrupt requests from external devices. **Answer:** **8259 Features (2 Marks)** • 8259 is a hardware device to support the interrupt mechanism. • It can support up to 8 vectored priority encoded interrupts to the microprocessor • Can be expanded (using more 8259) to accept up to 64 interrupt requests using master/slaves configuration • possible to mask individual interrupt request. **Pins Configuration of 8259A (4 Marks)**  **Block Diagram of 8259A (4 Marks)**	K3	CO2	3.1.1, 4.1.3, 5.1.1



OR

13

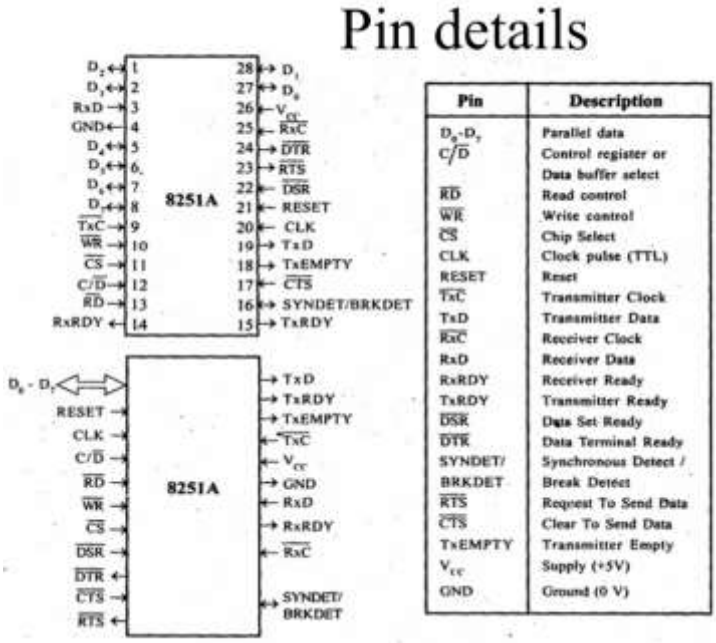
Design and explain a peripheral device which translates serial to parallel and parallel to serial data for synchronous mode of data transmission.

Answer:

USART Features (2 Marks)

- The INTEL 8251 is the industry standard Universal Synchronous / Asynchronous Receiver/Transmitter (USART) designed for data communications
- The 8251A is a programmable serial communication interface chip designed for synchronous and asynchronous serial data communication.
- The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously, it can receive serial data streams and convert them into parallel data character for the CPU

Pins Configuration of 8251 (4 Marks)



Pin	Description
D_0-D_7	Parallel data
C/$\overline{D}$	Control register or Data buffer select
$\overline{RD}$	Read control
$\overline{WR}$	Write control
$\overline{CS}$	Chip Select
CLK	Clock pulse (TTL)
RESET	Reset
$\overline{TxC}$	Transmitter Clock
TxD	Transmitter Data
$\overline{RxC}$	Receiver Clock
RxD	Receiver Data
RxRDY	Receiver Ready
TxRDY	Transmitter Ready
$\overline{DSR}$	Data Set Ready
$\overline{DTR}$	Data Terminal Ready
SYNDET/ BRKDET	Synchronous Detect / Break Detect
$\overline{RTS}$	Request To Send Data
$\overline{CTS}$	Clear To Send Data
TxEMPTY	Transmitter Empty
V_{CC}	Supply (+5V)
GND	Ground (0 V)

K3 | CO2 | 3.1.1, 4.1.3, 5.1.1

Block Diagram of 8251(4 Marks)