

# **8086 Basic Configuration and System Design**

**UCS1502 - MICROPROCESSORS AND INTERFACING**

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AP/CSE



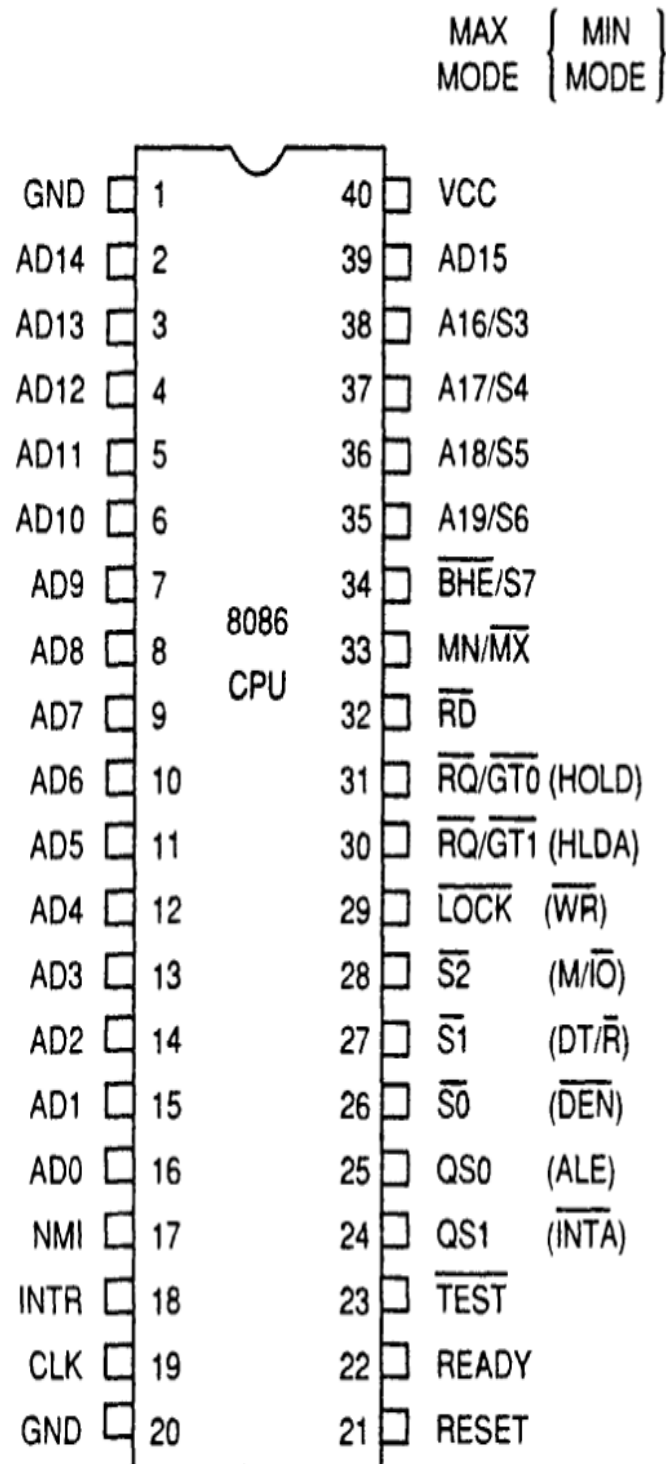
# Learning Objective

- To understand the minimum and maximum mode of operation
- To understand system design using 8086

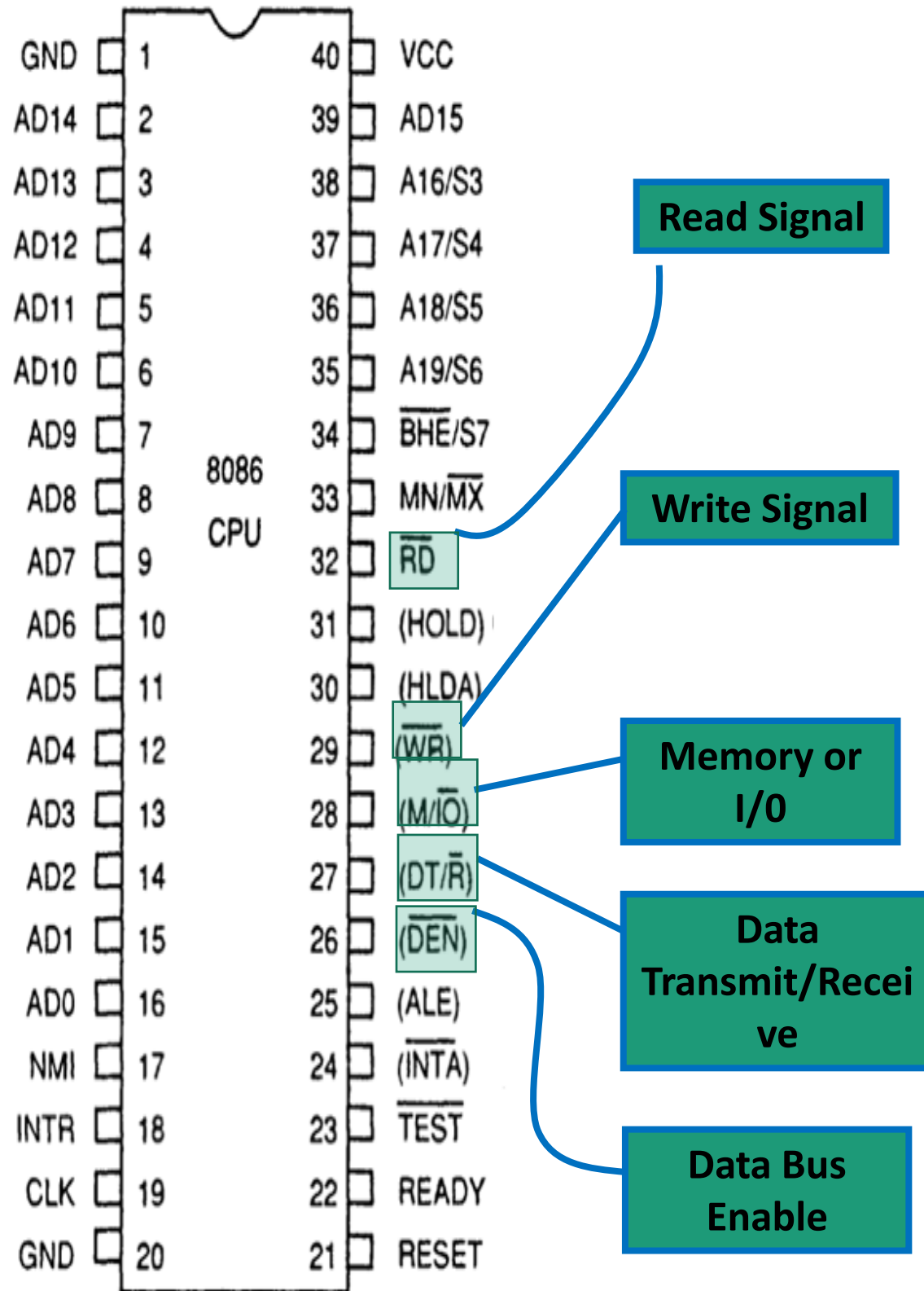
# Overview

- Pin Diagram of 8086
- Minimum mode
- Maximum mode
- Read / write cycle
- System Design

# INTEL 8086 - Pin Diagram



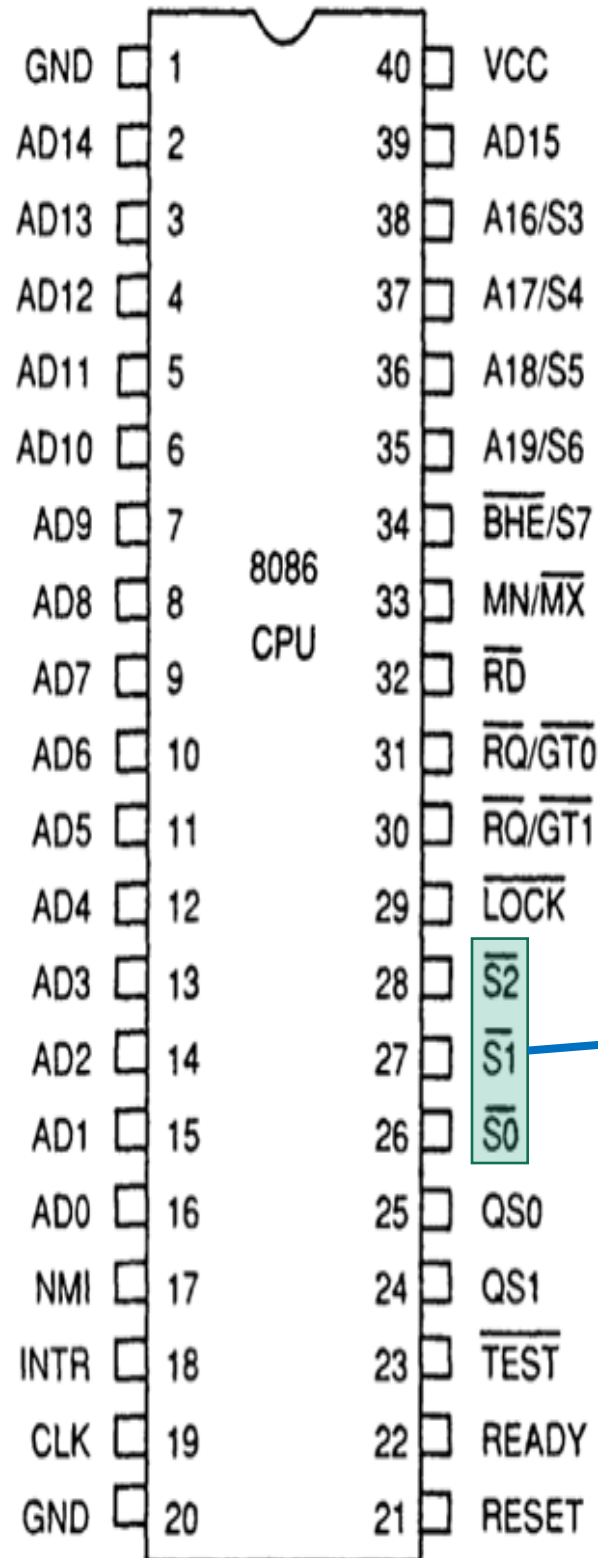
# Minimum Mode- Pin Details



# Maximum Mode - Pin Details

**S2 S1 S0**

000: INTA  
 001: read I/O port  
 010: write I/O port  
 011: halt  
 100: code access  
 101: read memory  
 110: write  
 memory  
 111: none -passive



## Status Signal

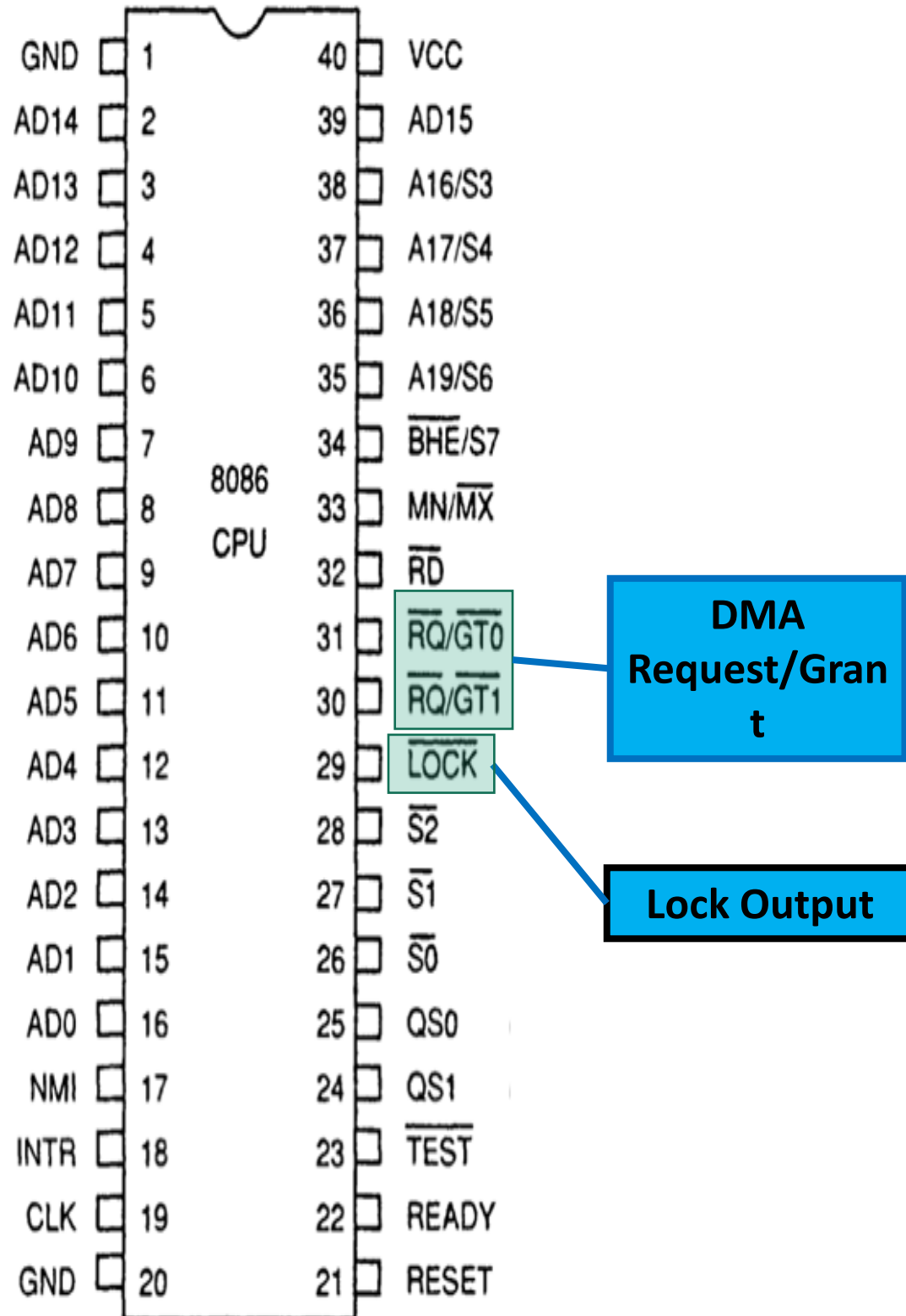
Inputs to 8288 to generate eliminated signals due to max mode.

# Maximum Mode - Pin Details

## Lock Output

Used to lock peripherals off the system

Activated by using the LOCK: prefix on any instruction



# Maximum Mode - Pin Details

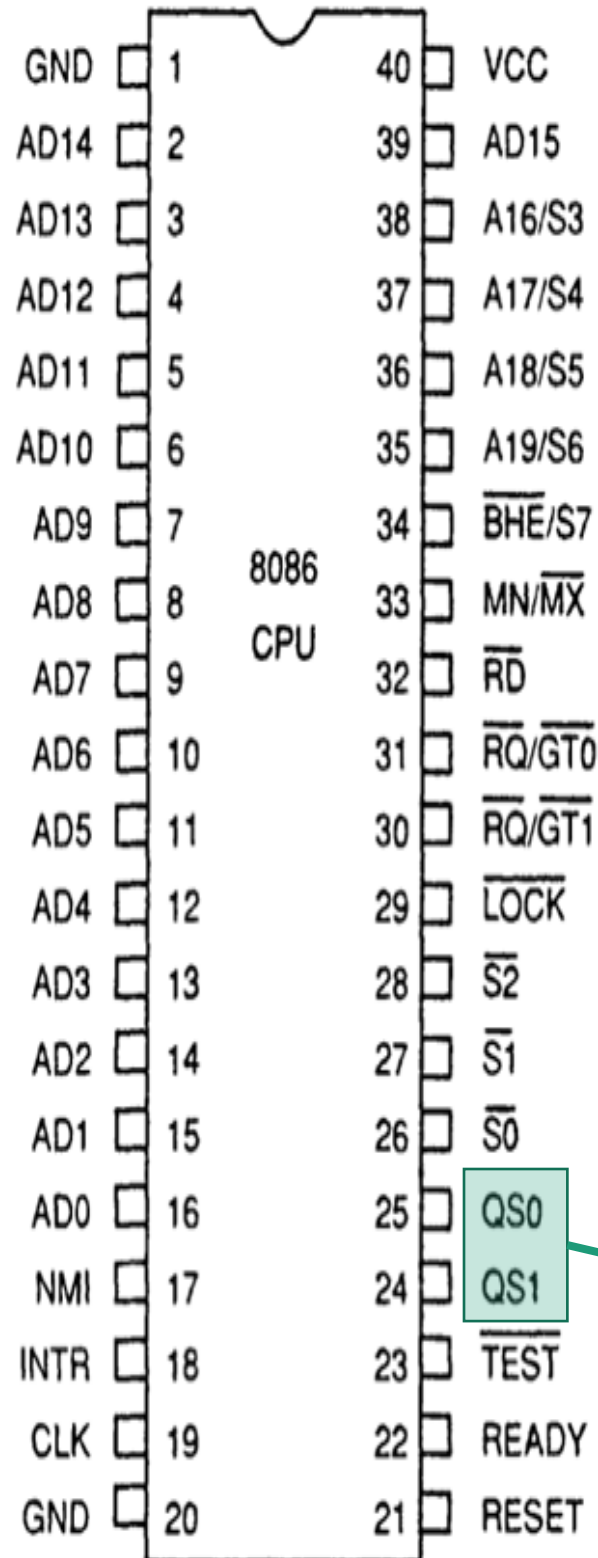
## QS1 QS0

00: Queue is idle

01: First byte of opcode

10: Queue is empty

11: Subsequent byte of opcode

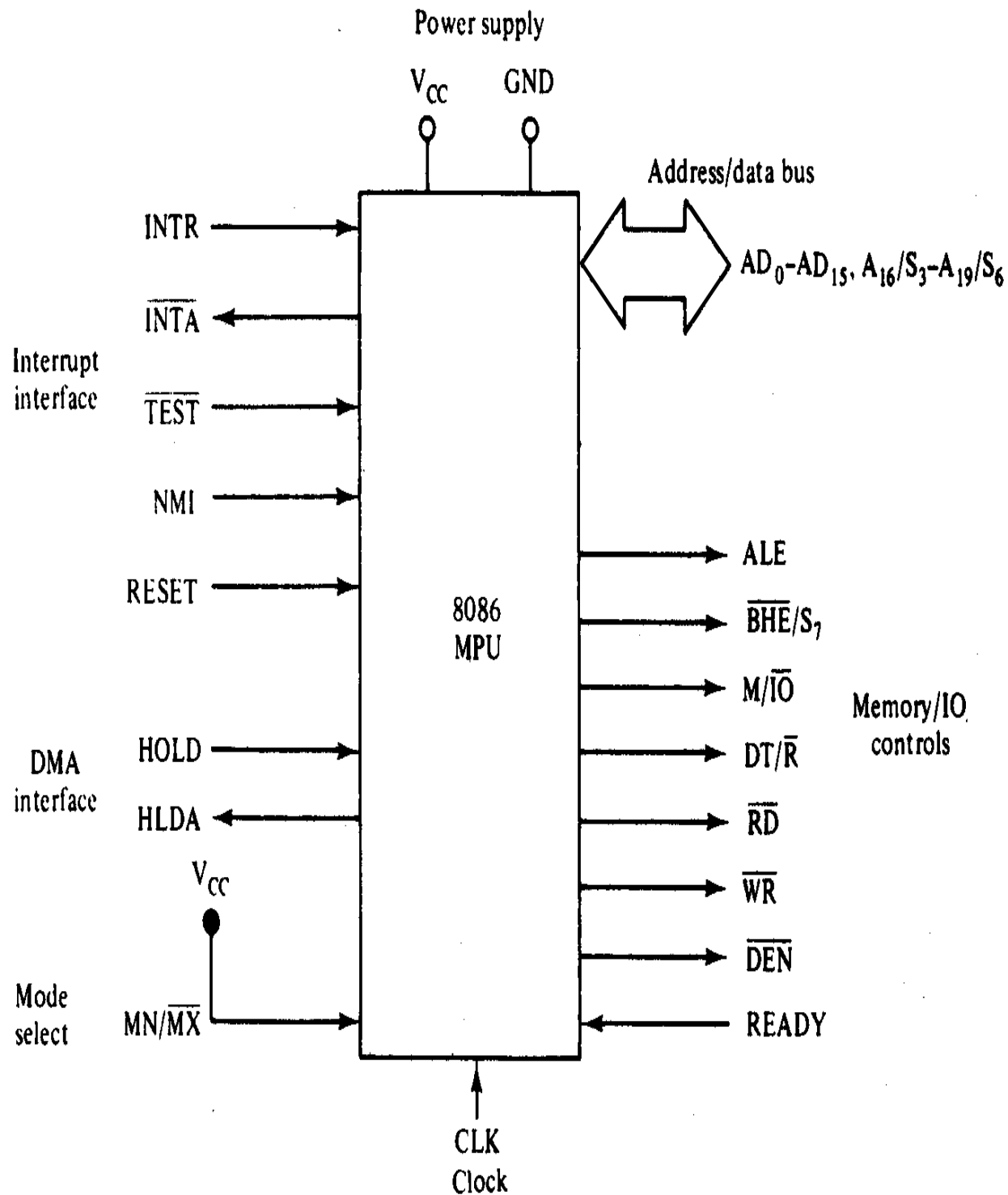


## Queue Status

Used by numeric coprocessor (8087)

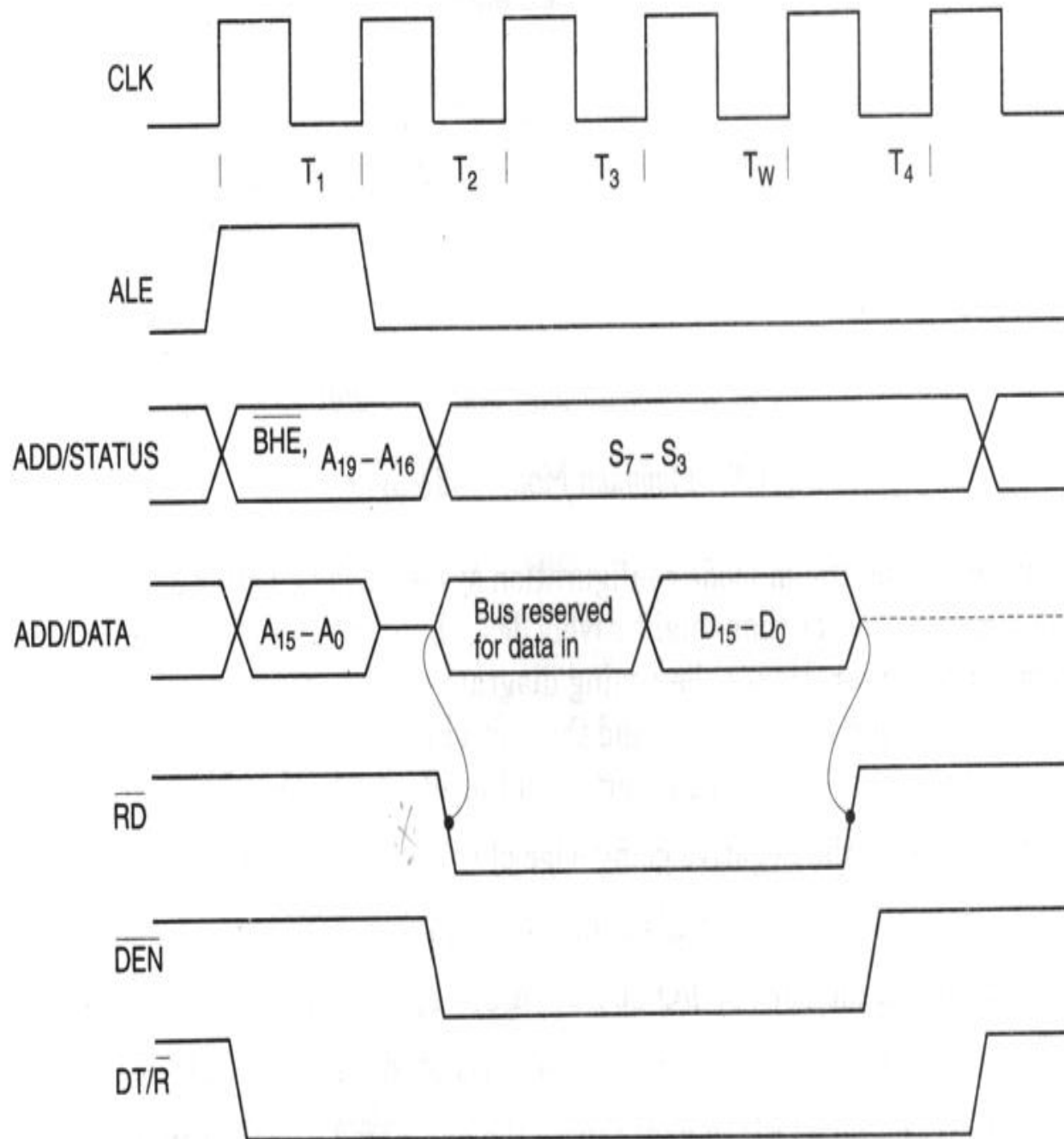


# Minimum Mode 8086 System

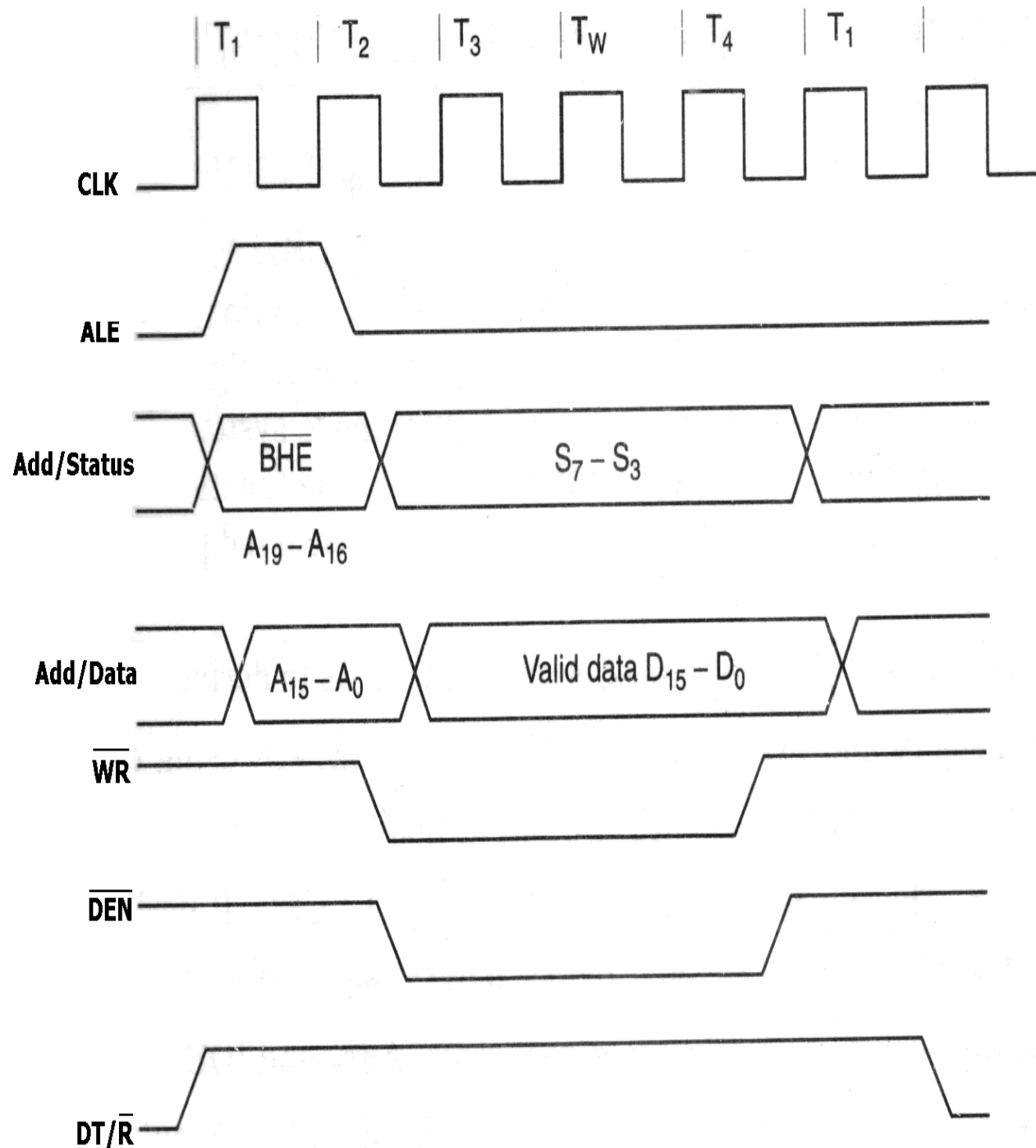


The diagram illustrates the internal architecture of an 8086 microprocessor system. On the left, the **8284 CLOCK GEN** block provides **RDY** and **RES** signals to the **8086** microprocessor. The **8086** block shows its various pins: **Clk** (clock), **MN/MX** (master/slave select, connected to **VCC**), **Reset**, **Ready**, **RD**, **WR**, **DEN** (data enable), **ALE** (address latch enable), **DT/R** (data bus transceiver enable), and **BHE** (bus high enable). The **ALE** signal is connected to the **STB** (latch strobe) input of the **Latches 2 or 3** block. The **DT/R** signal is connected to the **DIR** (direction) input of the **Transceivers** block. The **BHE** signal is connected to the **BHE** input of the **RAM** and **I/O** blocks. The **8086** also provides **ADD** (address) and **DATA BUS** signals to the **RAM**, **EPROM**, and **I/O** blocks. The **RAM** block has **RD**, **WR**, **CS<sub>H</sub>**, and **CS<sub>L</sub>** inputs. The **EPROM** block has **CE<sub>L</sub>**, **CE<sub>H</sub>**, **OE**, and **A0** inputs. The **I/O** block has **CS**, **RD**, and **WR** inputs. The **Transceivers** block has **DIR** and **G** inputs. The **STB** block has **STB** and **ADDR** inputs. The **DATA BUS** is shown as a bidirectional connection between the **8086** and the memory/I/O blocks.

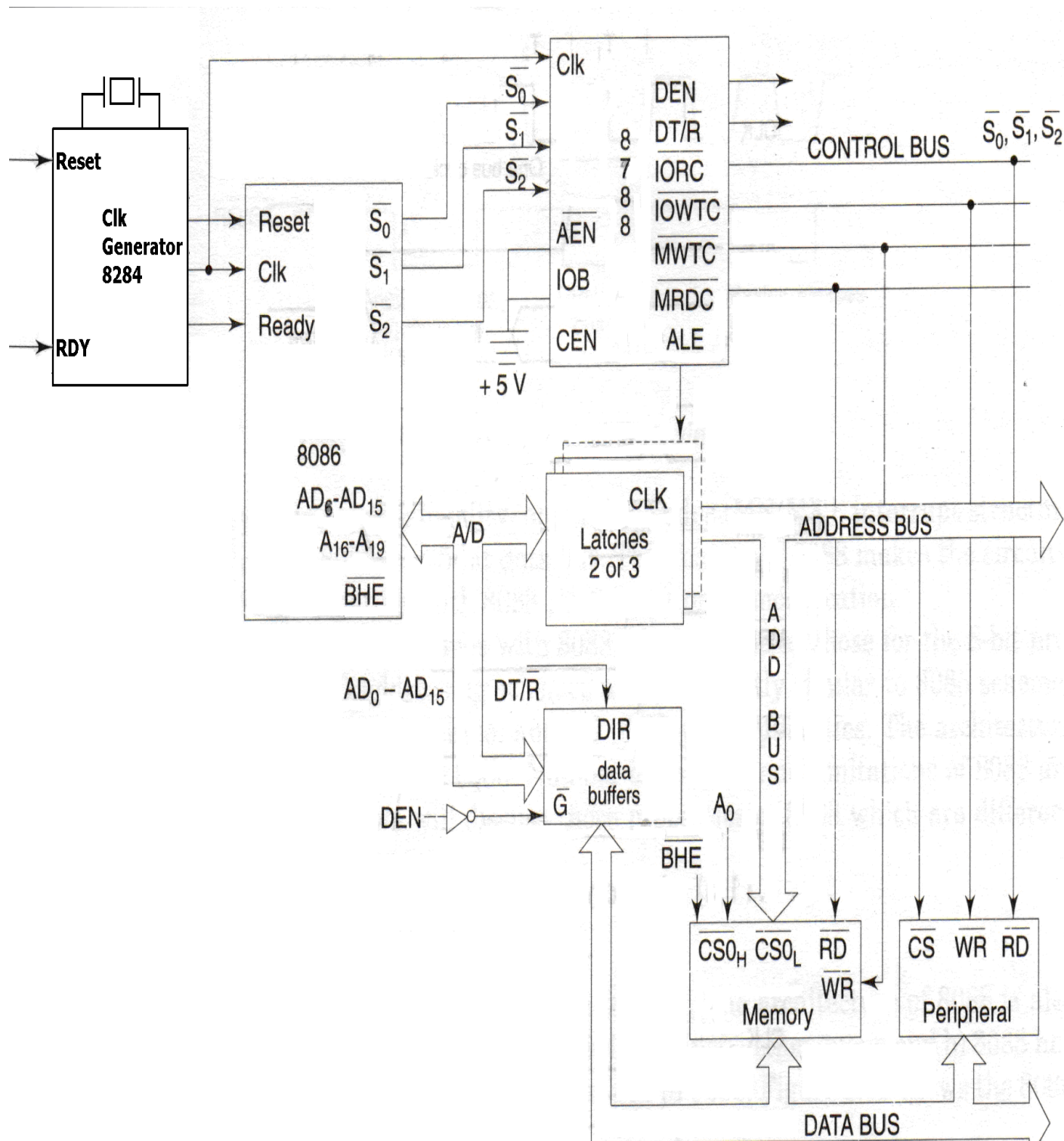
# 'Read' Cycle timing Diagram for Minimum Mode



# 'Write' Cycle timing Diagram for Minimum Mode



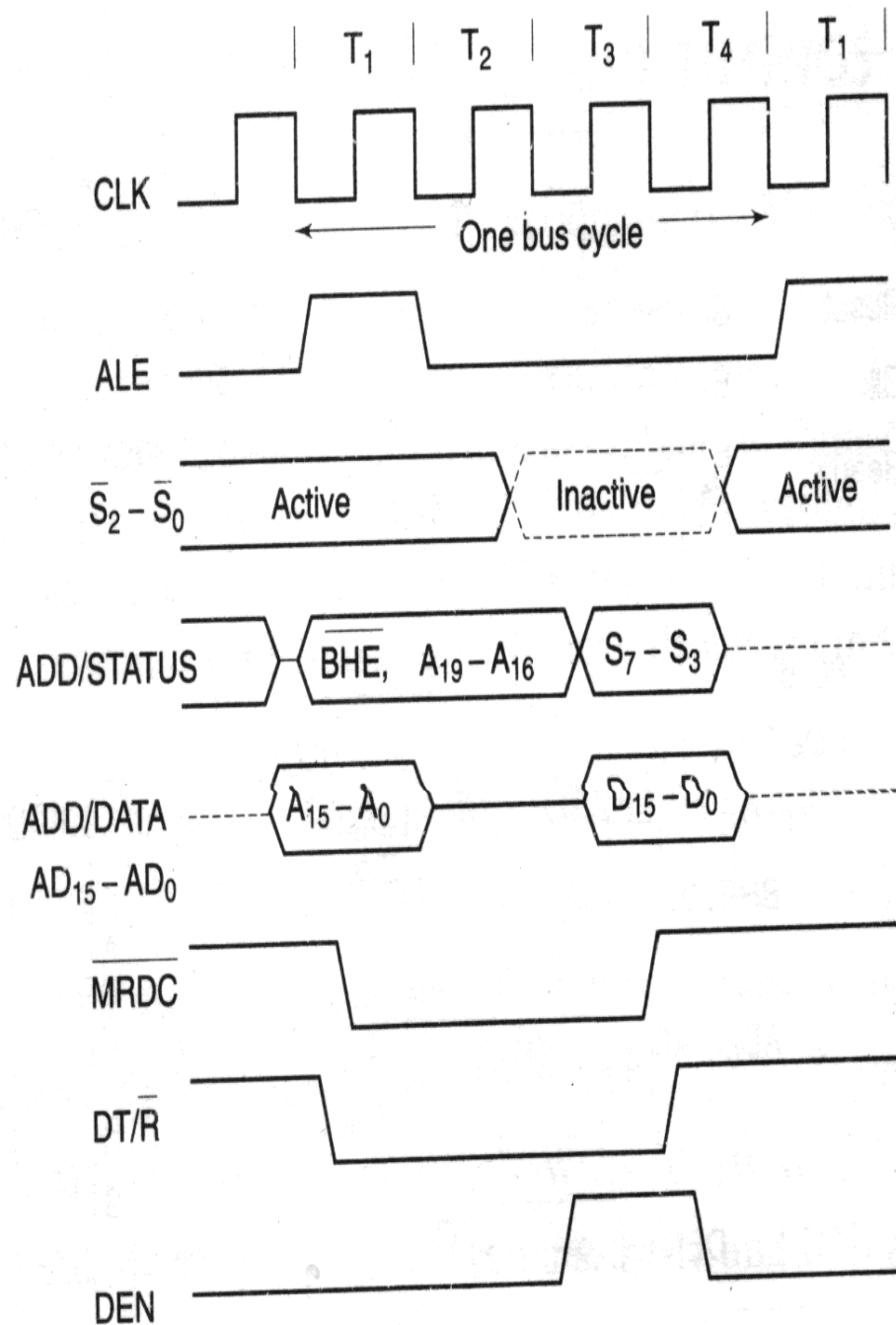
# Maximum Mode 8086 System



# Maximum Mode 8086 System

- Here, either a numeric coprocessor of the type 8087 or another processor is interfaced with 8086.
- The Memory, Address Bus, Data Buses are shared resources between the two processors.
- The control signals for Maximum mode of operation are generated by the Bus Controller chip 8788.
- The three status outputs  $S0^*$ ,  $S1^*$ ,  $S2^*$  from the processor are input to 8788.
- The outputs of the bus controller are the Control Signals, namely  $DEN$ ,  $DT/R^*$ ,  $IORC^*$ ,  $IOWTC^*$ ,  $MWTC^*$ ,  $MRDC^*$ ,  $ALE$  etc.

# Memory Read timing in Maximum Mode

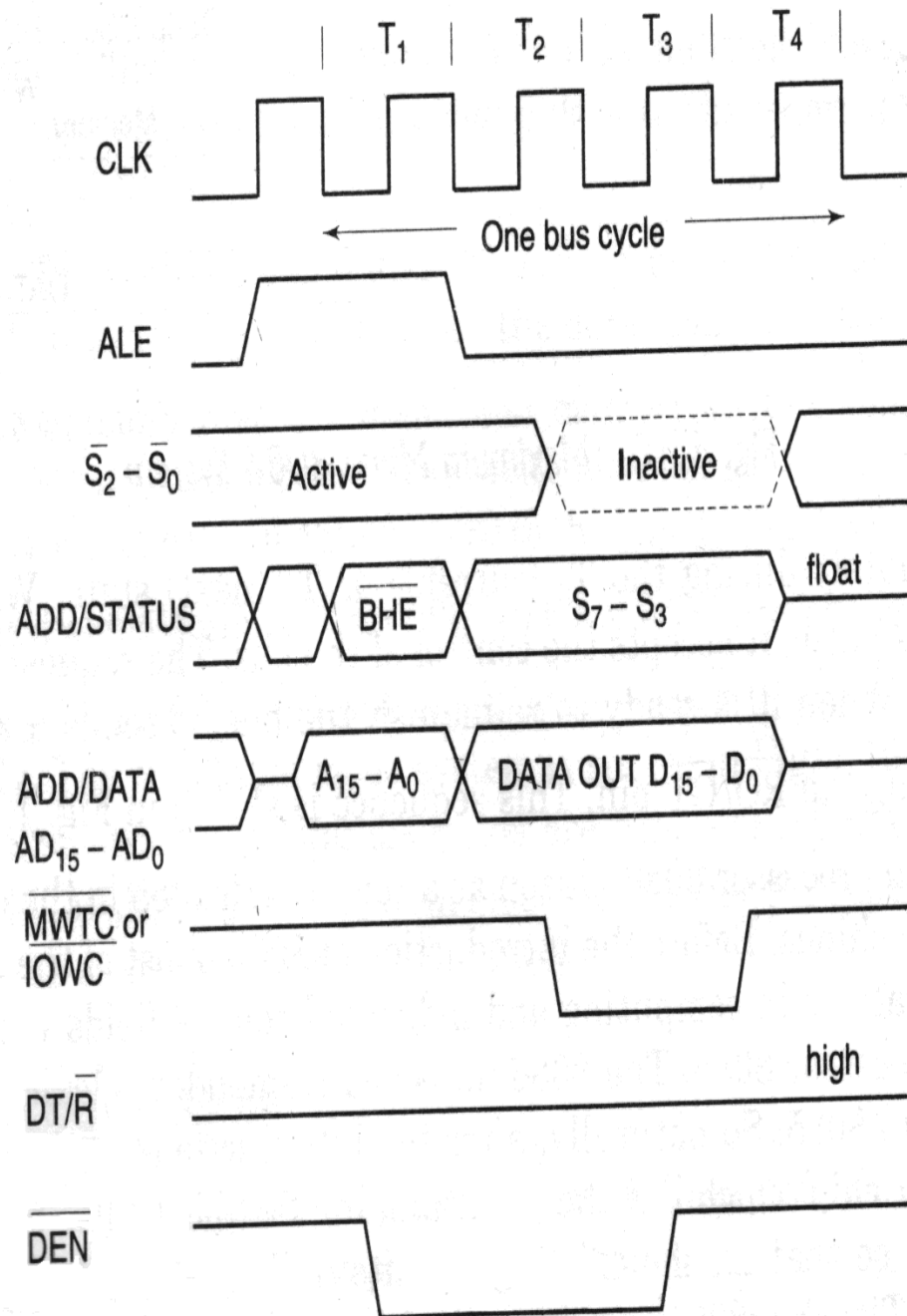


$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	Function
0	0	0	Interrupt acknowledge
0	0	1	I/O read
0	1	0	I/O write
0	1	1	Halt
1	0	0	Opcode fetch
1	0	1	Memory read
1	1	0	Memory write
1	1	1	Passive

**TABLE 8-6** Bus control functions generated by the bus controller (8288) using  $\overline{S_2}$ ,  $\overline{S_1}$ , and  $\overline{S_0}$



# Memory Write timing in Maximum Mode



$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	Function
0	0	0	Interrupt acknowledge
0	0	1	I/O read
0	1	0	I/O write
0	1	1	Halt
1	0	0	Opcode fetch
1	0	1	Memory read
1	1	0	Memory write
1	1	1	Passive

**TABLE 8-6** Bus control functions generated by the bus controller (8288) using  $\overline{S_2}$ ,  $\overline{S_1}$ , and  $\overline{S_0}$



# Check your understanding

- What is the difference between the minimum mode and maximum mode?
- Why do we need a bus controller?

# Summary

- Pin Diagram of 8086
- Minimum mode
- Maximum mode
- Read / write cycle
- System Design

# Reference

- Douglas V Hall, “Microprocessors and Interfacing, Programming and Hardware”, TMH, 2012.

Thank you