INTEL 8086 - Pin Diagram

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AP/CSE

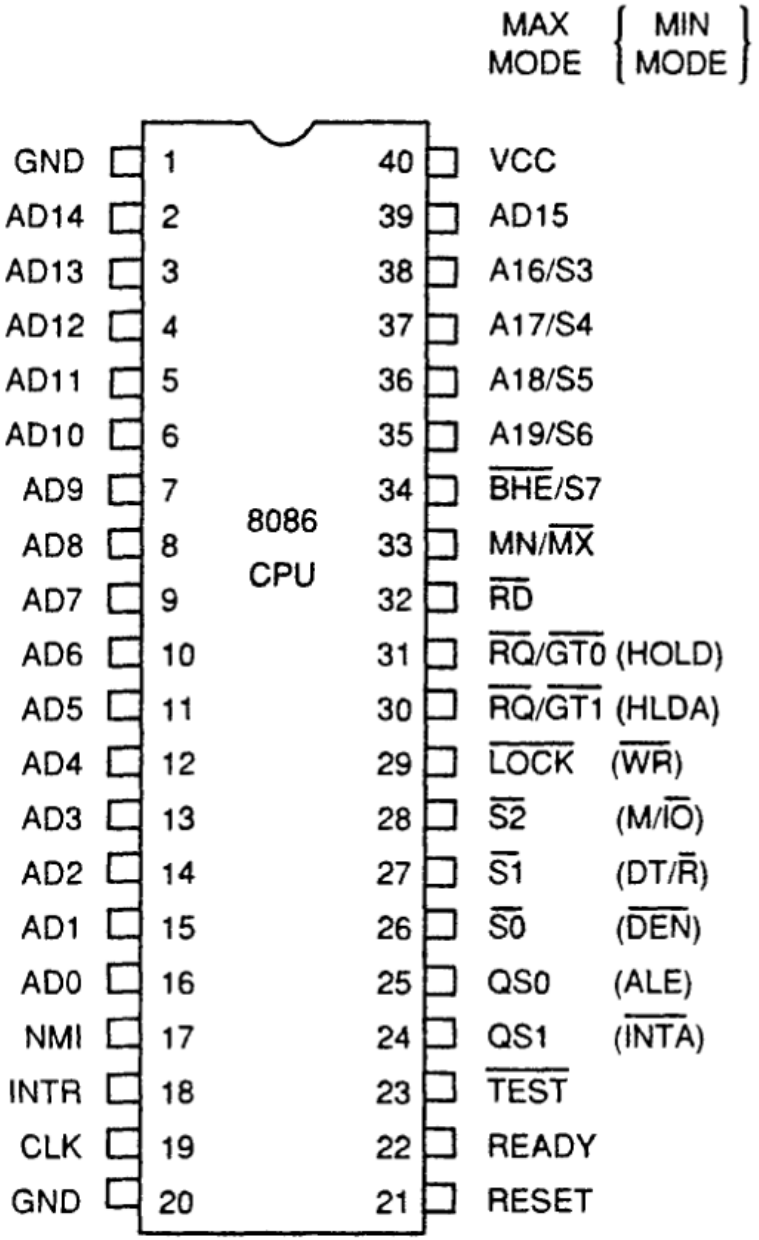
Learning Objective

- To understand the pin details of 8086
- To understand the purpose of each pins.

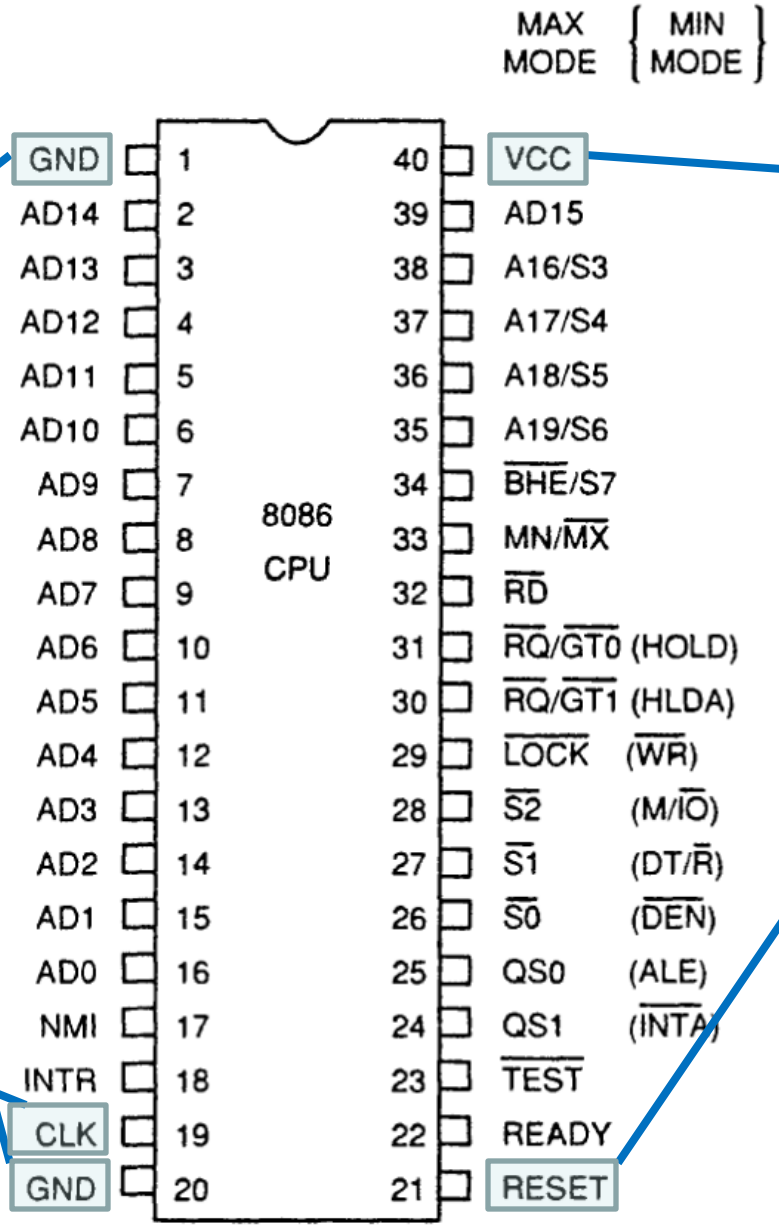
Overview

- Pin Diagram
- Modes of Operation
- Memory bank
- Control signals

INTEL 8086 - Pin Diagram



INTEL 8086 - Pin Details



Ground

Power Supply

5V ± 10%

Clock

Duty cycle: 33%

Reset

Registers, seg regs, flags

CS: FFFFH, IP: 0000H

If high for minimum 4 clks

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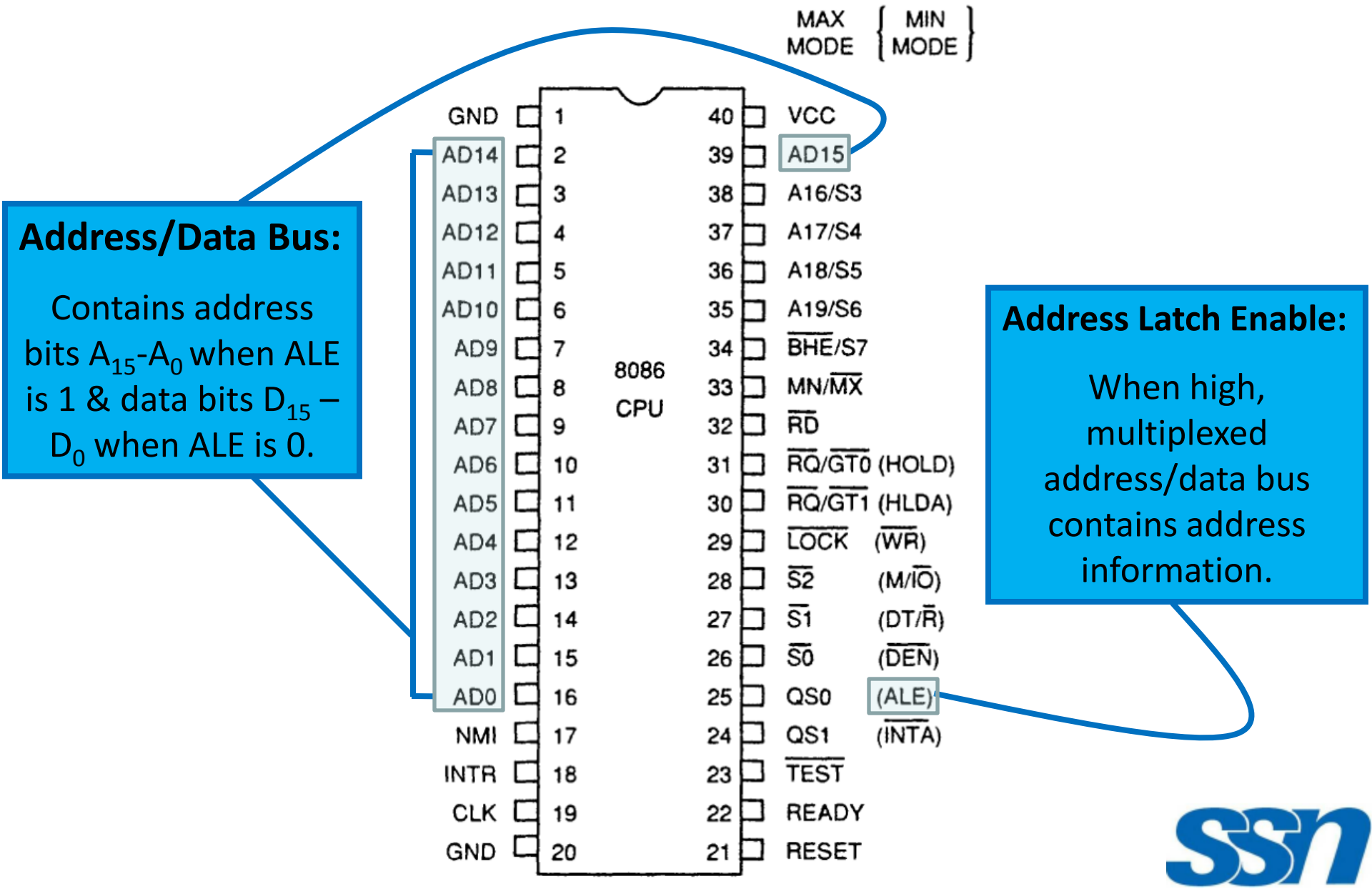

Address/Data Bus:

Contains address bits A_{15}-A_0 when ALE is 1 & data bits D_{15} – D_0 when ALE is 0.

Address Latch Enable:

When high, multiplexed address/data bus contains address information.

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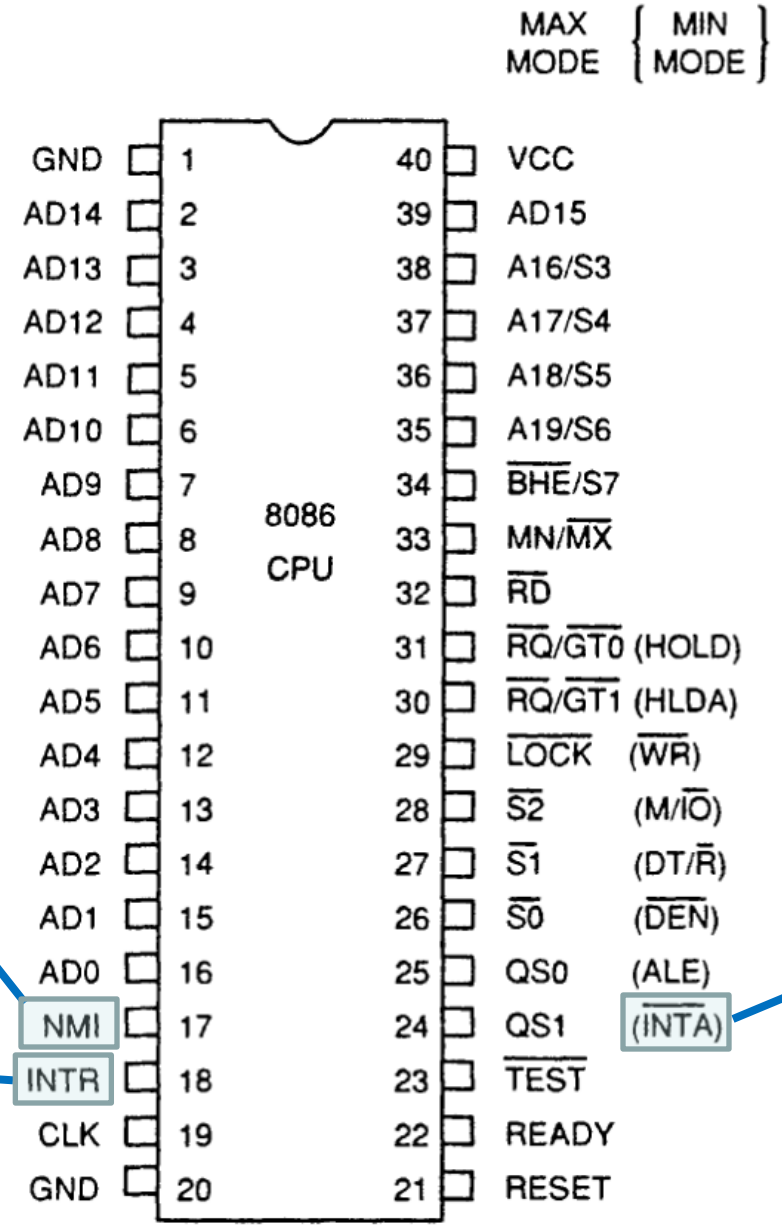
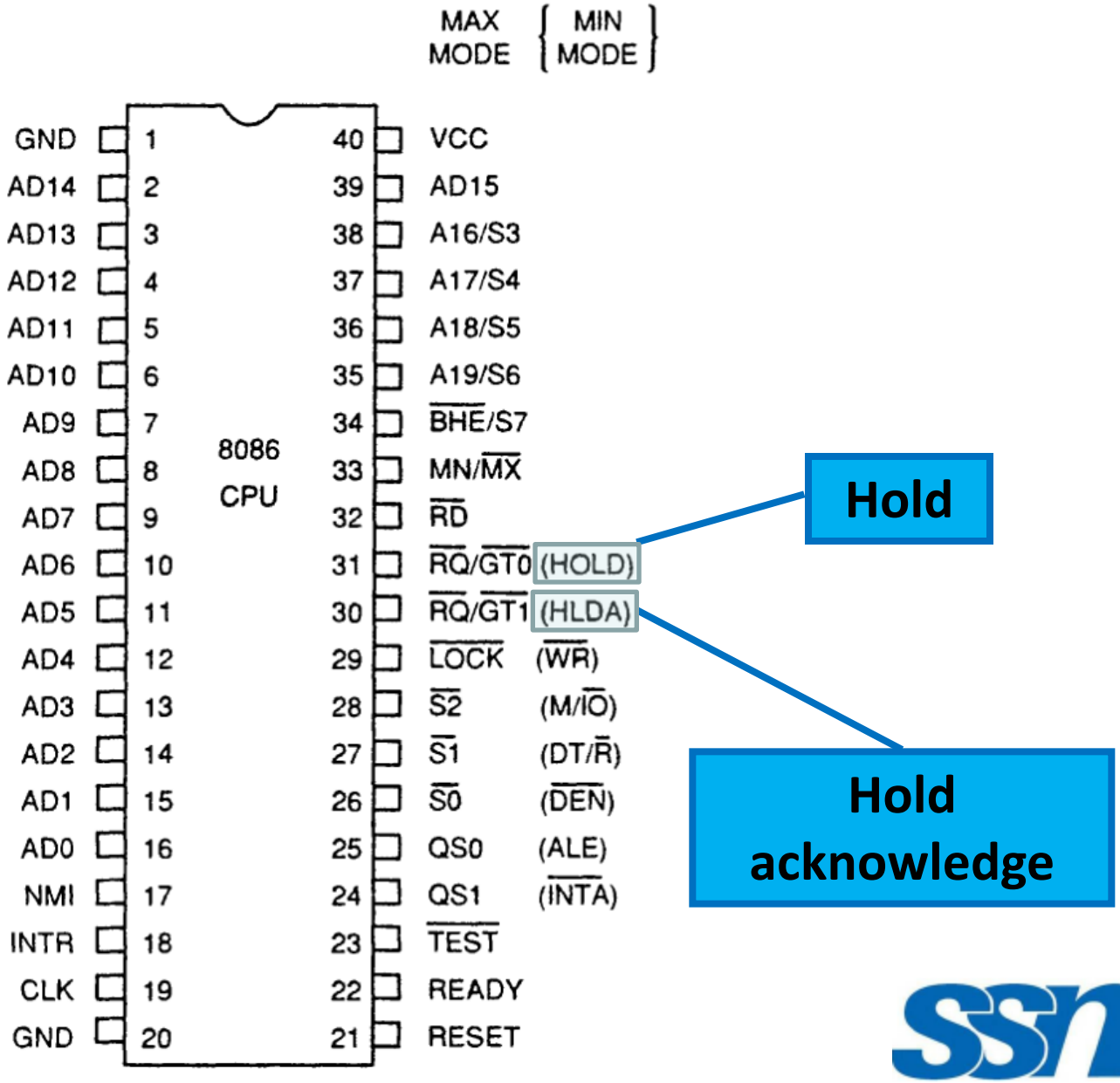


Non - maskable interrupt

Interrupt request

Interrupt acknowledge

INTEL 8086 - Pin Details



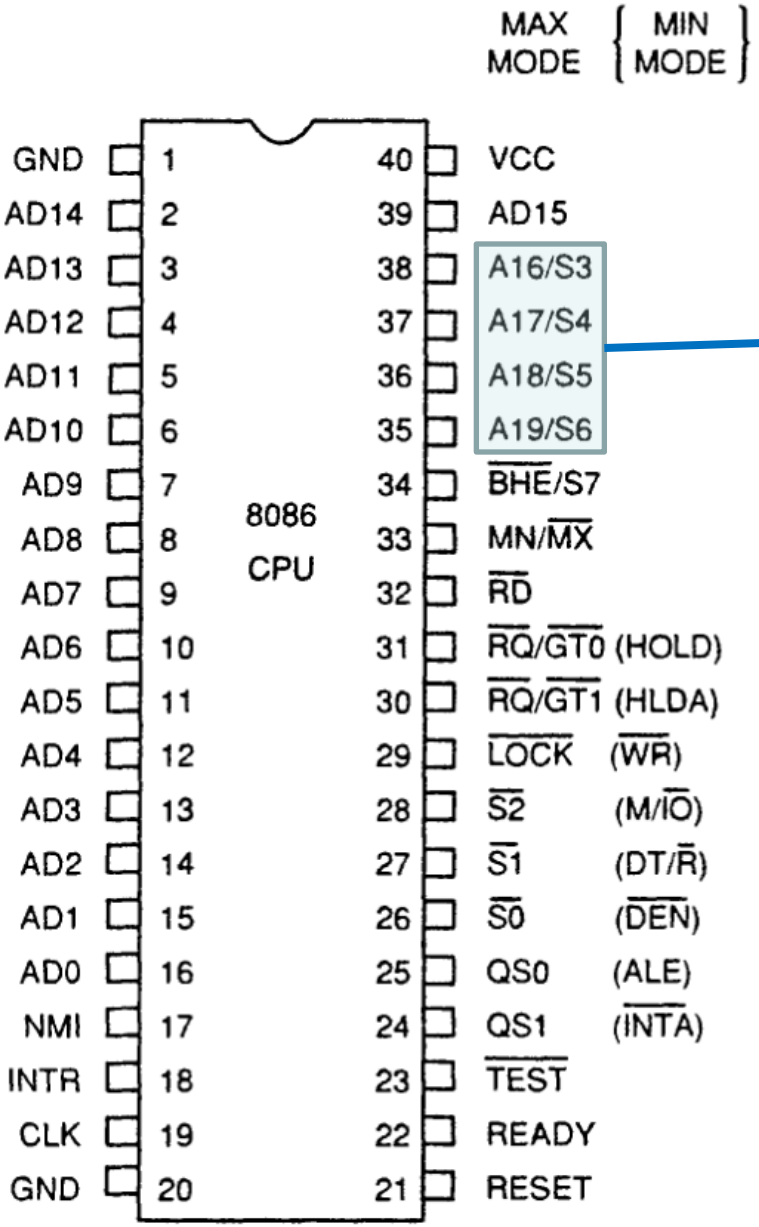
INTEL 8086 - Pin Details

S6: Logic 0.

S5: Indicates condition of IF flag bits.

S4-S3: Indicate which segment is accessed during current bus cycle:

S4	S3	*Function*
0	0	Extra segment
0	1	Stack segment
1	0	Code or no segment
1	1	Data segment



Address/Status Bus

Address bits A_{19} – A_{16} & Status bits S_6 – S_3

INTEL 8086 - Pin Details

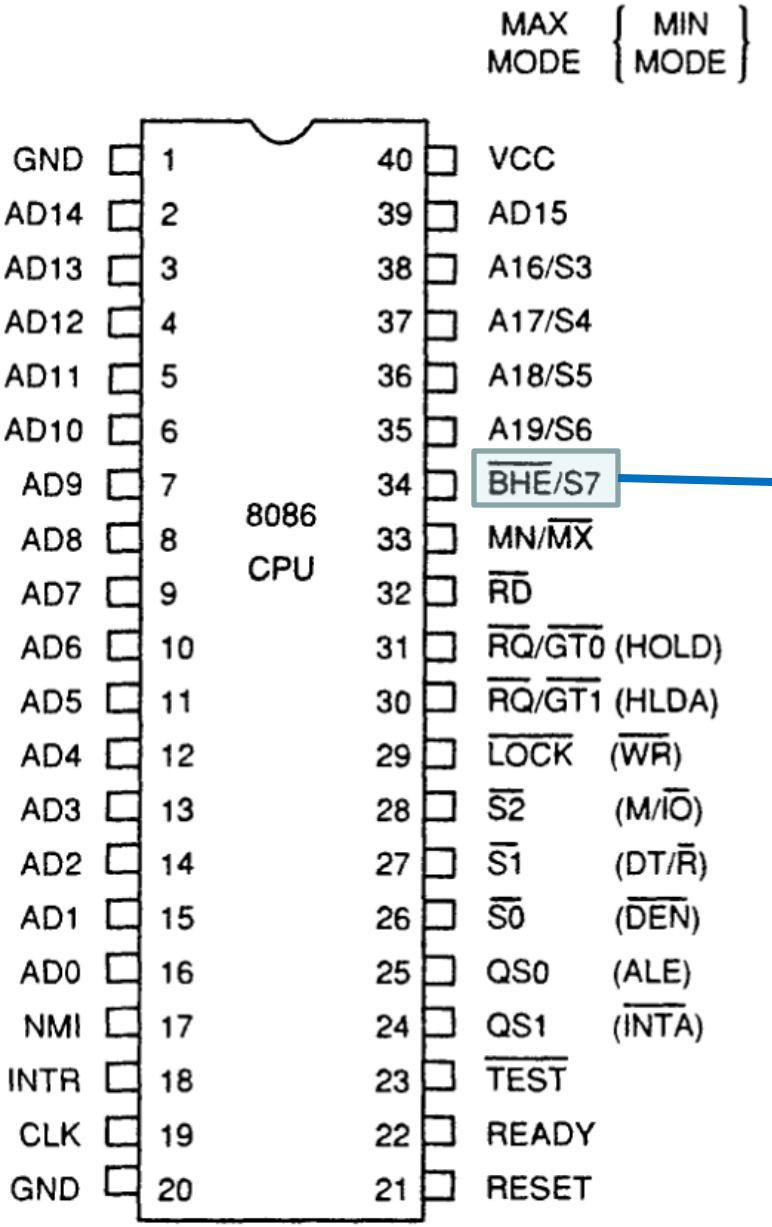
BHE#, A_0:

0,0: Whole word (16-bits)

0,1: High byte to/from odd address

1,0: Low byte to/from even address

1,1: No selection

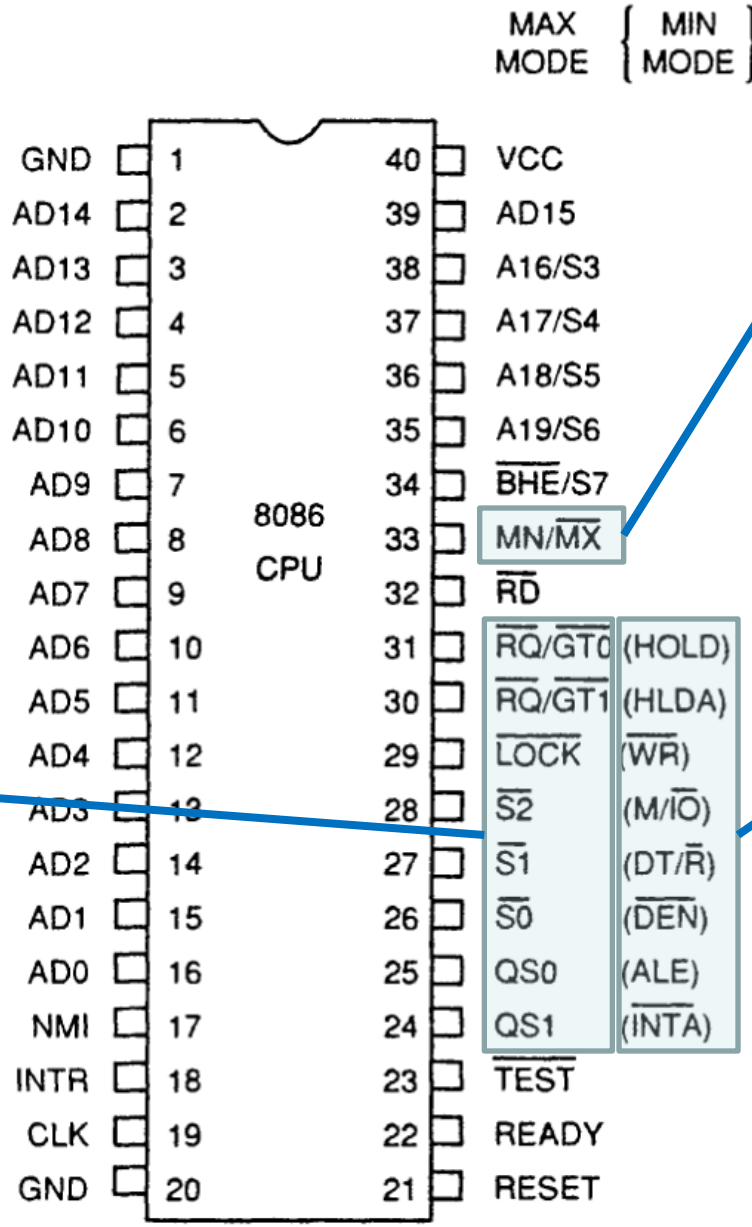


Bus High Enable/S7

Enables most significant data bits $D_{15} – D_8$ during read or write operation.

S_7: Always 1.

INTEL 8086 - Pin Details



Min/Max mode

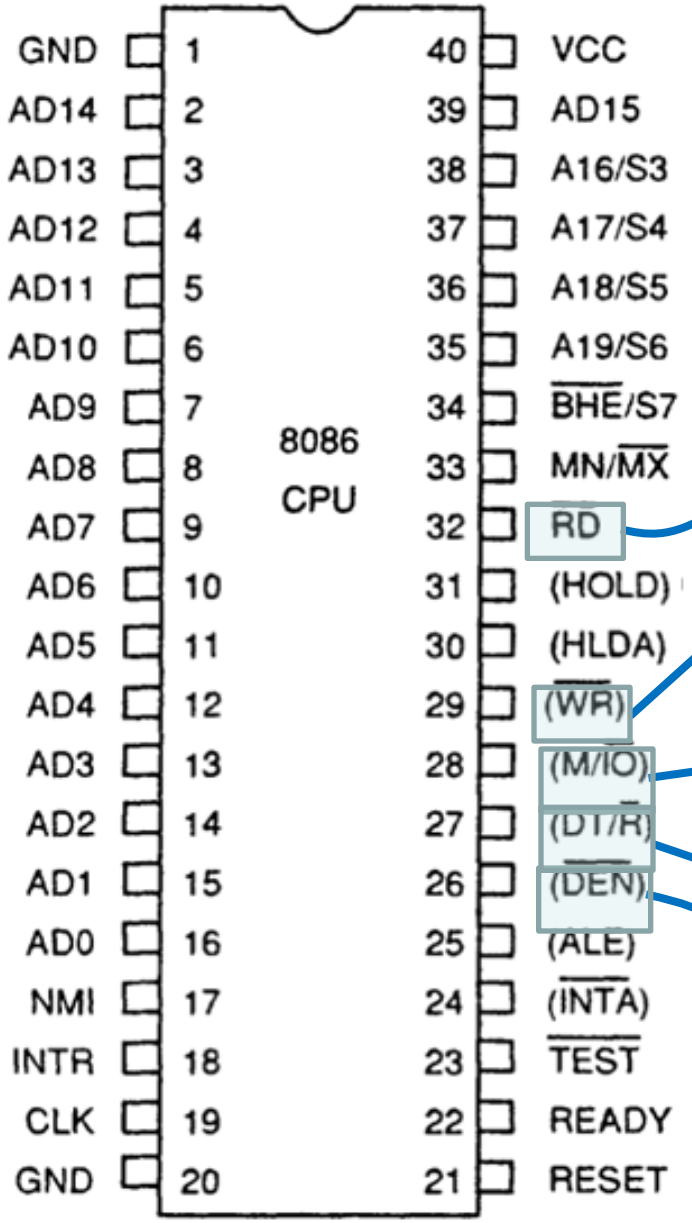
Minimum Mode: +5V

Maximum Mode: 0V

Minimum Mode Pins

Maximum Mode Pins

Minimum Mode- Pin Details



Read Signal

Write Signal

Memory or I/0

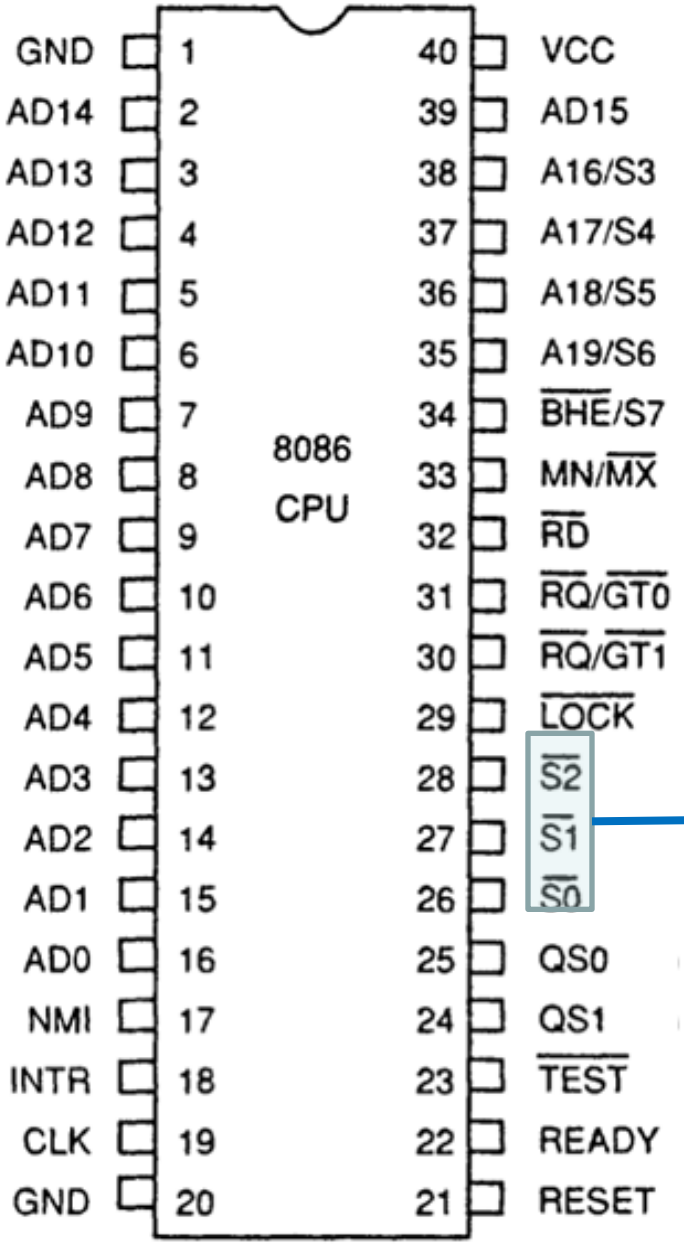
Data Transmit/Receive

Data Bus Enable

Maximum Mode - Pin Details

S2 S1 S0

000: INTA
001: read I/O port
010: write I/O port
011: halt
100: code access
101: read memory
110: write memory
111: none -passive



Status Signal

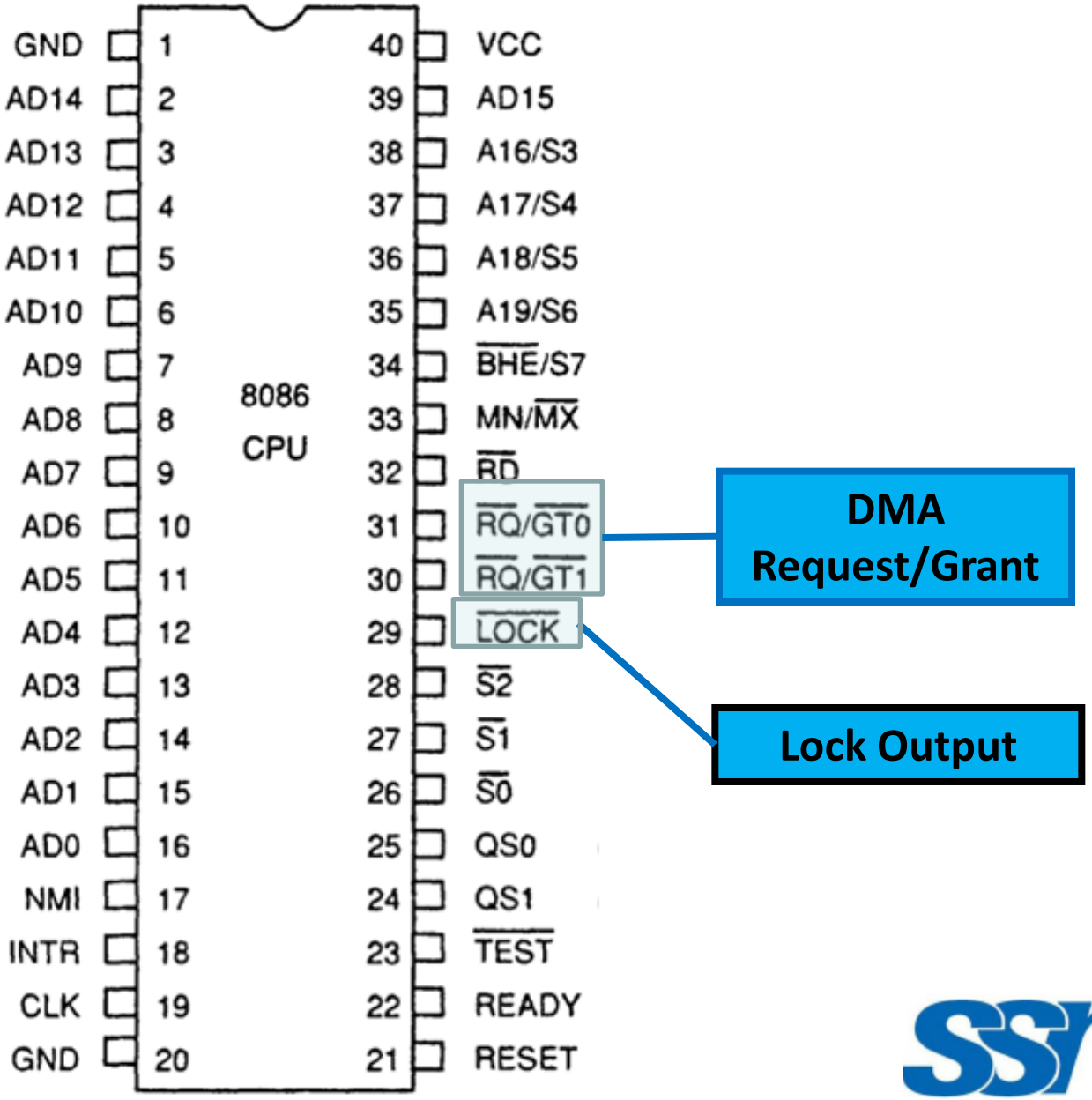
Inputs to 8288 to generate eliminated signals due to max mode.

Maximum Mode - Pin Details

Lock Output

Used to lock peripherals off the system

Activated by using the LOCK: prefix on any instruction



Maximum Mode - Pin Details

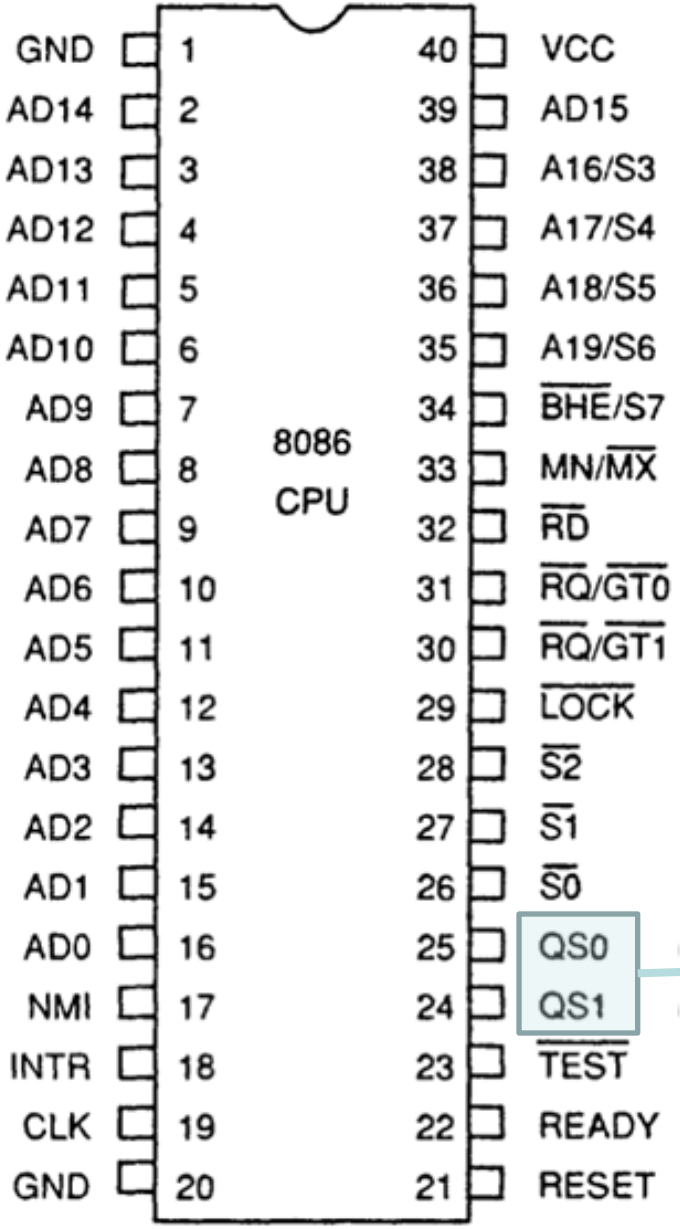
QS1 QS0

00: Queue is idle

01: First byte of opcode

10: Queue is empty

11: Subsequent byte of opcode



Queue Status

Used by numeric coprocessor (8087)

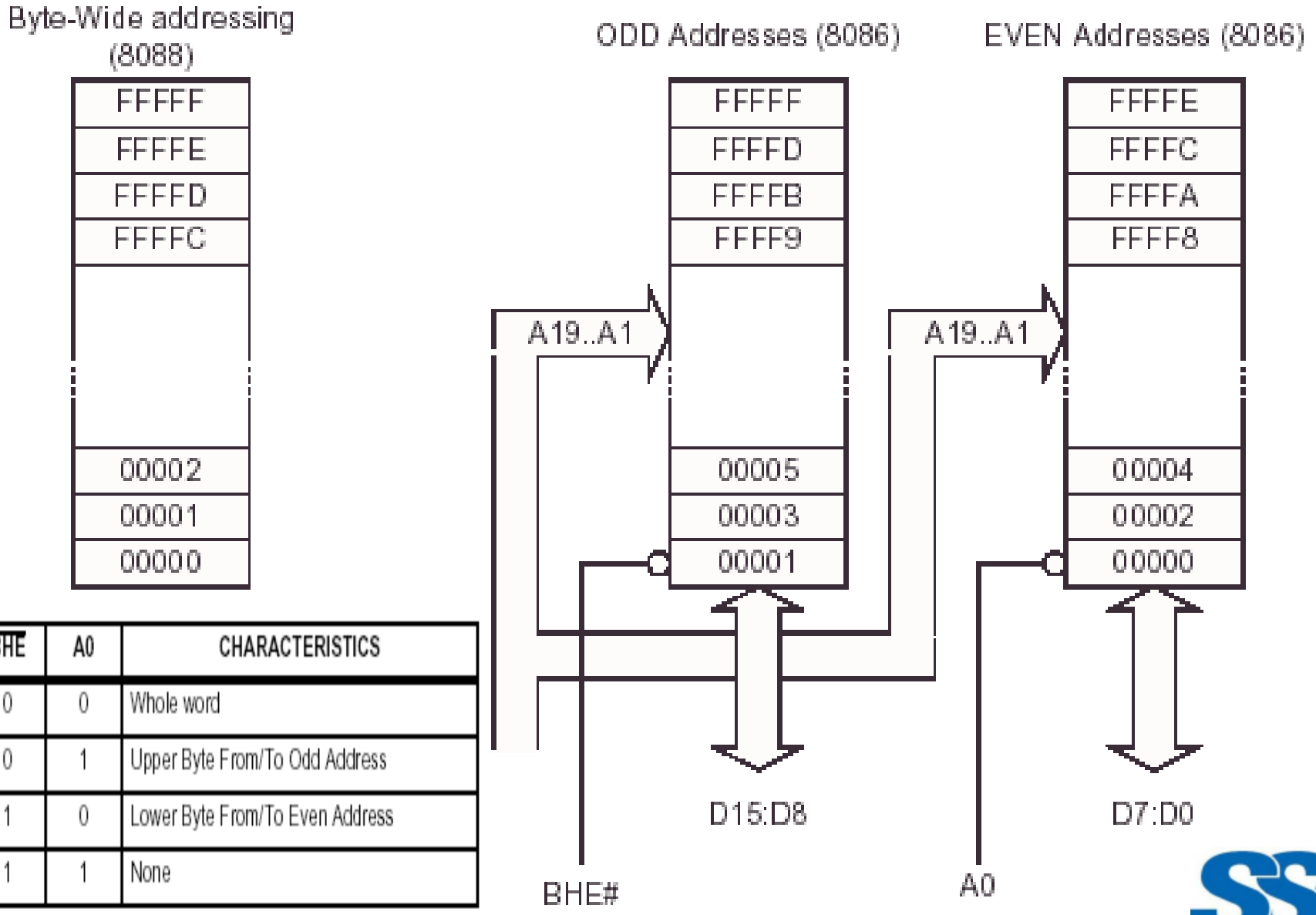
Test

- TEST pin is examined by the "WAIT" instruction.
- If the TEST pin is Low, execution continues.
- Otherwise the processor waits in an "idle" state.
- This input is synchronized internally during each clock cycle on the leading edge of CLK.

Lock

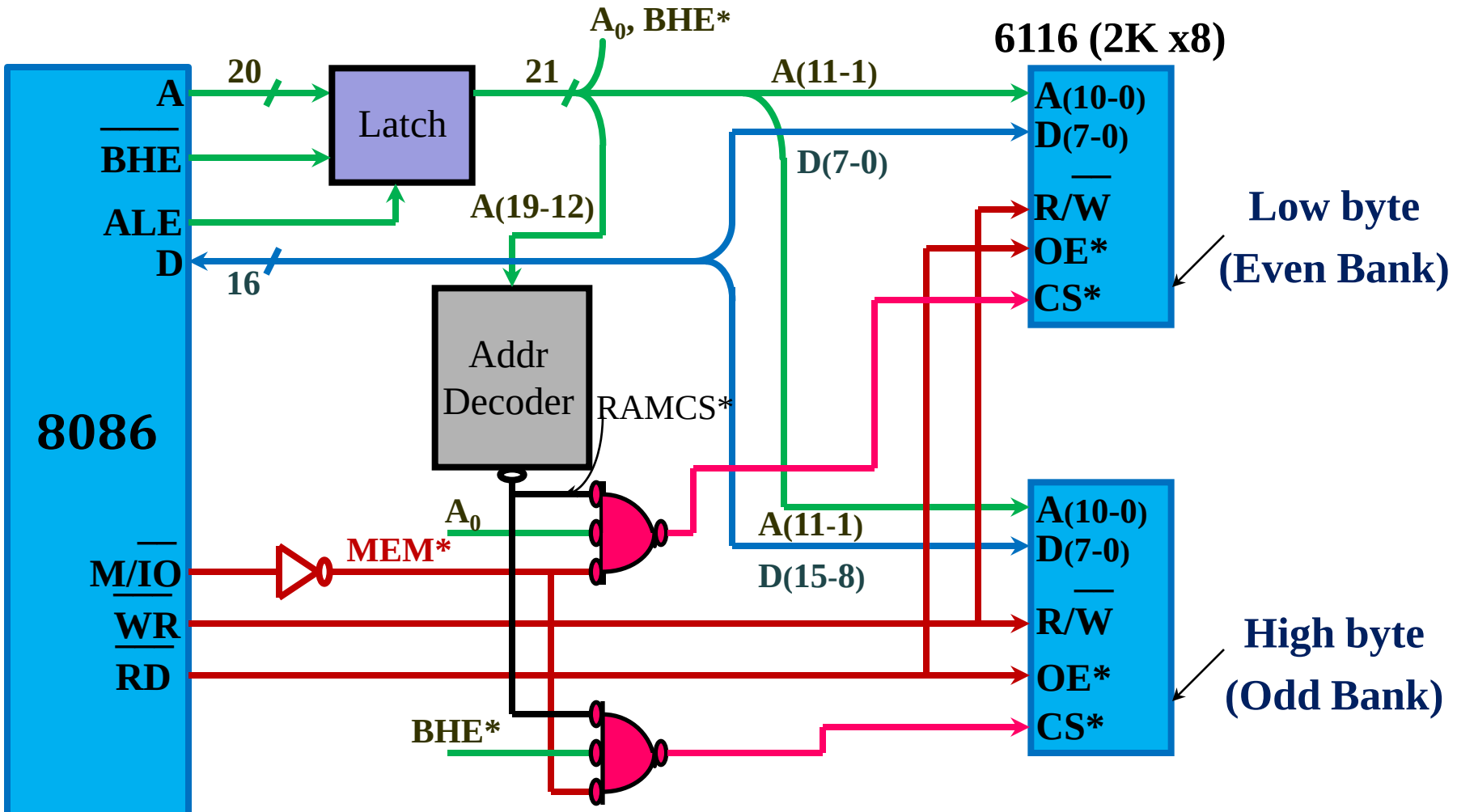
- It indicates to another system bus master, not to gain control of the system bus while LOCK is active Low.
- The LOCK signal is activated by the "LOCK" prefix instruction and remains active until the completion of the instruction.
- This signal is active Low and floats to tri-state OFF during 'hold acknowledge'.

Memory Banking



$\overline{BHE}$	A0	CHARACTERISTICS
0	0	Whole word
0	1	Upper Byte From/To Odd Address
1	0	Lower Byte From/To Even Address
1	1	None

Interface 8086 to 6116 Static RAM



8086 Control Signals

1. ALE
2. BHE
3. M/IO
4. DT/R
5. RD
6. WR
7. DEN

Summary

- Pin Diagram
- Modes of Operation
- Memory bank
- Control signals

Reference

- Doughlas V Hall, “Microprocessors and Interfacing, Programming and Hardware”, TMH, 2012.

Thank you