Saber Mahmoud Saber Mahmoud

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Egyptian | Male | Military Status: Postponed | DOB: 3 March 2002
portfolio

Objective

Dedicated and driven Electronics and Communications Engineering graduate with a passion for digital design and embedded systems. Seeking an opportunity to apply strong theoretical and practical knowledge in digital circuit design, while continuously learning and contributing to innovative engineering solutions in the field of digital systems.

Education

Faculty of Engineering – Cairo University. (2020-2025)
Department of Electronics and Communications.
Last year's Grade: Excellent.
Total years Grade: 83%

Courses and interns:

Digital Design Intern at Si-Vision

Jul 2024 – Oct 2024

• Conducted a literature review on various DMA controller types, architectures and the AXI bus interface

• Designed the architecture for an AXI-4 DMA that supports dynamic arbitration of 32 independent channels.

• Developed the AXI-4 DMA in SystemVerilog, strengthening my RTL design skills, and created a test plan to verify the various transaction scenarios.

• Performed linting with SpyGlass, resolved all violations, and synthesized the design using Design Compiler, refining constraints for improved timing and area efficiency.

Digital Verification Using System Verilog and UVM Under the Supervision of Eng. Kareem Waseem

Aug 2023 – Oct 2023

• Developed a deep understanding of SystemVerilog Datatypes, threading, Interfaces, subroutines.

• Acquired broad knowledge in developing Verification plans, extracting design requirements, and analyzing RTL code coverage results.

• Comprehended functional coverage models implementation and Constrained Random Stimulus generation for simulation-based verification using UVM.

• Mastered UVM structures, components, sequences, configurations, Phasing, TLM, and factory concepts.

• Grasped solid understanding of Object-Oriented Programming, formal verification techniques, assertion development and FPGA-based prototyping, and emulators.

Digital Design using Verilog HDL and FPGA flow using Vivado under supervision of Eng. Kareem Waseem

Jul 2023 - Aug 2023

• Developed a solid understanding of the Digital Design flow involving logic circuit modeling.

• Comprehended Static Linting Checks, Static Timing Analysis (STA) and Clock Domain Crossing (CDC).

• Learned how to Integrate IP cores using the IP Catalog and employ TCL commands to automate the Vivado and QuestaSim workflow.

• Acquired a deep understanding of FPGA-based Prototyping and addressing the Partitioning Challenges as well as the Timing and Physical Design constraints.

Full Embedded Systems Diploma under supervision of Eng/Mohamed Tarek covering:

Basic Concepts of Embedded Systems, C Programming, Data Structures (Linked-List, Stack and Queue), AVR Micro-controllers Interfacing (Implement all the drivers), C For Embedded Applications (Embedded C), Real Time OS(RTOS), Software Engineering, Embedded Tools, HW Labs.

Projects:

-Graduation project Accelerated YOLO-Based computer vision system enhanced with AXI-4 (Mentored by Electronic Research Institute (ERI) and Funded by ITIDA) This project focuses on the design, implementation, and hardware deployment of a pure-FPGA perception system with two main functions: object detection using a YOLO, and lane detection using a streaming edge detection pipeline. The emphasis is placed on minimizing reliance on embedded CPUs, operating systems, or external memory controllers, thereby ensuring full determinism, low latency, and predictable behavior qualities essential for real-time autonomous systems.
The project scope includes:
• Training and exporting a 4-bit quantized TinyYOLOv3 model.
• Compiling the model into a hardware accelerator using the FINN framework.
• Creating a custom Verilog-based post-processing module for binary object detection.
• Implementing a complete lane detection pipeline using classical methods in Verilog HDL.
• Integrating environmental sensors (light and temperature) via I²C and FSM-based control units.
• Synthesizing and deploying the complete system on ZCU102 and prototyping sub-systems on PYNQ-Z2 platforms.
• Evaluating performance through simulation, synthesis reports, and hardware testbench verification.

My Contributions
Designed and implemented a custom, hardware-friendly lane detection algorithm in System Verilog that accurately determines the number of lanes and current lane boundaries from a streaming Sobel binary image (processed row-by-row). Unlike computationally heavy methods like the Hough Transform, this solution is tailored for real-time FPGA deployment, achieving over 99% accuracy in practical test cases and a throughput of 2400 FPS, which is approximately 240× faster than its software counterpart.
Fully implemented the complete RTL lane detection pipeline including RGB-to-grayscale conversion, averaging filter, Sobel edge detection, buffering, edge analysis, and lane classification.
Developed a Temperature Control Unit to control the air conditioning system based on environmental input, using FSM design principles.
Verified the Light Control Unit and Temperature Control Unit using System Verilog Assertions (SVA) for robust functional and formal validation.
Actively participated in hardware debugging, ensuring signal-level correctness and timing closure during deployment on ZCU102 and PYNQ-Z2 boards.

- Design and Verification for Ultrasonic System A shared repository between Software, Embedded, and FPGA teams to handle sending and receiving ultrasonic waves from the appropriate transducers. The project is based on the Xilinx Zynq-7000 board.

My Contributions
strongly participating in the top module UVM environment developing along with the stimulus generation. Verification of the system decoder using SV and SVA. Design of the receiving block in the control unit besides the storage RAM for the same block.

-Design 32PointFFT: Designed a 32-point FFT using Cooley-Tukey Radix-2 DIT algorithm; implemented modular 2-point butterfly units in Verilog; verified via ModelSim, synthesized on FPGA using Vivado with pipelined architecture for low-latency performance.

UVM Verification of SPI Wrapper with Dual Port RAM Integration| Digital Verification Project
• Created a class-based SystemVerilog testbench for a FIFO and for an SPI-Slave connected to Dual-port RAM utilizing constraint randomization, SVA and functional and code coverage.
• Developed a complete top-level UVM environment for the SPI-Slave connected to Dual-port RAM

-**Designed and developed my personal portfolio website** to showcase my projects, skills, and achievements.

Technical Skills and tools

-Verilog -System Verilog -VHDL -SVA -UVM -Questa Sim. -Vivado -embedded C -Proteus -Questa Sim -Matlab

-JavaScript Fundamentals -Node.js

Activities

-Participated in the 7th Engineering Mathematics Research Day Forum, this research project was an incredibly rewarding experience, spanning approximately 80 days from initiation to the results presentation. It significantly enhanced my understanding of inverse kinematics, algorithm design, and robotic motion control. The process sharpened my skills in scientific research, mathematical modeling, and practical problem-solving, culminating in a deeper appreciation of kinematics' applications in robotics and automation.

Skills

- Excellent English -Self Motivated -Active Team Member -Leadership Skills -Presentation Proficiency -Sociable