Saber Mahmoud Saber Mahmoud

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Objective

Dedicated and driven Electronics and Communications Engineering graduate with a passion for digital design and embedded systems. Seeking an opportunity to apply strong theoretical and practical knowledge in digital circuit design, while continuously learning and contributing to innovative engineering solutions in the field of digital systems.

Education

Faculty of Engineering – Cairo University. (2020-2025)
Department of Electronics and Communications.
Last year's Grade: Excellent.
Total years Grade: 83%

Courses and interns:

SI-Vision Internship (2.5 months, Full-Time):

Completed a full-time internship at SI-Vision, including on-site sessions in a professional working environment. Accessed SI-Vision Academy and company servers, used SpyGlass for linting. Worked on a DMA project with an AXI4 interface under the supervision of a digital team leader and two senior engineers, culminating in a final presentation discussing the project's implementation and outcomes.

Digital Verification Diploma under the supervision of Eng/Kareem Waseem covering:

Fundamentals of System Verilog and System Verilog Assertions, interpreting coverage reports, building constraint blocks, simulating the design on Questa Sim, OOP basics, UVM structure and introduction to formal verification.

Digital Design Diploma under the supervision of Eng/Kareem Waseem covering:

Essential basics of Verilog HDL, Digital design flow, practicing testbench construction, design simulation on Model Sim, FPGA flow using Vivado tool, introduction to STA, metastability and some CDC solving techniques.

Full Embedded Systems Diploma under supervision of Eng/Mohamed Tarek covering:

Basic Concepts of Embedded Systems, C Programming, Data Structures (Linked-List, Stack and Queue), AVR Micro-controllers Interfacing (Implement all the drivers), C For Embedded Applications (Embedded C), Real Time OS(RTOS), Software Engineering, Embedded Tools, HW Labs.

Projects:

-Graduation project Accelerated YOLO-Based computer vision system enhanced with AXI-4 (Mentored by Electronic Research Institute (ERI) and Funded by ITIDA) This project focuses on the design, implementation, and hardware deployment of a pure-FPGA perception system with two main functions: object detection using a YOLO, and lane detection using a streaming edge detection pipeline. The emphasis is placed on minimizing reliance on embedded CPUs, operating systems, or external memory controllers, thereby ensuring full determinism, low latency, and predictable behavior qualities essential for real-time autonomous systems.
The project scope includes:
• Training and exporting a 4-bit quantized TinyYOLOv3 model.
• Compiling the model into a hardware accelerator using the FINN framework.
• Creating a custom Verilog-based post-processing module for binary object detection.
• Implementing a complete lane detection pipeline using classical methods in Verilog HDL.
• Integrating environmental sensors (light and temperature) via I²C and FSM-based control units.
• Synthesizing and deploying the complete system on ZCU102 and prototyping sub-systems on PYNQ-Z2 platforms.
• Evaluating performance through simulation, synthesis reports, and hardware testbench verification.
My Contributions Designed and implemented a custom, hardware-friendly lane detection algorithm in SystemVerilog that accurately determines the number of lanes and current lane boundaries from a streaming Sobel binary image (row-by-row input). Unlike computationally heavy methods like the Hough Transform, this algorithm is optimized for real-time FPGA deployment and delivers over 99% accuracy in practical test cases.

Fully implemented the entire lane detection system, including buffering, edge analysis, and lane classification.
Developed the Temperature Control Unit to control the air conditioning system based on environmental input, using FSM design principles.
Verified the Light Control Unit and Temperature Control Unit using SystemVerilog Assertions (SVA) for robust functional and formal validation.
Actively participated in hardware debugging, ensuring signal-level correctness and timing closure during deployment on ZCU102 and PYNQ-Z2 boards.

-**Design and verification for a Direct Memory Access (DMA)** controller which is a specialized hardware component that allows for efficient data transfers between different memory locations or between a peripheral device and memory without the involvement of the CPU, the design includes priority mechanism and much more. (check my portfolio).
-**Design Lane Detection System:** Designed a complete RTL lane detection system that processes road images through RGB-to-grayscale conversion, averaging filter, Sobel edge detection, and decision logic to identify lane count, boundaries, and current lane position.
- Design and Verification for Ultrasonic System I have contributed in an ultrasonic-zynq based-system with strongly participating in the top module UVM environment developing along with the stimulus generation. Verification of the system decoder using SV and SVA. Design of the receiving block in the control unit besides the storage RAM for the same block. The waveforms were generated using QuestaSim.
-Design 32PointFFT: Designed a 32-point FFT using Cooley-Tukey Radix-2 DIT algorithm; implemented modular 2-point butterfly units in Verilog; verified via ModelSim, synthesized on FPGA using Vivado with pipelined architecture for low-latency performance.
-**Designed UART protocol** Designed and implemented a UART module using Verilog/SystemVerilog, including transmitter/receiver modules, baud rate generation, and error detection, verified through simulation.
-Designed SPI slave connected with single port RAM using Verilog.
-Developed a complete UVM environment for verifying SPI slave connected with single port Ram.
-Verified SPI Slave connected with single port RAM using System Verilog.
-**Designed DSP48A1 in Spartan 6 FPGA with some extra logic** using Verilog.
-**verified SPI Slave using UVM environment** I have built a complete UVM environment for verifying SPI_Slave with a single port RAM. I have also designed the golden model for checking the output with it. The waveforms and the UVM packages were used through Questa Sim tool.
-**Developed a comprehensive smart car system integrating multiple subsystems**, including lighting control, parking assistance.
-**Implemented Distance Measuring and Displaying System** by Atmega 32 MC.
-**Developed a motor temperature monitoring system** using microcontroller-based design, which continuously tracks and monitors the temperature of motors in real-time.
-**Developed a secure door locking system using a microcontroller**, featuring password-based authentication for access control.
-**Developed a vehicle control system** using a microcontroller to manage various vehicle functions
-**Designed and developed my personal portfolio website** to showcase my projects, skills, and achievements.
-**Developed a Telegram bot to help me with managing my faculty tables** using the node-telegram-bot-api library, along with Express for a simple web server, and SQLite for database management. The bot can handle various commands related to schedules, lab sessions, deadlines, exams.

Technical Skills

-Verilog/System Verilog -SVA -UVM -Model Sim/Questa Sim. -FPGA flow by Vivado tool -FPGA -C/C++

-VHDL -Embedded Systems interfacing -Proteus -Visual Studio -Multisim -MATLAB

-MS office-JavaScript Fundamentals -SQLite -Node.js -React.js -Express.js

-Telegram Bot API -CSS Basics -Deployment and Hosting -HTML Basics -JavaScript Fundamentals

Activities

-Participated in the 7th Engineering Mathematics Research Day Forum, this research project was an incredibly rewarding experience, spanning approximately 80 days from initiation to the results presentation. It significantly enhanced my understanding of inverse kinematics, algorithm design, and robotic motion control. The process sharpened my skills in scientific research, mathematical modeling, and practical problem-solving, culminating in a deeper appreciation of kinematics' applications in robotics and automation.

-**Participated in the 8th Engineering Mathematics Research Day Forum**, Veinmatics-our team-project title was "Mathematical Modeling and Diagnosis of Atherosclerosis". Conducted an in-depth study on the causes and diagnosis of atherosclerosis, focusing on mathematical modeling to predict and analyze plaque buildup in arterial walls.

Skills

-Self Motivated **-Active Team Member** **-Leadership Skills** **-Good Speaker**

-Presentation Skills **-Sociable**

Languages

-Arabic: Native

-English: Good

Personal Information

- Date of Birth: 3, Mar 2002
- Gender: Male.
- Nationality: Egyptian.
- Military Status: Postponed.