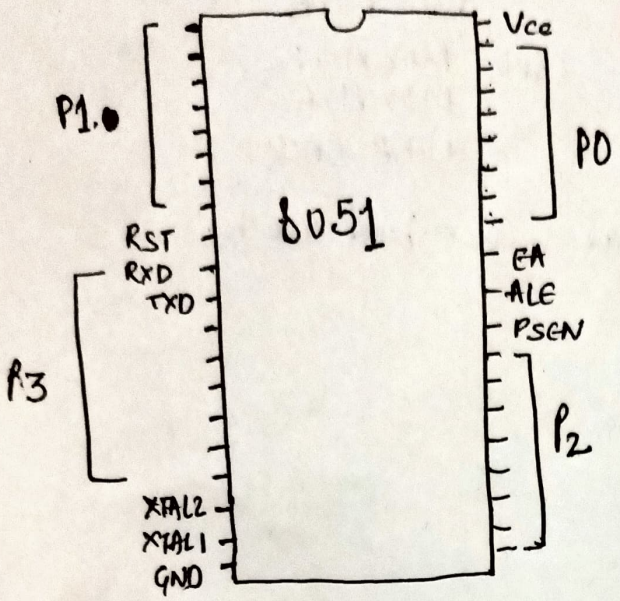
Input-Output-Programming



Port-0

This port need pull-up resister because of open drain.

Port-0 as output-(Toggle)

```
BACK: MOV A,#55H
      MOV P0,A
      ACALL DELAY
      MOV A,#0AAH
      MOV P0,A
      ACALL DELAY
      SJMP HERE BACK
```

> Port 0 as input

```
MOV A,#0FFH
MOV P0,A
BACK: MOV A,P0   ← input
      MOV P1,A
      SJMP BACK
```

- It can use as both address and data bus OR will combine with Port-2 to make 16 bit address.

Port-1

- MOV Port-1 as an output (Toggle)

```
      MOV A,#55H
BACK: MOV P1,A
      ACALL DELAY
      CPL A
      SJMP BACK
```

Port 1 as Input:

```
MOV A,#0FFH
MOV P1,A
MOV A,P1
MOV R7,A
ACALL DELAY
MOV A,P1
MOV R6,A
ACALL DELAY
MOV A,P1
MOV R5,A.
```

Part-2 Toggling all bits

```
    MOV A,#55H
BACK: MOV P2, A
      ACALL DELAY
      CPL A
      SJMP BACK
```

Part-3 Data Input

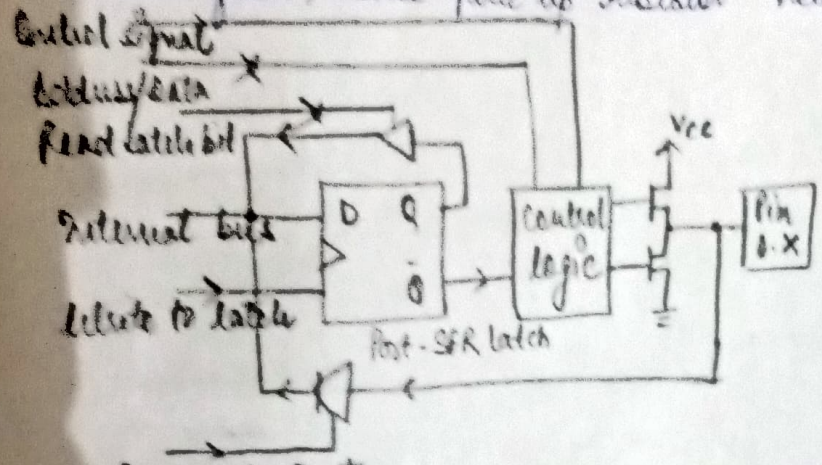
```
    MOV A, #0FFH
    MOV P2,A
BACK: MOV A, P2
      MOV P1,A
      SJMP BACK.
```

It is commonly used as other bits mask.

pin	fnc
P3.0	RXD
P3.1	TXD
P3.2	$\overline{INT0}$
P3.3	$\overline{INT1}$
P3.4	T0
P3.5	T1
P3.6	$\overline{WR}$
P3.7	$\overline{RD}$

PORT-0

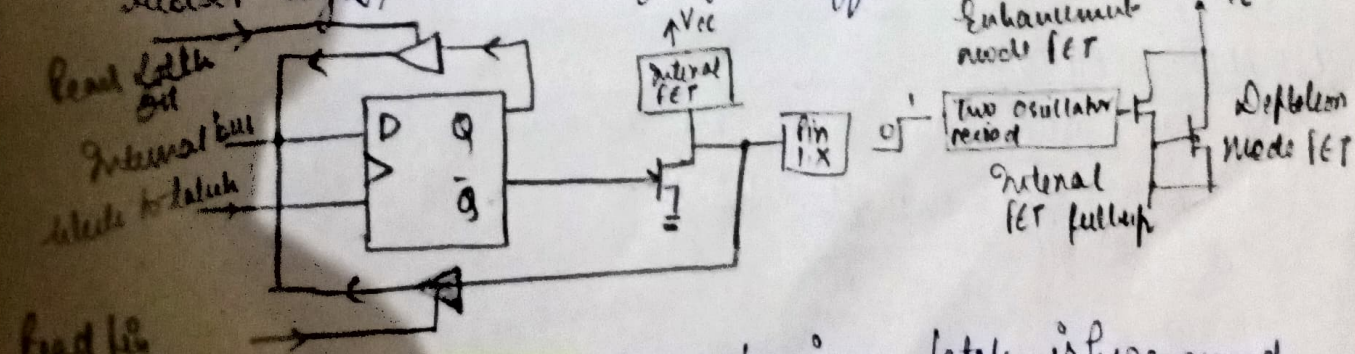
> When used as **Input**, 1 must be written by the program to the corresponding 0 latch by the program, must turning both the transistor off and then it will be connected to input buffer.
> When used as **output**, then pin latches will program to be 0. will turn on the transistor all latches that are program to 1 still float, hence pull up resistor needed.



> When it is used as **address bus**, upper fet will turn on & lower fet off to provide logic high at that pin
> & upper off & lower on to give low logic at that pin
> After address has been formed & latched into external circuit by address latch Enable (ALE), the bus will become **Data bus**
> Port-0 now reads data by external memory.

PORT-1

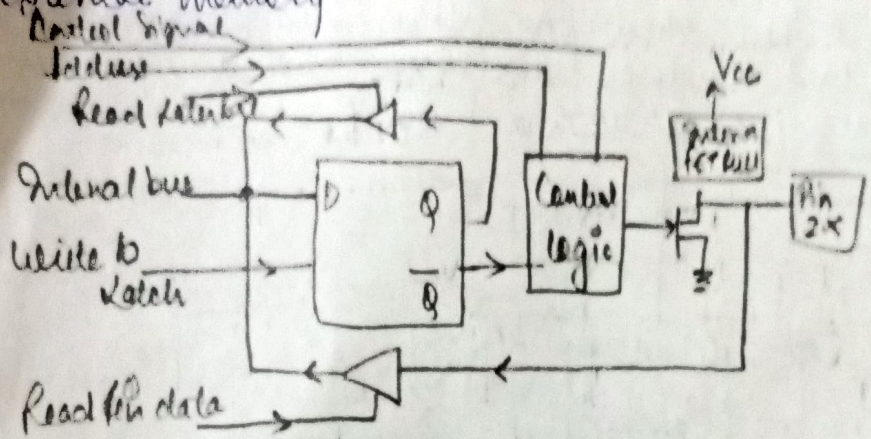
> When used as **input**, 1 is written by the program to the latch, turning lower fet off, which will get internal pull up resistor high, hence it will go from buffer.



> When used as **output**, lower fet is on, latch is programmed to 0, the pullup is off & the pin can drive the input of the external circuit low.

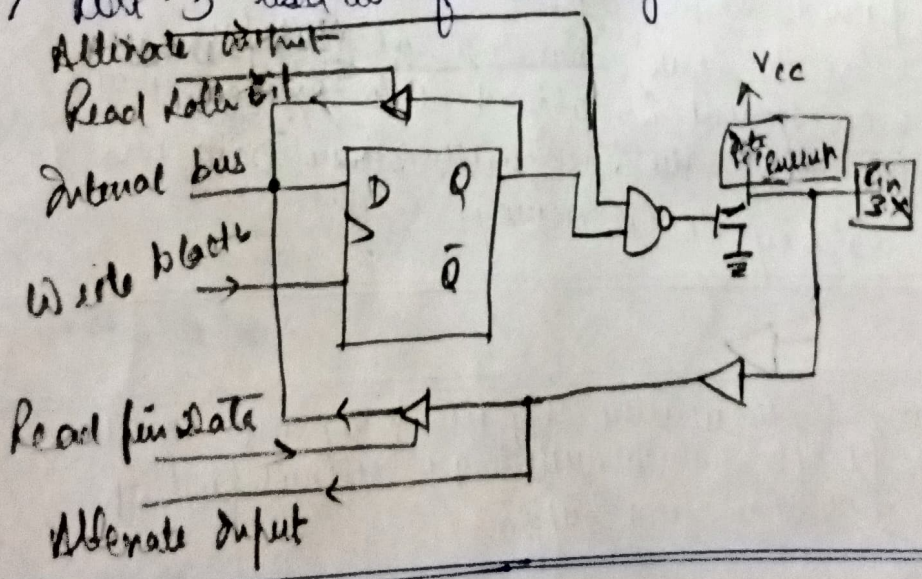
PORT-2

- Input / output func is same as port-1
- Alternate use need 16 bit address, use used with port-0 because of external memory.



PORT-3

- Input / Output func is similar as port-1
- Port-3 used as for other signals also



P3 bit	func
P3.0	RXD
P3.1	TXD
P3.2	$\overline{INT0}$
P3.3	$\overline{INT1}$
P3.4	T0
P3.5	T1
P3.6	$\overline{WR}$
P3.7	$\overline{RD}$

BIT ADDRESSEBILITY

- We can alter any single bit without touching rest using "SET X.Y' ↙ port ↘ bit, example P1.5

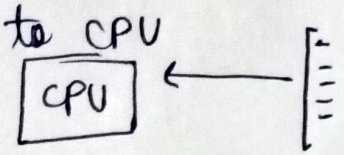
Read Input pins Vs port latch.

Reading port

Read the status of the Input pin

To make bit of any Input port we must write 1 to that bit.

Only some instruction used to get the external data at the pins to CPU



Read the internal latch of the output port

Some Instruction read the content of Internal port latch,

- The instruction reads the internal latch of the port and bring the data in CPU
- This data is AND with content of A
- the result rewritten back to port latch.
- the port pin data is changed & now has the same value as port latch

~~ANL~~	Px	ANL P1, A
ORL	Px	ORL P2, A
XRL	Px	XRL P0, A
JBC	PX.4, Target	JBC P1.1, TArget
CPL	PX.4	CPL P1.2
INC	Px	INC P1
DGC	Px	DGC P2
DJNZ	PX.4, Taeget	DJNZ P1, TARGET
MOV	PX.4, C	MOV P1.2, C
CLR	PX.4	CLR P2.3
SETB	PX.4	SETB P2.3

Latch.

Read-modify-write feature (reading the port & modifying value)

pin → latch port → CPU (operation with Accum) → Latch port → pin

Let suppose all pins are turn high means no current will come out but we want to ~~for reset~~ get output from.

P1.2 & P1.3

```
MOV A, #0xFF    11111111
ANL A, #0x9F    11001111
MOV P1, A
```