PROJECT REPORT

UNIVERSAL SYNCHRONOUS DECADE COUNTER

OBJECTIVE: -

To make a universal synchronous counter using Flip Flops.

ABSTRACT: -

The ICs used as counters are available in market, but if want to make a counter of mode 100 using two synchronous counters of mode 10 connected in cascade, it will not work because we have to apply clock pulse at same instant to both counters. Hence it will be a failure.

Our aim is to make a universal synchronous counter connected in cascade, for example we have two synchronous counters connected in cascade it will be counter of mode 100. And if we connect it with another synchronous counter it will be a mode 1000 counter which is a good thing.

APPARATUS: -

- AND gate (7408)
- J-K Flip-Flops (IC7473)
- LEDs
- 7-Segment Display
- BCD to 7-segment decoder (74LS47)
- MUX (74151)
- Resistors
- Buttons
- Jumper wires

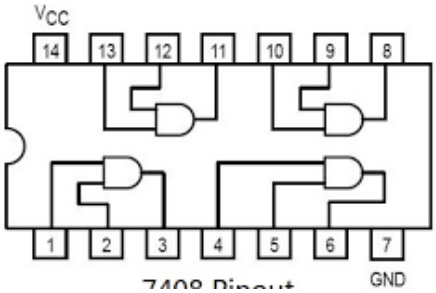

Figure 1: 7408 AND gate

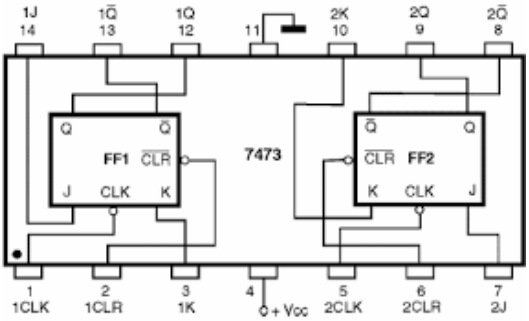

Figure 2: 7473 jk Flip-Flop

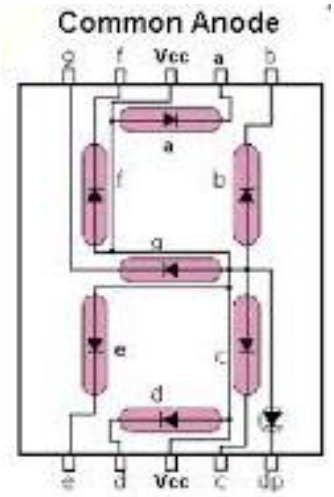

Figure 3: Common anode 7 Segment

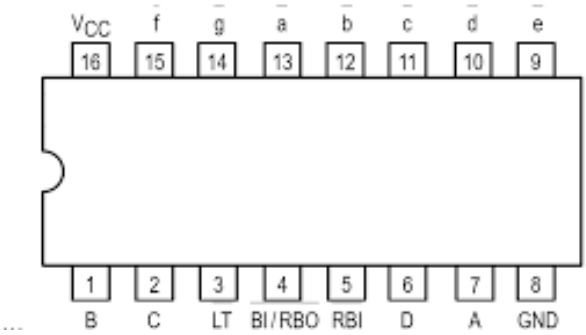

Figure 4: 7447 BCD Decoder

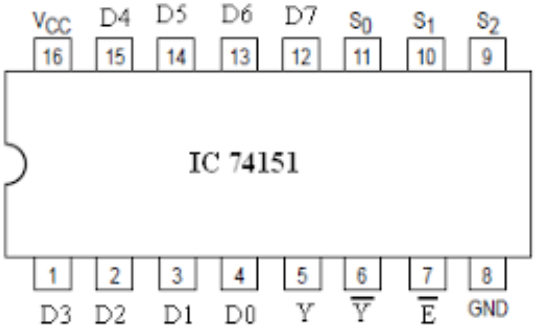

Figure 5: 74151 Multiplexer

LOGIC: -

The aim is that we have to make a synchronous decade counter using flip flops and combinational circuits. Master slave negative edge triggered j-k flip flops are used, we are using j-k flip flops due to the toggling ability of j-k flip flops. We can use them as T-flip flops by short circuiting the j and k inputs.

Now we have added a pin named “M” it mean mode if the pin “M” is 0 it will count up and if pin is HIGH or 1 it will count down. And the state diagram of the BCD up down counter is simple as shown below: -

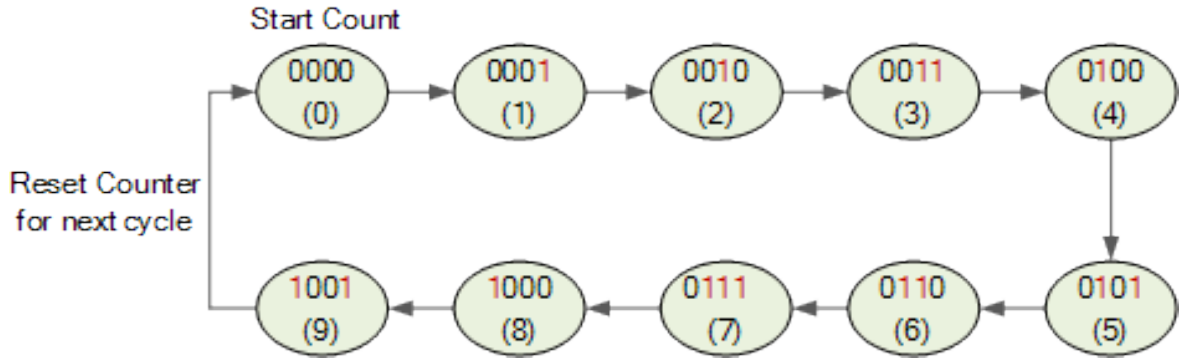

Figure 6: State diagram of BCD up counter

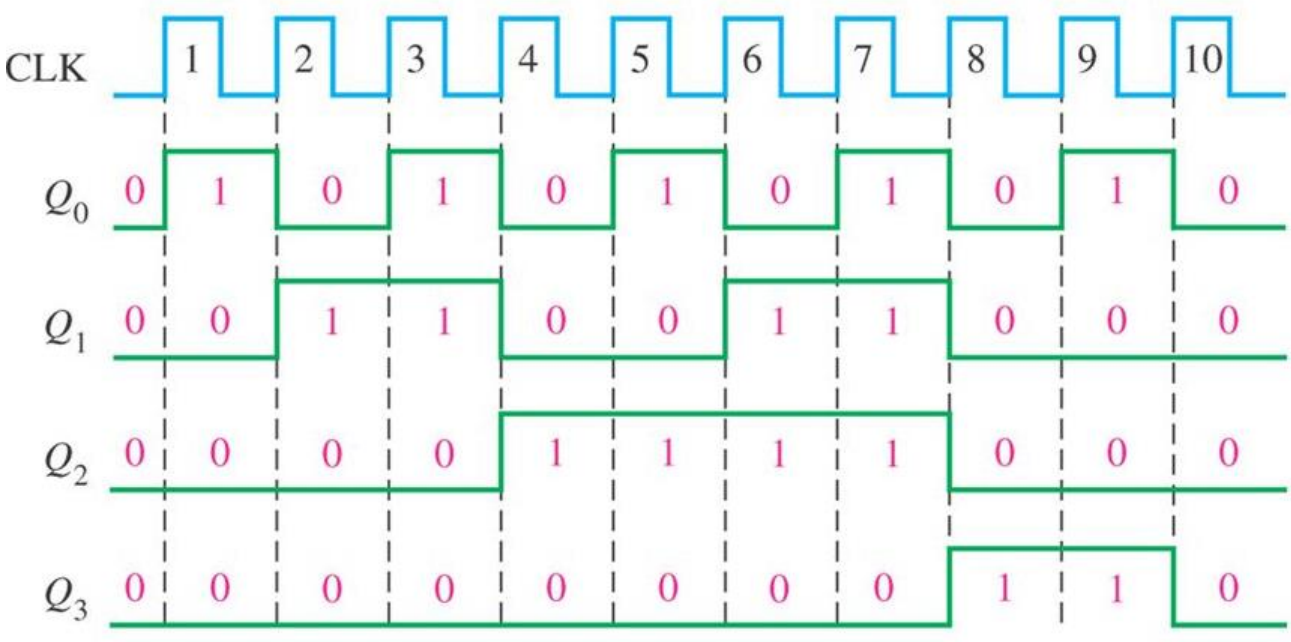

Figure 7: Timing Diagram of BCD up counter

The above diagram if timing diagram for decade up counter, here when a clock pulse is changing from low to high it counts the clock pulse and shown the output in binary form, every clock pulse if given to the other j-k flip flop which will change its state when previous on changed the state.

It can be called as a universal counter because when we cascade two counters using and OR gate then there will be such conditions that when precious counter approaches 9 and after that to 0 then next one counts to 1 and so on to 2. Thus, it can count to 99 in a synchronous manner, thus by cascading two counter we can make 100 mode counter and cascading of three counters will give a counter of mode 1000 and will count from 0 to 999.

Truth table used for the logic is sown below: -

Selection	Previous States				Next States				Flip Flop Inputs			
M	Q4	Q3	Q2	Q1	Q4*	Q3*	Q2*	Q1*	T4	T3	T2	T1
0	0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	1	0	0	1	0	0	0	1	1
0	0	0	1	0	0	0	1	1	0	0	0	1
0	0	0	1	1	0	1	0	0	0	1	1	1
0	0	1	0	0	0	1	0	1	0	0	0	1
0	0	1	0	1	0	1	1	0	0	0	1	1
0	0	1	1	0	0	1	1	1	0	0	0	1
0	0	1	1	1	1	0	0	0	1	1	1	1
0	1	0	0	0	1	0	0	1	0	0	0	1
0	1	0	0	1	0	0	0	0	1	0	0	1
0	1	0	1	0	x	x	x	x	x	x	x	x
0	1	0	1	1	x	x	x	x	x	x	x	x
0	1	1	0	0	x	x	x	x	x	x	x	x
0	1	1	0	1	x	x	x	x	x	x	x	x
0	1	1	1	0	x	x	x	x	x	x	x	x
0	1	1	1	1	x	x	x	x	x	x	x	x
1	0	0	0	0	1	0	0	1	1	0	0	1
1	0	0	0	1	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0	1	0	0	1	1
1	0	0	1	1	0	0	1	0	0	0	0	1
1	0	1	0	0	0	0	1	1	0	1	1	1
1	0	1	0	1	0	1	0	0	0	0	0	1
1	0	1	1	0	0	1	0	1	0	0	1	1
1	0	1	1	1	0	1	1	0	0	0	0	1
1	1	0	0	0	0	1	1	1	1	1	1	1
1	1	0	0	1	1	0	0	0	0	0	0	1
1	1	0	1	0	x	x	x	x	x	x	x	x
1	1	0	1	1	x	x	x	x	x	x	x	x
1	1	1	0	0	x	x	x	x	x	x	x	x
1	1	1	0	1	x	x	x	x	x	x	x	x
1	1	1	1	0	x	x	x	x	x	x	x	x
1	1	1	1	1	x	x	x	x	x	x	x	x

Here Q4, Q3, Q2 and Q1 are previous states of flip flops, M is selection pin for mode selection, Q4*, Q3*, Q2*, Q1* are next states of the flip flop based on the inputs T4, T3, T2 and T1.

Don’t care “X” are used for 4-bit numbers not included in BCD and the outputs not required in circuit.

By reduction method we found the following expressions for the counter circuit,

$$T_4 = \overline{M}Q_4Q_1 + \overline{M}Q_3Q_2Q_1 + M\overline{Q_3}\,\overline{Q_2}\,\overline{Q_1}$$

$$T_3 = \overline{M}Q_2Q_1 + MQ_3\overline{Q_2}\,\overline{Q_1} + MQ_D\,\overline{Q_2}\,\overline{Q_1}$$

$$T_2 = M\overline{Q_4}Q_1 + MQ_3\overline{Q_1} + MQ_D\,\overline{Q_1}$$

$$T_1 = \overline{M}\,\overline{Q_4}Q_1 + MQ_2\overline{Q_1} + MQ_3\,\overline{Q_1} + MQ_D\overline{Q_1}$$

CIRCUIT: -

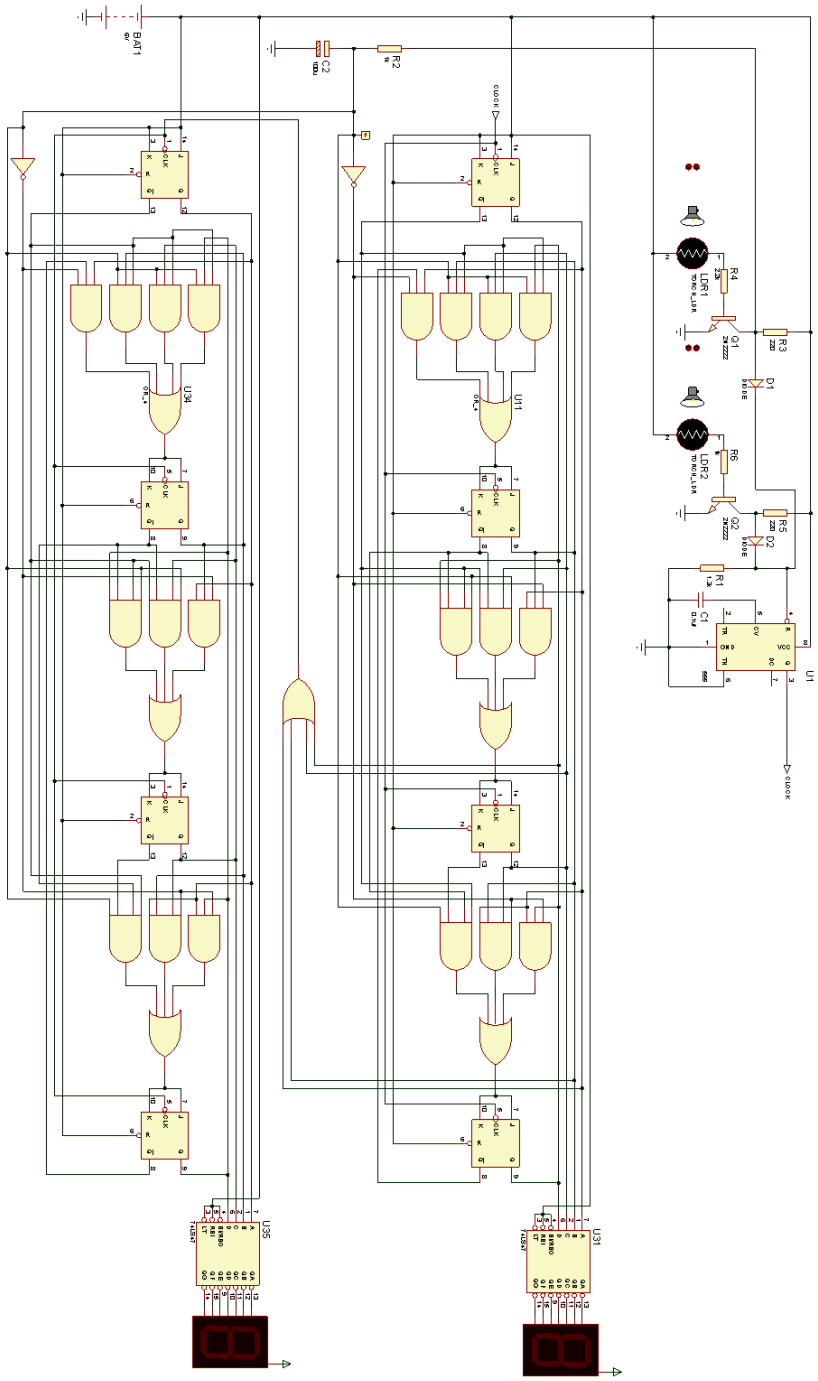

Figure 8: Circuit without reduction of mode 100 counter

The circuit was massive and huge so we considered to use MUX for implementation of combinational logics between two consecutive flip flops. Then we have a circuit using 8 x 1 MUX which is reduced to about half of the size.

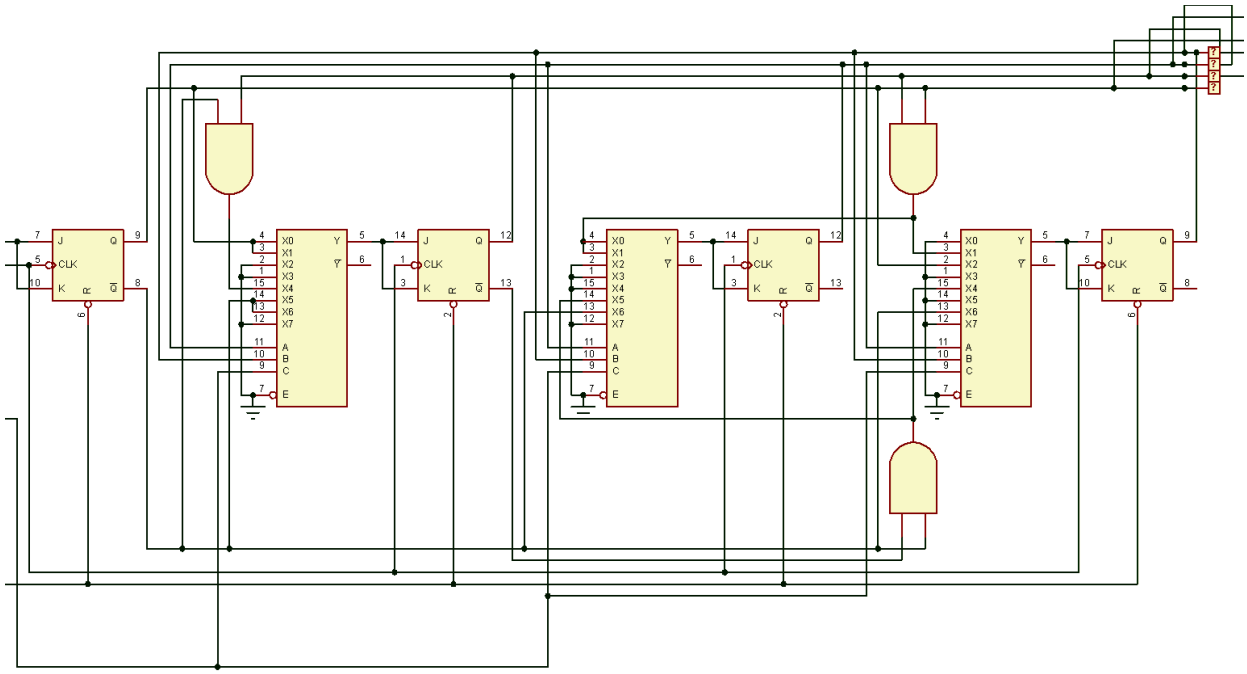

Figure 9: Circuit of mode 10 counter after reduction

We have implemented the combinational parts of the circuit using only 3 AND gates and MUX by reduction methods otherwise we have to use 64 AND gates for a flip flop which will be a massive and huge circuit.

CONCLUSION: -

The conclusion of the project is that we have implemented a circuit that can be used as a universal synchronous counter by cascading method of our desired mode.

- We can convert mode 10 counter to mode 100 counter by cascading two counters and an OR gate between them.
- We have reduced the circuit from a huge size to a small size by using MUX.
- A fast synchronous universal counter has been implemented.

SUBMITTED BY: -

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