Analysis of PPA Trade- off with Different Standard Cell Architectures for RISC V Processor

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Abstract: This study presents a comprehensive analysis of a RISC-V processor's performance using different threshold voltage (VT) cells—Low VT (LVT), Standard VT (SVT), and High VT (HVT)—across varying design effort levels—high, medium, and low. The investigation encompasses power consumption, timing slack, and physical area considerations. Synthesis was conducted using Genus electronic design automation (EDA) tool of Cadence, ensuring a consistent experimental setup. Our results highlight the trade-offs inherent in choosing different VT cells and effort levels, providing valuable insights for optimizing RISC-V processor designs based on specific application requirements. The findings contribute to the understanding of the interplay between power, timing, and area in semiconductor design, aiding designers in making informed decisions for efficient and tailored processor implementations.

1. Introduction

In the pursuit of enhancing the efficiency and adaptability of RISC-V processors, this experiment delves into a comprehensive analysis of critical design parameters, namely power consumption, timing performance, and physical area footprint. The investigation explores the impact of utilizing different threshold voltage (VT) cells—Low VT (LVT), Standard VT (SVT), and High VT (HVT)—across varying design effort levels—high, medium, and low.

The choice of VT cells plays a pivotal role in influencing the trade-offs between power, timing, and area in semiconductor design. The experiment aims to elucidate how the selection of specific VT cells, coupled with different levels of design effort, contributes to the overall performance characteristics of a RISC-V processor. The Genus synthesis tool, integrated into electronic design automation frameworks, serves as a key enabler for conducting observation with precision and consistency.

As semiconductor technologies evolve, the need to strike an optimal balance between performance and resource utilization becomes increasingly paramount. The outcomes of this experiment are anticipated to provide valuable insights for designers and engineers, guiding them in making informed decisions when tailoring RISC-V processor configurations to meet the unique requirements of diverse applications. By examining the intricate interplay between power, timing, and area, this experiment seeks to contribute to the on-going discourse in semiconductor design and facilitate advancements in processor optimization.

2. RISC V Processor

The RISC-V processor is an open-source, modular, and scalable instruction set architecture (ISA) designed based on Reduced Instruction Set Computing (RISC) principles. Its versatility spans from low-power embedded systems to high-performance computing. RISC-V promotes customization, transparency, and collaboration, making it a popular choice for educational purposes, research, and diverse applications across the technology landscape.

a RISC-V processor follows a streamlined process:

1. **Instruction Fetch**: Retrieve the next instruction from memory.
2. **Instruction Decode**: Understand the operation and operands of the instruction.
3. **Execute**: Perform the specified operation using the ALU.
4. **Memory Access**: If needed, read or write data in memory.
5. **Write Back**: Store the result in the destination register or memory.

The study was conducted utilizing semiconductor technology with an 180nm process node. This specific process node, characterized by a minimum half-pitch of approximately 180 nanometres, served as the foundation for implementing and evaluating the RISC-V processor. The choice of the 180nm technology node allowed for a detailed examination of performance, power consumption, and area considerations within this particular semiconductor manufacturing context.

3. Threshold Voltage Cells

- **Low-VT (LVT) Cells:**

LVT cells are designed with a lower threshold voltage. This is suitable for high-performance applications where speed is crucial. It may exhibit higher leakage power but offers faster switching speeds. LVT cells might result in a relatively larger cell area due to the emphasis on performance.

- **Standard-VT (SVT) Cells:**

SVT cells represent a balanced choice in terms of threshold voltage. This is commonly used for a mix of performance and power considerations. It strikes a balance between power efficiency and speed. SVT cells typically provide a moderate cell area, making them versatile for various applications.

- **High-VT (HVT) Cells:**

HVT cells have a higher threshold voltage. This is Ideal for low-power applications where minimizing leakage is critical. It offers improved power efficiency but may have slower switching speeds. HVT cells may result in a relatively smaller cell area due to the emphasis on power savings.

4. Effort Level

- **High Effort:**
  Optimization Focus:
  Power: Aggressively optimize for minimal power consumption.
  Timing: Prioritize achieving the highest possible performance and minimizing critical path delays.
  Area: Strive to minimize the overall chip area without compromising power and timing objectives.
  Application:
  It is suitable for scenarios where power efficiency, high performance, and compact chip area are critical, even at the expense of longer synthesis times.

- **Medium Effort:**
  Optimization Focus:
  Power: Optimize for a balanced power profile, considering both active and standby power.
  Timing: Aim for a moderate performance level without extreme emphasis on speed.
  Area: Seek a reasonable compromise between chip area and optimization goals.
  Application:
  Appropriate for general-purpose applications where a balance between power, performance, and area is essential. It offers a reasonable trade-off between optimization and synthesis time.

- **Low Effort:**
  Optimization Focus:
  Power: Emphasize simplicity and power savings over aggressive optimization.
  Timing: Tolerate relaxed timing constraints to ease pressure on critical paths.
  Area: Allow for a more relaxed approach to minimize the impact on chip area.
  Application:
  It is ideal for less critical applications where power consumption, performance, and chip area are not top priorities. It is suitable for quick design iterations and faster synthesis times.

These effort levels provide a spectrum of optimization strategies, allowing designers to tailor the synthesis process to the specific requirements and priorities of the RISC-V processor implementation. The choice of effort level depends on the application, design goals, and the desired trade-offs between power, timing, area, and synthesis time.

5. Design and Synthesis

In this study, the Genus synthesis tool was employed to implement a RISC-V processor using various threshold voltage (VT) cells—High-VT (HVT), Low-VT (LVT), and Standard-VT (SVT)—across different effort levels. The primary objective was to explore the impact of these VT cells and effort levels on the synthesis outcomes, with a focus on power consumption, timing performance, and chip area.

The consistency of the Genus tool was maintained throughout the study to ensure a fair and reliable comparison. Effort levels were varied—High, Medium, and Low—to investigate the trade-offs and optimizations for power, timing, and area.

A suitable clock constraints and tcl (tool command language) script file were taken as the inputs for the synthesis operation and area report, timing report and power report was output along with the gate level netlist.

Power metrics, including dynamic and leakage power, were recorded using Genus, providing insights into the energy efficiency of each configuration. Timing metrics, such as critical path delays and slack, were analysed to understand the performance implications. Additionally, Genus was used to capture area metrics, aiding in the assessment of chip area requirements.

To enhance the reliability of the findings, multiple synthesis runs were conducted, leveraging Genus' capabilities for validation and reproducibility. The documentation of Genus synthesis parameters, settings, and tool versions added transparency to the methodology.

The analysis of Genus-generated results revealed distinct trends across VT cells and effort levels. Optimal configurations were identified based on the study's objectives, providing valuable insights for future RISC-V processor designs.

6. Power Analysis

This study investigates the power characteristics of a RISC-V processor by varying threshold voltage (VT) cells (High, Low, Standard) under different effort levels (High, Medium, and Low). The analysis explores how different combinations impact dynamic and leakage power. Findings offer insights into power efficiency trade-offs, aiding in the selection of optimal VT cells and effort levels for RISC-V processor designs.

- **LVT Cell with High Effort**

Instance	Cells	Leakage Power(nW)	Dynamic Power(nW)	Total Power(nW)
PROCESSOR	22	11.057	92810.488	92821.545

- **SVT Cell with High Effort**

Instance	Cells	Leakage Power(nW)	Dynamic Power(nW)	Total Power(nW)
PROCESSOR	22	2.283	75062.926	75065.209

- **HVT Cell with High Effort**

Instance	Cells	Leakage Power(nW)	Dynamic Power(nW)	Total Power(nW)
PROCESSOR	22	14.995	59836.845	59851.840

Under high effort of optimization the power consumption of cells are in the following order HVT<SVT<LVT.

- **LVT Cell with Medium Effort**

```
                                        Leakage     Dynamic
Total
          Instance           Cells Power(nW)   Power(nW)
Power(nW)
-------------------------------------------------------------------
-----
PROCESSOR                     3456  2758.209 47309686.578
47312444.787
  datapath_m..g_file_module  1783  1878.499 29381307.943
29383186.443
```

- **SVT Cell with Medium Effort**

```
                                        Leakage     Dynamic
Total
          Instance           Cells Power(nW)   Power(nW)
Power(nW)
-------------------------------------------------------------------
-----
PROCESSOR                     3745   563.985 37275212.558
37275776.543
  datapath_m..g_file_module  1837   370.454 22466398.476
22466768.931
```

- **HVT Cell with Medium Effort**

```
                                        Leakage     Dynamic
Total
          Instance           Cells Power(nW)   Power(nW)
Power(nW)
-------------------------------------------------------------------
-----
PROCESSOR                     4034  3525.783 29489403.543
29492929.326
  datapath_m..g_file_module  1860  2170.497 17667102.270
17669272.767
```

Under medium effort of optimization the power consumption of cells are in the following order
HVT<SVT<LVT.

- **LVT Cell with Low Effort**

```
                                        Leakage     Dynamic
Total
          Instance           Cells Power(nW)   Power(nW)
Power(nW)
-------------------------------------------------------------------
-----
PROCESSOR                     4170  3058.216 30430480.153
30433538.369
  datapath_m..g_file_module  2220  1913.770 17738656.270
17740570.040
```

- **SVT Cell with Low Effort**

```
                                        Leakage     Dynamic
Total
          Instance          Cells Power(nW)   Power(nW)
Power(nW)
-------------------------------------------------------------
-----
PROCESSOR                    5258   658.711 28654602.844
28655261.555
  datapath_m..g_file_module  2395   386.779 14188200.303
14188587.081
```

- **HVT Cell with Low Effort**

```
                                        Leakage     Dynamic
Total
          Instance          Cells Power(nW)   Power(nW)
Power(nW)
-------------------------------------------------------------
-----
PROCESSOR                    5336  4222.886 22217244.052
22221466.938
  datapath_m..g_file_module  2440  2302.682 11395424.994
11397727.676
```

Under low effort of optimization the power consumption of cells are in the following order HVT<SVT<LVT.

7. Timing Analysis

This study rigorously examines the timing dynamics of a RISC-V processor, systematically varying threshold voltage (VT) cells (High, Low, Standard) under different effort levels (High, Medium, Low). The analysis is designed to elucidate the intricacies of critical path delays, slack, and overall timing performance. The findings provide nuanced insights into the impact of VT cell selection and effort levels on timing constraints, aiding in strategic decision-making for optimal timing outcomes in RISC-V processor designs.

- **LVT Cell with High Effort**

```
Cost Group   : 'clock' (path_group 'clock')
Timing slack :    5454ps
Start-point  : IFU_module_PC_reg[2]/CK
End-point    : IFU_module_PC_reg[4]/SE
```

- **SVT Cell with High Effort**

```
Cost Group   : 'clock' (path_group 'clock')
Timing slack :    5021ps
Start-point  : IFU_module_PC_reg[2]/CK
End-point    : IFU_module_PC_reg[4]/SE
```

- **HVT Cell with High Effort**

```
Cost Group   : 'clock' (path_group 'clock')
Timing slack :    4380ps
Start-point  : IFU_module_PC_reg[2]/CK
End-point    : IFU_module_PC_reg[4]/SE
```

Timing slack of cells under high effort level is in the following order:

LVT>SVT>HVT

- **LVT Cell with Medium Effort**

```
Cost Group   : 'clock' (path_group 'clock')
Timing slack :       8ps
Start-point  : IFU_module_PC_reg[2]/CK
End-point    :
datapath_module_reg_file_module/reg_memory_reg[31][31]2081/SI
```

- **SVT Cell with Medium Effort**

```
Cost Group   : 'clock' (path_group 'clock')
Timing slack :       1ps
Start-point  : IFU_module_PC_reg[2]/CK
End-point    :
datapath_module_reg_file_module/reg_memory_reg[31][31]2081/SI
```

- **HVT Cell with Medium Effort**

```
Cost Group   : 'clock' (path_group 'clock')
Timing slack :       1ps
Start-point  : IFU_module_PC_reg[4]/CK
End-point    :
datapath_module_reg_file_module/reg_memory_reg[31][23]2073/D
```

Timing slack of cells under medium effort level is in the following order:

LVT>SVT=HVT

- **LVT Cell with Low Effort**

```
Cost Group   : 'clock' (path_group 'clock')
Timing slack :       8ps
Start-point  : IFU_module_PC_reg[2]/CK
End-point    :
datapath_module_reg_file_module/reg_memory_reg[31][31]2081/SI
```

- **SVT Cell with Low Effort**

```
Cost Group   : 'clock' (path_group 'clock')
Timing slack :    -413ps (TIMING VIOLATION)
Start-point  : IFU_module_PC_reg[2]/CK
End-point    :
datapath_module_reg_file_module/reg_memory_reg[31][31]2081/SI
```

- **HVT Cell with Low Effort**

```
Cost Group   : 'clock' (path_group 'clock')
Timing slack :   -4537ps (TIMING VIOLATION)
Start-point  : IFU_module_PC_reg[2]/CK
End-point    :
datapath_module_reg_file_module/reg_memory_reg[31][31]2081/SI
```

Timing slack of cells under low effort level is in the following order:

LVT>SVT>HVT

8. Area Analysis

An area analysis complements the timing analysis by providing a comprehensive understanding of the physical space occupied by the RISC-V processor. It involves assessing the impact of threshold voltage variations and effort levels on component layout, transistor sizing, and overall area utilization. The findings from this analysis can guide designers in making informed decisions for optimal area outcomes in RISC-V processor designs.

- **LVT Cell with High Effort**

```
Instance Module  Cell Count  Cell Area  Net Area   Total Area
Wireload
-----------------------------------------------------------------
------------
PROCESSOR                22    518.918     0.000      518.918
<none> (D)

 (D) = wireload is default in technology library
```

- **SVT Cell with High Effort**

```
Instance Module  Cell Count  Cell Area  Net Area   Total Area
Wireload
-----------------------------------------------------------------
------------
PROCESSOR                22    518.918     0.000      518.918
<none> (D)

 (D) = wireload is default in technology library
```

- **HVT Cell with High Effort**

```
Instance Module  Cell Count  Cell Area  Net Area   Total Area
Wireload
-------------------------------------------------------------------
------------
PROCESSOR                 22    518.918     0.000      518.918
<none> (D)

 (D) = wireload is default in technology library
```

Area of cells under high effort level is in following order:

LVT=SVT=LVT

- **LVT Cell with Medium Effort**

```
             Instance              Module   Cell Count  Cell Area
Net Area   Total Area  Wireload
-------------------------------------------------------------------
-------------------------------------
PROCESSOR                                        3456 120625.244
0.000   120625.244    <none> (D)
  datapath_module_reg_file_module REG_FILE       1783  80585.366
0.000    80585.366    <none> (D)

 (D) = wireload is default in technology library
```

- **SVT Cell with Medium Effort**

```
             Instance              Module   Cell Count  Cell Area
Net Area   Total Area  Wireload
-------------------------------------------------------------------
-------------------------------------
PROCESSOR                                        3745 123016.925
0.000   123016.925    <none> (D)
  datapath_module_reg_file_module REG_FILE       1837  81001.166
0.000    81001.166    <none> (D)

 (D) = wireload is default in technology library
```

- **HVT Cell with Medium Effort**

```
             Instance              Module   Cell Count  Cell Area
Net Area   Total Area  Wireload
-------------------------------------------------------------------
-------------------------------------
PROCESSOR                                        4034 125531.684
0.000   125531.684    <none> (D)
```

```
  datapath_module_reg_file_module REG_FILE        1860  81480.168
0.000    81480.168    <none> (D)

 (D) = wireload is default in technology library
```

Area of cells under medium effort level is in following order:

LVT<SVT<HVT

- **LVT Cell with Low Effort**

```
             Instance              Module   Cell Count  Cell Area
Net Area   Total Area  Wireload
-----------------------------------------------------------------
-------------------------------------
PROCESSOR                                          4170 127660.580
0.000   127660.580    <none> (D)
  datapath_module_reg_file_module REG_FILE        2220  83542.536
0.000    83542.536    <none> (D)

 (D) = wireload is default in technology library
```

- **SVT Cell with Low Effort**

```
             Instance              Module   Cell Count  Cell Area
Net Area   Total Area  Wireload
-----------------------------------------------------------------
-------------------------------------
PROCESSOR                                          5258 139582.397
0.000   139582.397    <none> (D)
  datapath_module_reg_file_module REG_FILE        2395  85994.093
0.000    85994.093    <none> (D)

 (D) = wireload is default in technology library
```

- **HVT Cell with Low Effort**

```
             Instance              Module   Cell Count  Cell Area
Net Area   Total Area  Wireload
-----------------------------------------------------------------
-------------------------------------
PROCESSOR                                          5336 139795.287
0.000   139795.287    <none> (D)
  datapath_module_reg_file_module REG_FILE        2440  86113.843
0.000    86113.843    <none> (D)

 (D) = wireload is default in technology library
```

Area of cells under low effort level is in following order:

LVT<SVT<HVT

9. Sensitivity Analysis

The analysis reveals that LVS cells exhibit higher power consumption, making them less favourable from a design perspective. On the other hand, HVT cells demonstrate the least power consumption. Notably, effort levels play a crucial role in optimizing power consumption, with high effort levels resulting in the most significant reduction in power. Consequently, from a design standpoint, achieving a power-efficient design is attainable by leveraging HVT cells with a high effort level.

LVT cells exhibit the most positive time slack, indicating minimal delay and superior speed. Conversely, low effort displays negative time slack, signifying potential timing violations, which is undesirable from a design standpoint. Therefore, the optimal choice aligns with utilizing LVT cells in conjunction with high effort, ensuring both enhanced speed and adherence to critical timing constraints in the design.

Under high effort levels for the RISC-V processor, all cells (HVT, SVT, LVT) exhibit uniform area utilization. In contrast, medium and low effort levels reveal variation, with LVT cells occupying the least area and HVT cells occupying the maximum. The study emphasizes the substantial impact of effort levels on area optimization. In conclusion, the most optimized area for the RISC-V processor is achieved with LVT cells under high effort conditions.

10. Conclusion

The comprehensive analysis of the RISC-V processor design reveals intricate trade-offs across power consumption, timing performance, and area utilization. LVS cells, while exhibiting higher power consumption, are deemed less favourable in the overall design perspective. Conversely, HVT cells demonstrate superior power efficiency, positioning them as a more attractive choice. The pivotal role of effort levels in power optimization is evident, with high effort levels yielding the most substantial reduction in power consumption. Therefore, achieving a power-efficient design is deemed attainable by strategically employing HVT cells in conjunction with a high level of effort.

In terms of timing considerations, LVT cells emerge as the frontrunners, showcasing the most positive time slack and, consequently, and superior speed. This contrasts with low effort levels that result in negative time slack, indicating potential timing violations—an undesirable scenario from a design standpoint. Consequently, the optimal choice leans towards the utilization of LVT cells paired with high effort. This combination ensures not only enhanced speed but also adherence to critical timing constraints, contributing to an overall robust design.

Shifting the focus to area optimization, under high effort levels, a noteworthy uniformity is observed in the area utilization of all cells (HVT, SVT, and LVT). In contrast, medium and low effort levels introduce variation, with LVT cells occupying the least area and HVT cells claiming the maximum. This underscores the substantial impact of effort levels on area optimization. As a conclusive recommendation, the study advocates for the most optimized area in the RISC-V processor design achieved through the utilization of LVT cells under conditions of high effort.

In summary, the study provides a nuanced understanding of the interplay between power consumption, timing dynamics, and area utilization in the context of a RISC-V processor. The recommended design approach involves strategically combining HVT cells for power efficiency and LVT cells for optimal speed and adherence to timing constraints under the umbrella of high effort, offering a balanced and efficient solution for RISC-V processor development.

11. Reference

- **https://github.com/ash-olakangal/RISC-V-Processor**
- **https://www.synopsys.com/glossary/what-is-risc-v.html**
- **https://siliconvlsi.com/what-is-the-difference-between-lvt-hvt-and-svt-cells-in-vlsi/**
- **https://www.ece.lsu.edu/koppel/v/2022/syn-sol.tcl.html**
- **https://www.coursehero.com/file/p5bb0kj5/5-Elaborating-the-design-elaborate-The-elaborate-command-constructs-design/**