An efficient PMOS-based LDO design for large loads

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Abstract. A stable low dropout (LDO) voltage regulator topology is presented in this paper. LDOs (Low Drop-Outs) are linear voltage regulators that do not produce ripples in the DC voltage. Despite the close proximity of the supply input voltage to the output, this regulator will maintain the desired output voltage. Based on a detailed comparison between NMOS and PMOS-based LDOs, we decided to opt for a PMOS design because it does not require an additional charge pump as compared to NMOS. A demonstration of how Miller capacitance enhances overall design stability is also presented here. Multiple pass elements are arranged in parallel in order to increase the current carrying capacity of the pass network.

Keywords: Low Dropout Regulator (LDO) · Operational Transconductance Amplifier (OTA) · Voltage Regulator · Miller Compensation

1 Introduction

Since the development of the VLSI industry and the consequent scaling down of devices following Moore's law, transistor sizes have significantly decreased. As a result, supply voltages have also been reduced. Therefore, voltage regulators are needed, which output a fixed voltage despite varying input voltages. The IC's other parts receive this fixed output voltage as a supply. There are two main types of regulators: linear and switching. LDOs are linear regulators that are commonly used in VLSI chips. The reduction in supply voltage due to scaling has made LDOs an important component of power management ICs because we require lower input-output voltage differences, i.e., lower dropout.

An LDO consists of four main blocks [1]: an error amplifier, a pass element, a feedback network, and a load. An error amplifier is a differential amplifier based on an OTA or Operational Transconductance Amplifier. Like an Opamp, it has similar characteristics. OTAs, on the other hand, are designed for capacitive loads, while OPAMPs are designed for resistive loads. MOSFETs or BJTs can be used as the pass element. It is preferable to use MOSFETs because they are not very sensitive to temperature changes [2]. A simple resistive voltage divider network can be used as a feedback network.

The design has been simulated using LTspice developed by Linear Technology and Analog Devices. It is widely used for analog circuit simulations.

2 Comparative study between performances of PMOS and NMOS LDOs

The two main architectural types of the LDO [3] is shown in Fig. 1, the difference between them is the type of pass transistor. The first one is a PMOS pass transistor, whereas the second is an NMOS pass transistor.

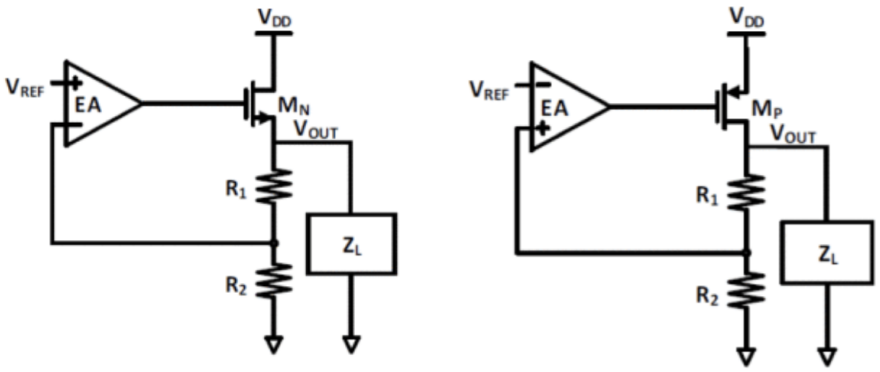

Fig. 1. Block level design of PMOS and NMOS based LDO

Three major components make up a typical LDO circuit, namely a high gain error amplifier [4], a pass transistor, and a feedback network. Using the pass transistor to control the load current, the High gain error amplifier compares output voltages with reference voltages, and the error amplifier receives a return voltage signal from resistors that act as voltage-voltage feedback to sense output voltages from the LDO.

2.1 The reason behind selecting a PMOS-based design

The dropout voltage of PMOS is lower than that of NMOS. However, because the NMOS pass transistor is connected as a common drain, it leads to a small output resistance at high load currents due to the increase in transconductance. This makes it more cumbersome to fabricate the IC since an additional charge pump [5] is required to support a wide range of load currents. PMOS LDO has higher loop gain as compared to NMOS-based LDO. PMOS is, however, a bit slower compared to NMOS since the mobility of electrons is greater than that of holes, thus PMOS design occupies a larger area which accounts for larger capacitances. This makes the PMOS LDO [6] slower than its NMOS counterpart. Thus, we have selected PMOS for our design by balancing odds and favours.

3 Error Amplifier Design

The error amplifier [7] is a two-stage OTA. The first stage is a differential amplifier stage. The second stage is a gain-enhancing common source stage. We have used a current mirror biasing for the first stage formed by MOSFETs M_1 and M_6. The MOSFETs M_2 and M_3 form the inverting and non-inverting terminals of the OTA respectively. The design has been done for 180nm technology. The current flowing through M_6 is copied in M_1 and is twice the current flowing through M_4 and M_5 each since the same current flows through M_4 and M_5 due to equal gate-source voltage. C_c is the Miller Compensation capacitance and C_L is the load capacitance. The miller capacitance has been added to increase the stability of the error amplifier.

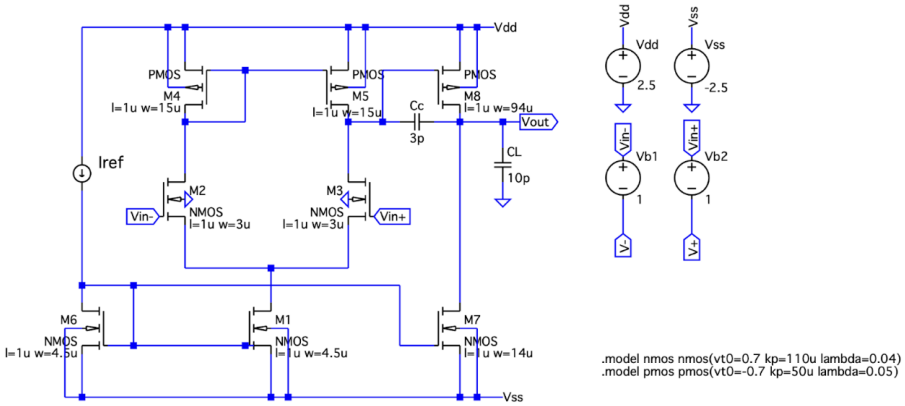

Fig. 2. Circuit diagram of error amplifier

4 Significance of Miller Compensation Capacitance

The compensation capacitance has been used to stabilize the system by increasing its phase margin. Mosfet M_4 is diode-connected, so it has a very low output impedance ($1/g_{m_4}$). Hence, the overall port impedance at the drain of M_4 is low. However, the port impedances at the drains of M_5 and M_8 are very high (comparable to the r_o). This forms two low-frequency poles ($1/(r_o * C_L)$). Each pole contributes a -90^o phase shift, and thus a total phase shift of -180^o at low frequencies. This results in 0^o phase margin and the OTA will oscillate in negative feedback. Thus, we are adding a compensation capacitor [8] between the drain of M_5 and M_8. Now, the output impedance at the drain of M_5 will see a much larger capacitance according to Miller's theorem and this pole will shift towards a lower frequency. The other pole shifts towards higher frequency. Thus the system will essentially become a 1st order system with a significant

phase margin (60^o). Thus, the OTA will function as an amplifier instead of an oscillator.

5 Proposed PMOS LDO

The architecture of this LDO is similar to a basic LDO regulator. A voltage reference of 1.2V [9] is generated by the bandgap which is given to the negative terminal of the error amplifier. The output of the error amplifier block is fed to the gate terminal of the PMOS pass network and at the drain, a resistive divider network is connected. The feedback voltage from the resistive divider is fed back to the positive terminal of the error amplifier to ensure negative feedback.

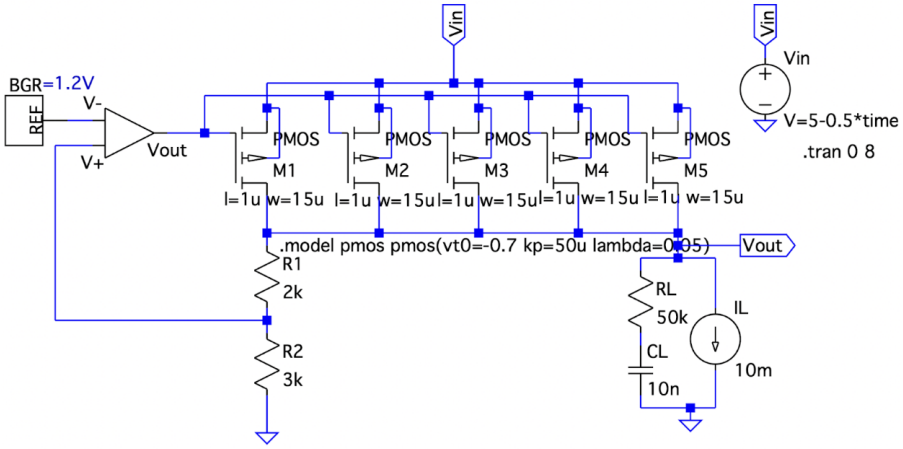

Fig. 3. Circuit design of PMOS based LDO

5.1 Working Principle of Circuit

From Fig. 2, the error amplifier is in negative feedback. This is because according to Barkhausen criteria, the total phase shift should be -180^o for negative feedback. The gate-drain phase shift is -180^o and the voltage is fed back to the positive terminal. Therefore, the total phase shift is calculated to be -180^o. We can assume a virtual short condition for negative feedback in opamp. Thus, $V_+ = V_- = V_{REF}$ which leads to the following working formula for V_{OUT}.

$$V_{out} = V_{REF} * (R_1 + R_2)/R_2 \tag{1}$$

Now, let's understand the LDO regulation principle intuitively. If the load current increases, the current through the pass element cannot increase immediately. It will undergo some transient. Initially, the required additional load

current is drawn from the load capacitor. This will lead to a decrease in the output node voltage. This output voltage reduction will lead to a decrease in the feedback voltage. Therefore, the gate voltage of the pass element will also decrease, because the voltage has been fed back to the positive terminal. Thus, the source-gate voltage of the PMOS pass element increases, which finally increases the current through the pass network to the required level. The same is the scenario when the load current drops. In this way, the output voltage and the load current are maintained by the LDO.

5.2 Simulation and Analysis

The 2-stage OTA [10] forming the error amplifier was simulated in LTspice. The OTA was designed for a DC differential voltage gain greater than 5000 and a Gain Bandwidth Product (GBP) of 5MHz. The bode plot of the OTA was obtained as shown in Fig. below.

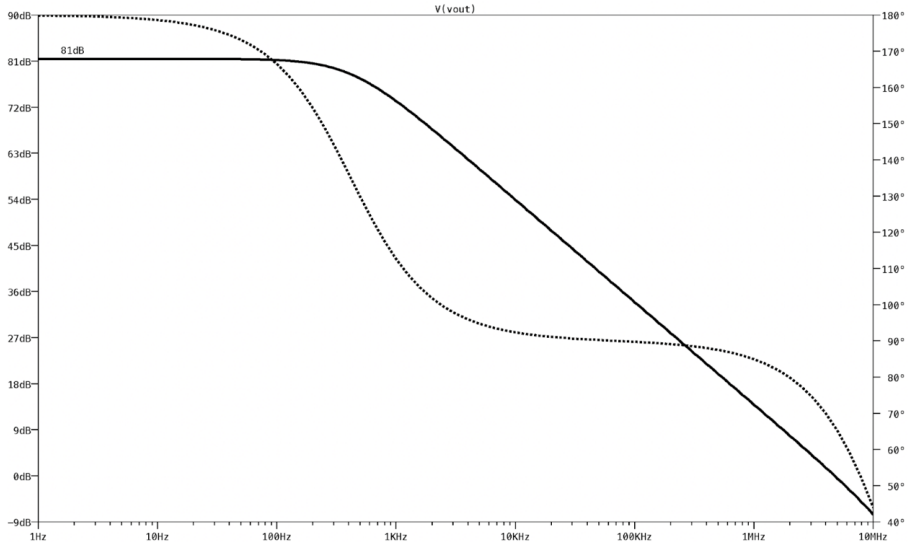

Fig. 4. Bode plot of the OTA

The DC gain has been found to be 81dB = 11220 which is greater than 5000 as expected . The 3dB cutoff frequency is found to be 440Hz. Thus, the GBP evaluates to 5MHz which matches our design constraints.

We observed the behaviour of the LDO for varying load currents in Fig. 6. It is found that as load current increases the performance of the LDO degrades since the dropout voltage increases [11,12]. The LDO supplies a maximum current of 23mA after which output voltage cannot be regulated.

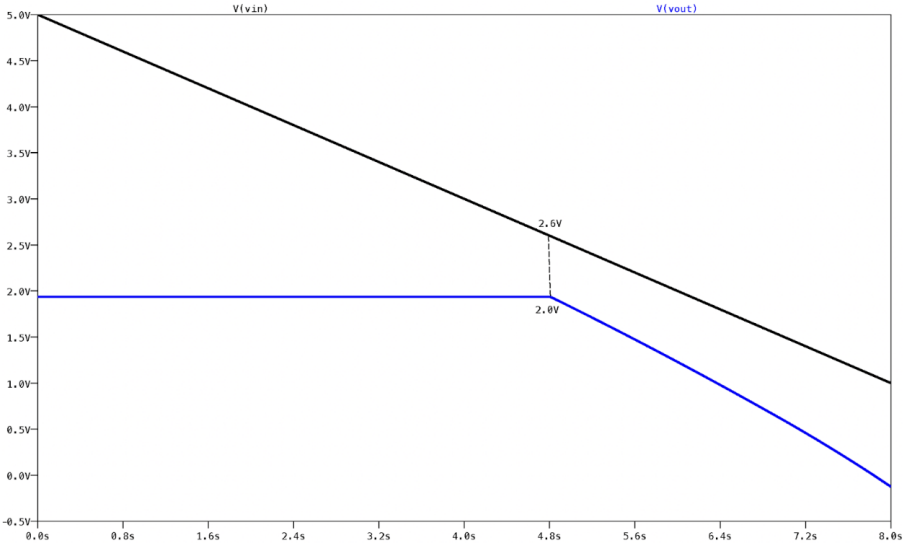

Fig. 5. The LDO circuit was simulated for a load current [13] of 10mA and the input supply was varied from 5.0V to 1.0V. The output was maintained at 2.0V as given by equation (1) until V_{in} drops below 2.6V. Therefore, the dropout voltage is (2.6 - 2.0) V = 0.6V

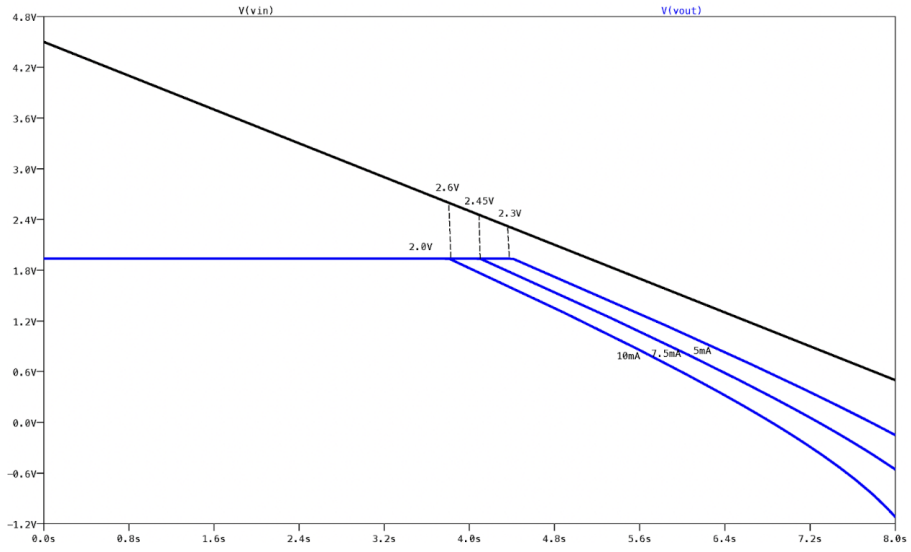

Fig. 6. Behaviour of the LDO for varying load currents

5.3 Result Summary

Table 1. Simulation and analysis results of the PMOS based LDO

Parameters	Values	
Input Voltage	1.0V - 5.0V	
Output Voltage	2.0V	
Reference Voltage	1.2V	
Dropout Voltage	I_{LOAD} = 5mA	0.3V
	I_{LOAD} = 7.5mA	0.45V
	I_{LOAD} = 10mA	0.6V
Power Consumed	I_{LOAD} = 5mA	7.42mW
	I_{LOAD} = 7.5mA	10.25mW
	I_{LOAD} = 10mA	12.31mW
Miller Capacitance	3pF	
Maximum Tolerable Load Current	23mA	

6 Conclusion

This paper illustrates how low dropout (LDO) voltage regulator topology can be applied to voltage regulator design and why PMOS-based designs are preferred. The simulation clearly shows that the proposed technique can tolerate up to 23mA of current, which is an excellent result as compared to other LDOs. The PMOS-based design was stabilized with an efficient compensation technique and a Miller Capacitance of 3pF was used to achieve 60^o phase margin.

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