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Comparative Design of NMOS and PMOS Capacitor-less Low Dropout Voltage Regulators (LDOs) Suited for SoC Applications

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ABSTRACT

In this paper, two architectures of Low Dropout Voltage Regulator (LDO) using NMOS and PMOS pass transistors is designed and implemented using 130nm CMOS technology. The performance of the two designs is compared while using the same quiescent current, input voltage, output voltage, and compensation capacitors. The two architectures can provide output voltage of 1V from a 1.2V supply voltage and supporting output current from 30µA to 100mA while consuming a quiescent current of 6µA. Both LDOs can support a range of loading capacitor 0-50pF. The NMOS LDO is designed with an auxiliary charge pump (CP) to step up input voltage of 1.2V to 2V, thus three architectures of CPs are discussed, designed, and optimized to provide a stable 5µA using a 1MHz of switching frequency. The cross-coupled CP is chosen to be the auxiliary CP because it consumed the smallest silicon area. Both LDOs are fully integrated and consume low power so that it can be used in SoCs. The PVT simulations are implemented to ensure the reliability of the design, also the specifications are compared to other techniques reported previously.

Keywords: Low Dropout Regulator (LDO), Capacitor-less LDO, Charge Pump, System-on-chip (SoC)

I. INTRODUCTION

Modern technology systems are pushing towards complete System-on-Chip (SoC) solutions in order to reduce the footprint area and cost. To achieve this, an essential power management unit is going to be used, where regulators are one of the main building blocks to power up other circuits. The main function of regulators is generating an accurate, noise-free and stable output voltage in case of varying the current of the load and/or the input voltage. There are mainly two types of voltage regulators, switching and linear regulators. Switching regulators have higher efficiency compared with linear regulators [1], on the other hand switching regulators may require a complex clocking scheme, as well as using inductors and/or capacitors in switching regulators is mandatory that require large silicon area (in order to support large load current) making integration more difficult [2], unlike linear regulators that consume less silicon area and have higher power supply rejection ratio [3]. For linear regulators, LDOs are preferred because of the low dropout voltage which improves the efficiency of the regulator [3, 4]. There are two main architectures of the LDO as shown in Fig.1, the difference between them is the type of the pass transistor, the first one is PMOS pass transistor and the second is NMOS pass transistor. In order to make a comparison between these two architectures at a specific range of current, a CP with the NMOS architecture is going to be used in order to generate a proper gate drive voltage [5].

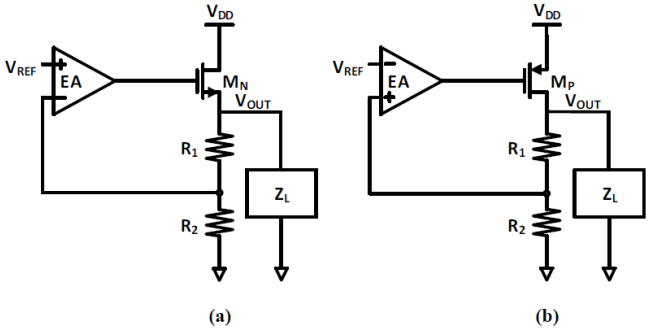


Fig. 1: Basic topology of LDOs (a) NMOS (b) PMOS.

II. CHARGE PUMP

Charge pump (CP) circuit is used to boost the power supply voltage to a higher voltage or provide a voltage of reverse polarity [6]. Their operation principle based on closed systems where regulation happens by letting

the pump on as long as the output voltage is less than the regulation level [7]. For SoCs, Many blocks may require supply voltages higher than the nominal supply voltage that is available for the complete systems such as power management unit and reading/writing EEPROMs at embedded systems for example [8]. Basic elements of CPs are switches to transfer charge and capacitors to work as storage element [9]. Power efficiency is one of the main challenges for designing the CP. The CP should provide a stable output voltage (minimum ripples) along the desired load current range while using minimum silicon area. Start-up time also is an important specification as it can limit the functionality and the performance of the next blocks, also faster start-up time reduce the power consumption during transients and improves the overall efficiency [10]. The output voltage ripples also can affect the performance of sensitive analog circuits such as reference voltage generators, op-amps, and charge pump control circuitry. A comparative design between three architectures of charge pumps (MOSFET-based Dickson, Bootstrap and Cross-coupled) shown in Fig. 2 has been made MOSFET-based Dickson, Bootstrap, and Cross-coupled. Responses of each one are discussed in the simulation results section.

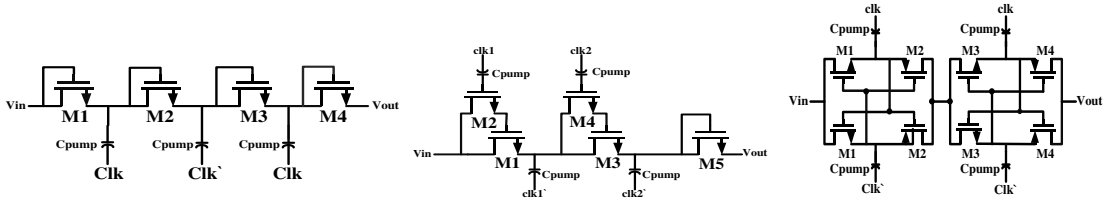


Fig. 2: Charge pumps used in this work (a) Dickson based on MOS, (b) Bootstrapped and (c) Cross-Coupled.

III. Low Dropout Voltage Regulator

A Conventional circuit for LDO consists of three main blocks [11]. The 1st one is a high gain Error Amplifier (EA) so that it can compare the output voltage with the reference voltage, the 2nd element is the pass transistor that is used to control the load current, and the 3rd element is the feedback network is implemented by resistors as a voltage-voltage feedback to sense the output voltage of the LDO and provides a return voltage signal to EA. LDO design specifications can be divided into three categories [12]: static-state specifications, dynamic-state specifications, and high-frequency specifications. Static-state specifications include line regulation, load regulation, and temperature coefficient. Meanwhile, dynamic-state specifications test the response of the LDO to a change in the system such as transient response. PSRR and output noise are considered as a high-frequency specification. One of the most important specifications is the quiescent current (I_Q) of the LDO, to improve the power efficiency I_Q should be reduced, power efficiency (η) can be calculated as $\eta = \frac{Pdeliverd}{Psupplied} = \frac{Vout\ I_{Load}}{Vin\ (I_{Load} + I_Q)}$ Whereas reducing I_Q degrades the transient response, bandwidth, and the slaw rate [13]. Improving transient response can be achieved by increasing I_Q so that it can charge/discharge the parasitic capacitance at the gate of the pass transistor [11], so there is a trade-off between power efficiency and transient response.

A. PMOS LDO

The common choice in LDO design is PMOS LDO because it has a lower dropout voltage compared with NMOS LDO [14]. On the other hand, this architecture has problems in stability, as it has at least two low-frequency poles. One at the gate of the power transistor (ω_{Pgate}) and the second at the output of the LDO (ω_{Pout}) [3] and the location of the ω_{Pout} changes as the load current change [15]. A Complex compensation technique is required in order to ensure the stability of the system all over the load current range and this requires either a very large output capacitance to move ω_{Pout} to lower frequencies in order to be the dominant pole [16] or a very low quiescent current is used in the driver circuit of the pass transistor (at the gate) to move ω_{Pgate} to lower frequency in order to be the dominant pole which will degrade the transient response [17]. Miller compensation technique is used in this work to solve the stability problem as shown in Fig. 3(a), by using C_C the ω_{Pgate} is shifted to lower frequency ensuring the stability of the system all over the load current range.

B. NMOS LDO

The NMOS pass transistor is connected as common drain which leads to a small output resistance at high load current as the transconducatce will be increased with the load current causing ω_{Pout} to be shifted to high frequency [18]. To support a wide range of load current, two possible approaches are used: the 1st one is by

increasing the pass transistor width which will increase the parasitic capacitances and as a result will negatively affect the transient response. The 2nd approach is by stepping up the voltage at the gate of the pass transistor using a CP [19] as shown in Fig. 3(b). Using a CP will increase the silicon area of the LDO as well as will increase the noise (ripples) especially at the switching frequency at the output voltage of the LDO [20]. Using a CP will help increase the gate voltage of the transistor, thus supplying higher currents using a smaller size pass transistor.

IV. Simulation Results

The two architectures of LDOs (NMOS and PMOS type) and the three mentioned topologies of CPs are simulated in standard 130-nm CMOS technology using Cadence Virtuoso. Both LDOs are designed to provide a 1V output voltage from a supply voltage of 1.2V (dropout voltage 200mV) while they can provide load current from 30µA to 100mA using a testing load capacitance of 50pF. The three architectures of CPs are designed to raise the supply voltage from 1.2V to 2V and can support load current up to 5µA.

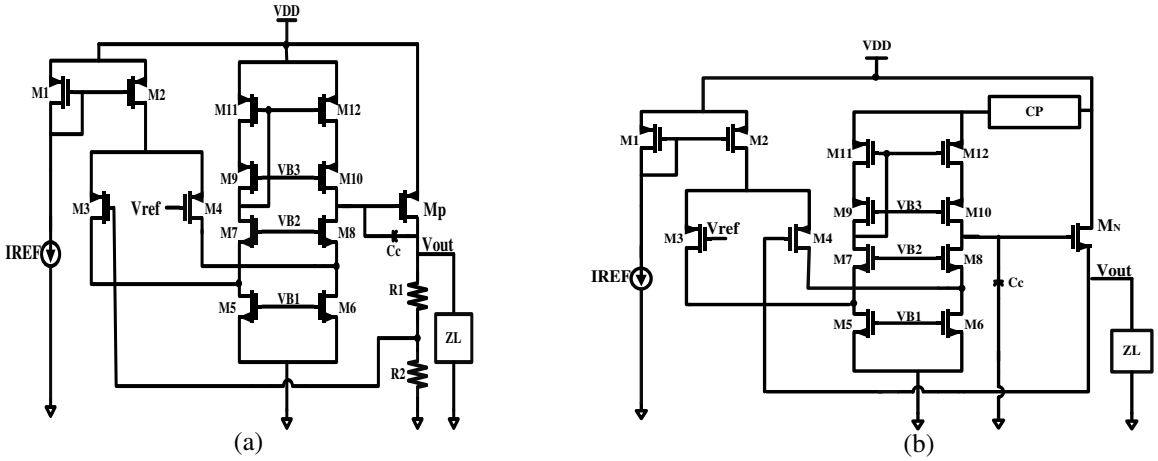


Fig. 3: Transistor level architectures of (a) PMOS LDO, and (b) NMOS LDO.

A. Charge Pump

The transient response of the three different topologies is shown in Fig. 4, which are designed using Deep-nwell transistors. Bootstrapped requires the lowest startup time of 43.95µsec while Dickson's startup time is 80µsec and Cross-Coupled is 108µsec.

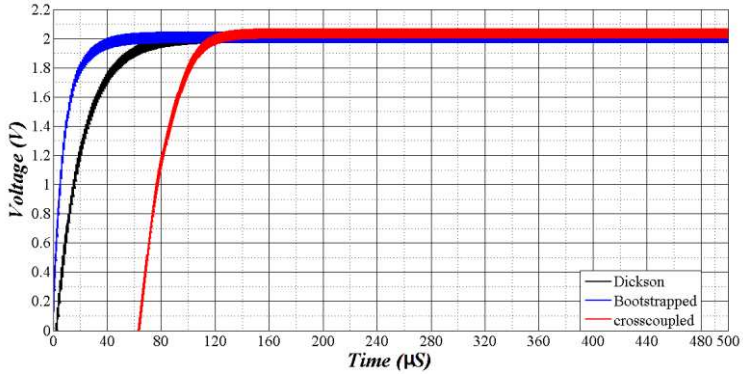


Fig. 4: Transient response of the three charge pump architectures using a load capacitor C_{PL} of 50pF.

B. LDO

Transient Response: the transient response of the two architectures of the LDO is shown in Fig. 5. The PMOS LDO can fully recover in 1.6µsec and 1.4µsec with undershoot of 841mV and overshoot of 200mV and the NMOS LDO can fully recover in 555.2nsec and 972nsec with undershoot 336.7mV and with overshoot of 200mV while the load current is switched between 100mA (full load) and 30µA (light load) with rise/fall time of 100nsec on both cases. The settling time is measured when the output voltage of the LDO reached 90% of its final value.

Frequency Response: Fig. 6(a) shows loop gain and phase at the worst case of 50pF load capacitance.

PMOS LDO loop gain and phase at the minimum and maximum load is 55.9dB and 46^0 in case of light load (30µA), and 61dB and 88.1^0 at high load current (100mA), respectively. Fig. 6(b) shows the NMOS LDO loop gain and phase at the minimum and maximum load are 65.7dB and 57.3^0 in case of light load (30µA), and 64.7dB and 88.88^0 at high load current (100mA), respectively.

Power Supply Rejection (PSRR): Fig. 7(a) shows that at 10KHz the PSRR is -45.8dB at light load (30µA) and -33.6dB at full load (100mA) for PMOS LDO, Fig. 7(b) shows that the PSRR is -53.2dB at light load and -50.3dB at full load current for NMOS LDO.

Line/Load Regulation: The line regulation is simulated at 30mA while VDD is changed from 1.25V to 1.35V. The PMOS LDO has a line regulation of 0.02mV/V and the NMOS LDO has a line regulation of 0.192mV/V. The load regulation is simulated at 1.2V supply voltage while the load current is changed all over the load range (30uA - 100mA). The PMOS LDO has load regulation of 0.019mV/mA and the NMOS LDO has load regulation of 0.0017mV/mA.

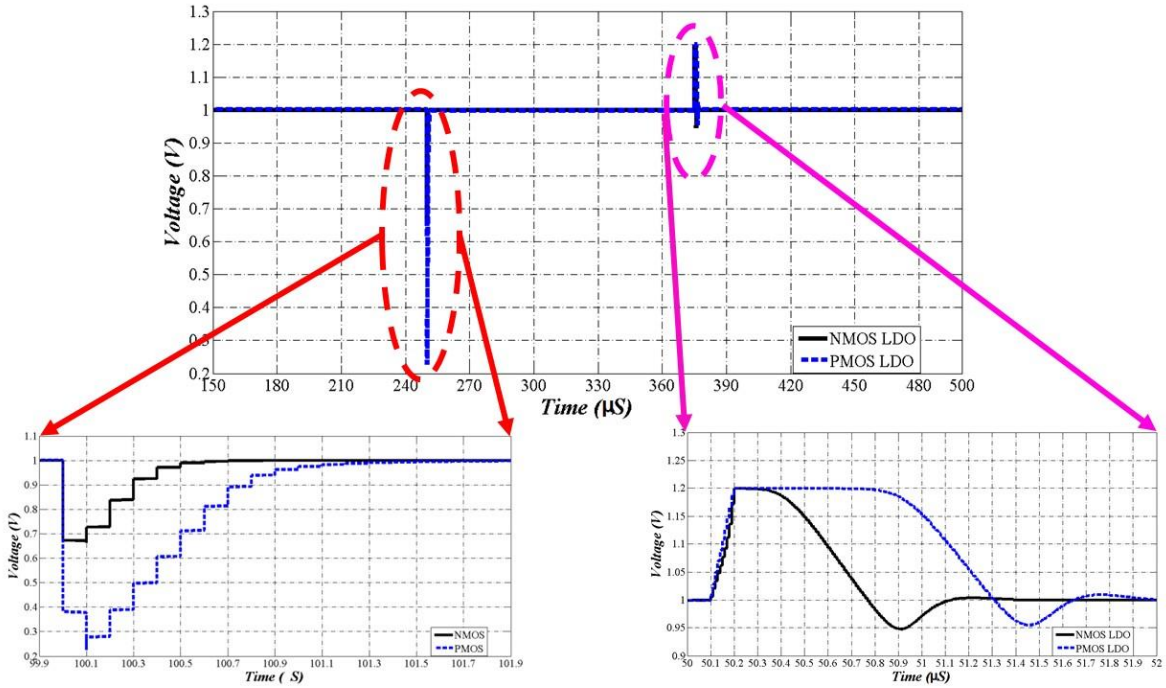
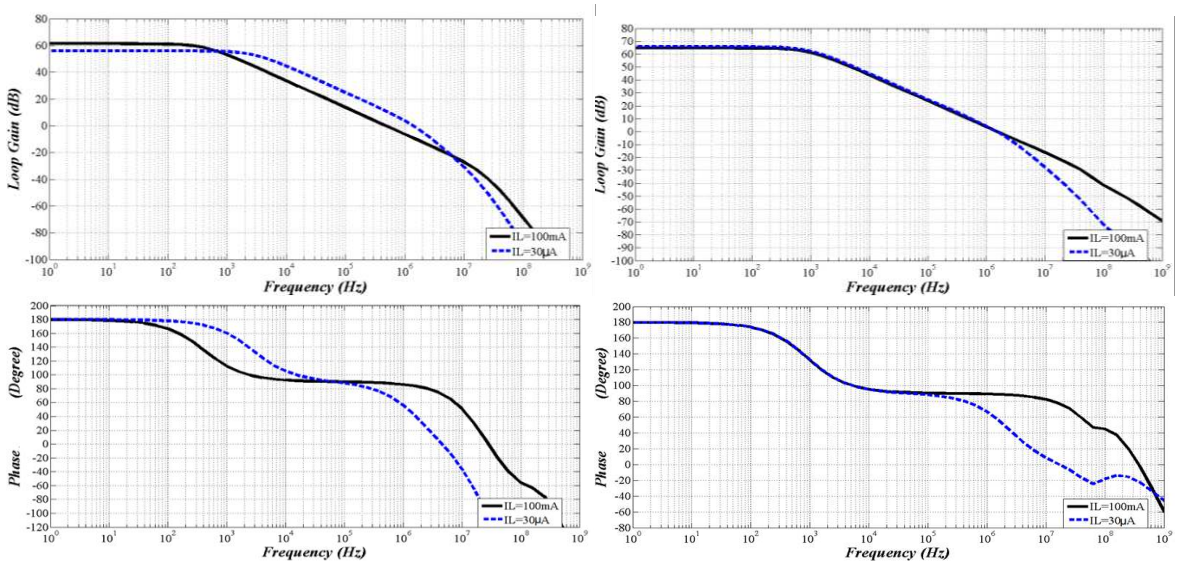
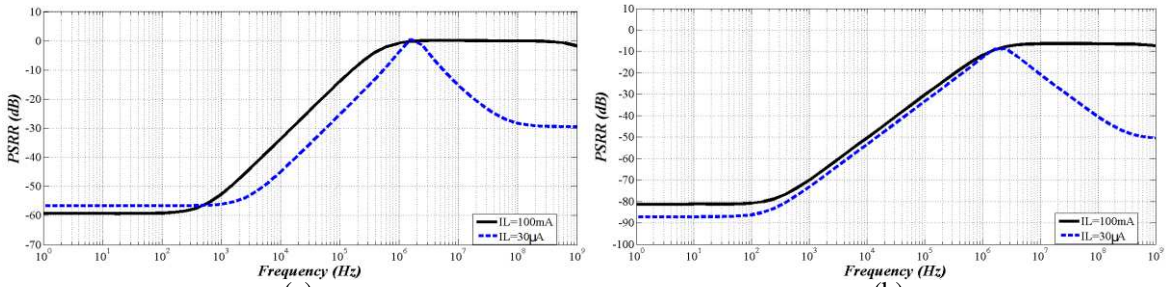


Fig. 5: Simulated output voltage transient response of PMOS LDO and NMOS LDO.



(a) (b)

Fig. 6: Simulated loop gain and loop phase of (a) PMOS LDO and (b) NMOS LDO.



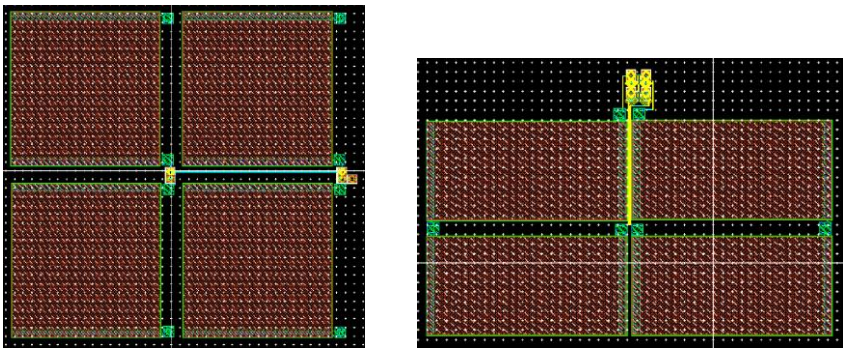
(a) (b)

Fig. 7: PSRR at light and high load current for (a) PMOS LDO and (b) NMOS LDO.

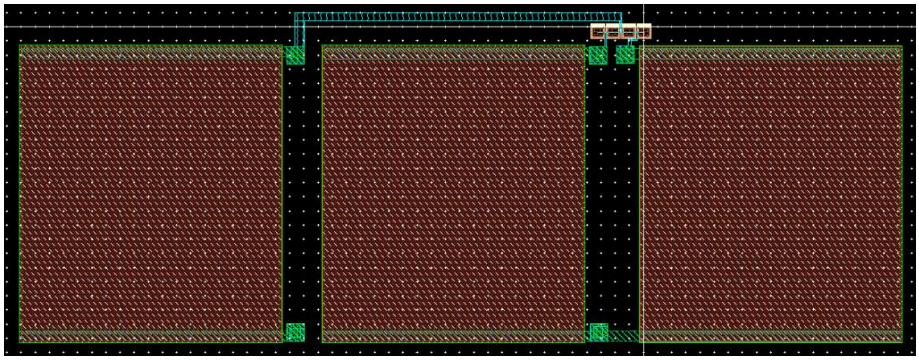
V. LAYOUT AND POST-LAYOUT SIMULATIONS

Both types of LDO and the three topologies of charge pumps have been designed and implemented using 130nm CMOS technology. The layout and post-layout simulations are implemented using Virtuoso, whereas verifications (LVS and DRC) and parasitics (RC) extraction are done using Calibre. Layout of the charge pumps is shown in Fig. 8. In order to do a good comparison, the charge pumps are designed to step up the input voltage from 1.2V to 2V and supply the same load current of 5µA while using a switching frequency of 1MHz. In order to supply this load current, Dickson charge pump is designed with 3-stages using 9pF for each pumping capacitor other two topologies required only 2-stages, whereas the cross-coupled required smallest area compared to the other two CPs by using 4 pumping capacitors of 5pF and the bootstrapped required 7pF pumping capacitors. All charge pumps are connected to a loading capacitor (C_{PL}) of 50pF at the output to decrease output ripples (not included in the layout).

The layout of PMOS LDO is shown in Fig. 9 whereas the layout of NMOS LDO without CP is shown in Fig. 10 and the Layout of NMOS LDO included with cross-coupled that is used because of its smallest area is shown in Fig. 11. The complete circuits (CPs and LDOs) are fully integrated on the chip without using any external components as a result, the two capacitor-less LDOs can be used to be integrated into SoCs.



(a) (b)



(c)

Fig. 8: The layout of the three charge pumps used (a) Bootstrapped, (b) cross-coupled, and (c) Dickson MOS based.

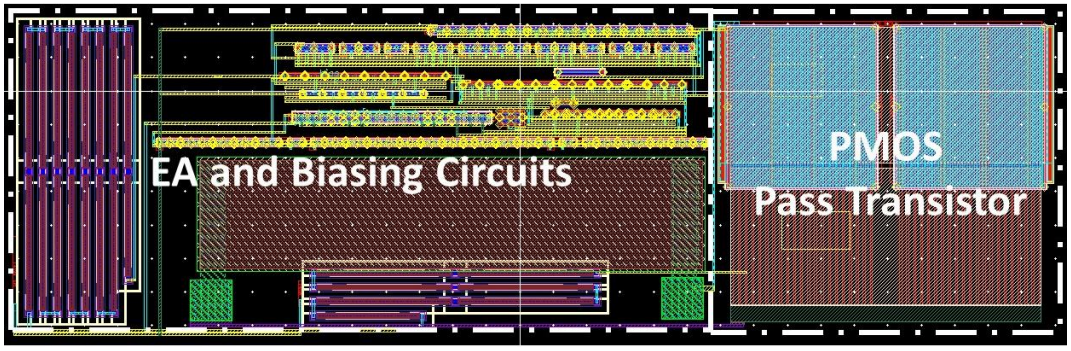


Fig. 9: Layout of the PMOS LDO.

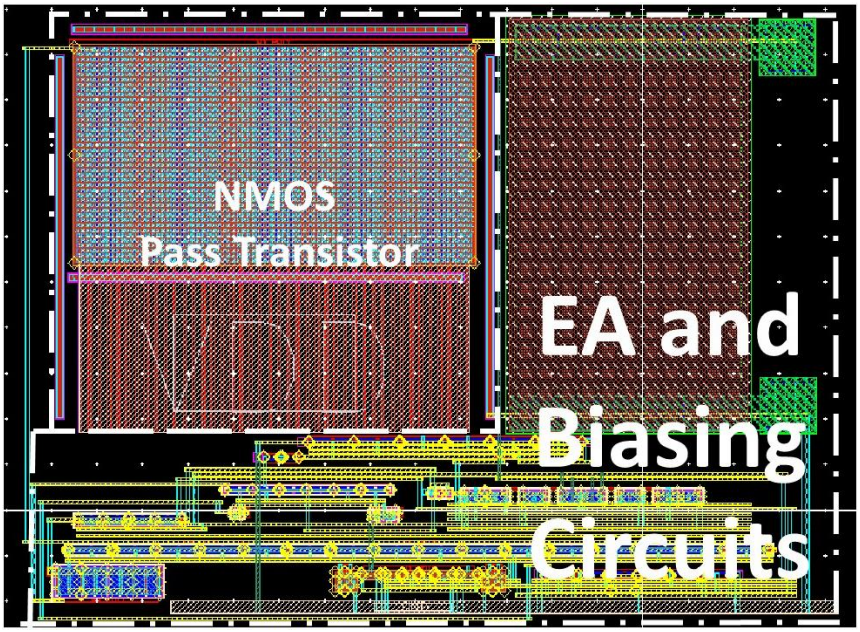


Fig. 10: Layout of the NMOS LDO.

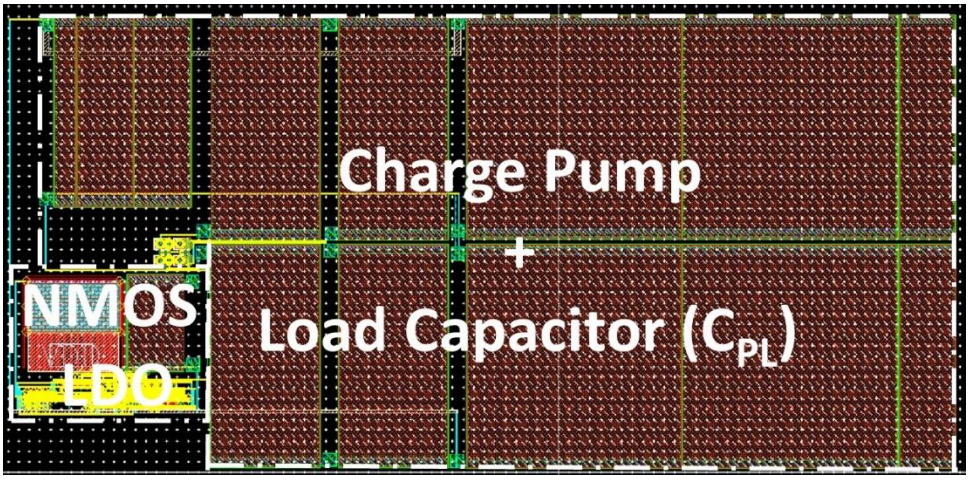


Fig. 11: Layout of the NMOS LDO integrated and connected with the cross-coupled CP.

Fig. 12 shows post-layout simulations of the transient response of the architectures of the LDO. When the load current is switched between 30µA to 100mA with rise/fall time of 100nsec, the PMOS LDO can fully recover in 1.412µsec/1.634 µsec, respectively with undershoot/overshoot of 784mV/200mV, respectively. The NMOS LDO can fully recover 644nsec/1.038µsec with undershoot/overshoot of 385mV/200mV, respectively.

Post layout simulations are performed to include effect of the parasitic extractions. For the charge pump parasitic capacitances and resistances lead to an increase in the ripples and the start-up time, whereas for the LDOs they lead to an increase in the settling time in both cases overshoot and undershoot one main reason for this degradation is the large stack of metals that are used in the pass transistor branch to support the high load current. This stack of metals provides large parasitic capacitors that are added to the output capacitor causing a decrease in the phase margin of the system especially at low load current.

The performance of the three CPs is summarized in Table 1. All specifications tested in this table includes a load capacitor C_{PL} of 50pF. The cross-coupled has the lowest ripple voltage of 56.1mV (post-layout) that makes it more attractive to be used to supply the NMOS LDO as it will have the lowest effect on the output voltage as well as it has the lowest power consumption compared to other topologies, on the other hand, the cross-coupled has the highest startup.

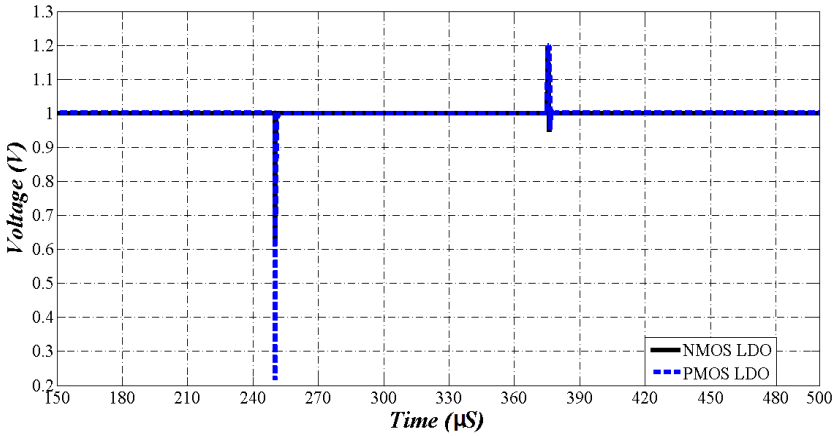


Fig. 12: Post-layout simulations for the transient response of the PMOS and NMOS LDOS.

The performance of the two types of LDOs is also summarized and compared in Table 2. Both LDOs are designed to consume equal quiescent current and also to support equal load currents, load capacitance, and a compensation capacitor. The NMOS LDO design used a larger area than PMOS LDO due to the fully integrated CP. To compare different LDO architectures the following figure of merit (FoM) formula is used [21]:

$$FoM = \frac{C_L \, \Delta V_{out} I_Q}{\Delta I_{out,max}{}^2}$$

The FoM is calculated based on the worst case of 50pF load capacitance. The NMOS LDO has lower FoM (better performance) than PMOS LDO due to it has lower undershoot voltage than the PMOS LDO, whereas the dynamic power of the CP that's used integrated with the NMOS LDO is not included in this FoM as the static power consumption which is related to I_Q is equal in both LDOs, but the NMOS LDO consumes dynamic power too (~7 µW) due to the integrated CP and its switching scheme which consumes power that is not ignorable compared to I_Q (~6µA) i.e. the NMOS LDO roughly consumes double of the power of the PMOS LDO). In order to check the robustness of the proposed designs of the two LDOs, post-layout simulations have been implemented for different process corners (slow-slow, fast-fast, slow-fast, and fast-slow), supply voltage variations from 1.1V to 1.3V, and a temperature range from -45°C to 60°C. Results are shown in Table 3. The performance of the two designed regulators is compared with previously reported regulators. Even though the design LDOs have simple architectures they have better FoM than all other regulators, this due to that both LDOs designed to have a wide current range and consume minimum quiescent current. Although the two designed regulators have low quiescent current, they have a better settling time than reported techniques except [19] that consumes very high quiescent current, support lower load current, and higher FoM than our two designed LDOs.

Table 1: Comparison Result of the Three Topologies of CPs.

Parameters	Dickson	bootstrapped	Cross coupled

Test	Simulation	Layout	Simulation	Layout	Simulation	Layout
Area (mm^2)	------	.03481	------	0.0378	------	0.0297
Frequency(MHz)	1		1		1	
Input voltage(V)	1.2		1.2		1.2	
Output voltage(V)	2		2		2	
C_{PL}(pF)	50		50		50	
Pump Cap(pF)	9.08		7		5	
Output current(µA)	5		5		5	
No. of stages	3		2		2	
Ripple Vp-p(mV)	52.2	69.3	65	75.7	20	56.1
Startup time (µs)	80	144.17	43.59	53.6	108	152
Power consumption(µW)	12.96		10.08		7.2	

Table 2: Summarized Results of the Two LDO Architectures.

Parameters		PMOS LDO		NMOS LDO	
Area (mm2)		0.00724		0.096	
Load current range (mA)		0.03	100	0.03	100
Phase margin (deg)		46^0	88^0	57.3^0	88.88^0
Loop gain (dB)		55.9	61	65.7	64.8
PSRR @10k (dB)		-45	-33.6	-49.25	-46.2
Queiscent current (IQ) (µA)		6		6	
Line regulation (mV/V)		0.02		0.192	
Load regulation (mv/mA)		0.019		0.0017	
Overshoots	Settling time (µsec)	1.634		1.038	
	Δv (mV)	200		200	
Undershoots	Settling time (µsec)	1.412		0.644	
	Δv (mV)	-784		-336.75	
Compensation capacitor (pF)		1		1	
LDO load capacitor (pF)		0-50		0-50	
FoM (fsec)		29.5		16.11	

Table 3: PVT Simulation Results.

Parameters	Best		Typical		Worst	
Type	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS
Gain (dB) (@I_L=30u)	72.31	75.37	55.95	65.72	32.57	31.66
PM (deg) (@I_L=30u)	60.78	119.2	45.91	57.33	42	55.93
Gain (db) (@I_L=100mA)	79.39	75.25	61.26	64.26	35.92	30.41
PM @100m(deg) (@I_L=100mA)	96.39	98.37	88.13	88.89	84.01	86.67

Table 4: Comparison of this Work with State-of-Art techniques.

		This Work		[19]	[22]	[23]	[24]	[25]	[26]
		PMOS LDO	NMOS LDO						
Year		2018	2018	2016	2014	2014	2012	2018	2017
Technology (µm)		0.13	0.13	0.065	0.5	0.18	0.35	0.13	0.13
Area (mm^2)		0.00724	0.096	0.154	0.7	0.14	0.0987	0.007	0.0113
Input Voltage (V)		1.2	1.2	2.4	2	1.8	1.2	1.4 - 2.2	1.6 - 2.6
Output Voltage (V)		1	1	1	1.8	1.6	1	1.2 - 2	1.5
Dropout Voltage (mV)		200	200	50	200	200	200	200	300
Quiescent current (µA)	Min.	6	6	161	78	55	28	60	24
	Max.					80	380		
Under/Overshoot (mV)		-784	-336.75	195	-134.4	-80	-105	-297	-75
		200	200		16.3	120	50	180	65
Settling time (µsec)		1.634	1.038	0.5**	2.5	6	4**	0.437	0.19
ΔI_{out} (mA)		0.03 -100	0.03 -100	1 - 31	0-100	0 -50	0 - 100	0.1 - 50	0 - 50
Edge time (nsec)		100	100	200	1000	100	0	100	100
Output Current (mA)	Min	0.3	0.3	1	0	0	100	0.1	0
	Max	100	100	31	100	50	50	50	50
Line Regulation (mV/V)		0.02	0.192	--	0.13204	--	0.39	2.1	10
Load Regulation (mV/mA)		0.019	0.0017	0.2	0.0041	0.14	0.078	0.022	--
C_L (pF)		0 - 50	0 - 50	30	0 – 100	100	100	100	100
PSRR @ 10kHz (dB)		-45	-49.25	-40	N/A	-60**	-47.9	--	<-60**
FoM (fsec)		29.5	16.11	65	105.1	264	29.4	1145.2	140

** Estimated from figure.

CONCLUSION

Two architectures of LDOs are designed and optimized to consume low quiescent current while providing a stable output voltage. Three charge pumps are designed and compared in terms of output ripples, area, and power consumption. Post-layout simulations results show that the two LDO architectures can support a wide range of load current with a competitive transient response and FoM compared to previously reported techniques. Both LDOs, including the CP used in the NMOS LDO, are fully integrated and suitable for SoC applications with no need for off-chip components.

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