Design Procedure of a Conventional Low-Dropout Circuit

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1. Abstract

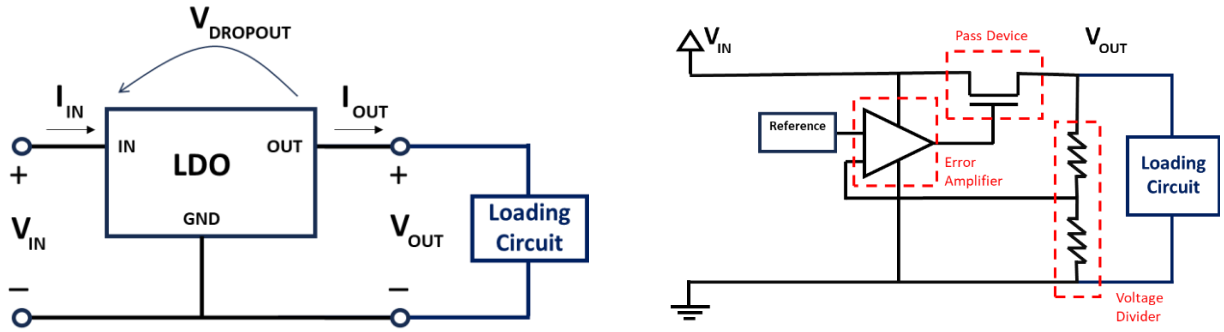
This project discusses the design procedure of a conventional Low Dropout Voltage Regulator (LDO) circuit. The circuit consists of 2 stages, a 5-transistor operational transconductance amplifier (OTA) & a pass transistor, designed in 45nm CMOS technology. The circuit produces a regulated voltage of 0.9V using a reference voltage of 0.75V & a supply of 1.2V. A comparison is made between 2 compensation techniques to show how the stability, the PSRR, & the step-response behavior differ.

Supporting a load current range of 5mA ~ 30mA & a load capacitor of 200pF, the circuit achieves a worst-case PSRR of 8.894 dB, a loop gain of 43.22 dB, an offset of mean = 770uA & standard deviation = 1.513mV (1-sigma), with a current consumption of 250 uA (excluding the load current).

2. Introduction

2.1 Motivation

LDOs play a crucial role in modern electronic systems by providing stable and regulated output voltages despite varying input voltages and load conditions. The dropout voltage of the LDO represents the difference between the input supply voltage and the regulated output voltage. The LDO operates within a "regulation region," where the Pass Device is in the saturation region & delivers a stable output over various input supplies and output loads. An LDO includes a reference voltage, an error amplifier, a feedback network, and a series pass element, as shown in Fig.1(b). [1-3]



(a) (b)

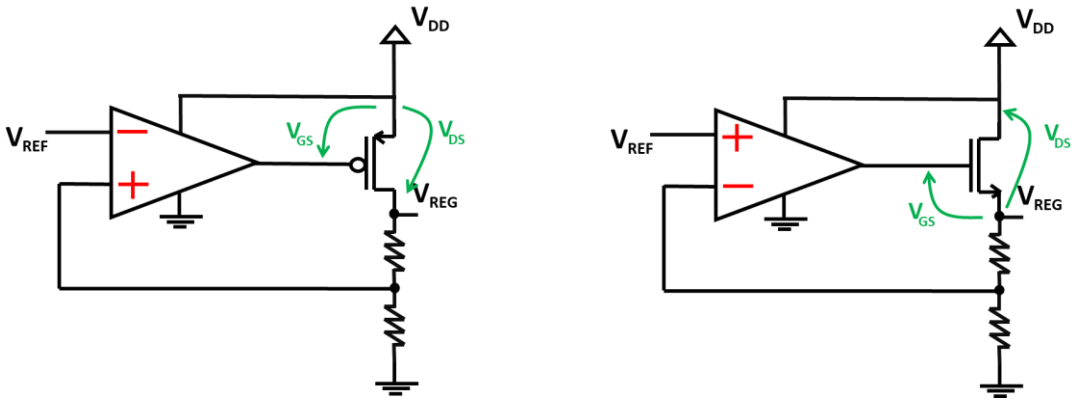
Fig.1. LDO Block Diagram

(a) Top-Level View, (b) Main Blocks

2.2 Main Topologies

The 2 main LDO topologies based on the type of the pass device are LDOs using a PMOS pass transistor & those using an NMOS pass transistor. PMOS LDOs typically feature a lower dropout voltage and simpler construction, making them a common topology. However, this design often grapples with stability concerns due to the presence of two low-frequency poles, one at the pass device's gate and another at the regulated output node. As we will discuss later, addressing these stability challenges necessitates the implementation of compensation techniques to ensure the LDO loop's stability.

NMOS pass-device LDOs typically exhibit faster response times owing to the higher mobility of electrons relative to holes. Moreover, NMOS LDOs, employing a common-drain configuration, exhibit reduced output resistance on the pass-device side as the transconductance (gm) of the pass transistor increases with the load current. This pushes the output pole to higher frequencies, particularly under higher load currents. However, it's worth noting that NMOS LDOs designed to support high current loads with a wide load range necessitate the inclusion of a charge pump circuit to elevate the pass-device's gate voltage. This addition contributes to an increase in LDO area and introduces some noise considerations. [4-6]

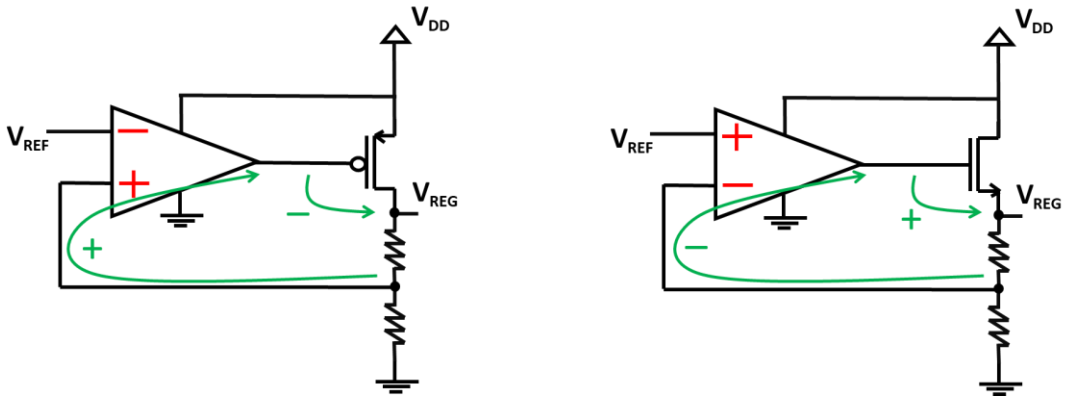


(a) (b)

Fig.2. LDO Topologies

(a) with PMOS pass device, (b) with NMOS pass device

The LDO loop is connected differently in the 2 topologies, mainly to form a negative-feedback system. In the case of the PMOS-based LDO, the PMOS pass-device is in a common-source configuration with the regulated output connected to the drain of the pass-device. Since the path from the gate-to-drain gives a negative gain, the feedback path is connected to the positive input of the OpAmp to give an overall negative-feedback loop, as shown in Fig. 3(a). On the other hand, the NMOS pass-device is used in the source-follower configuration with the regulated output connected to the source node which gives a positive gain from gate-to-source. In this case, the feedback is connected to the negative input of the Error Amplifier, as shown in Fig. 3(b).

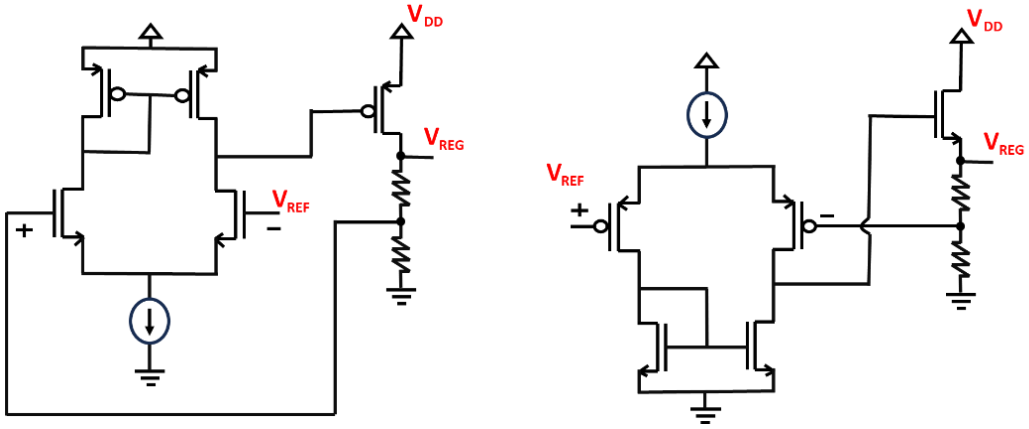


(a) (b)

Fig.3. LDO loop connections

(a) for PMOS pass-device LDOs, (b) for NMOS pass-device LDOs

Another difference in the LDO loop of the 2 topologies is the type of OpAmp used as the Error Amplifier. For the best Power-Supply Rejection (PSR), it is preferred to use an NMOS OpAmp with a PMOS pass-device, or a PMOS OpAmp with an NMOS pass-device, as explained in Ref [3] & shown in Fig. 4. In the following sections, the PMOS pass-device with an NMOS Error Amplifier is studied further.



(a) (b)

Fig.4. LDO Error Amplifiers

(a) NMOS Error Amplifier, (b) PMOS Error Amplifier

3. Basic Operation

3.1 DC Voltage Relationships

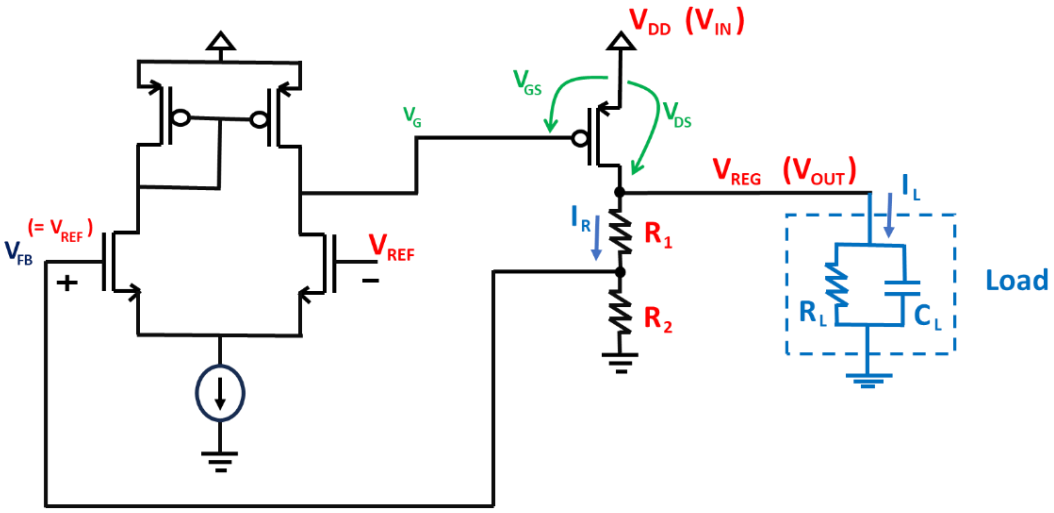


Fig.5. PMOS LDO with the operation points & the load

Since the resistances in the LDO's feedback form a voltage divider, the desired value for the regulated output voltage is determined mainly by the ratio between the 2 resistances & the value of the reference voltage, based on the following equation:

$$V_{REG} = \frac{R_1+R_2}{R_2} V_{REF} \quad (1)$$

The pass device is used to provide the current needed by the load while being in the saturation region. Most of the pass device's drain current should flow into the load, so R_1 & R_2 should be large enough so that I_R would be negligible. The load current can be found using the MOSFET's square-law equation:

$$I_L = I_D - I_R$$
$$= \frac{1}{2} \mu_n C_{OX} \frac{W}{L} \left(V_{SG} - |V_{TH,p}|\right)^2 - \frac{V_{REG}}{(R_1+R_2)} \quad (2)$$

All the devices must operate in saturation mode to ensure the correct operation. For the error amplifier, the transistors of the opamp must stay in the saturation region regardless of the load current value. At high load currents, the node voltage V_G is low (V_{SG} of pass-device is high), which could reduce the V_{DS} of the NMOS devices. While at low load currents, V_G is high (V_{SG} of pass-device is low), which could reduce the V_{SD} of the PMOS devices of the opamp. For the pass-device to be in saturation, its V_{DS} should be greater than the overdrive voltage, as shown below:

$$V_{SD} > V_{SG} - |V_{TH,p}| \quad (3)$$

$$V_{REG} < V_G + |V_{TH,p}| \quad (4)$$

3.2 AC Operation & Compensation Techniques

To ensure the stability of feedback control systems like LDOs, compensation is necessary. An RC network in the LDO helps stabilize the control loop by adding phase margin and reducing the risk of oscillations. In this sub-section, 2 types of these RC compensation techniques are discussed.

3.2.1 Miller Compensation

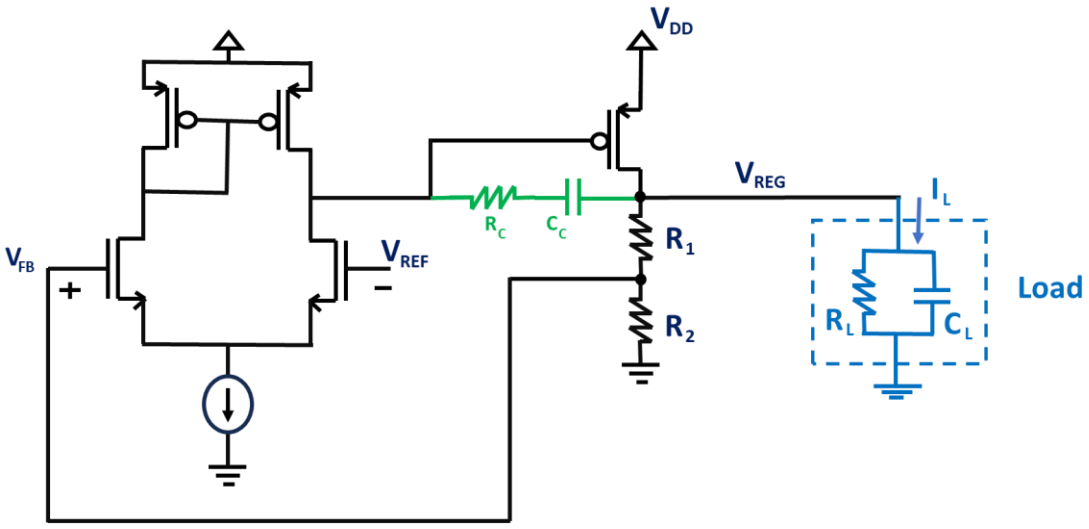


Fig.6. LDO with Miller Compensation

In Miller compensation, a capacitor C_C is connected in negative feedback between the pass device's gate (input) & drain (output) to give a large equivalent capacitor at the gate. This causes the dominant pole at the pass device's gate to be shifted away from the non-dominant pole at the pass device's drain, resulting in a better phase margin & a more stable system. [7-8] The following equations show the frequencies at which the dominant pole, the non-dominant pole, & the zero are located:

$$Dominant\ Pole: \quad \omega_{P1} = \frac{1}{r_{O,diff} \cdot \left(\left(g_{m,pass} \cdot R_L \right) \cdot C_C + C_{gs,pass} \right)} \tag{5}$$

$$Non-Dominant\ Pole: \quad \omega_{P2} = \frac{g_{m,pass}}{C_{gs,pass} + C_L} \tag{6}$$

$$Zero: \quad \omega_Z = \frac{1}{C_C \cdot \left({}^{1}/_{g_{m,pass}} - R_C \right)} \tag{7}$$

3.2.2 RC (Lead-Lag) Compensation

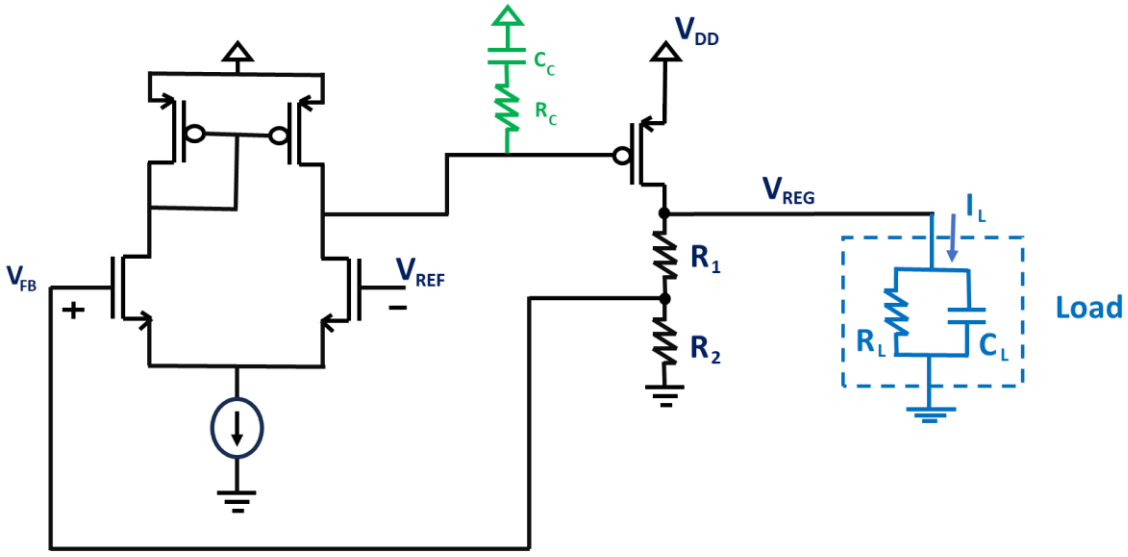


Fig.7. LDO with RC (Lead-Lag) Compensation

In this RC compensation, the added capacitor C_C & resistance R_C are used to create a pole & a zero pair. The values of C_C & R_C are determined to create the dominant pole and to set the zero location to cancel out the closest non-dominant pole. [9]

$$Dominant\ Pole: \quad \omega_{P1} = \frac{1}{(r_{O,diff} + R_C).C_C} \tag{8}$$

$$Zero: \quad \omega_Z = \frac{1}{R_C \,.\, C_C} \tag{9}$$

$$Non-Dominant\ Poles: \quad \omega_{P2} = \frac{1}{C_{gs,pass}\,(r_{O,diff} \;//\; R_C)} \tag{10}$$

$$\omega_{P3} = \frac{1}{R_L \,.\, C_L} \tag{11}$$

4. Results and Discussion

4.1 DC Analysis

In the DC analysis, the transistors are sized to ensure they are all in saturation for minimum load current (maximum $V_{G,pass}$) & for maximum load current (minimum $V_{G,pass}$). The values of the resistive divider are chosen to provide the 5/6 ratio from V_{REG} to V_{FB} & should be much bigger than R_L so that almost all the current from the pass-device flows in the load. The total current consumption of the LDO, excluding the load current, is ~250uA. This includes 100uA from the OpAmp (50uA at both sides of the current-mirror) & 150uA from the resistive divider.

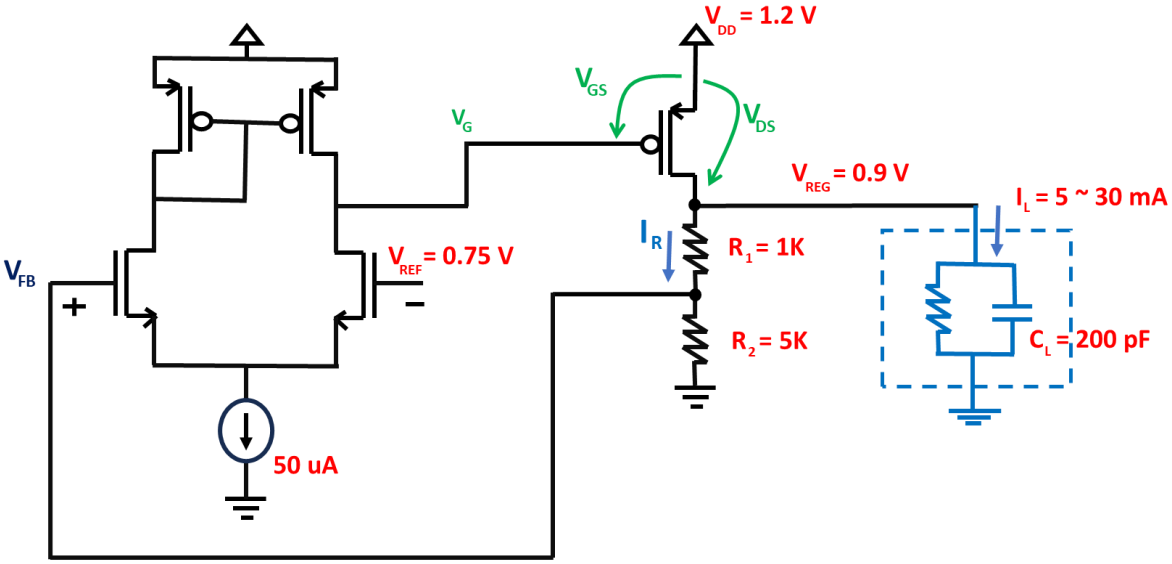


Fig.8. LDO with design values

4.2 Monte-Carlo Analysis

The Monte-Carlo analysis is done based on the DC analysis testbench to measure the offset between V_{FB} & V_{REF}. The offset's mean & variation are measured at different X values, where X is the scaling factor multiplied by all the transistor dimensions (W & L). As X increases, mismatch reduces [10], as a result, the offset & its variation reduce. Running Monte-Carlo for 500 samples, the offset variation Vs X is shown in Table 1.

Table 1: Monte-Carlo Simulation Results

Aspect Ratio = $\frac{X.W}{X.L}$	Offset	
	Mean	Variation
X = 1	3.698m	6.786m
X = 2	1.552m	3.248m
X = 4	0.770m	1.513m

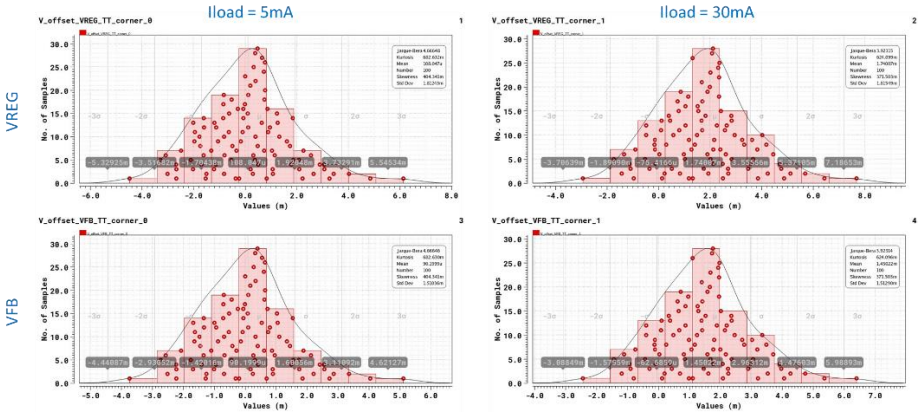


Fig.9. Offset Probability Distributions for X=4

4.3 AC, STB, & Transient Analyses

While changing the locations of the poles & the zero introduced by the compensation network, AC, STB, & Transient Analyses are observed together, since their measurements are all related. Through the AC analysis, we can observe the PSRR & the noise profiles of the system, while the STB analysis shows the closed-loop gain and phase. From equation (12), we can see how PSRR is related to the open-loop gain [11]. From the sweeps in Fig. 10, we can also see how increasing the PM (improving the stability) reduces the ringing in the output's step-response [12].

$$PSRR^{-1}(s) = \frac{V_{REG}(s)}{V_{DD}(s)} = \frac{H_{supply}(s)}{(1+ L_{OL}(s))} \tag{12}$$

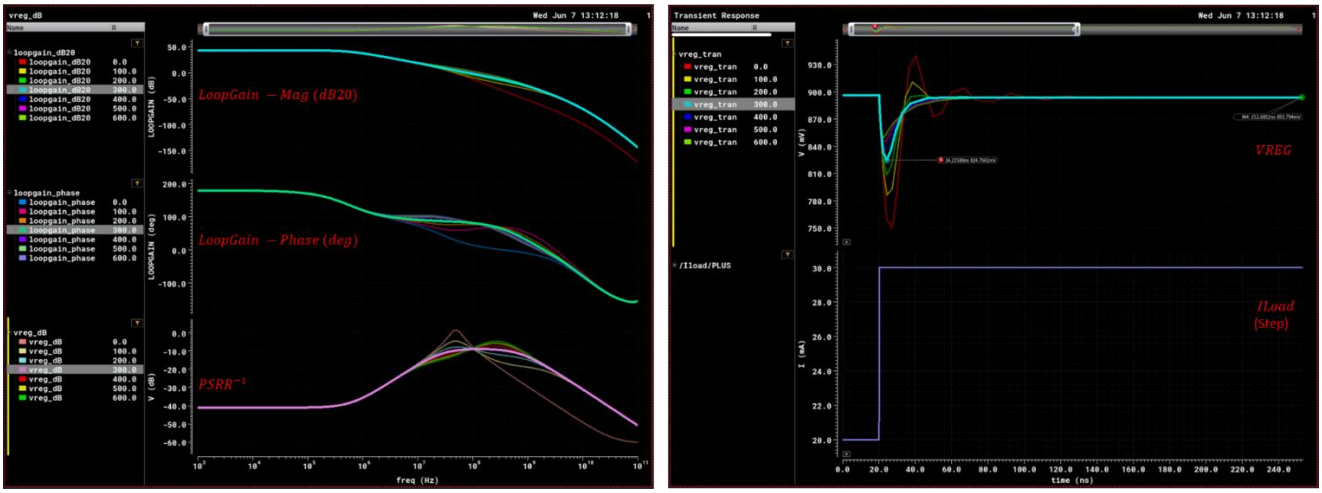


Fig.10. PSRR, Gain, Phase, & Step response of the LDO at different R_C

(Plots are for LDO with RC (Lead-Lag) Compensation & with I_{load} = 30m)

4.4 Noise Analysis

The output noise is related to the closed-loop gain, thus also effected by the zero & pole locations. The main contributors of the noise in the system are the bandgap (reference voltage), the resistor divider, and the input stage of the Opamp [13-14]. The bandgap noise is not considered in this study, so the noise observed at V_{REG} is mainly due to the noise of the resistor divider & the Opamp shaped by the closed-loop. The output noise profile is shown in Fig. 11.

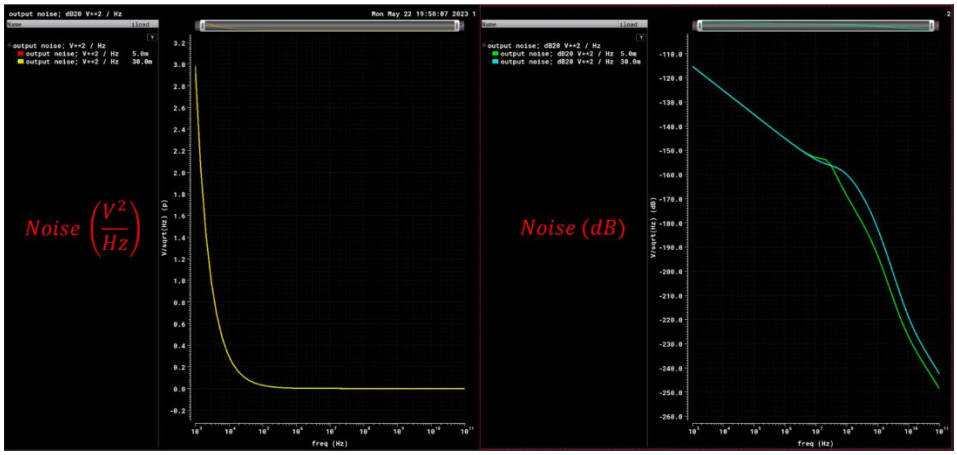
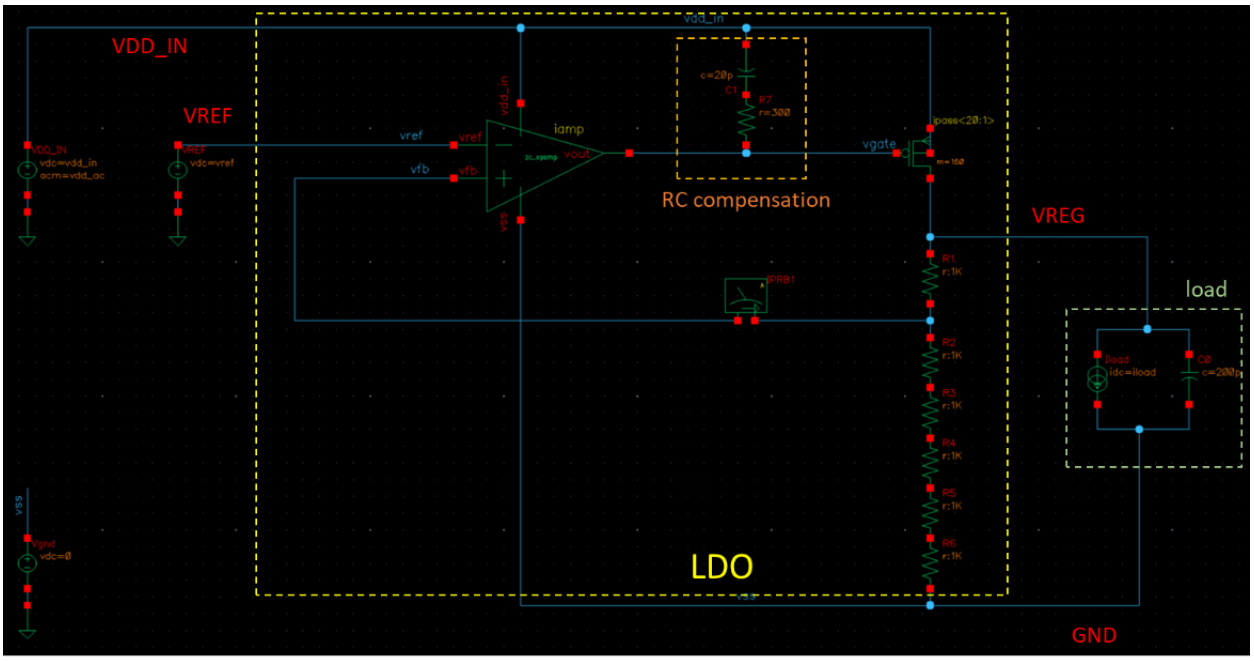


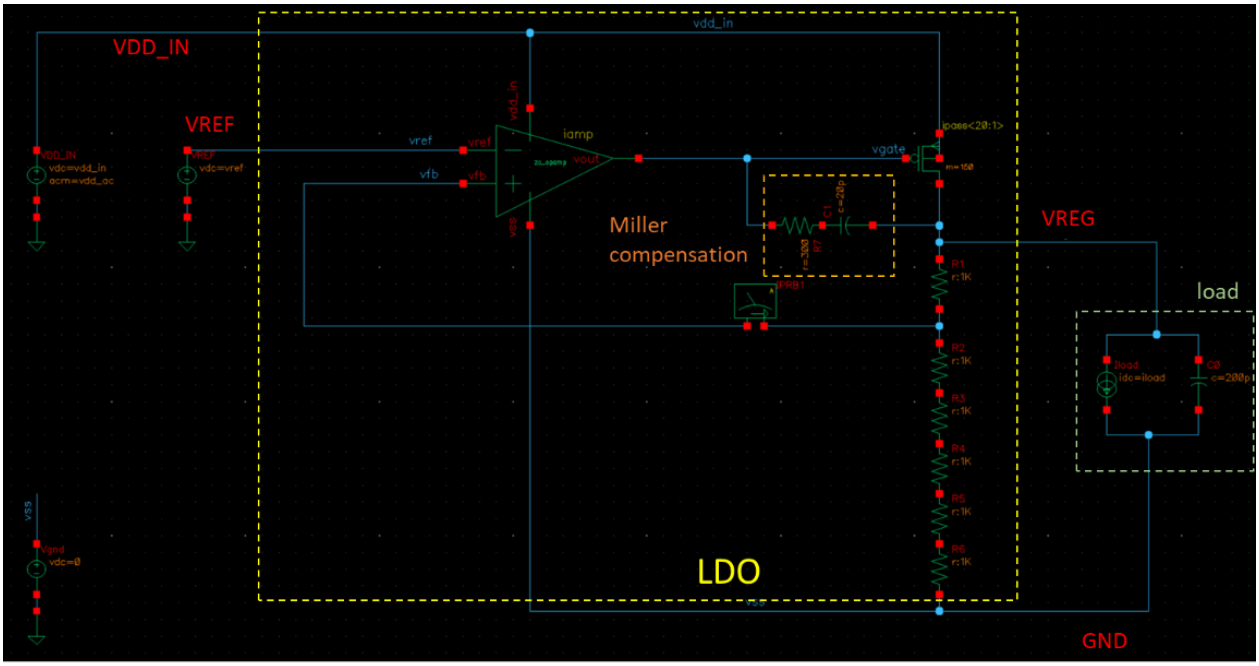
Fig.11. Output Noise of the LDO at I_{load} = 5m & 30m

4.5 Schematics & Results

The circuit schematics used for simulations on Virtuoso are shown in Fig. 12. Table 2 gives a summary of the results. Based on the PSRR results, the RC compensation is the preferred compensation technique in this study.



(a)



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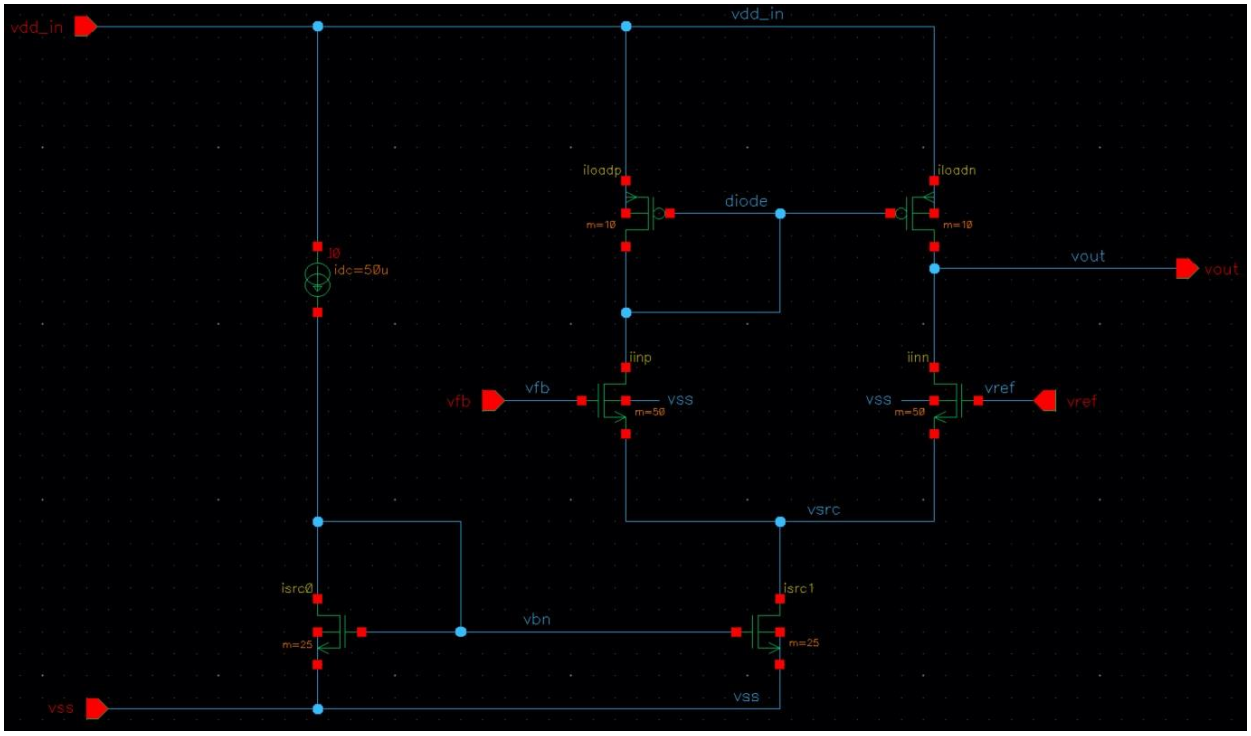

(c)

Fig.12. LDO Schematics on Virtuoso Cadence

(a) with RC Compensation, (b) with Miller Compensation, (c) OpAmp used as Error Amplifier

Table 2: Summary of Final Results

Parameters		Value	
Supply Voltage		1.2 V	
Reference Voltage		0.75 V	
Regulated Voltage		0.9 V	
Load Current Range		5 mA – 30 mA	
Load Capacitor		200 pF	
Compensation	R	300 Ohms	
	C	20 pF	
		RC (Lead-Lag) Comp.	**Miller Comp.**
DC Gain (min)		43.22 dB	
Phase-Margin (min)		60.34 deg	99.23 deg
PSRR	@ DC	41.14 dB	41.14 dB
	@ 1 MHz	35.73 dB	15.33 dB
	@ 1 GHz	13.13 dB	8.24 dB
	Worst case	8.89 dB	1.44 dB
Output Noise	Integrated from 1MHz to 10GHz	191.7 uV^2	104 uV^2
Settling time (99%)		16.29 ns	20.05 ns
Offset	Mean (μ)	770.2 uV	
	Std Dev (σ)	1.513 mV	

5. Conclusion

This paper explores the design process and technical foundation of a traditional LDO circuit. By conducting simulations, we investigated the impact of two compensation techniques on PSRR, PM, Noise, and Settling time.

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