Low Dropout Regulators

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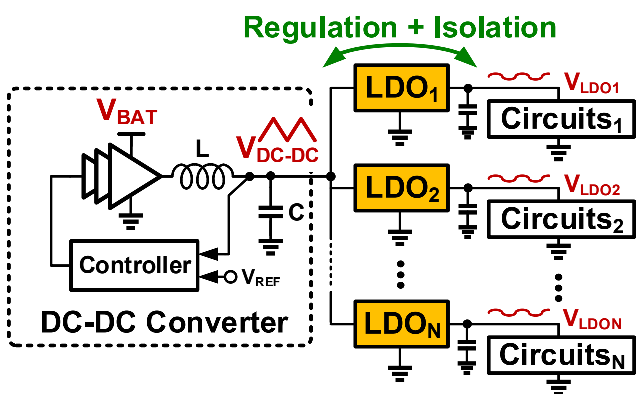
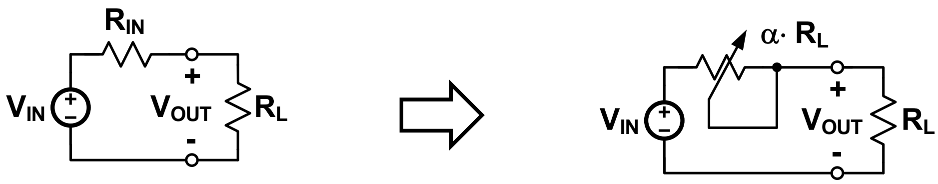
Updated Slides: https://uofi.box.com/CICC15-LDO

Role of a Low Dropout Regulator



- ❑ Ripple suppression
- ❑ Isolation
- ❑ Low noise

Conceptual LDO Regulator Implementation



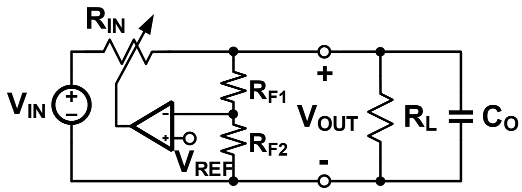
$$V_{OUT} = \frac{R_L}{R_{IN} + R_L} V_{IN}$$

$$V_{OUT} = \frac{V_{IN}}{\alpha + 1}$$

- ❑ Output voltage generated using a resistive divider
  - ■ Fixed divide ratio → sensitive to load current changes

- ❑ Feedback loop regulates R_{IN} such that it is always a desired fraction of load current
  - ■ Output voltage is independent of load current

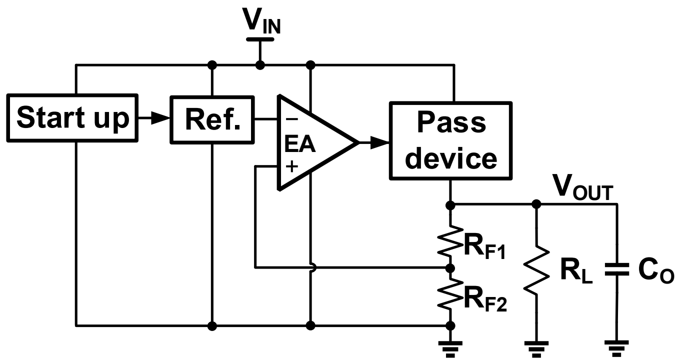
Conceptual LDO Regulator Implementation



- ❑ Feedback adjusts R_{IN} such that $V_{OUT} = V_{REF}$
  - ■ Ideally independent of V_{IN}

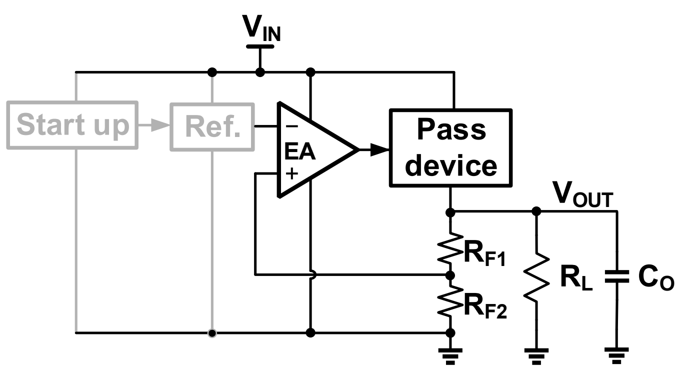
- ❑ Output capacitor (C_O) used to “filter” ripple/noise

LDO Block Diagram



- Bandgap circuit provides fixed reference voltage
- Feedback resistors used to level shift output voltage
  - Output voltage can be varied by changing R_{F2}
- Variable resistor is implemented using “pass device”
  - Usually NMOS or PMOS

LDO Block Diagram



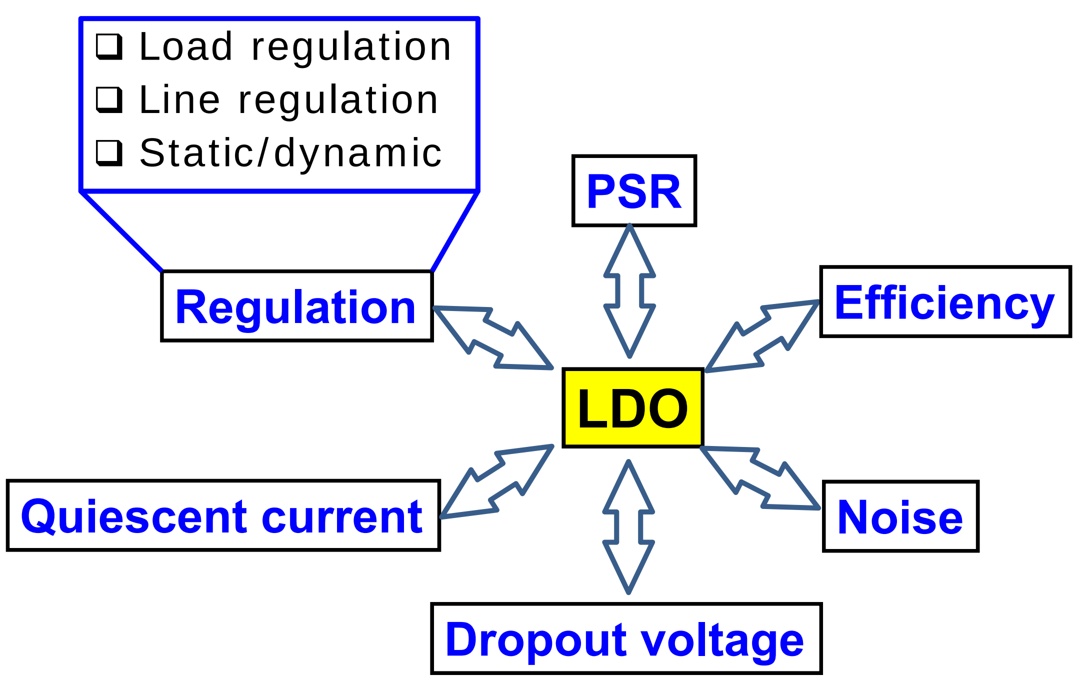
- Bandgap circuit provides fixed reference voltage
- Feedback resistors used to level shift output voltage
  - Output voltage can be varied by changing R_{F2}
- Variable resistor is implemented using “pass device”
  - Usually NMOS or PMOS

- **This tutorial: Regulation loop design**

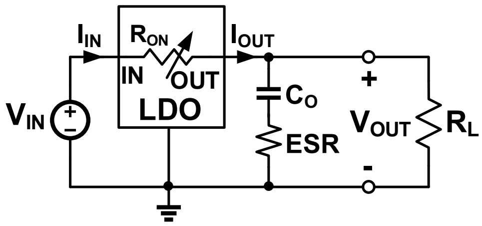
Tutorial Roadmap

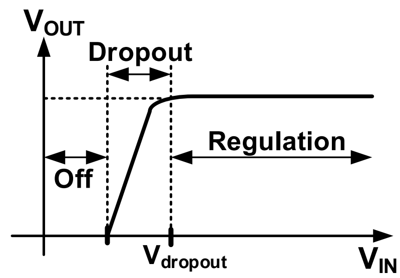
- ❑ Performance metrics
- ❑ Stability
- ❑ Power supply rejection
- ❑ Summary

Performance Metrics



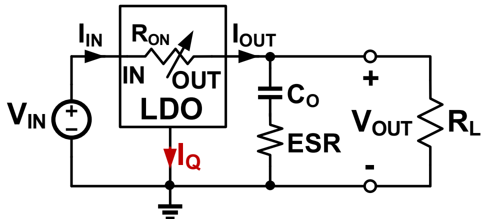
Dropout Voltage





- V_{IN}-V_{OUT} at which V_{OUT} is no longer regulated
- Dropout voltage depends on pass device/load current
- Dropout voltage is in the range of 0.1 to 0.5V

Quiescent Current



$$I_Q = I_{IN} - I_{OUT}$$

- I_Q is mainly due to bias currents in:
  - Reference generator
  - Error amplifier
  - Feedback resistors
  - Support circuits
- I_Q is almost independent of load current

Efficiency

$$\text{Current efficiency}: \eta_{\mathrm{I}} = \frac{\mathrm{I_{OUT}}}{\mathrm{I_{IN}}} \times 100$$

$$\eta_{\mathrm{I}} = \frac{\mathrm{I_{OUT}}}{\mathrm{I_{OUT}} + \mathrm{I_Q}} \times 100$$

Efficiency

$$\text{Current efficiency}: \eta_{\mathrm{I}} = \frac{\mathrm{I_{OUT}}}{\mathrm{I_{IN}}} \times 100$$

$$\eta_{\mathrm{I}} = \frac{\mathrm{I_{OUT}}}{\mathrm{I_{OUT}} + \mathrm{I_Q}} \times 100$$

$$\text{Power efficiency}: \eta = \frac{\mathrm{I_{OUT}} \mathrm{V_{OUT}}}{(\mathrm{I_{OUT}} + \mathrm{I_Q})\, \mathrm{V_{IN}}} \times 100 \approx \frac{\mathrm{V_{OUT}}}{\mathrm{V_{IN}}} \times 100$$

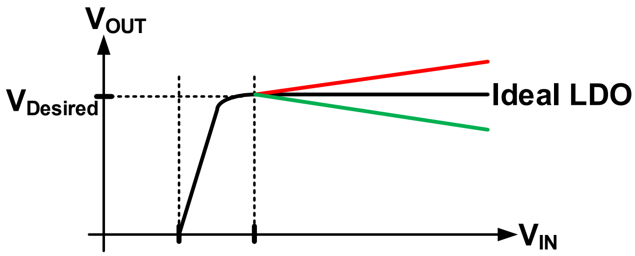
Example:

$$\mathrm{V_{OUT}} = 1.8\,\mathrm{V}, \quad \mathrm{V_{IN}} = 2.5\,\mathrm{V}, \quad \mathrm{I_{OUT}} = 25\,\mathrm{mA}, \quad \mathrm{I_Q} = 50\,\mu\mathrm{A}$$

$$\begin{aligned} \Longrightarrow \eta_{\mathrm{I}} &= 99.8\% \\ \eta &= 71.86\% \end{aligned}$$

Line Regulation

- Measure of LDO's ability to maintain desired V_{OUT} with varying V_{IN} (static metric)



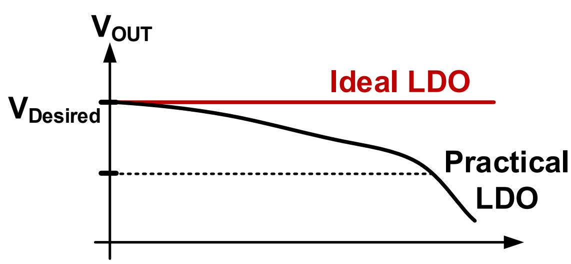
$$\text{Line regulation } L_R = \frac{\Delta V_{OUT}}{\Delta V_{IN}}$$

$$\Delta V_{LR} = \Delta V_{IN} \times \text{Line regulation}$$

$$\Delta V_{LR} = [\text{mV/V}]@\Delta V_{IN} = V_1$$

Load Regulation

- Measure of LDO's ability to maintain desired V_{OUT} with varying I_{OUT}

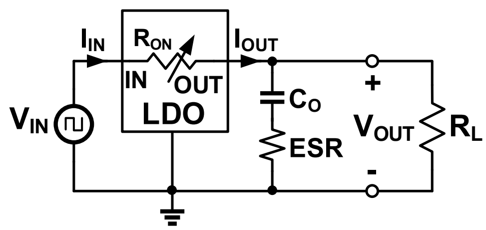


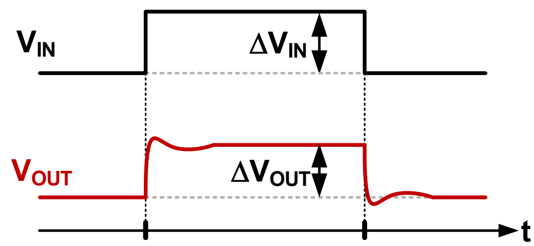
$$\text{Load regulation} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}}$$

$$\Delta V_{LDR} = \Delta I_{OUT} \times \text{Output resistance}$$

Line Transient Response

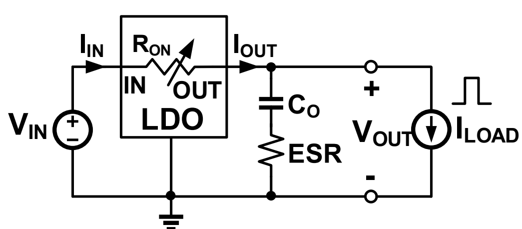
- Measure of LDO's ability to maintain desired V_{OUT} with varying V_{IN} (dynamic metric)

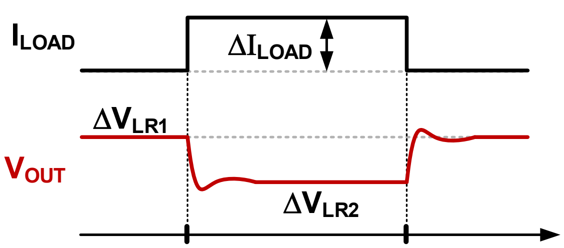




Load Transient Response

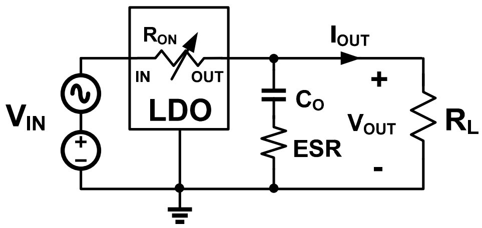
- Measure of LDO's ability to maintain desired V_{OUT} with varying I_{OUT} (dynamic metric)

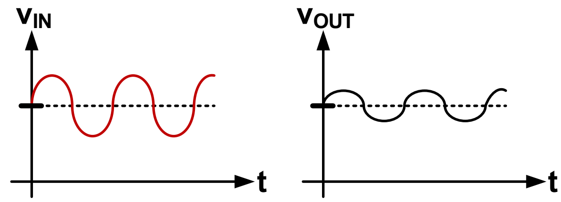




Power Supply Rejection

- Regulator's ability to reject V_{OUT} variations due to changes in V_{IN}





$$\boxed{\mathrm{PSR(f)} = \frac{\Delta \mathrm{V_{OUT}(f)}}{\Delta \mathrm{V_{IN}(f)}}}$$

- Similar to line regulation BUT measured vs. frequency

- Similar to line transient BUT measured for "small signal" variations

Accuracy

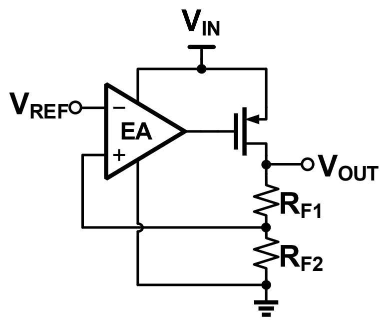
- Includes all non-ideal effects:

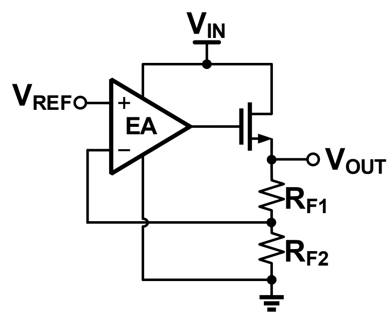
1. Line/load regulation
2. Reference voltage drift
3. Error amplifier offset drift
4. Feedback resistor tolerance

$$\boxed{\mathrm{Accuracy} \approx |\Delta \mathrm{V_{LR}}| + |\Delta \mathrm{V_{LDR}}| + \sqrt{\Delta \mathrm{V^2_{O,REF}} + \Delta \mathrm{V^2_{O,EA}} + \Delta \mathrm{V^2_{R}}}}$$

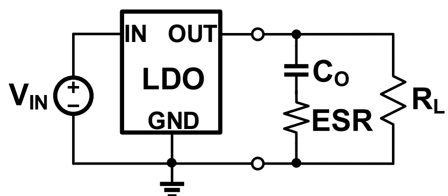
LDO Types

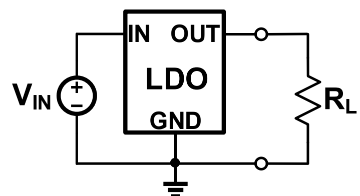
Pass device: PMOS or NMOS



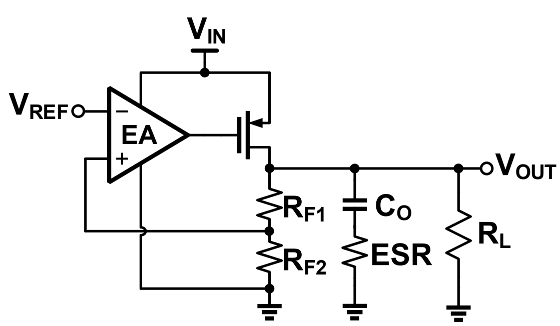


Cap or Cap-less LDOs





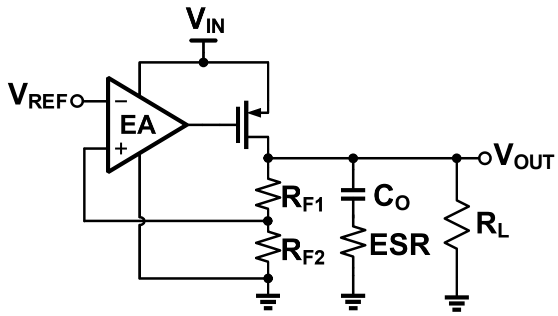
PMOS LDO w/ Output Capacitor[1]

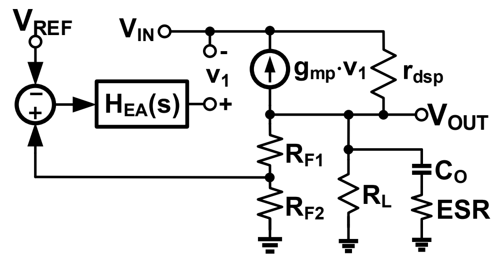


$$V_{OUT} = V_{REF}\left[1 + \frac{R_{F1}}{R_{F2}}\right]$$

- ❑ PMOS pass device
  - ■ Dropout voltage is approximately V_{DSAT} (0.1-0.4V)
- ❑ Output capacitor C_O placed off chip
  - ■ Comes with ESR

Output Voltage Calculation



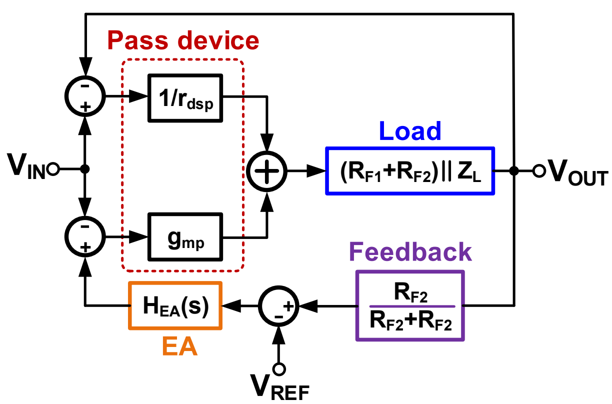


- Use KCL/KVL to calculate transfer functions

$$H_{IN} = \frac{V_{OUT}}{V_{IN}} \qquad H_{REF} = \frac{V_{OUT}}{V_{REF}}$$

$$V_{OUT} = H_{IN}V_{IN} + H_{REF}V_{REF}$$

Signal Flow Representation



$$Z_L = R_L || \left(\frac{1}{sC_O} + R_{ESR}\right)$$

$$@\ DC\ Z_L = R_L \qquad H_{EA}(s) = A_{EA0} \qquad (R_{F1} + R_{F2})||R_L = R_{FL}$$

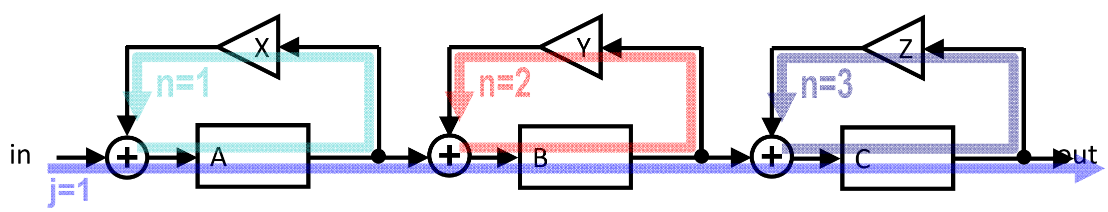
- Use Mason's gain rule to find transfer functions

Mason's Gain Rule

$$\boxed{H = \frac{\sum_j M_j \Delta_j}{\Delta}}$$

H = transfer function of the system
j = index number of a forward path from input to output
M_j = gain of forward path j from input to output
$\Delta = 1-\sum(\text{all loop gains})$
$+\sum(\text{nontouching loop gains multiplied two at a time})$
$-\sum(\text{nontouching loop gains multiplied three at a time})$
$+\sum(\text{nontouching loop gains multiplied four at a time})\cdots$
Δ_j = Δ calculated after excluding all feedback loops that intersect with forward path j

Mason's Gain Rule: Example

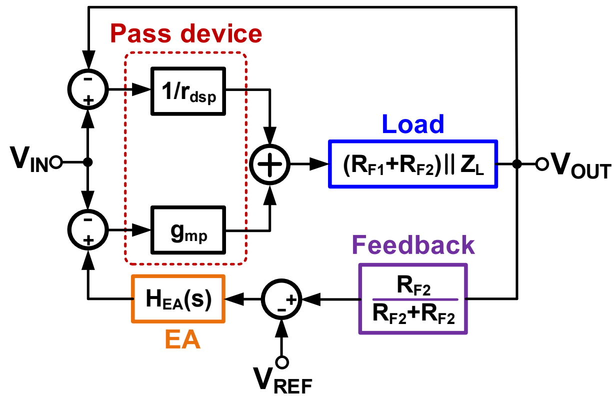


$$H = \frac{\sum_j M_j \Delta_j}{\Delta}$$

- M_1 = ABC
- Δ_1 = 1
- $\Delta = 1 - (L_1 + L_2 + L_3) + (L_1 L_2 + L_2 L_3 + L_3 L_1) - (L_1 L_2 L_3)$
  $= 1 - (AX+BY+CZ) + (AXBY+BYCZ+CZAX) - (AXBYCZ)$

$$\boxed{H = \frac{ABC}{1-(AX+BY+CZ)+(AXBY+BYCZ+CZAX)-(AXBYCZ)}}$$

Output Voltage Calculation (due to V_{REF})

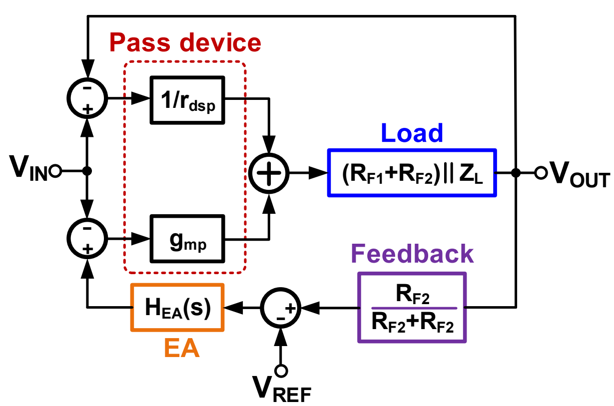


$$\frac{V_{OUT}}{V_{REF}} = \frac{A_{EA0}.g_{mp}.R_{FL}}{1 + A_{EA0}.g_{mp}.R_{FL}.\beta + R_{FL}/r_{dsp}}$$

$$\boxed{\frac{V_{OUT}}{V_{REF}} = \frac{A_{EA0}.g_{mp}.r_{dsp}}{1 + A_{EA0}.g_{mp}.r_{dsp}.\beta + r_{dsp}/R_{FL}}}$$

$$\approx \frac{1}{\beta} \text{ if } A_{EA0}.g_{mp}.R_{FL}.\beta \gg 1$$

Output Voltage Calculation (due to V_{IN})



$$\beta = \frac{R_{F2}}{R_{F1} + R_{F2}}$$

$$@ \text{ DC } Z_L = R_L$$

$$H_{EA}(s) = A_{EA0}$$

$$(R_{F1} + R_{F2})\,||R_L = R_{FL}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{g_{mp}.R_{FL} + 1/r_{dsp}R_{FL}}{1 + A_{EA0}.g_{mp}.R_{FL}.\beta + \frac{R_{FL}}{r_{dsp}}}$$

$$\boxed{\frac{V_{OUT}}{V_{IN}} = \frac{1 + g_{mp}r_{dsp}}{1 + \left(A_{EA0}.g_{mp}.r_{dsp}\beta + \frac{r_{dsp}}{R_{FL}}\right)}}$$

$$\frac{V_{OUT}}{V_{IN}} \approx \frac{1}{A_{EA0}.\beta} \quad \text{if } g_{mp}r_{dsp} \gg 1$$

Line Regulation

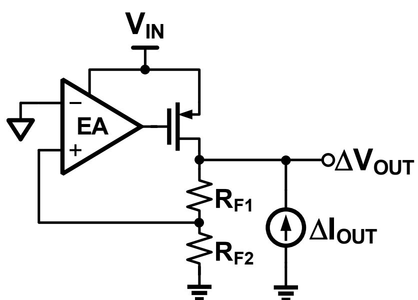
$$L_R = \frac{\Delta V_{OUT}}{\Delta V_{IN}} = \frac{1 + g_{mp} r_{dsp}}{1 + A_{EA0} . g_{mp} . r_{dsp} . \beta}$$

$$\Longrightarrow L_R \approx \frac{1}{\beta A_{EA0}}$$

$$\Delta V_{OUT} = \frac{\Delta V_{IN}}{\beta A_{EA0}} + \frac{(\Delta V_{REF} + \Delta V_{OS})}{\beta}$$

- ❑ Changes in V_{IN} suppressed by error amp. gain
- ❑ Reference and offset voltage drift amplified by feedback factor

Load Regulation



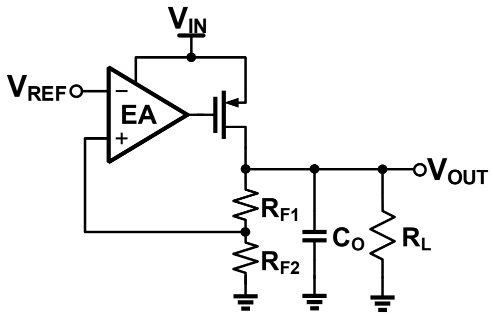
$$L_{DR} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}}$$

$$\Delta I_{OUT} = \frac{\Delta V_{OUT}}{[r_{dsp} || (R_{F1} + R_{F2})]} + \Delta V_{OUT} . \beta . A_{EA0} . g_{mp}$$

$$\Longrightarrow L_{DR} \approx \frac{r_{dsp} || (R_{F1} + R_{F2})}{1 + \beta A_{EA0} . g_{mp} . [r_{dsp} || (R_{F1} + R_{F2})]} \approx \frac{r_{dsp}}{1 + T_0}$$

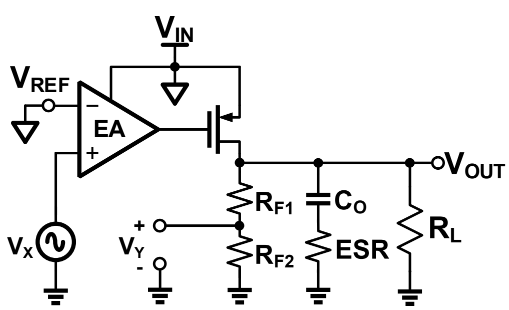
- ❑ Output impedance lowered by loop gain

Stability



- ❑ Closely-spaced poles compromise stability
- ❑ Needs frequency compensation
  - ■ Pole-zero "cancellation"
  - ■ Pole splitting

Loop Gain

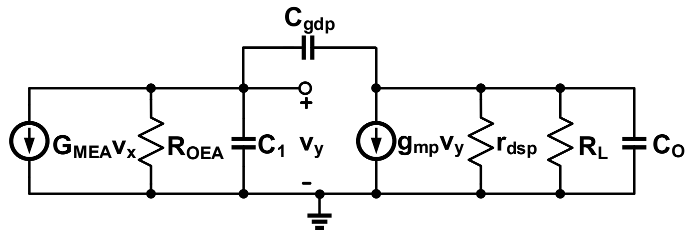


$$\text{Loop gain } T(s) = \frac{-V_Y}{V_X} = H_{EA}(s).g_{mp}.\left[r_{dsp} || \left(R_{F1} + R_{F2}\right) || Z_L\right].\beta$$

$$= A_{EA0}.g_{mp}.\left[r_{dsp} || \left(R_{F1} + R_{F2}\right)\right].\beta$$

$$\text{DC loop gain } T_0 \approx A_{EA0}.g_{mp}.r_{dsp}.\beta$$

Loop Gain Transfer Function



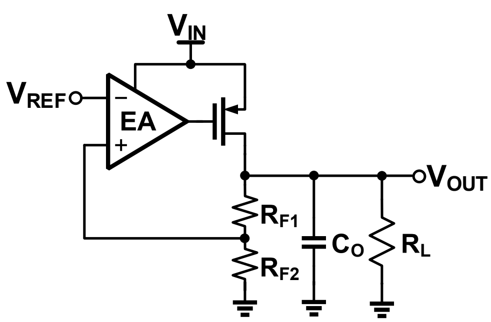
$$T(s) = \frac{-v_y(s)}{v_x(s)} = \frac{\beta G_{MEA}.R_{OEA}.g_{mp}.R_{out}\left(1 - sC_{gdp}/g_{mp}\right)}{1 + bs + as^2}$$

$$R_{OUT} = r_{dsp} || R_L || (R_{F1} + R_{F2})$$

$$a = (C_O + C_{gdp})R_{OUT} + (C_1 + C_{gdp})R_{OEA} + g_{mp}R_{OUT}R_{OEA}C_{gdp}$$

$$b = R_{OEA}R_{OUT}(C_1C_{gdp} + C_1C_O + C_OC_{gdp})$$

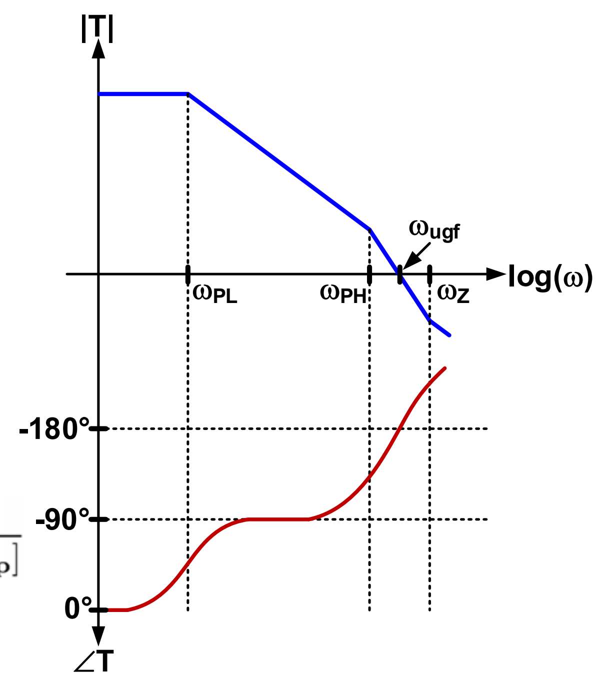
Approximate Pole Zero Locations



$$\omega_{PL} \approx \frac{1}{R_{OUT}.C_O}$$

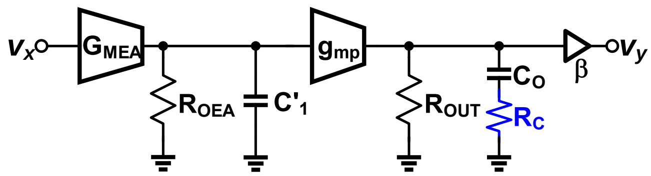
$$\omega_{PH} \approx \frac{1}{R_{OEA}.\left[C_1 + g_{mp}.R_{OUT}.C_{gdp}\right]}$$

$$\omega_Z \approx \frac{g_{mp}}{C_{gdp}}$$



Frequency Compensation – I [1]

- Introduce zero by adding series resistor R_C



$$Z_{out} = R_{OUT} || \left(\frac{1}{sC_O} + R_C \right)$$

$$= \frac{(1 + sR_C C_O) . R_{OUT}}{1 + s(R_{OUT} + R_C) . C_O}$$

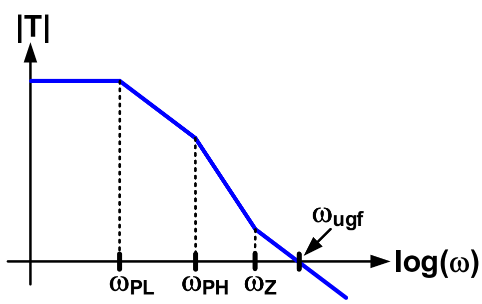
$$\boxed{T(s) = \frac{\beta . G_{MEA} . R_{OEA} . g_{mp} . R_{OUT} . (1 + s/\omega_Z)}{(1 + s/\omega_{PH})(1 + s/\omega_{PL})}}$$

Loop Gain Bode Plot (Compensated)

$$\omega_Z = \frac{1}{R_C . C_O}$$

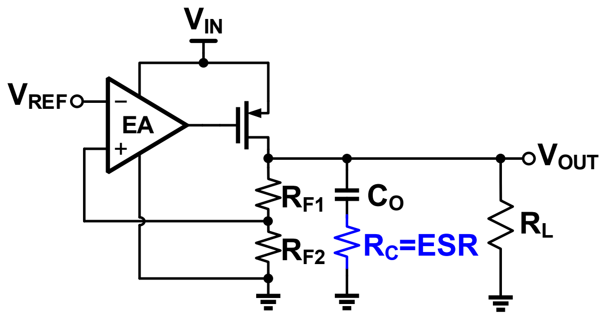
$$\omega_{PH} = \frac{1}{R_{OEA} . C'_1}$$

$$\omega_{PL} = \frac{1}{(R_{OUT} + R_C) . C_O}$$



$$\boxed{\Phi_M \approx \arctan\left(\frac{\omega_{ugf}}{\omega_Z}\right)}$$

Typical LDO Implementation

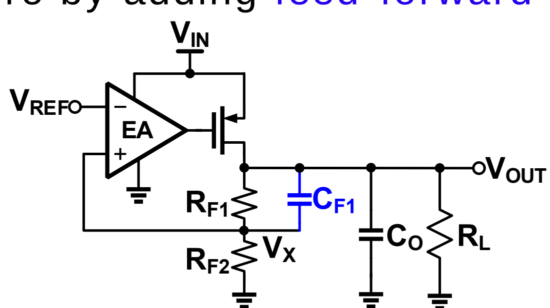


- Choose C_O and R_{ESR} to achieve desired phase margin
- Vendors specify min. R_{ESR} and C_O for stable operation

Can we introduce zero without using ESR resistance?

Frequency Compensation – II[2]

- Introduce zero by adding feed-forward capacitor

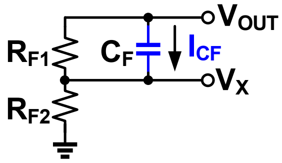


$$\frac{V_X(s)}{V_{OUT}(s)} = \left(\frac{R_{F2}}{R_{F1}+R_{F2}}\right)\cdot\left(\frac{1+sC_{F1}R_{F1}}{1+sC_{F1}(R_{F1}||R_{F2})}\right)$$

$$\boxed{\omega_{ZF} = \frac{1}{R_{F1}C_{F1}}} \qquad \boxed{\omega_{PF} = \frac{1}{(R_{F1}||R_{F2})C_{F1}}}$$

$$\frac{\omega_{PF}}{\omega_{ZF}} = 1 + \frac{R_{F1}}{R_{F2}} = \frac{V_{OUT}}{V_{REF}}$$

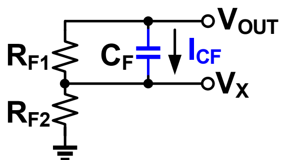
How to Eliminate ω_{PF}?



$$(V_{OUT} - V_X)(sC_F + 1/R_{F1}) = V_X/R_{F2}$$

$$V_{OUT}(sC_F + 1/R_{F1}) = V_X(1/R_{F1} + 1/R_{F2} + sC_F)$$

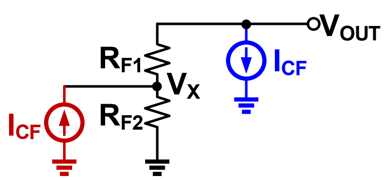
How to Eliminate ω_{PF}?



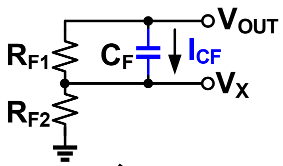
$$(V_{OUT} - V_X)(sC_F + 1/R_{F1}) = V_X/R_{F2}$$

$$V_{OUT}(sC_F + 1/R_{F1}) = V_X(1/R_{F1} + 1/R_{F2} + sC_F)$$

$$I_{CF} = (V_{OUT} - V_X)(sC_F)$$



How to Eliminate ω_{PF}?



$$(V_{OUT} - V_X)(sC_F + 1/R_{F1}) = V_X/R_{F2}$$

$$V_{OUT}(sC_F + 1/R_{F1}) = V_X(1/R_{F1} + 1/R_{F2} + sC_F)$$

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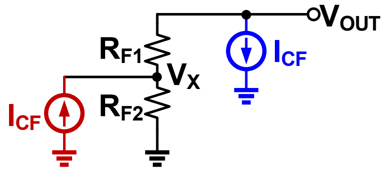
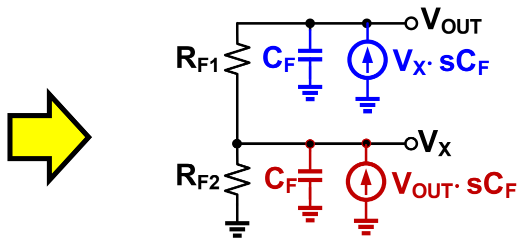
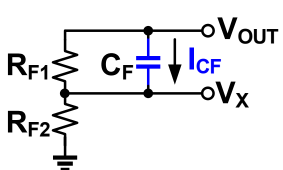




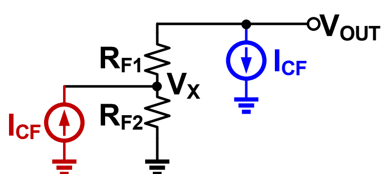
How to Eliminate ω_{PF}?

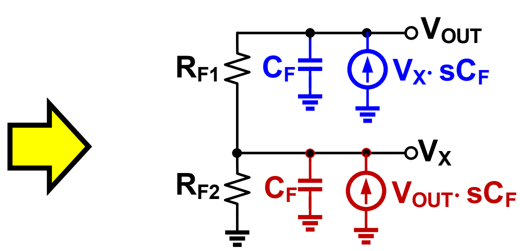


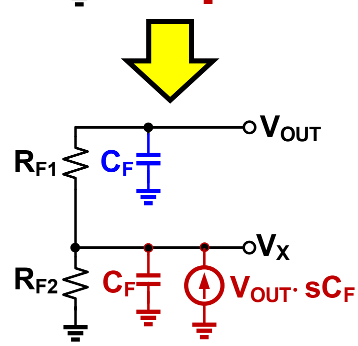
$$(V_{OUT} - V_X)(sC_F + 1/R_{F1}) = V_X/R_{F2}$$

$$V_{OUT}(sC_F + 1/R_{F1}) = V_X(1/R_{F1} + 1/R_{F2} + sC_F)$$

$$I_{CF} = (V_{OUT} - V_X)(sC_F)$$



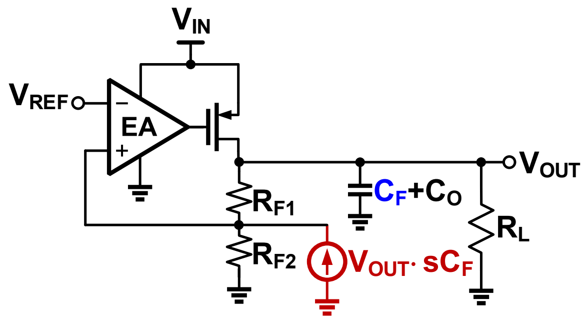




$$\frac{V_X(s)}{V_{OUT}(s)} = \left(\frac{R_{F2}}{R_{F1} + R_{F2}}\right)(1 + sC_{F1}R_{F1})$$

$$\omega_{ZF} = \frac{1}{R_{F1}C_F}$$

Frequency Comp. – II Implementation



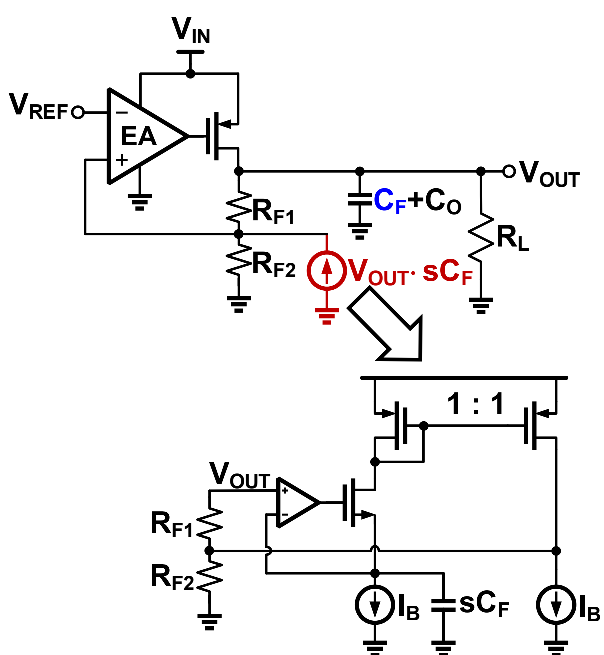
$$\omega_{PL} = \frac{1}{R_{OUT}\left(C_O - \frac{C_F}{\beta}\right)}$$

$$\omega_{PH} = \frac{1}{R_{OEA}\left[C_1 + g_{mp}R_{OUT}C_{gdp}\right]} \text{ (same as before)}$$

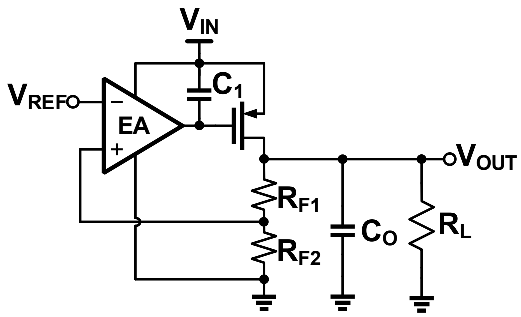
$$\omega_{ZF} = \frac{1}{R_{F1}C_F}$$

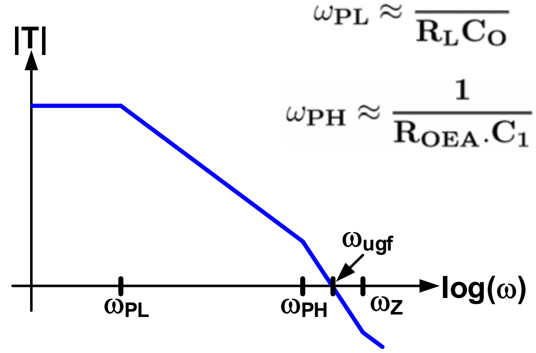
$$\omega_{ZF} \sim \omega_{PH} < \omega_{UGF}$$

VCCS Implementation



Frequency Compensation – III





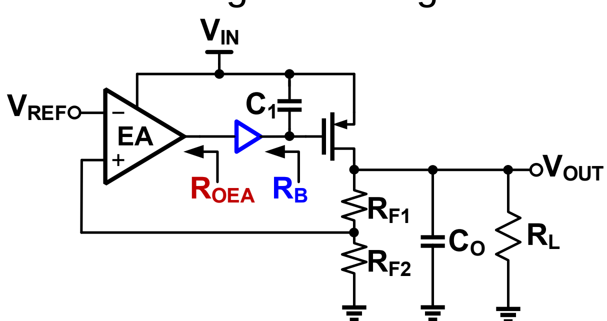
$$\omega_{PL} \approx \frac{1}{R_L C_O}$$

$$\omega_{PH} \approx \frac{1}{R_{OEA}.C_1}$$

- ❑ Make $\omega_{PH} > \omega_{ugf}$
- ❑ Reducing C_1 is difficult
  - C_1 is set by I_{LOAD} and V_{DSAT} of pass device
- ❑ Reducing R_{OEA} degrades load/line regulation

Frequency Compensation – III[3]

- ❑ Shield C_1 from loading EA using a buffer

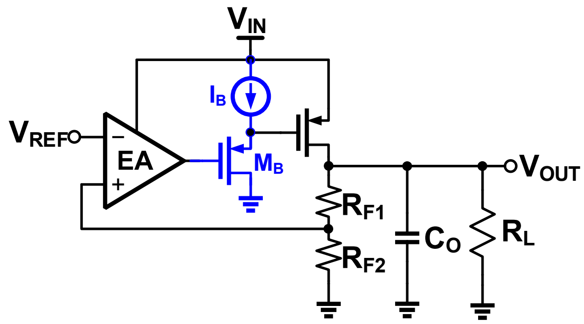


$$\omega_{PL} = \frac{1}{R_L C_O}$$

$$\omega_{PH} = \frac{1}{R_{OEA}.C_x} \qquad C_x = C_{OEA} + C_{IBUF} \ll C_1$$

$$\omega_{PB} = \frac{1}{R_B.C_1} \qquad R_B \ll R_{OEA}$$

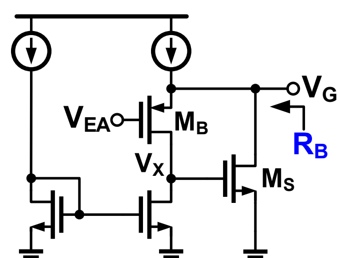
Buffer Implementation



$$R_B \approx 1/g_{mB} \propto \frac{1}{(W/L)I_B}$$

- ❑ Source follower as a buffer
  - Small input capacitance
  - Lower output impedance → large power
- ❑ Use feedback to lower output impedance

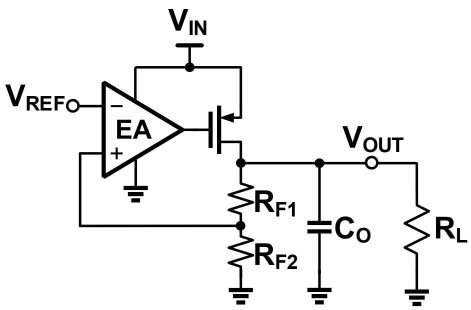
Improved Buffer



$$R_B \approx \frac{1}{(g_{mB}.R_x).g_{mS}} = \frac{1}{g_{mB}.(g_{mS}.R_x)}$$

- ❑ Shunt feedback reduces output impedance
  - Reduction factor proportional to loop gain
- ❑ Low power

Cap-less LDO



$$\omega_{P1} = \omega_{PL} = \frac{1}{R_{OEA}.(C_1 + g_{mp}.R_{OUT}.C_{gdp})}$$

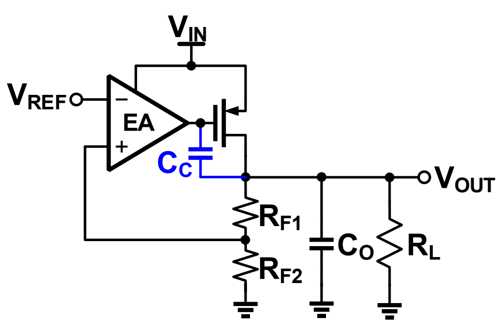
$$\omega_{P2} = \omega_{PH} = \frac{1}{R_{OUT}.C_O}$$

$$\omega_Z = \frac{g_{mp}}{C_{gdp}}$$

- ❑ C_O less than few hundred pF
  - ■ Difficult to make output pole dominant

- ❑ Need to make EA output pole dominant
  - ■ Miller compensation
  - ■ Cascode compensation

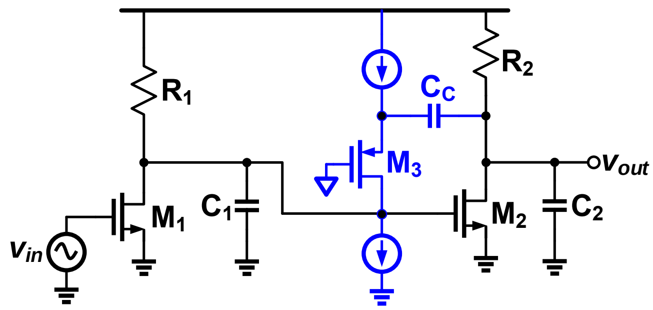
Miller Compensation



- ❑ Stability is compromised at large cap loads
  - ■ Need large compensation capacitor (C_O < $5C_C$)
  - ■ Sensitive to load current variation

- ❑ Poor high frequency PSR

Cascode Compensation[4]

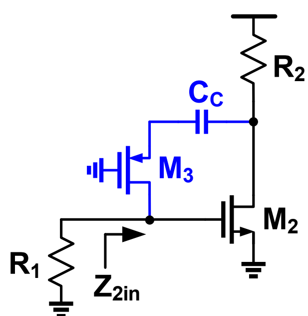


- ❑ Suppresses feed-forward path
  - ■ Moves RHP zero to a very high frequency

- ❑ Preserves Miller multiplication of C_C

- ❑ Pushes second pole to even higher frequencies

Cascode Compensation: Intuition

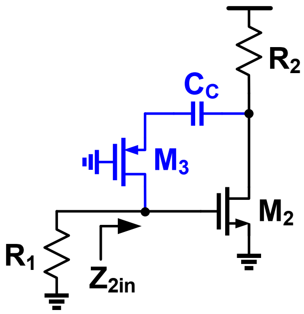


$$I_T = [V_T - (-g_{m2}R_2V_T)]\,C_C s$$

$$Z_{2in} = \frac{V_T}{I_T} = \frac{1}{(1+g_{m2}R_2)\,C_C}$$

$$\Longrightarrow\ \omega_{p1} \approx \frac{1}{R_1 g_{m2} R_2 C_C}$$

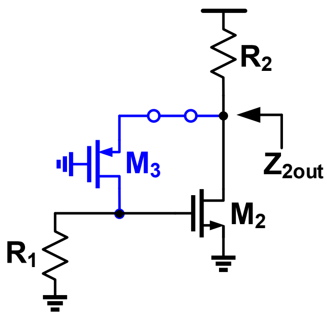
Cascode Compensation: Intuition



$$I_T = [V_T - (-g_{m2}R_2V_T)]\, C_C s$$

$$Z_{2in} = \frac{V_T}{I_T} = \frac{1}{(1+g_{m2}R_2)\, C_C}$$

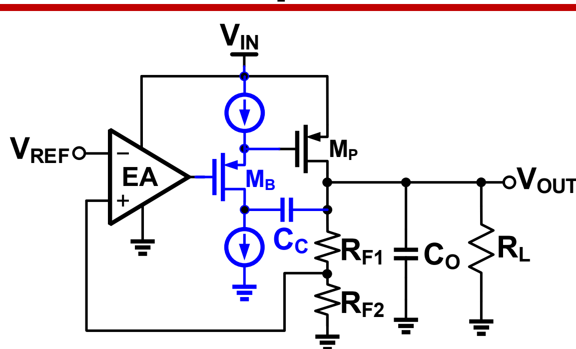
$$\Longrightarrow \ \omega_{p1} \approx \frac{1}{R_1 g_{m2} R_2 C_C}$$



$$I_T = g_{m2}(g_{m3}R_1)V_T + \frac{V_T}{R_2}$$

$$\Longrightarrow \ \omega_{p2} \approx \frac{g_{m2}\,(g_{m3}R_1)}{C_2}$$

LDO w/ Cascode Compensation

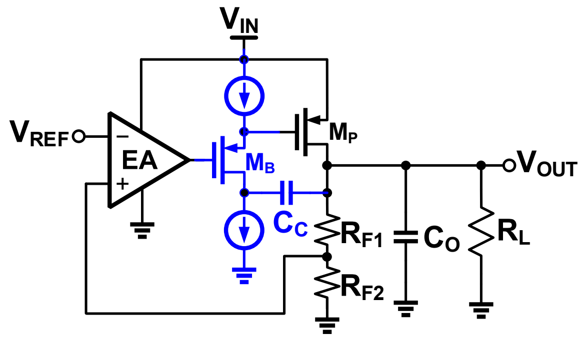


$$T(s) = \frac{\beta . g_{mEA} . g_{mp} . R_{OEA} . R_{OUT}}{1 + s\left(R_{OEA}.C_1 + R_{OUT}.C_C + R_{OUT}.C_O + g_{mEA}.R_{OUT}.R_{OEA}.C_C\right) + s^2 R_{OEA}.R_{OUT}.C_1\left(C_C + C_O\right)}$$

$$p_1 \approx \frac{1}{\left(R_{OEA}C_1 + R_{OUT}\left(C_C + C_O\right) + g_{mp}R_{OEA}R_{OUT}C_C\right)}$$

$$p_2 \approx \frac{R_{OEA}C_1 + R_{OUT}\left(C_C + C_O\right) + g_{mp}R_{OEA}R_{OUT}C_C}{R_{OEA}\cdot R_{OUT}\cdot C_1\left(C_C + C_O\right)}$$

Cascode Compensation[5]



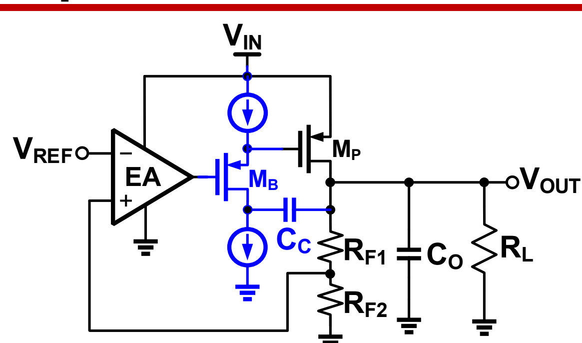
$$p_1 \approx \frac{1}{\left(R_{OEA}C_1 + R_{OUT}\left(C_C + C_O\right) + g_{mp}R_{OEA}R_{OUT}C_C\right)}$$

$$p_2 \approx \frac{R_{OEA}C_1 + R_{OUT}\left(C_C + C_O\right) + g_{mp}R_{OEA}R_{OUT}C_C}{R_{OEA}\cdot R_{OUT}\cdot C_1\left(C_C + C_O\right)}$$

For small C_O

$$p_1 \approx \frac{1}{g_{mp}R_{OEA}R_{OUT}C_C} \qquad p_2 \approx \frac{g_{mp}C_C}{C_1\left(C_C + C_O\right)}$$

Cascode Compensation[5]



$$p_1 \approx \frac{1}{\left(R_{OEA}C_1 + R_{OUT}\left(C_C + C_O\right) + g_{mp}R_{OEA}R_{OUT}C_C\right)}$$

$$p_2 \approx \frac{R_{OEA}C_1 + R_{OUT}\left(C_C + C_O\right) + g_{mp}R_{OEA}R_{OUT}C_C}{R_{OEA}\cdot R_{OUT}\cdot C_1\left(C_C + C_O\right)}$$

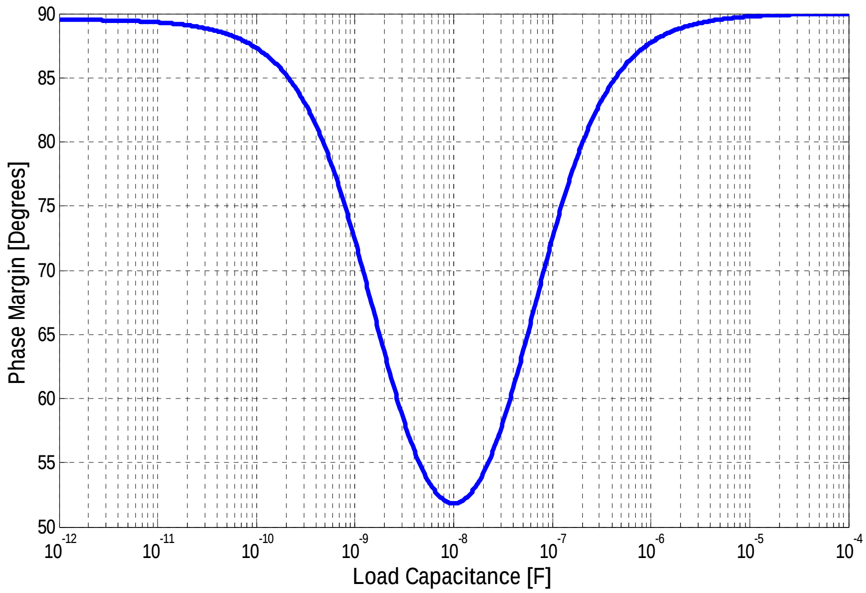
For large C_O

$$p_1 \approx \frac{1}{R_{OUT}\left(C_C + C_O\right)} \qquad p_2 \approx \frac{1}{R_{OEA}C_1}$$

Stability Quality Factor

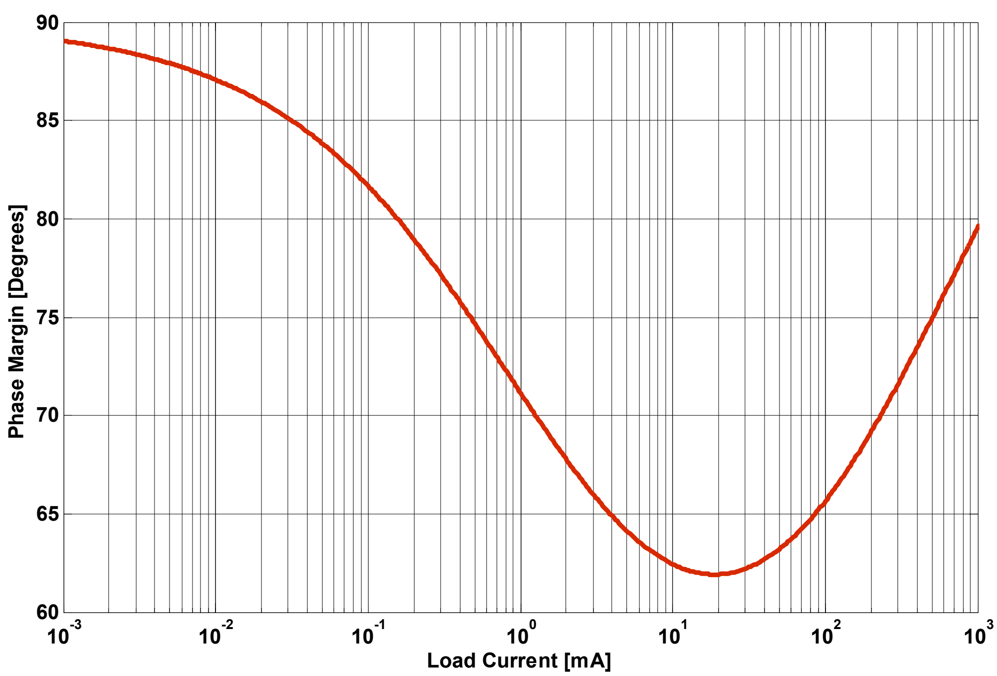
$$S \equiv p_2/\omega_{UGF} \qquad \frac{\partial S}{\partial C_O} = 0 \implies {C_O}^* \approx (g_{mp}R_1 - 1)\,C_C$$

$$S_{MIN} = \frac{4}{g_{m1}R_1}\cdot\left(\frac{C_C}{C_1}\right) \implies \uparrow C_C \text{ or } \downarrow C_1$$

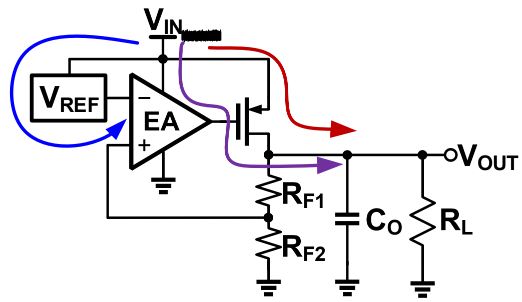


Phase Margin Vs. I_L [3]

$$\frac{\partial S}{\partial g_{mp}} = \frac{4}{g_{m1}R_1}\frac{C_C}{C_1}.$$



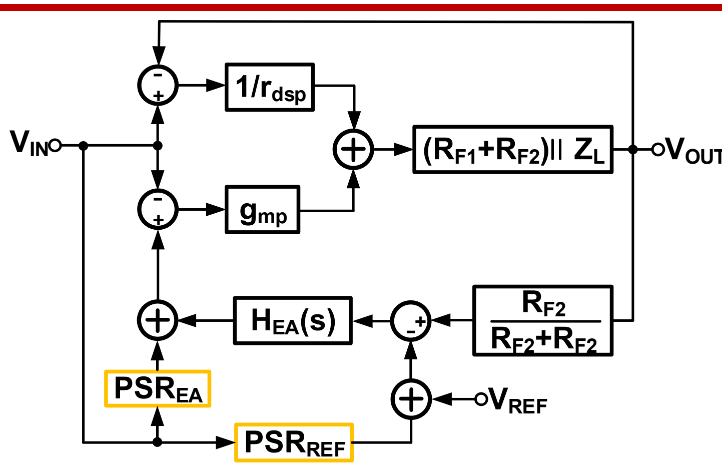
Power Supply Rejection



- ❑ Many paths from input to output
  - Reference generator
  - Error amplifier
  - Pass device

- ❑ Need to evaluate their combined effect on PSR

PSR Calculation

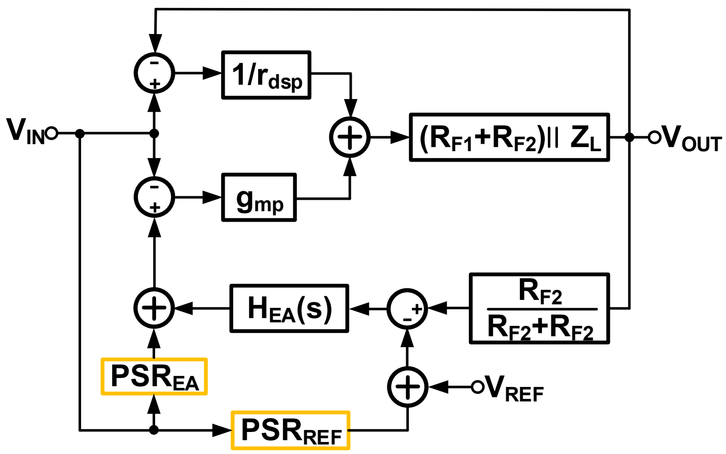


- ❑ PSR_{EA} = PSR of error amplifier

- ❑ PSR_{REF} = PSR of reference generator

- ❑ Signal flow analysis to determine overall PSR

PSR Calculation

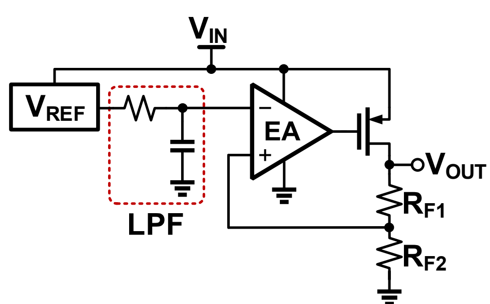


$$\left.\frac{V_{OUT}}{V_{IN}}\right|_{pass} = \frac{\left(g_{mp} + \frac{1}{r_{dsp}}\right)\left[(R_{F1}+R_{F2})\,||Z_L\right]}{1 + g_{mp}\left[(R_{F1}+R_{F2})\,||Z_L\right]\cdot\beta\cdot H_{EA}(s) + \frac{1}{r_{dsp}}\left[(R_{F1}+R_{F2})\,||Z_L\right]}$$

$$\left.\frac{V_{OUT}}{V_{IN}}\right|_{EA} = \frac{-PSR_{EA}\cdot g_{mp}\cdot\left[(R_{F1}+R_{F2})\,||Z_L\right]}{D(s)}$$

$$\left.\frac{V_{OUT}}{V_{IN}}\right|_{REF} = \frac{PSR_{REF}\cdot H_{EA}(s)\cdot g_{mp}\cdot\left[(R_{F1}+R_{F2})\,||Z_L\right]}{D(s)}$$

Reducing Noise Leakage from Reference

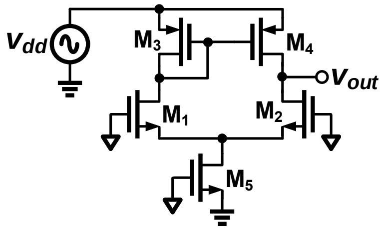


$$\left.\frac{V_{OUT}}{V_{IN}}\right|_{REF} = \frac{PSR_{REF}\cdot H_{EA}(s)\cdot g_{mp}\cdot\left[(R_{F1}+R_{F2})\,||Z_L\right]}{D(s)}$$

- ❑ PSR_{REF} sees low pass response
- ❑ Noise leakage improved by using a low pass filter

Error Amplifier PSR (Type – A)

- PSR_{EA} depends on amplifier topology

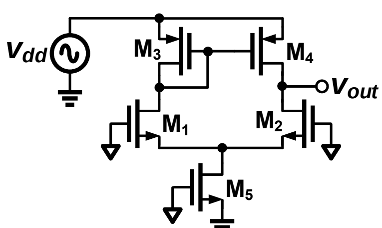


$$\frac{v_{out}}{v_{dd}} = -G_M \cdot R_{out}$$

$$R_{out} = (r_{ds2}||r_{ds4})$$

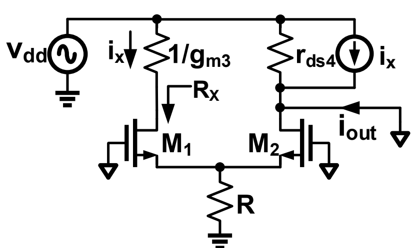
Error Amplifier PSR (Type – A)

- PSR_{EA} depends on amplifier topology



$$\frac{v_{out}}{v_{dd}} = -G_M \cdot R_{out}$$

$$R_{out} = (r_{ds2}||r_{ds4})$$



$$i_{out} = 2i_x + \frac{v_{dd}}{r_{ds4}}$$

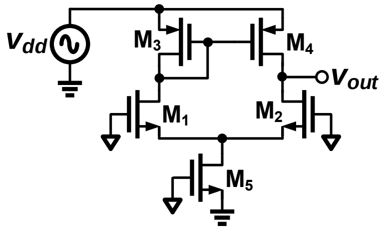
$$R_x \approx g_{m1}.r_{ds1} \cdot \frac{1}{g_{m2}} + r_{ds2} \simeq 2r_{ds1}$$

$$i_x = \frac{v_{dd}}{1/g_{m3} + 2r_{ds1}} \approx \frac{v_{dd}}{2r_{ds1}}$$

$$\Longrightarrow G_M = r_{ds1}||r_{ds4}$$

Error Amplifier PSR (Type – A)

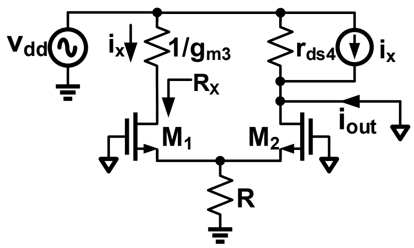
- ❑ PSR_{EA} depends on amplifier topology



$$\frac{v_{out}}{v_{dd}} = -G_M \cdot R_{out}$$

$$R_{out} = (r_{ds2} || r_{ds4})$$

$$\boxed{\frac{v_{out}}{v_{dd}} \approx 1}$$



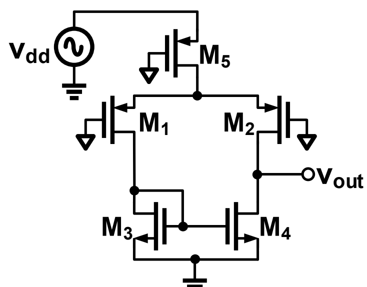
$$i_{out} = 2i_x + \frac{v_{dd}}{r_{ds4}}$$

$$R_x \approx g_{m1} . r_{ds1} . \frac{1}{g_{m2}} + r_{ds2} \simeq 2r_{ds1}$$

$$i_x = \frac{v_{dd}}{1/g_{m3} + 2r_{ds1}} \approx \frac{v_{dd}}{2r_{ds1}}$$

$$\Longrightarrow G_M = r_{ds1} || r_{ds4}$$

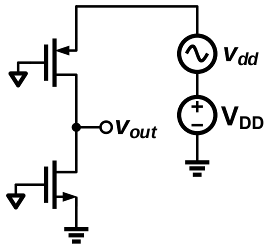
Error Amplifier PSR (Type – B)



$$v_{out} \approx 0$$

- ❑ None of the supply-noise appears at the output
  - ■ PSR = ∞
- ❑ Good for regulator with NMOS output stage
  - ■ Prevents noise leakage through NMOS gate

PMOS Output Stage PSR

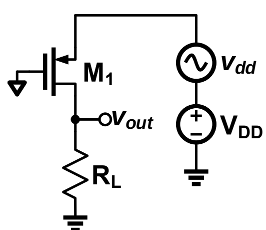


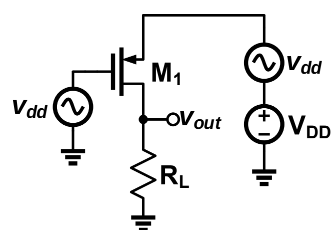
$$\frac{v_{out}(s)}{v_{dd}(s)} \approx g_{m1}\left(r_{ds1} || R_L\right)$$

- ❑ Two scenarios for PSR calculation

1. Gate of M_1 not coupled to V_{DD}
   - Behaves as a common gate stage

PMOS Output Stage PSR





$$\frac{v_{out}(s)}{v_{dd}(s)} \approx g_{m1}\left(r_{ds1} || R_L\right)$$

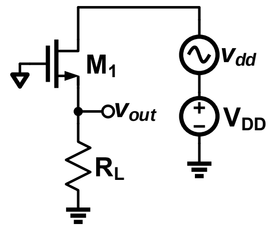
$$\frac{v_{out}(s)}{v_{dd}(s)} = \frac{R_L}{r_{ds1} + R_L}$$

- ❑ Two scenarios for PSR calculation

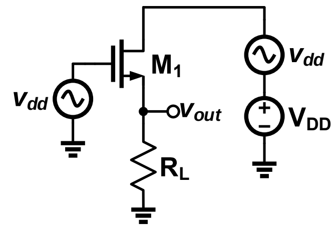
1. Gate of M_1 not coupled to V_{DD}
   - Behaves as a common gate stage

2. Gate of M_1 tightly coupled to V_{DD}
   - Becomes a resistor divider

NMOS Output Stage PSR



$$\boxed{\frac{v_{out}(s)}{v_{dd}(s)} = \frac{1}{r_{ds1}}\left(\frac{1}{g_{mn1}}||r_{ds1}||R_L\right) \approx \frac{1}{g_{m1}r_{ds1}}}$$



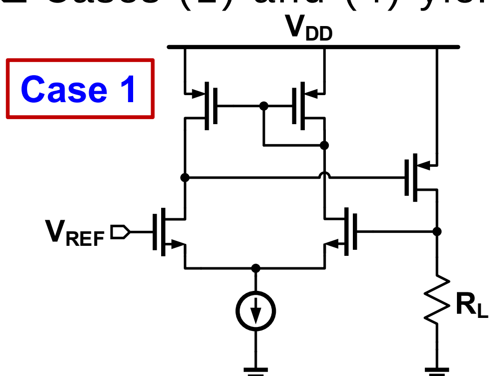
$$\boxed{\frac{v_{out}(s)}{v_{dd}(s)} \approx 1}$$

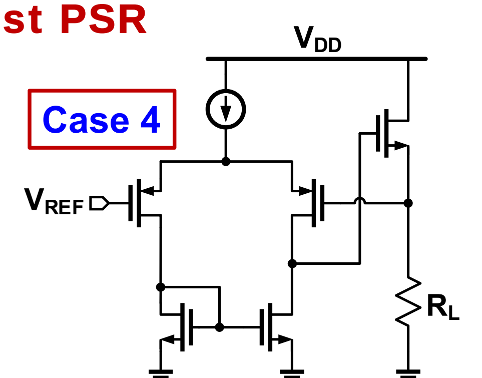
- ❑ Two scenarios for PSR calculation

1. Gate of M_1 not coupled to V_{DD}
   - M_1 acts as a cascode
2. Gate of M_1 tightly coupled to V_{DD}
   - Behaves as a source follower

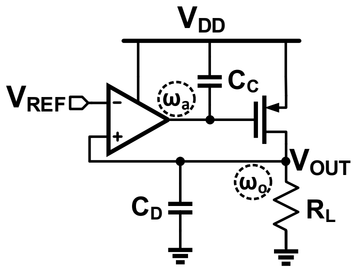
Error Amp. and Output Stage Possibilities[6]

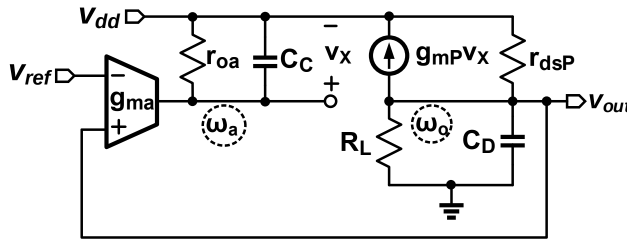
- ❑ Four possibilities
  1. NMOS amplifier & PMOS output stage
  2. NMOS amplifier & NMOS output stage
  3. PMOS amplifier & PMOS output stage
  4. PMOS amplifier & NMOS output stage
- ❑ Cases (1) and (4) yield **best PSR**





Regulator PSR$_{1/2}$





$$\omega_a = \frac{1}{r_{oa} C_C}$$

$$\omega_o = \frac{1}{(r_{dsP} \parallel R_L)\, C_D}$$

$$A_a = g_{ma} r_{oa}$$

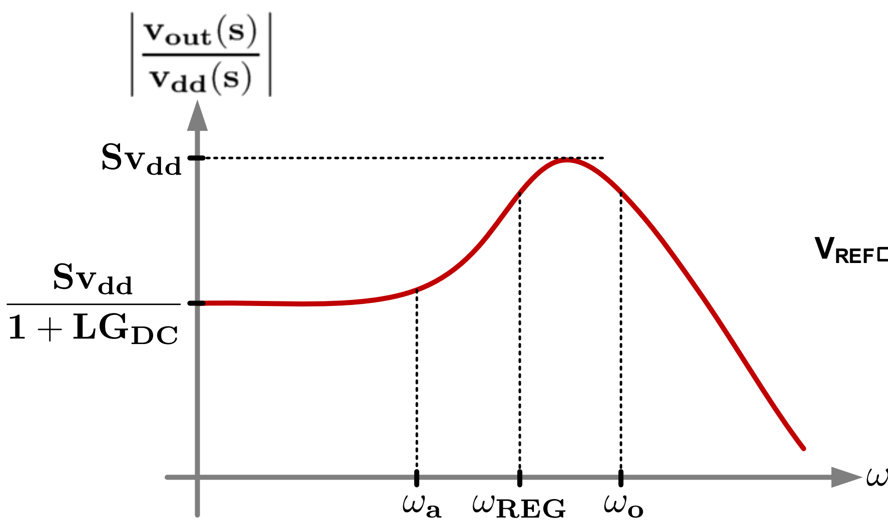
$$A_o = g_{mP} (r_{dsP} \parallel r_{vco})$$

$$S_{V_{dd}} = \frac{R_L}{R_L + r_{dsP}}$$

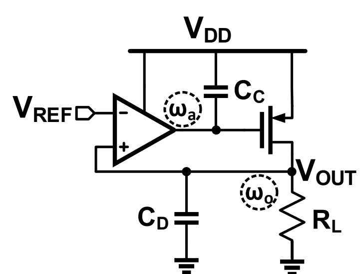
$$\frac{v_{out}(s)}{v_{dd}(s)} = \frac{S_{V_{dd}} \left(1 + \frac{s}{\omega_a}\right)}{\left(1 + \frac{s}{\omega_a}\right)\left(1 + \frac{s}{\omega_o}\right) + A_a A_o}$$

$$\frac{v_{out}(s)}{v_{dd}(s)} = \frac{S_{V_{dd}}}{\left(1 + \frac{s}{\omega_o}\right)(1 + LG(s))}$$

Regulator PSR$_{2/2}$



$\omega_a \ll \omega_o$

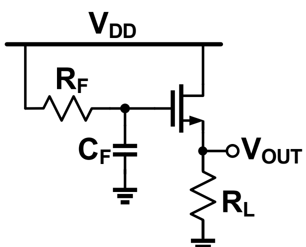


$$\frac{v_{out}(s)}{v_{dd}(s)} = \frac{S_{V_{dd}} \left(1 + \frac{s}{\omega_a}\right)}{\left(1 + \frac{s}{\omega_a}\right)\left(1 + \frac{s}{\omega_o}\right) + A_a A_o}$$

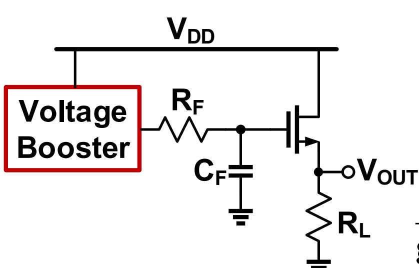
PSR Improvement Techniques

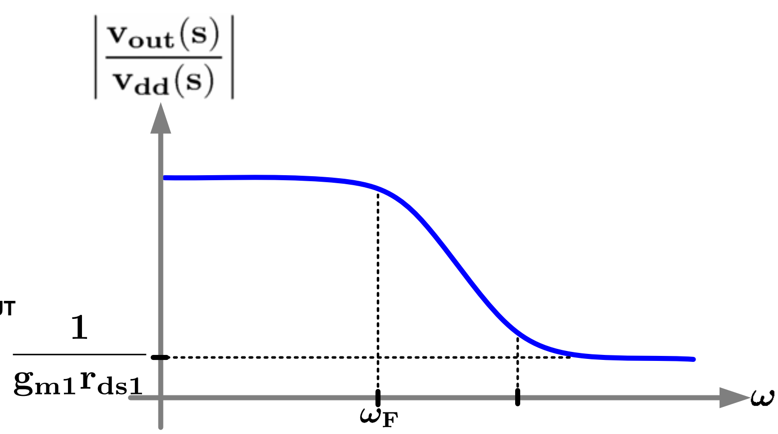
1. NMOS output stage
2. Make regulator output pole dominant
3. Cascaded regulators
4. Replica regulators

NMOS Output Stage LDO



$$\frac{v_{out}(s)}{v_{dd}(s)} = \frac{1}{r_{ds1}}\left(\frac{1}{g_{m1}} \,||\, r_{ds1} \,||\, R_L\right)\frac{1}{1+R_F C_F s}$$



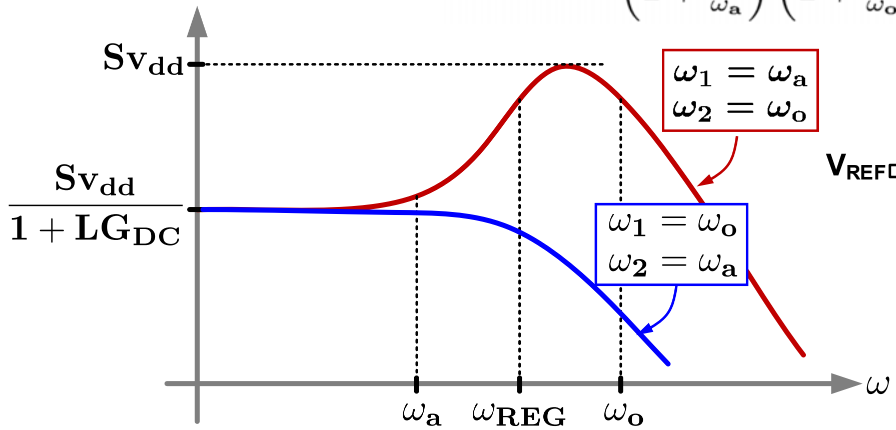


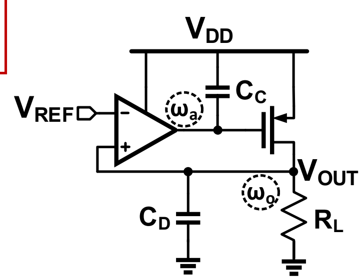
- ❑ Large dropout voltage
- ❑ Poor low frequency PSR

PMOS LDO w/ Output Pole Dominant

$$\left|\frac{v_{out}(s)}{v_{dd}(s)}\right| \qquad \frac{v_{out}(s)}{v_{dd}(s)} = \frac{S_{v_{dd}}\left(1+\frac{s}{\omega_a}\right)}{\left(1+\frac{s}{\omega_a}\right)\left(1+\frac{s}{\omega_o}\right)+A_a A_o}$$

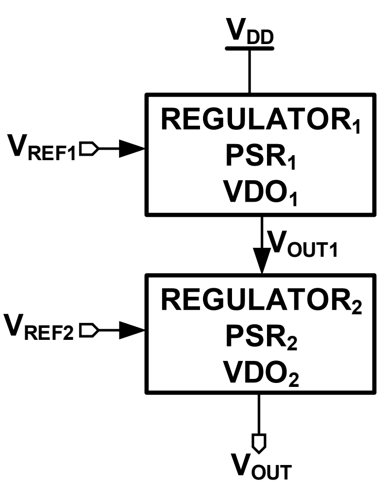
$$\omega_o \ll \omega_a$$

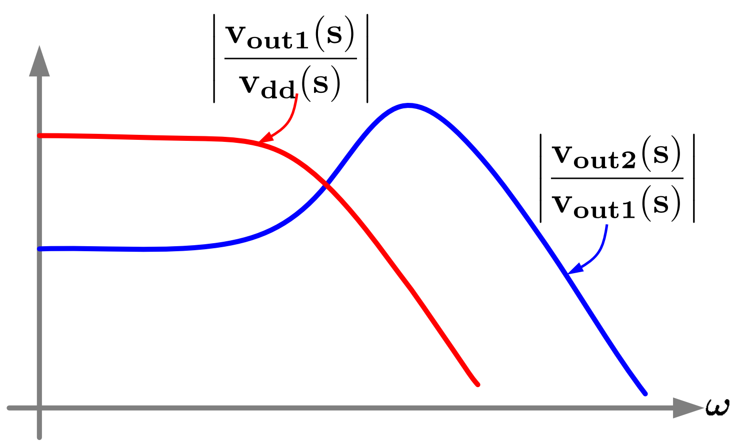




- ❑ No peaking in the supply noise transfer curve
  - ■ Superior supply noise rejection
- ❑ Needs very large capacitors: C_C and C_D

Cascaded LDOs



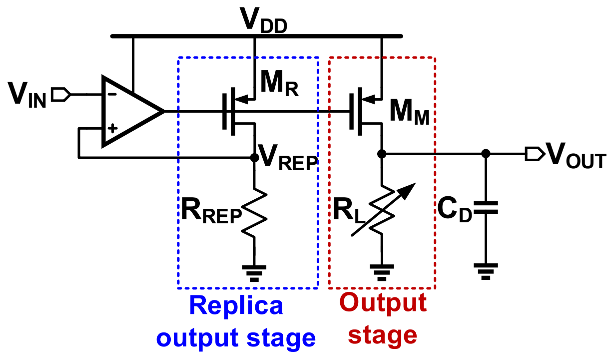


$$\text{PSR [dB]} = \text{PSR}_1\text{ [dB]} + \text{PSR}_2\text{ [dB]}$$

$$\text{Dropout voltage } V_{OD} = V_{OD1} + V_{OD2}$$

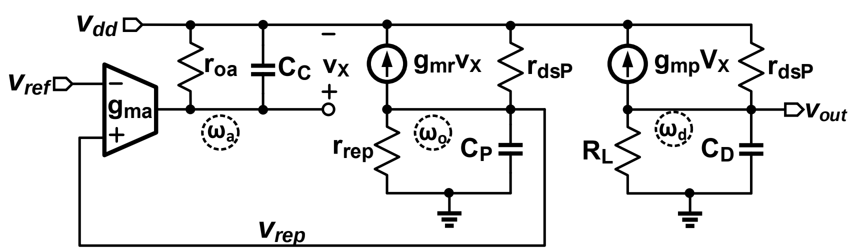
- ❑ Dropout voltage traded for PSR
- ❑ Co-optimize the regulators for best PSR

Replica-based LDO[7],[8]



- ❑ Indirect output regulation
  - Only scaled replica output is regulated
  - Accuracy depends on matching
- ❑ Stability independent of the load
  - Variable load outside the feedback loop
- ❑ Exhibits superior PSR performance

Replica-based LDO PSR$_{1/2}$

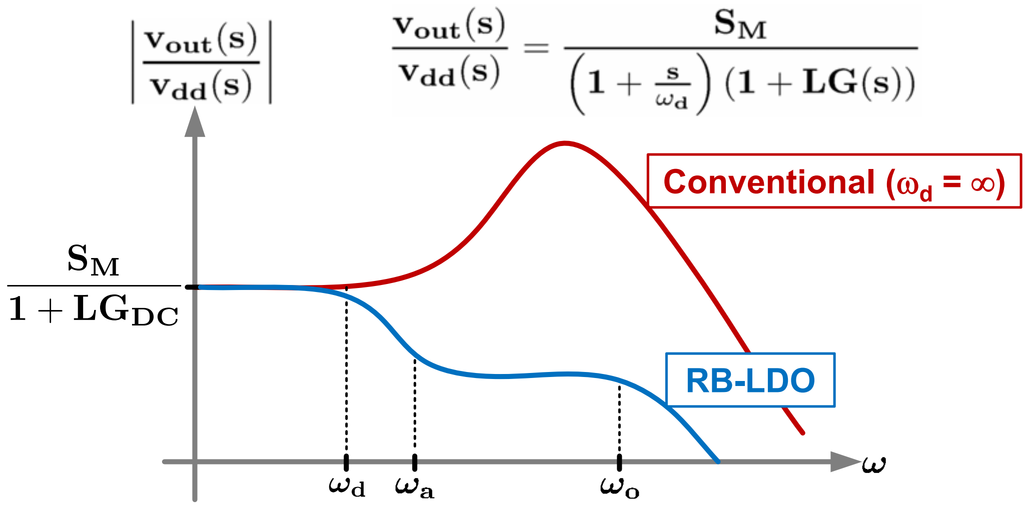


$$S_M = \frac{R_L}{R_L + r_{dsM}}$$

$$\frac{v_{out}(s)}{v_{dd}(s)} = \frac{S_M\left(1+\frac{s}{\omega_a}\right)\left(1+\frac{s}{\omega_o}\right)}{\left(1+\frac{s}{\omega_d}\right)\left[\left(1+\frac{s}{\omega_a}\right)\left(1+\frac{s}{\omega_o}\right)+A_aA_o\right]}$$

$$\frac{v_{out}(s)}{v_{dd}(s)} = \frac{S_M}{\left(1+\frac{s}{\omega_d}\right)(1+LG(s))}$$

Replica-based LDO PSR$_{2/2}$



- Large PSR improvement beyond ω_d
- $\omega_d > \omega_a$ eliminates "peaking"

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