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Conference Paper · October 2005

DOI: 10.1109/CICC.2005.1568779 · Source: IEEE Xplore

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A Low Noise, High Power Supply Rejection Low Dropout Regulator for Wireless System-on-Chip Applications

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Abstract - This paper presents a novel two-stage low dropout regulator (LDO) that minimizes output noise via a pre-regulator stage and achieves high power supply rejection via a simple subtractor circuit in the power driver stage. The LDO is fabricated with a standard 0.35um CMOS process and occupies 0.26mm^2 and 0.39mm^2 for single and dual output respectively. Measurement showed PSR is 60dB at 10kHz and integrated noise is 21.2uVrms ranging from 1kHz to 100kHz.

I. INTRODUCTION

Recently, there is a lot of focus on designing high performance low dropout regulator (LDO) with low noise and high PSR specification due to the wide spread popularity of hand-held products such as cellular phones and PDA (Personal Digital Assistant) [1]. The high performance LDO is commonly employed as radio frequency (RF) LDO providing quiet power supply in wireless RF system. Generally, a LDO is a closed-loop system consisting of an error amplifier, a resistive feedback network and a series pass transistor (PMOS in this case) as shown in Fig.1.

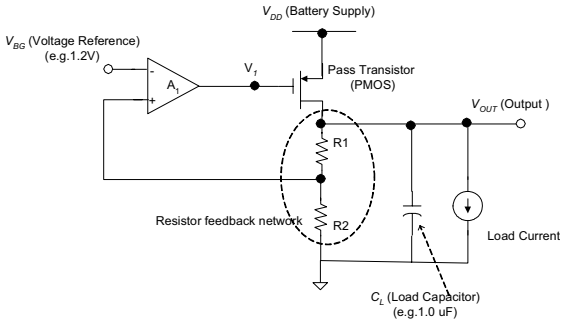

Fig.1 Conventional LDO

In Fig.1, The DC value of LDO output (V_{OUT}) can be expressed as

$$V_{OUT} = V_{BG}\left(1+\frac{R_1}{R_2}\right) \tag{1}$$

where V_{BG} is the voltage reference and is generally the output of a quiet voltage source such as the bandgap reference. Two specification parameters [2][3] that are usually of challenge are the power supply rejection and low integrated noise.

A. Power supply rejection

Power supply rejection (PSR) measures the LDO's ability to suppress power supply noise from its output. Assuming the contribution of supply noise due to the bandgap reference is negligible, the small signal variations of v_{out} due to supply noise (v_{dd}) is given by

$$v_{out} = A_{dd}v_{dd} + A_1 g_{mp} r_{dsp}\beta(-v_{out}) \tag{2}$$

where A_{dd} is the power gain v_{out}/v_{dd}, and A_1 is the open-loop gain of the error amplifier, β is the feedback factor $R_2/(R_1+R_2)$,g_{mp} and r_{dsp} are the transconductance and output impedance of the pass transistor PMOS respectively.

Using the methodology as in [4], the output of LDO due to total power supply noise at low frequency can be further shown as [5]

$$v_{out} = \left[\frac{1-A_{p1}}{A_1\beta} + \frac{1}{g_{mp}r_{dsp}}\cdot\frac{1}{A_1\beta}\right]v_{dd} \tag{3}$$

where A_{p1} is the power gain = v_1/v_{dd}. From (3), to achieve high PSR, an easy technique to improve PSR is to increase the error amplifier gain A_1 and reduce the gain factor $1/\beta$ if possible. Alternatively, one should try to design the error amplifier such that $A_{p1} \rightarrow 1$. For this to happen, v_1 needs to be close to v_{dd} which means having the voltage at V_1 tracks with the voltage at the source terminal of pass PMOS (which is connected to power supply).

B. Integrated Noise

Another important circuit performance is the total integrated noise of a LDO over the band of interest (f_2 - f_1). In conventional design, the total noise of the regulator is mainly contributed by different noise sources as illustrated in Fig.2. V_{n_R1} and V_{n_R2} are equivalent noise voltage of R_1 and R_2, V_{n_BG} is the bandgap noise and V_{n_in} is the input-referred noise of error amplifier itself.

The total noise power V_{n1}^2 due to the resistor feedback network is given by

$$V_{n1}^2 = V_{n\_R1}^2 + \left(\frac{R1}{R2}\right)^2 V_{n\_R1}^2 \tag{4}$$

The total noise power V_{n2}^2 due to the noise seen at the input of LDO is given by

$$V_{n2}^2 = \left(\frac{1}{\beta}V_{n\_in}\right)^2 + \left(\frac{1}{\beta}V_{n\_BG}\right)^2 \quad (5)$$

The integrated noise $V_{n\_o}^2$ $(f_2 - f_1)$ is given by

$$V_{n\_o}^2 = \int_{f1}^{f2}\left(V_{n1}^2 + V_{n2}^2\right)df$$

$$= \int_{f1}^{f2}\left(V_{n\_R1}^2 + \left(\frac{R1}{R2}\right)^2 V_{n\_R1}^2 + \left(\frac{1}{\beta}V_{n\_in}\right)^2 + \left(\frac{1}{\beta}V_{n\_BG}\right)^2\right)df \quad (6)$$

where $1/\beta$ is the closed-loop gain of the LDO decided by the ratio of V_{OUT} and V_{BG} ($V_{OUT}/V_{BG} = 1/\beta$). There are two ways to reduce $V_{n\_o}^2$: (a) increase the transistor's area of first stage (such as input pair) and current consumption of the error amplifier in order to reduce V_{n2}^2. (b) reduce the values of R_1 and R_2 in order to reduce V_{n1}^2. This will also result in an increase in the quiescent current consumption. In the case of system-on-chip (SoC) application, several similar LDOs can co-exist on the same chip and the increase in area and current consumption can become a serious problem.

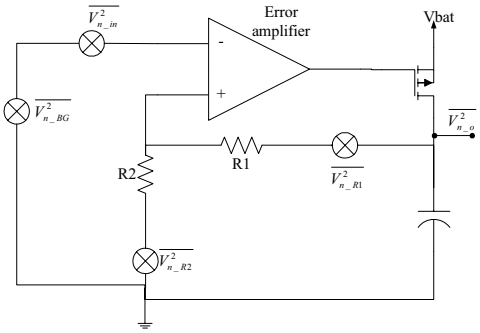

Fig.2 Noise sources of conventional LDO

II. IMPROVED LDO

A. Power supply rejection improvement

From (3), the PSR can be improved by having $A_{p1} \rightarrow 1$. Thus, the basic idea to improve PSR is to have an additional voltage subtractor stage as shown in Fig.3 inserted between the pass PMOS and the error amplifier, which feeds the supply noise directly into the feedback loop and modulates the pass PMOS gate with respect to the source terminal. Note that the input terminals to the error amp need to be reversed with the addition of subtractor which would produce a phase inversion in the loop. The subtractor can be easily implemented using two NMOS transistors illustrated in Fig.3. Using a two-stage miller amplifier [4], the contribution of supply noise at V_2 would be small compared to the supply noise at diode MN1, thus v_2 (the gate voltage at MN2) = 0. The output of subtractor stage is given by (via resistance division)

$$v_1 = \frac{r_{dsN2}}{1/g_{mN1} + r_{dsN2}}v_{dd} \quad (7)$$

where g_{mN1} and r_{dsN2} are the transconductance of N1 and output impedance of N2 respectively. If $g_{mN1} >> g_{dsN2}$, eq.(7) would become

$$v_1/v_{dd} \approx 1 \text{ or } A_{p1} \approx 1 \quad (8)$$

Thus, with (3) and (8), it can be shown that the PSR of the modified LDO, is improved and given by

$$v_{out} = \frac{1}{g_{mp}r_{dsp}}\frac{g_{mN1}}{g_{mN2}}\frac{1}{A_1\beta} \quad (9)$$

Both transconductance of the NMOS transistors (g_{mN1} and g_{mN2}) can be made equal. This ensures the loop-gain does not increase which could jeopardize the stability of the system. Similar results can also be observed if MN1 is replaced by a PMOS MP11 with gate and drain terminals tied in a 'diode' connection. The LDO is internally compensated via Cc1.

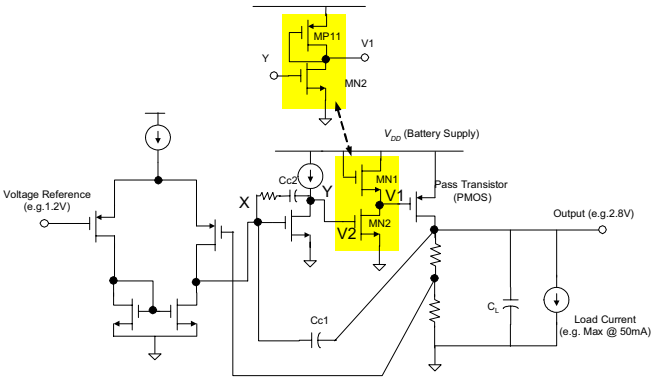

Fig.3 Implementation of PSR-boost technique

The diode connection of the subtractor provides a low impedance node ($1/g_m$) to push the parasitics pole of the pass PMOS, leaving the dominant pole due to the main miller loop (via Cc1) at node X. Another non-dominant pole at node Y is pushed away by the secondary miller loop(via Cc2).

B. Noise improvement

From (6), the total noise can be improved by reducing the gain factor $1/\beta$ and eliminating the noise term due to the resistors noise. The improvement can be made by a two-stage architecture which consists of a pre-regulator and a power driver stage as shown in Fig.4. The pre-regulator stage is formed by a reference buffer for level-shifting the bandgap-reference voltage and a RC low pass filter (LPF). Note that the bandgap reference voltage is typically fixed (e.g.1.2V) and serve as general reference voltage mainly for the rest of the

low noise modules such as baseband or RF channels. The power driver is a voltage follower configuration with a pass PMOS as its final stage so as to be able to drive the required current load. The output noise of each LDO V_{n_o} equals to

$$V_{n\_o}^{\ 2} = \int_{f1}^{f2} \left(V_{n\_in}^{\ 2} + \left(\left| \frac{1}{sRC+1} \right| V_{n\_pre} \right)^2 \right) df \tag{10}$$

where V_{n_in} is the input referred noise of the power driver itself and V_{n_pre} is the output noise of the pre-regulator. If the LPF's cut-off frequency is well below the starting frequency f_1, the second noise term in (10) can be filtered off and the final output noise can be simplified to

$$V_{n\_o}^{\ 2} = \int_{f1}^{f2} \left(V_{n\_in}^{\ 2} \right) df \tag{11}$$

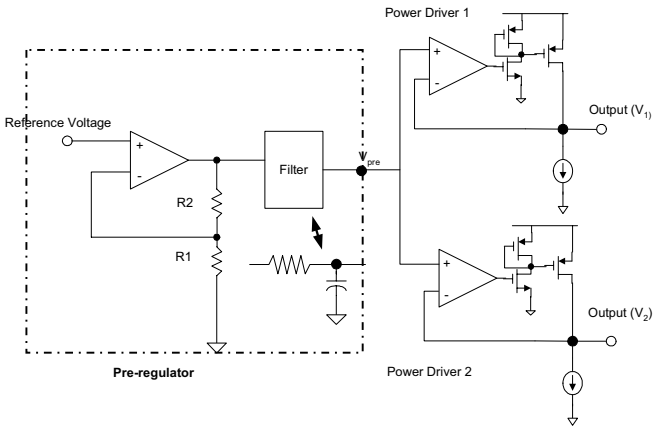

Fig.4 Proposed low noise regulators with dual output

Comparing with (6), the only noise term left in (11) is the input-referred noise of power driver. In addition, the input-referred noise does not contain any gain factor $1/\beta$. It is apparent that the larger the feedback factor $1/\beta$, which means a low bandgap reference voltage and a high output voltage setting, the larger it would be the difference in noise performance.

The proposed architecture also has the following advantages: (a) LDOs with the same output voltage setting can share the same pre-regulator and LPF. The area savings are significant especially in the SoC applications where several LDOs of similar specifications are required to be on the same chip. (b). The PSR is further improved by a factor of β, since the power driver is a unity gain feedback power amplifier, the supply noise seen at output is then given by (using the subtractor stage in the power driver)

$$v_{out} = \frac{1}{g_{mp} r_{dsp}} \frac{g_{mN1}}{g_{mN2}} \frac{1}{A_1} \tag{12}$$

The filter in Fig.4 can be implemented by a simple first-order RC filter. Since the density of on-chip capacitor is low (eg. 4fF/μm^2), normally the filter capacitor C is set smaller than 100pF to save area. Therefore, the resistance of R should be hundreds of Mega-ohms if the filter's cut-off frequency is set to be less than 10 Hz. Certain CMOS processes have very high-density on-chip resistor (eg. 100kΩ/square), which can further reduce the area of the filter. If such resistor is not available in the process, the circuit in [6] could be used in realizing a large resistor.

III EXPERIMENTAL RESULTS

The proposed LDO is fabricated in a 0.35um CMOS process. The chip micrograph is as shown in Fig.5 with the left and right portion illustrate the implemenation for single and dual output respectively. Note that in the dual output case, the error amplifier is shielded with a top-plate metal to shield off any noise coupling. All measurements are performed at room temperature. The external load capacitor is 1uF.

The noise density of the proposed LDO is plotted in Fig.6. At the condition of V_{DD}=3.6V and current load of 100mA, it is observed that the integrated noise of the proposed LDO is measured to be 21.2uVrms for frequency range from 1kHz to 100kHz. The noise contribution from bandgap reference is negligible since it using an external supply with a large RC low pass filter.

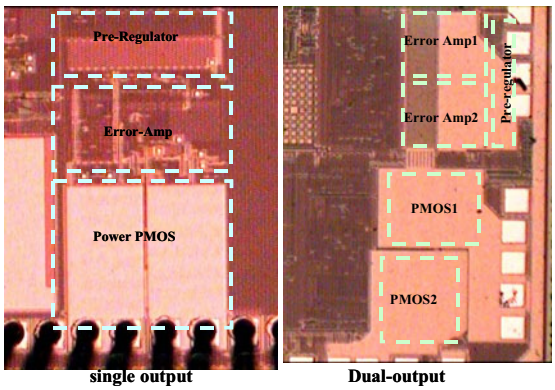

Fig.5 ChipMicrograph

For PSR measurement, V_{DD} = 3.1V, V_{OUT} = 2.8V, thus the dropout voltage is 300mV. A sine-wave of 100mVpp is injected and the frequency is swept from 10Hz to 100kHz. The performances of this circuit have been compared with the present state-of-the-art product [7]. It is a very low-noise BJT LDO with quiescent current that is comparable with this design. The good noise performances of this design and the one described in [7] are comparable. However, this design shows a better PSR. Fig. 7 shows at least 15 dB improvement in a wide frequency range (up to 100kHz). Another important feature is the transient response. This design is able to respond

to current step changing from 0 to 100 mA in 1us with minimum ringing. The measured plot is shown in Fig. 8. The use of a bipolar technology gives a wide-bandwidth that made difficult for circuit compensation. Because of this, the transient response of the circuit described in [7] has a longer and ringing transient when compared with this project.

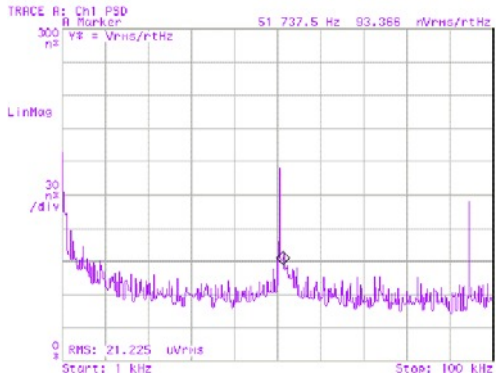

Fig.6 Noise Measurement of proposed LDO

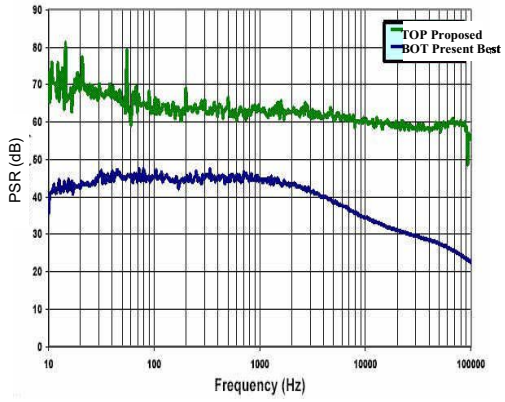

Fig.7 PSR of proposed and present best LDO

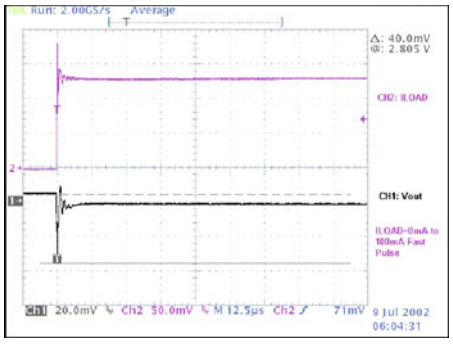

Fig 8 Transient response of proposed LDO (top : I_{OUT}, bottom : V_{OUT})

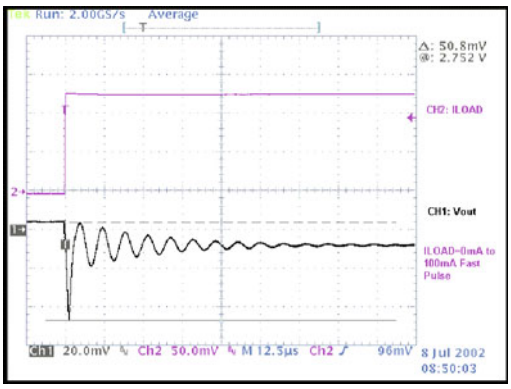

Fig.9 Transient response of present best LDO (top : I_{OUT}, bottom : V_{OUT})

IV CONCLUSION

By incorporating a pre-regulator stage and simple voltage subtractor circuit in the power driver, the LDO could achieve significant improvement in integrated noise and PSR. The proposed design does not add much complexity to the system stability compensation. It also consumes little silicon space and power, and is suitable for low voltage operation. In a wireless SoC chip, where several RF LDOs are required with similar specifications, the proposed technique could result in significant area savings by sharing the pre-regulator and have different power drivers serving different outputs which is usually for isolation purpose. The measurements are compared with the present state-of-the-art LDO. The obtained result shows that this circuit is able to obtain similar excellent noise performances but it is better in the PSR and transient control.

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