A Hybrid NMOS/PMOS Low-Dropout Regulator with Fast Transient Response for SoC Applications

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***Abstract*—In this paper, a new architecture of a fully integrated low-dropout voltage regulator (LDO) is presented. It is composed of hybrid architecture of NMOS/PMOS power transistors to relax stability requirements and enhance the transient response of the system. The LDO is designed in UMC 130 nm CMOS technology and is capable of producing a stable output voltage of 1.1 V from 1.3 V single supply with recovery settling time ≅ 500 nsec. The LDO can supply current from 10 µA to 100 mA consuming quiescent current of 23.7 µA and 83.5 µA, respectively. The performance of the proposed technique is compared with other reported techniques and gives a better performance. It can support load capacitance from 0-50 pF with phase margin that increases from 47º at low load (10 µA) to 80º at high load (100 mA) and power supply rejection ratio (PSRR) less than -9 dB up to 1 MHz.**

Keywords—Low-dropout regulator, Capacitor-less LDO, Fast transient response, System-On-Chip (SoC)

I. INTRODUCTION

In order for the size and cost of portable systems to be minimized, system-on-chips (SoCs) that provide high integration in a small size are utilized. For all portable devices powered by batteries, some types of regulation is needed to provide a stable supply voltage in the presence of varying load and battery conditions. There are two main types of regulators; switching regulators and linear regulators. Even though switching regulators have a high power efficiency compared to with linear regulators, they are noisier (specially at switching frequency) and less stable than linear regulators that provide highly stable voltage with less noise. This makes linear regulators very attractive to noise sensitive blocks such as RF blocks in mobile phones. In addition, linear regulators can be integrated on chip with minimum external passive components, while switching regulators require bulky off-chip components. One type of linear regulators that is used extensively in SoCs for power management is LDO to power up sub-blocks of a system individually [1]. LDO specifications are classified into three categories [2]: 1) static-state specifications; 2) dynamic-state specifications and 3) high frequency specifications. Static-state specifications are related to the performance of the LDO in the steady state such as line and load regulations, whereas dynamic-state specifications measure how the LDO responds to a change in the system, for example, change in the output voltage due to a sudden change in the load current. PSRR and output noise are regarded as high frequency specifications. A well-designed LDO should provide very low output ripples and a stable output voltage that can recover fast enough from a sudden change in the load current or the line voltage with minimum under/overshoots and with high immunity to supply noise. It should also support a wide-range of load currents and be able to meet all these specifications without any off-chip components to minimize area and cost. Conventional NMOS and PMOS LDOs are shown in Fig 1(a) and Fig. 1(b), respectively. Stable output voltage with minimum line/load regulation can be achieved if the error amplifier (EA) is designed with a very high open-loop gain, which requires multi-stages in modern CMOS technology. This renders stability of the LDO system a tough task, and the LDO starts to oscillate especially at low load currents. Fast transient response can be realized if the LDO has both a high bandwidth and a high slew-rate. Therefore, a high quiescent current is required to improve the bandwidth and slew-rate. The tail current used in the EA sets the maximum current to charge and discharge the gate capacitance of the power transistors (M_P, M_N) [3], which will increase the power consumption of the LDO. In addition, the compensation needed for the stability decreases the bandwidth of the LDO. All these contradictory constraints and trade-offs make conventional LDOs unable to meet all the requirements simultaneously. In this paper, a new architecture for a capacitor-free LDO is presented in order to provide a wide-range of load currents while maintaining stability all over the range starting from 10µA up to 100mA. In the proposed architecture, the trade-offs between stability,

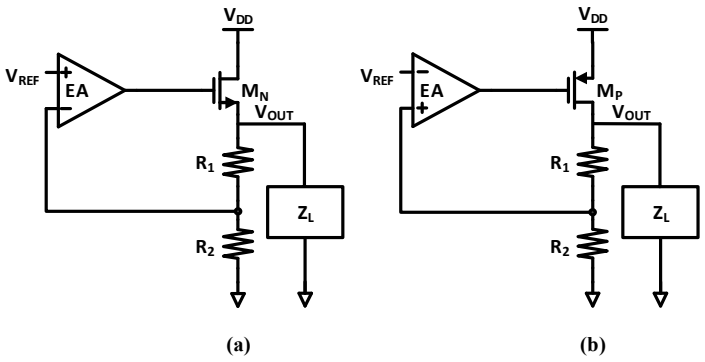

Fig. 1. Conventional LDOs (a) NMOS (b) PMOS.

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transient response, power, and area are relaxed to maintain a fast recovery time at low power consumption and area.

II. Proposed Architecture

A. PMOS Power Transistor LDO

The PMOS LDO is mostly used to supply high currents with low dropout voltage. However, this topology has stability problems, especially at light loads, mainly due to the two poles at the gate of the power transistor (M_P) and at the output of the LDO. The gate pole is at low frequency because of the high output resistance of the EA and the large parasitic capacitance of M_P, which is designed large enough to supply high load current at low dropout voltage. On the other hand, the LDO output pole is dependent on the load capacitance and resistance, which changes with the load current, thus shifting the position of the pole and makes it a complex task to achieve stability all over the full load range. Thus, either a large compensation capacitor is used to separate these two poles or a complex compensation technique is needed to maintain the stability with an acceptable phase margin [2].

B. NMOS Power Transistor LDO

The NMOS LDO has the advantage of shifting the output pole to high frequencies as the current increases due to the increase in transconductance (g_m) of the power transistor (M_N) and the decrease in the output resistance of the source follower [4]. However, for this architecture, the LDO's output voltage should be less than the gate voltage by at least one V_{gs}. For high load currents, this would result in either an impractical size of M_N or a very limited output voltage leading to a large area, or a large dropout voltage which will in turn increase the power dissipated in the pass transistor. The conventional NMOS LDO also suffers from low loop-gain because the NMOS transistor is used as a source follower and therefore a multi-stage amplifier is often used to improve line/load regulation [4].

C. Proposed Hybrid NMOS/PMOS Power Transistors

The proposed hybrid NMOS/PMOS architecture is shown in Fig. 2. It provides better stability and transient response while maintaining low dropout voltage in a wide-range of load currents. At light loads (10 µA-1 mA) M_P is OFF and M_N is used to provide the current to the output, as shown in Fig. 2, relaxing the stability requirements for the system without the need for complex compensation techniques or large compensation capacitors. At load currents larger than 1 mA, M_P starts to conduct supplying current to the output along with M_N and hence it boosts the loop gain at high loads without the need for very large size of M_N.

As shown in Fig. 2, a high-gain EA is used for better load/line regulation. The output (V_{EA}) is fed to the output through two paths. The first path is a level shifter whose shifted-voltage is applied to the gate of M_N. The second path is an inverting amplifier stage (A_2) that provides a 180º phase shift, to ensure negative feedback within this path, that drives the gate of M_P. This system can be viewed as two parallel LDOs using the same EA, thus higher current range can be supplied using the proposed architecture while maintaining better transient response as will be shown in the simulation results. The supply V_{DD} feeds the whole system and a fully integrated two-stage voltage doubler used as a charge pump (CP) to supply voltage only to the Flipped Voltage Follower (FVF) circuit. The FVF is consuming very low current, thus relaxing the design requirements needed by the CP.

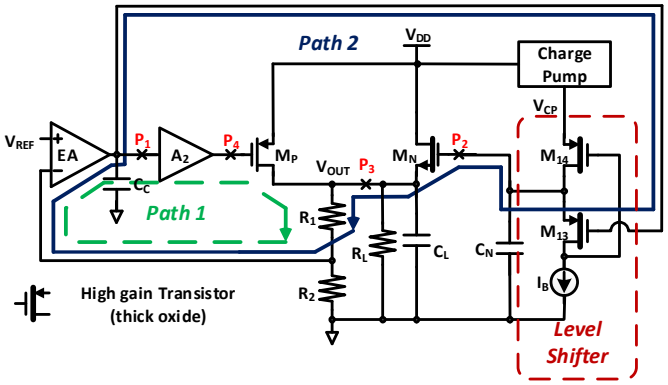

Fig. 2. Block diagram of the proposed architecture.

III. Circuit Implementation and System Analysis

A. Circuit Implementation

The EA is implemented as single-stage folded cascode op-amp (PMOS differential pair) in order to provide a high gain without introducing extra internal low-frequency poles. A_2 is implemented as a simple common-source (CS) amplifier with small drain resistance (10 kΩ) that is designed to provide a 180º phase shift without introducing extra gain in the loop (gain ≅ 0 dB). The level shifter is implemented as a simple FVF [5] that provides low output impedance at a low consumption current compared with a conventional voltage-follower. The FVF is supplied by a charge pump that steps up the supply voltage V_{DD} from 1.3 V to ≅ 2.3 V. M_N is used to supply higher currents at a small size due to the increase in V_{gs}. The charge pump is implemented as a two-stage voltage doubler [6] using a simple non-overlapping clocking mechanism in addition to using only standard transistors implemented in deep N-WELL. The CP output is applied only to the FVF that requires a very low biasing current (≅ 6 uA). As a result, the design of the charge pump is relaxed using low clock frequency (1 MHz) and small pumping capacitors (4 pF), thus decreasing the power consumption and area needed for the CP. M_N together with transistors of the FVF are implemented using high voltage (thick oxide) transistors.

An under/overshoot circuit is used in the proposed system that is composed of an overshoot circuit [7] and an undershoot circuit [8] to enhance the slew rate at the gate of M_P.

B. System Analysis

Fig. 3 shows the small-signal model of the power transistors used to calculate the output voltage as follows:

$$V_{out} = \left(-g_{mp}\, V_{gp} + g_{mn} V_{gn} - V_{out}\, g_{mn} - \frac{V_{out}}{r_{op}} - \frac{V_{out}}{r_{on}}\right) \frac{R_L}{1+SC_L R_L} \quad (1)$$

where

$$V_{gp} = -\, A_1(S)\, A_2(S)\, (V_{REF} - \beta V_{out}) \quad (2)$$

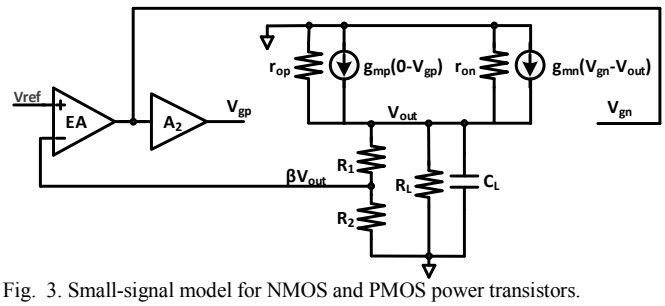

Fig. 3. Small-signal model for NMOS and PMOS power transistors.

$$V_{gn} = A_1(S)\,(V_{REF} - \beta V_{out}) \qquad (3)$$

where $A_1(S)$ is the gain of the EA and $A_2(S)$ is the gain of A_2. Ignoring (V_{out}/r_{op}) and (V_{out}/r_{on}), we can obtain the loop gain (LG) of the overall system using equations (1-3):

$$LG = \beta\,\frac{A_1(S)\,(g_{mp}A_2(S) + g_{mn})\,\frac{R_L}{1+SC_LR_L}}{1 + g_{mn}\,\frac{R_L}{1+SC_LR_L}} \qquad (4)$$

The proposed system has two main cases:

Light Load: 10 µA ≤ I_L ≤ 1 mA

Only path 2, shown in Fig. 2, is working, while the amplifier A_2 and M_P are totally OFF ($g_{mp} = 0$).

The system in this case is a three-stage LDO. The main poles that affect the system are labelled in Fig. 2. A dominant pole P_1 is created at the output of the EA using a compensation capacitor C_C of 700 fF.

$$P_1 = \frac{1}{R_{out,EA}\,C_c} \qquad (5)$$

The second pole P_2, in this case, is at the output of the LDO at load capacitance C_L of 50 pF. One of the main benefits of using M_N is the low output resistance that appears at the output of the LDO, which helps moving this pole to high frequencies as the load current increases.

$$P_2 = \frac{1}{R_{out,N}\,C_L}, and\ R_{out,N} = \frac{1}{g_{m,N}} \qquad (6)$$

where $R_{out,N}$ is the output resistance of M_N.

The third pole P_3 is at the gate of M_N and is given by:

$$P_3 = \frac{1}{R_{out,FVF}\left(C_{par,N} + C_N\right)} \qquad (7)$$

where $R_{out,FVF}$ is the output resistance of the FVF to decrease its output resistance and $C_{par,N}$ is the total parasitic capacitance at the gate of M_N. C_N is an extra 900 fF capacitor added to improve PSRR at high frequencies.

High Load: 1 mA ≤ I_L ≤ 100 mA

The system is working with the two paths, shown in Fig. 2, fully conducting current to the output. In this case, M_P is conducting current to the load and thus introducing a 4th pole P_4 given by:

$$P_4 = \frac{1}{R_{out,A2}\,C_{par,P}} \qquad (8)$$

where $R_{out,A2}$ is the output resistance of A_2, and $C_{par,P}$ is the total parasitic capacitance at the gate of M_P.

A small output resistance ($R_{out,A2} = 10\,k\Omega$) leads to a high-frequency P_4 that has minimum effect on the overall system's stability. Also, in this case, as P_2 is shifed with the load to higher frequencies and P_3 is a fixed pole; at some point of load (≅2 mA), the 2nd and 3rd pole are changing their locations.

C. Sizing of Power Transistors

Sizing the power transistors play a key role in the overall system's performance, system stability, transient response, and PSRR. M_P provides the high speed path to react fast enough to any abrupt changes in the loop. M_N provides the low-output impedance to enhance the phase margin of the system especially at light load.

Fig. 4 shows the current distribution, for the proposed design, in both power transistors while load current is changing from 10 µA to 100 mA. M_N provides the whole current at light load up to 1 mA and M_P starts to conduct afterwards. This provides a good balance for the design trade-off to achieve different system specifications.

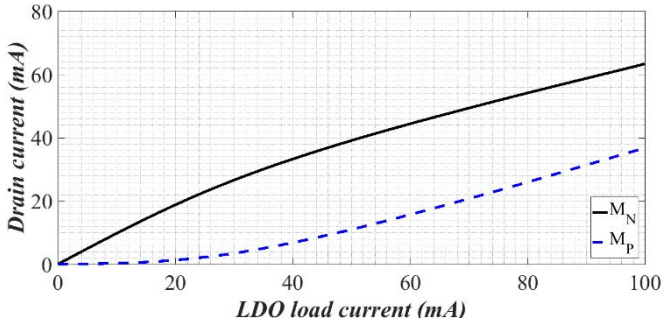

Fig. 4. Current sharing between the two power transistors

IV. Simulation Results

The proposed LDO has been designed and simulated using UMC *130 nm* CMOS technology. Fig. 5 shows the LDO loop gain and phase at minimum and maximum load currents at the worst case of C_L (50 pF). The minimum PM is 47° at 10 µA of load current.

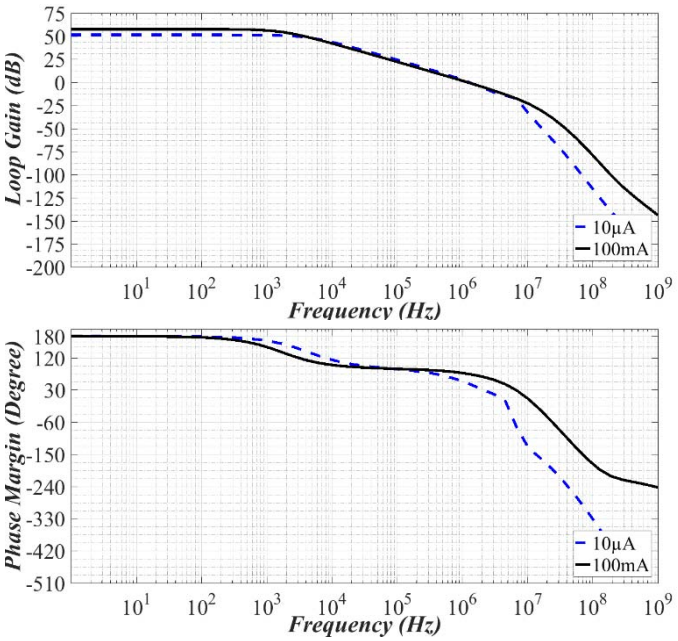

Fig. 5. Simulated loop gain and phase of the proposed LDO.

Fig. 6 shows the load transient response of the LDO while I_L is switching between 10 µA to 100 mA with a rise/fall edge of 100 nsec. The system can fully recover in ≅ 500 nsec with overshoots of 200 mV and undershoots of 285.8 mV.

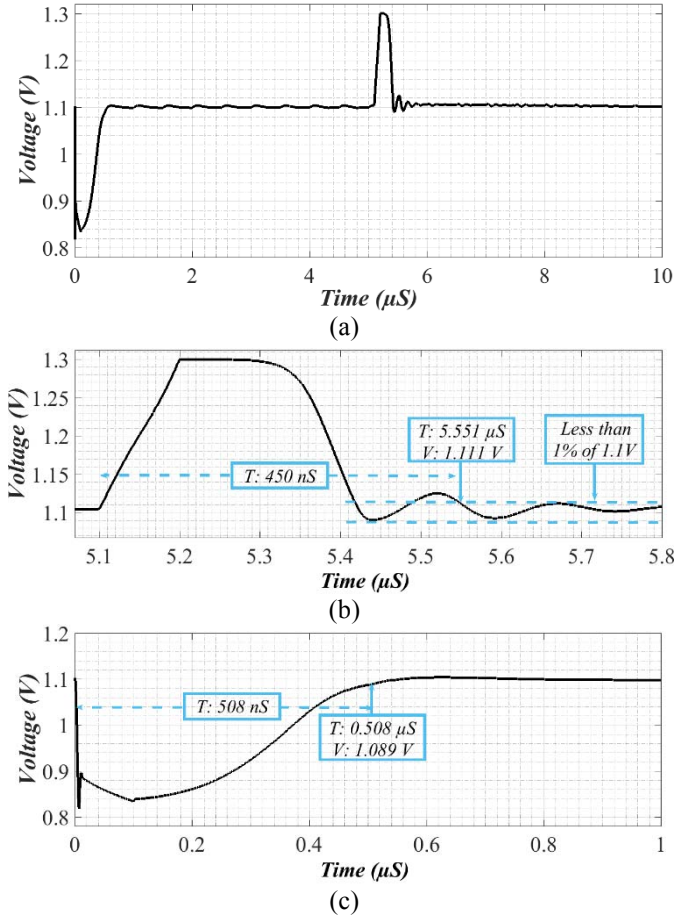

Fig. 6. Load transient response of the proposed LDO at C_L = 50pF with load current switching from 10µA to 100mA. (a) Full response (b) Overshoots (c) Undershoots.

The line transient response is simulated while V_{DD} changes between 1.3 V to 1.4 V with a 100 nsec rise/fall time. The glitches at low load current (10 µA) are +18 mV to -9 mV and the glitches at high load current (100 mA) are +53 mV to -43 mV. PSRR is simulated at maximum and minimum load currents and at different values of C_L with results showing gain less than -9 dB up to 1 MHz. The performance of the proposed LDO is summarized and compared with previously reported regulators in Table I. The comparison shows that the proposed LDO has smaller FoM than all other designs except [11] that has a slower transient response at larger rise/fall time and also consuming higher quiescent current.

V. Conclusion

A hybrid NMOS/PMOS power transistor LDO is presented and analyzed in this paper. The usage of both power transistors is to relax the stability requirements of the LDO by shifting the output pole to higher frequencies as the load increases and hence a small compensation capacitor is required. Simulations results in 130nm CMOS show that the proposed LDO supported wide-range load currents with fast transient response at low power consumption. It is also suitable for SoC applications since no off-chip components are needed.

Table I. Comparison between proposed technique and other reported techniques.

		Our work *	[9]	[10]	[4]	[11]
Year		2017*	2014	2016	2015	2012
Type (Analog/Digital)		Analog	Analog	Hybrid A/D	Analog	Analog
Process (nm)		130	180	180	65	0.35
Minimum V_{in} (V)		1.3	1.8	1.43	2.4	1.2
V_{out} (V)		1.1	1.6	1.0	1	1
Dropout Voltage		0.2	0.2	0.043	0.05	0.2
I_Q (µA)	Min I_L	23.7	55	1000	10	28
	Max I_L	83.3	80			380.1
Under/Overshoot (mV)		-285.5	-80	-400	195	-105
		200	120	200		50
Settling time (µsec)		0.5	6	30	500	~4***
ΔI_{out} (mA)		0.01 -100	0 -50	10 - 90	1 - 31	0 - 100
Rise/fall edge (nsec)		100	100	100	0.2	1000
I_{out}	Min (µA)	10	0	0	1000	0
	Max (mA)	100	50	100	30	100
Line Regulation (mV/V)		0.718	--	1.0	--	0.39
Load Regulation (mV/mA)		0.0015	0.14	0.01	0.2	0.0782
C_L (pF)		0 - 50	100	N/A	30	100
PSRR @ 10kHz (dB)		-45	-60	-50.75	-40	-47.9
PSRR @ 1MHz (dB)		-9	-70	--	-16***	-13
FOM (fsec)**		57.54	440	N/A	85	43.4

* Simulated Results. ** FOM= ($C_L \Delta V_{out} I_Q / \Delta I_{out,MAX}^2$) [12]
*** Estimated from figure.

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