**LDO Project Description**

The objective of this design project is to implement an LDO circuit in 45nm technology that produces a **regulator output of 0.9v** with a supply voltage of 1.2v & a bandgap reference voltage of 0.75v.

The design specifications that need to be achieved are:

|  |  |
| --- | --- |
| Supply Voltage | 1.2 V |
| Reference Voltage | 0.75 V |
| Regulated Voltage | 0.9 V |
| Load Current | 5 mA – 30 mA |
| Load Capacitor | 200 pF |
|  |  |
| DC Gain | > 40 dB |
| Phase-Margin | > 60 degrees |
| Min PSRR | > 5 dB |
| PSRR (for freq < 10M) | > 30 dB |
| Offset Std Dev (σ) | < 2 mV |