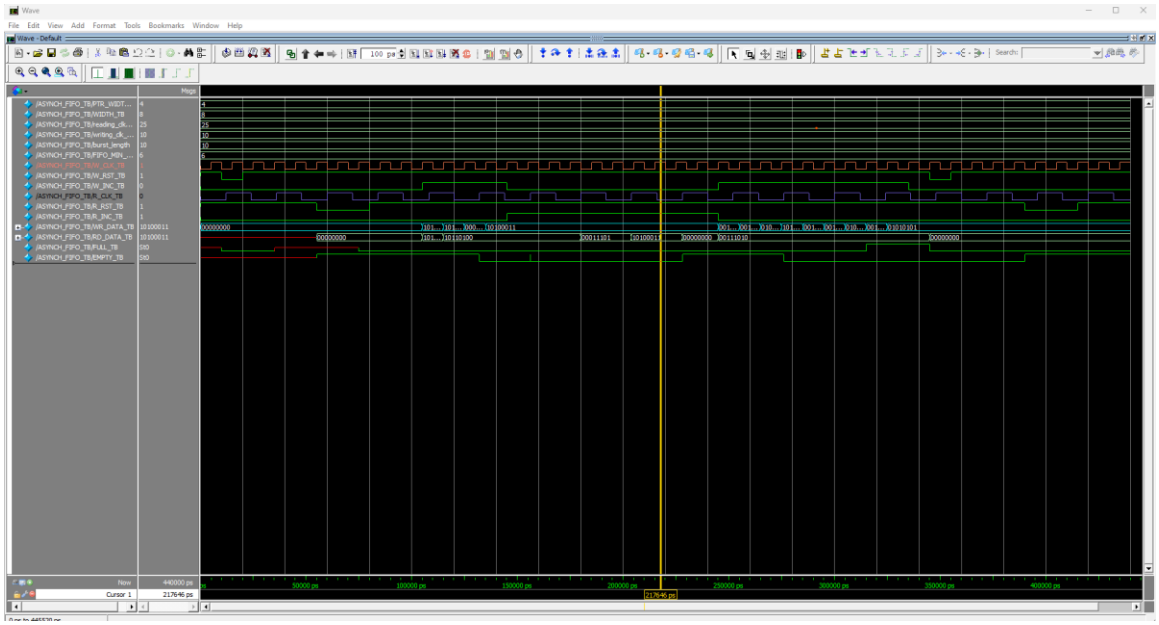

```
add wave -position insertpoint  \
sim:/ASYNCH_FIFO_TB/PTR_WIDTH_TB \
sim:/ASYNCH_FIFO_TB/WIDTH_TB \
sim:/ASYNCH_FIFO_TB/reading_clk_period \
sim:/ASYNCH_FIFO_TB/writing_clk_period \
sim:/ASYNCH_FIFO_TB/burst_length \
sim:/ASYNCH_FIFO_TB/FIFO_MIN_DEPTH \
sim:/ASYNCH_FIFO_TB/W_CLK_TB \
sim:/ASYNCH_FIFO_TB/W_RST_TB \
sim:/ASYNCH_FIFO_TB/W_INC_TB \
sim:/ASYNCH_FIFO_TB/R_CLK_TB \
sim:/ASYNCH_FIFO_TB/R_RST_TB \
sim:/ASYNCH_FIFO_TB/R_INC_TB \
sim:/ASYNCH_FIFO_TB/WR_DATA_TB \
sim:/ASYNCH_FIFO_TB/RD_DATA_TB \
sim:/ASYNCH_FIFO_TB/FULL_TB \
sim:/ASYNCH_FIFO_TB/EMPTY_TB
VSIM 7> run -all
# Test passed: FULL flag is not set.
# Read Data: b4
# Read Data: 1d
# Read Data: a3
# Read Data: 00
# Test passed: EMPTY flag is set after reading all data.
# Test passed: FULL flag is set on overflow.
# Test passed: FIFO reset correctly, EMPTY flag is set.
# Break in Module ASYNCH_FIFO_TB at D:/Eltemsah/verilog projects/Asynchronous FIFO/RTL/ASYNCH_FIFO_TB.v lin
e 160

VSIM 8>
```

Project | Transcript | Objects | sim

Project : ASYNCHRONOUS_FIFO | Now: 440 ns Delta: 0 | /ASYNCH_FI