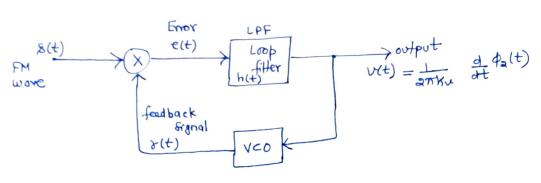
FM Demodulation using Phase Locked Loop (PLL):

PLL consists of three major components:

- 1. multiplier
- 2. Loop filter
- 3. VCO



that when the control voltage is zero, two conditions are satisfied:

- 1. The frequency of the VCO is precisely set at fe.
- ? The VCO olp has a go phase-shift writ. the unmodulated carrier wave.

$$8(t) = A_c \sin \left(2\pi f_c t + \phi_i(t) \right) \qquad \text{i'lp to the PLL}$$

$$8(t) = A_c \sin \left(2\pi f_c t + 2\pi k_f \int_{0}^{\infty} m(t) dt \right)$$
where
$$\phi_i(t) = 2\pi k_f \int_{0}^{\infty} m(t) dt$$

$$\gamma(t) = A_{\nu} \cos\left(2\pi f_{c}t + \phi_{z}(t)\right) - ... \text{ olp of VCO}$$
where $\phi_{z}(t) = 2\pi k_{\mu} \int \nu(t) dt$
Instantaneous freq. of VCO = $\omega_{c} + \frac{1}{2t} \phi_{z}(t) = \omega_{c} + 2\pi k_{\nu} \nu(t)$
where $f_{z}(t) = \phi_{z}(t) = 2\pi k_{\nu} \nu(t)$

$$v(t) = \frac{1}{2\pi K_{L}} \frac{d}{dt} \phi_{a}(t)$$

- The object of the PLL is to generate a VCO output 8(t) that has the same phase angle as the input FM signal 8(t).

$$\phi_1(t) = 2\pi k_{+} \int m(t) dt$$

The time-varying phase $\phi_i(t)$ is due to modulation by a message signal m(t), in which case we wish to recover $\phi_i(t)$ and thereby produce an estimate of m(t).

of of multiplier =
$$A_c S_{10}$$
 (wet $+ A_1(t)$) $A_v cos(wet + \phi_2(t))$

$$= \underbrace{A_c A_v}_{S_{10}} S_{10} \left(\phi_1(t) - \phi_2(t) \right) + \underbrace{A_c A_v}_{S_{10}} S_{10} \left(a_v ct + \phi_1(t) + \phi_2(t) \right)$$
high feq. component

high they, comporent suppressed by the Loop filter

Effective input to the Loop filter:

$$e(t) = \frac{AcAv}{2} \sin \left(\phi_{1}(t) - \phi_{2}(t) \right)$$

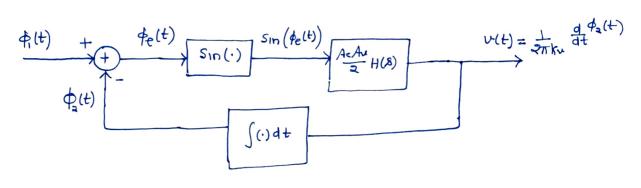
$$e(t) = \frac{AcAv}{2} \sin \left(\phi_{e}(t) \right) \qquad \text{where } \phi_{e}(t) = \phi_{1}(t) - \phi_{2}(t)$$

let h(t) -.. impulse response of the loop filter.

$$v(t) = e(t) *h(t)$$

$$= \int_{-\infty}^{\infty} e(t) h(t-t) dt$$

$$v(t) = \frac{AcAv}{2} \int_{-\infty}^{\infty} sin(\phi_{e}(t)) h(t-t) dt$$



⇒ when the phase error pett) is zero, the PLL is said to be in phase-lock.