

2017-2021 Scheme and Syllabus

SEMESTER: I Physics Group												
Sl No	Course Code	Course Title	Course Type	Teaching Dept.	Teaching Hours/week				Examination			Credits
					L #	T #	P #	S #	CIE *	SEE *	Total	
1	17MAT11	Engineering Mathematics – I	BS [^]	MAT	4	1			50	50	100	4.5
2	17PHY12	Engineering Physics	BS [^]	PHY	4	1			50	50	100	4.5
3	17CIV13	Engineering Mechanics	EC ^{\$}	CV	4	1			50	50	100	4.5
4	17EME14	Elements of Mechanical Engineering & Workshop practice	EC ^{\$}	ME	4		2		50	50	100	5.0
5	17ELE15	Basic Electrical Engineering	EC ^{\$}	EEE	4	1	1		50	50	100	5.0
6	17PHL16	Engineering Physics Lab	BS [^]	PHY			3		50	50	100	1.5
7	17CIP17	Constitution of India & Professional Ethics	Hu [@]	HUM	2				100 ₊	-	-	-
8	17ENG18	Communicative English	Hu [@]	HUM	2				100 ₊	-	-	-
					TOTAL				300	300	600	25.0

SEMESTER: I

Chemistry Group

Sl No	Course Code	Course Title	Course Type	Teaching Dept.	Teaching Hours/week				Examination			Credits
					L #	T #	P #	S #	CIE *	SEE *	Total	
1	17MAT11	Engineering Mathematics – I	BS [^]	MAT	4	1			50	50	100	4.5
2	17CHE12	Engineering Chemistry	BS [^]	CHE	4	1			50	50	100	4.5
3	17CCP13	Computer Concepts & C Programming	EC ^{\$}	CS/IS	4	1			50	50	100	4.5
4	17CED14	Computer Aided Engineering Drawing	EC ^{\$}	ME	2		4		50	50	100	4.0
5	17ELN15	Basic	EC ^{\$}	ECE	4	1			50	50	100	4.5

		Electronics Engineering									
6	17CPL16	Computer Programming Lab	EC ^{\$}	CS/IS		3		50	50	100	1.5
7	17CHL17	Engineering Chemistry Lab	BS [^]	CHE		3		50	50	100	1.5
8	17CIV18	Environment al Studies	Hu [@]	HUM	2			100 ₊	-	-	-
TOTAL							350	350	700	25.0	

SEMESTER:II

Sl No	Course Code	Course Title	Course Type	Teaching Dept.	Teaching Hours/week				Examination			Credits
					L #	T #	P #	S #	CIE *	SEE* *	Total	
1	17MAT21	Engineering Mathematics – II	BS [^]	MAT	4	1			50	50	100	4.5
2	17PHY22	Engineering Physics	BS [^]	PHY	4	1			50	50	100	4.5
3	17CIV23	Engineering Mechanics	EC ^{\$}	CV	4	1			50	50	100	4.5
4	17EME24	Elements of Mechanical Engineering & Workshop practice	EC ^{\$}	ME	4		2		50	50	100	5.0
5	17ELE25	Basic Electrical Engineering	EC ^{\$}	EEE	4	1	1		50	50	100	5.0
6	17PHL26	Engineering Physics Lab	BS [^]	PHY			3		50	50	100	1.5
7	17CIP27	Constitution of India & Professional Ethics	Hu [@]	HUM	2				100 ₊	-	-	-
8	17ENG28	Communicative English	Hu [@]	HUM	2				100 ₊	-	-	-
		TOTAL							300	300	600	25.0

SEMESTER: II

Chemistry Group												
Sl No	Course Code	Course Title	Course Type	Teaching Dept.	Teaching Hours/week				Examination		Credits	
					L #	T #	P #	S #	CIE *	SEE* *		
1	17MAT21	Engineering Mathematics – II	BS^	MAT	4	1			50	50	100	4.5
2	17CHE22	Engineering Chemistry	BS^	CHE	4	1			50	50	100	4.5
3	17CCP23	Computer Concepts & C Programming	EC\$	CS/IS	4	1			50	50	100	4.5
4	17CED24	Computer Aided Engineering Drawing	EC\$	ME	2		4		50	50	100	4.0
5	17ELN25	Basic Electronics Engineering	EC\$	ECE	4	1			50	50	100	4.5
6	17CPL26	Computer Programming Lab	EC\$	CS/IS			3		50	50	100	1.5
7	17CHL27	Engineering Chemistry Lab	BS^	CHE			3		50	50	100	1.5
8	17CIV28	Environmental Studies	Hu@	HUM	2				100+	-	-	-
		TOTAL							350	350	700	25.0

SEMESTER: III											
Sl No	Subject Code	Subject Name	Course Type	Teaching Dept.	Teaching Hours/week			Examination			Credits
					L #	T #	P #	CIE *	SEE* *	Total	
1	17MAT31	Engineering mathematics - III	BS	MAT	3	2	-	50	50	100	4
2	17 EC 32	Analog Electronics Circuits	PC	EC	4			50	50	100	4
3	17 EC 33	Digital Electronics	PC	EC	3			50	50	100	3

4	17 EC 34	Network analysis	PC	EC	3	2		50	50	100	4
5	17 EC 35	Signals and systems	PC	EC	3	2		50	50	100	4
6	17 EC 36	Microcontroller	PC	EC	4			50	50	100	4
7	17ECL37	Analog Electronics Lab	PL	EC	-	-	2	50	50	100	1
8	17 EC L38	Digital Electronics Lab	PL	EC	-	-	2	50	50	100	1
							TOTAL	400	400	800	25

SEMESTER: IV

Sl No	Subject Code	Subject Name	Course Type	Teaching Dept.	Teaching Hours/week			Examination			Credits
					L #	T #	P #	CIE *	SEE* *	Total	
1	17 MAT41	Engineering mathematics - IV	BS	MAT	3	2	-	50	50	100	4
2	17 EC42	Linear Integrated circuit	PC	EC	4			50	50	100	4
3	17 EC43	Digital signal processing	PC	EC	3	2		50	50	100	4
4	17EC44	Field and waves	PC	EC	3	2		50	50	100	4
5	17EC45	Advanced Microcontroller	PC	EC	4			50	50	100	4
6	17EC46	DSD using VERILOG	PC	EC	3			50	50	100	3
7	17ECL47	DSD using Verilog Lab	PL	EC	-	-	2	50	50	100	1
8	17ECL48	Microcontroller Lab	PL	EC	-	-	2	50	50	100	1
							TOTAL	400	400	800	25

SEMESTER: V

Sl No	Subject Code	Subject Name	Course Type	Teaching Hours/week			Examination			Credits
				L #	T #	P #	CIE*	SEE**	Total	
1	17EC51	Control system	PC	4			50	50	100	4
2	17EC52	Analog	PC	4			50	50	100	4

		communication								
3	17EC53	Fundamentals of VLSI	PC	4			50	50	100	4
4	17EC54	Data structures using C++	PC	4			50	50	100	4
5	17EC55	Microwave and RADAR	PC	4			50	50	100	4
6	17ECE56X	Program elective -1	PE	3			50	50	100	3
7	17ECL57	Digital Signal Processing Lab	PL	-	-	2	50	50	100	1
8	17ECL58	LIC+AC Lab	PL	-	-	2	50	50	100	1
							400	400	800	25

SEMESTER: VI

Sl No	Subject Code	Subject Name	Course Type	Teaching Hours/week			Course Type			Credits
				L [#]	T [#]	P [#]	CIE*	SEE**	Total	
1	17EC61	Computer communication network	PC	4			50	50	100	4
2	17EC62	Digital communication	PC	4			50	50	100	4
3	17EC63	Antenna and wave propagation	PC	4			50	50	100	4
4	17EC64	Operation research	HU	4			50	50	100	4
5	17ECE65X	Program elective-2	PE	3			50	50	100	3
6	17ECO66X	Open elective-1	OE	4			50	50	100	4
7	17ECL67	VLSI Lab	PL	-	-	2	50	50	100	1
8	17ECL68	Computer Communication network lab	PL	-	-	2	50	50	100	1
		Total					400	400	800	25

SEMESTER: VII

Sl No	Sub code	Subject Name	Course Type	Teaching Hours/week			Exam			Credits
				L	T	P	CIE	SEE	Total	
1	17EC71	Optical fiber Communication	PC	4			50	50	100	4
2	17EC72	Information theory and coding	PC	4			50	50	100	4
3	17EC73	Power electronics	PC	4			50	50	100	4
4	17ECH74	Entrepreneurship development,	HU	3			50	50	100	3

		management & IPR									
5	17EC75X	Program elective-3	PE	3			50	50	100	3	
6	17EC76X	Open elective-2	OE	4			50	50	100	4	
7	17ECL77	ADC Lab	PL	-	-	2	50	50	100	1	
8	17ECL78	Power Electronics Lab	PL	-	-	2	50	50	100	1	
9	17ECP79	Internship and Mini project	IN/MP	-	-	15	50	50	100	2	
10	17ECP83	Major project –Phase 1	PC				25+25			1	
										Total	26

SEMESTER: VIII

Sl No	Sub Code	Subject Name	Course Type	Teaching Hours/week			Exam			Credits
				L	T	P	CIE	SEE	Total	
1	17EC81	Wireless communication(4G,5G)	PC	4			50	50	100	4
2	17EC82X	Program elective -4 +(Industry Guest Lecture)	PE	3 +1			50	50	100	4
3	17EC83X	Program elective -5 (MOOC Based Elective)	PE	3			50	50	100	3
4	17ECP84	Major project-final Submission & evaluation								13
									Total	24

List of Program Electives			List of Open Electives
	P. Elective - 1	V Sem	
Sl. No.	Subject code	Subject name (Program Elective-1)	
1		Multi Media Communication-1	
2		OOPs/Python	
3		FPGA Architecture and	

		applications			
4		MEMS			
5		COA			
	P.Elective-2	VI Sem		Open Elective -1	VI Sem
Sl. No.	Subject code	Subject name (Program Elective-2)	Sl. No	Subject code	Subject name(Open Elective-1)
1		Multi Media Communication - 2/IOT			Sensors and Actuators
2		ASIC Design			Microcontroller
3		Analog and mixed mode VLSI			Essentials of NCC
4		RTOS/Embedded OS			MEMS
5		ANN/ML			Basics of Signal Processing
					Control systems
					Automotive Electronics

	P.Elective-3	VII Sem			
Sl. No.	Subject code	Subject name (Program Elective-3)		Open Elective -2	VII Sem
1		Satellite communication	Sl. No.	Subject code	Subject name (Open elective-2)
2		IP networking			Adhoc wireless network
3		Adhoc			ANN
4		Advanced DSP			Sensors and Actuators
5		System verilog			Avionics
	P. Elective -4	VIII Sem			
		Subject name (Program Elective-4)			
1		Cryptography			
2		Error control coding			
3		Automotive electronics			
4		Low power VLSI			
	P. Elective -5	VIII Sem , MOOC Based Elective			
1		AWS/Hadoop/Cloud Computing/Data Analytics			

2		SDN/NFV					
3		SoC					
4		Mobile Communication					
		Android Applications Development					

III SEMESTER

ENGINEERING MATHEMATICS-III

Course Code	17MAT31	Credits	04
Hours/Week(L-T-P)	3-2-0	CIE Marks	50
Total Hours	39(L)+26(T)	SEE Marks	50
Exam Hours	03	Course Type	Core

PRE-REQUISITES

1. Differential and integral calculus
2. Matrices, Taylor series

COURSE OUTCOMES

1. Students will be able to apply Fourier theory to analyse harmonic and periodic functions.
2. Students can apply concepts of Z transforms to Engg. Problems
3. Students can apply concepts of Laplace transforms to control systems
4. Students can use the concept of numerical interpolation to fit the given data and extrapolate the same
5. Students will be able to numerically integrate and solve differential equations arising in Engg. Field.

COURSE CONTENTS

UNIT-1 (11Hrs)

Z- transforms: Definition, Standard Z transforms, Linearity property, Damping Rule, Shifting rule, multiplication by n, Initial and final value theorems (no proof), bivariate z transforms, region of convergence, Inverse by partial fractions method, convolution theorem. Solution of difference equations. (no derivations or proof)

UNIT-2 (11 Hrs)

Fourier series: Euler's formulae, Dirichlet's conditions for Fourier series expansion, change of

interval, Even and odd function, half range series, Practical harmonic analysis.

Fourier Transforms: Definition, Complex Fourier transforms, Cosine and Sine transforms, Inverse Fourier transforms

UNIT-3 (11 Hrs)

Laplace Transforms: Definition, Transforms of standard functions (derivations and problems),

Transforms of $e^{at}f(t)$, $t^n f(t)$, $\frac{f(t)}{t}$, Laplace transforms of derivatives and integrals (no derivations), Laplace transforms of periodic functions, unit step function (no derivations), Dirac delta function . Inverse Laplace transforms, convolution theorem (without proof), solutions of 1st and 2nd order ODE using Laplace transforms

UNIT-4 (11 Hrs)

Interpolation- Newton's forward and backward formula, Newton's divided difference formulae and Lagrange's formula for unequal intervals and inverse interpolation by Lagrange's formula, valuation of derivatives using Newton's forward and backward difference interpolation formulae

Numerical Integration - Trapezoidal, Simpson's $\frac{1}{3}$ and $\frac{3}{8}$ rule, Weddle's rule

UNIT-5 (11 Hrs)

System of equations: Solution of system of equations by LU decomposition, Solution of Tridiagonal system by Thomas algorithm, Eigen values of symmetric matrix by Jacobi method, Power method

Numerical solution of ordinary differential equations: Taylor's series method, Runge-Kutta 4th order method

TEXT BOOKS

- Higher Engg. mathematics by Dr. B S Grewal, 42nd Edition
- Introductory methods of numerical analysis, by S SSastry, PHI India

REFERENCE BOOKS

- Advanced Engg. Mathematics by Erwin E Kreyszig, 8th edition, Wiley.
- Numerical Methods by Jain , Iyengar and Jain, New Age, 6th edition, 2012

TEACHING METHODOLOGY

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class

COURSE ASSESSMENT METHOD

CIE:

- Tutorials - 10 Marks
- Surprise tests - 10Marks.

- Three mid examinations, 30 Marks each will be conducted and the Average of best of two will be taken.

SEE:

- Two Questions are to be set from each unit, carrying 20 Marks each.
- Students have to answer 5 questions selecting one full question from each unit

CO-PO-PSO MAPPING

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	*	*												
CO2	*	*												
CO3	*	*												
CO4	*	*	*											
CO5	*	*	*											

ANALOG ELECTRONICS CIRCUITS

Course Code	17EC32		Credits	04
Hours/Week(L-T-P)	4-0-0		CIE Marks	50

Total Hours	52(L)		SEE Marks	50
Exam Hours	03		Course Type	Core

PRE-REQUISITES

Basic of electronics engineering

COURSE OUTCOMES

- Define, understand and explain the structure, V-I characteristics, working of analog electronic devices like diodes, Bipolar Junction Transistors (BJTs), JFETs and MOSFETs.
- Illustrate DC and AC analysis of BJT, JFET and MOSFET amplifier circuits.
- Interpret the performance characteristics of transistor based amplifiers and their frequency Response.
- Design analog electronic circuits such as diode clippers and clampers, amplifiers using BJTs, JFETs and MOSFETs, power amplifiers, feedback amplifiers, oscillators for given specifications.
- Apply the knowledge of analog circuits for various applications in electronic systems.

COURSE CONTENTS

UNIT-1 (11Hrs)

Diode and its Applications:

Load line analysis, Rectifiers with Capacitor filters (with derivation), Nonlinear applications of diode (Clippers & Clampers).

BJTDC Analysis:

Operating point, Fixed bias circuits, Emitter stabilized biased circuits, Voltage divider biased

BJT AC Analysis:

BJT re modelling (CB, CE configuration), CE Fixed bias configuration, Emitter Bias ,Voltage divider bias, (Derivation of Z_i, Z_o, A_v, A_i for the configuration)

T1:2.2,2.6,2.7,2.8,2.9, T1:4.2,4.3,4.4,4.5, T1:5.4,5.8,5.9,5.10

UNIT-2 (11 Hrs)

Metal-Oxide Field Effect Transistor (MOSFET): MOS Field –Effect Transistor, Two-Terminal MOS Structure, N-Channel Enhancement –Mode MOSFET, Ideal MOSFET Current-Voltage Characteristics-NMOS Device, p-Channel Enhancement –Mode MOSFET, Ideal MOSFET Current-Voltage Characteristics-PMOS Device, Additional MOSFET structures and Circuit Symbols, MOSFET DC Circuit Analysis: Common-Source circuits, DC load line and region of operation,

Common-MOSFETs configurations

DC Circuit Analysis: Junction Field Effect Transistor (JFET): Introduction, Construction and characteristics of JFET , Transfer Characteristics, Fixed bias

T2-3.1, 3.2, T1-Ch6 :6.1,6.2, 6.3, Ch7 : 7.1,7.2

AC Analysis:

MOSFET Amplifiers: Graphical Analysis, load line and Small-Signal parameters, AC Equivalent Circuit, Small-Signal Model. Common Source, Source Follower (Common Drain), Common Gate

JFET Amplifiers: Small-Signal Equivalent Circuit, Small-Signal Analysis

T2-4.1-4.2,4.3,4.4,4.5,4.9

UNIT-3 (11 Hrs)

Multistage Amplifiers: Multistage (CS-CS),(CS-CE) Cascode (CS-CG) Amplifiers

JFET Frequency Response: logarithms, Decibels, low frequency response FET Amplifier, Miller effect capacitance, High frequency response JFET amplifier, Multistage frequency effects,

T2-4.8, T1-9.2,9.3,9.7,9.8,9.10,9.11

UNIT-4 (11 Hrs)

Feedback and Oscillator Circuits: Feedback Concepts, Effect of negative feedback on Input impedance, Output impedance, Gain and Bandwidth product, feedback topologies: Voltage Series Feedback, Voltage Shunt Feedback, Current Series Feedback, Current Shunt Feedback, Practical feedback circuit based on FET

Oscillator operation, Phase shift oscillator, Wein bridge oscillator, Tuned oscillator circuit, Crystal oscillator, UJT oscillator.

T1:14.1,14.2,14.3,14.5,14.6,14.7,14.8,14.9,14.10

UNIT-5 (11 Hrs)

Power Amplifiers: Introduction, Definitions and amplifier types : series fed class A amplifier, Transformer coupled Class A amplifiers, Class B amplifier operations, Class B amplifier circuits, Class C and Class D amplifier circuits.

Discrete Transistor Voltage Regulation: Discrete transistor voltage regulation-Series and Shunt voltage regulators.

T1:12.1,12.2,12.3,12.4,12.5,12.8, T1:15.5

TEXT BOOKS

1: Robert L. Boylestad and Louis Nashelsky, “Electronic Devices and Circuit Theory”, PHI/Pearson Education, 9th Edition.

2: Donald A. Neamen, "Electronic Circuit Analysis and Design", TATA McGraw Hill, 3rd Edition 2.

REFERENCE BOOKS

- David A. Bell, "Electronic Devices and Circuits", PHI, 4th Edition, 2004
- Malvino, Albert Paul "Electronic Principles", 6th edition ,2000
- Jacob Millman & Christos C. Halkias, "Electronic Devices and Circuits", Tata -McGraw Hill, 1991

TEACHING METHODOLOGY

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class

COURSE ASSESSMENT METHOD

CIE:

- Tutorials - 10 Marks
- Surprise tests - 10Marks.
- Three mid examinations, 30 Marks each will be conducted and the Average of best of two will be taken.

SEE:

- Two Questions are to be set from each unit, carrying 20 Marks each.
- Students have to answer 5 questions selecting one full question from each unit

CO-PO-PSO MAPPING

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	*	*	*	*	*				*		*			
CO2	*	*	*	*	*				*		*			
CO3	*	*	*	*	*				*		*			
CO4	*	*	*	*	*				*		*			
CO5	*	*	*	*	*				*		*	*		

DIGITAL ELECTRONICS

Course Code	17EC33	Credits	04
Hours/Week(L-T-P)	4-0-0	CIE Marks	50
Total Hours	52	SEE Marks	50

Exam Hours	03		Course Type	Core
------------	----	--	-------------	------

PRE-REQUISITES

Students must have the knowledge of

- Various Number systems
- Logic gates
- Boolean algebra
- Logic families

COURSE OUTCOMES

- Students will possess the ability to identify basic requirements for a design application.
- Students will have a thorough understanding of the fundamental concepts and techniques used in digital electronics.
- Students will possess the ability to understand, analyze and design various combinational and sequential circuits.
- Students will be able to explain the elements of digital system abstractions such as digital representation of information, digital logic, Boolean algebra and Finite State Machines (FSM).
- Students will be able to design the memory required for digital devices

COURSE CONTENTS

UNIT-1 (11Hrs)

Boolean algebra and Combinational Networks:

Definition of Boolean algebra and theorems, Boolean formulas and functions, canonical formulas: minterm and maxterm, Equation complementation, Equation simplification and Reduction Theorems, Gates and combinational networks, Incomplete Boolean functions and Don't care conditions, Additional Boolean operations and gates, Gate Properties.

Text 1: Ch 3. 3.1 to 3.10

UNIT-2 (11 Hrs)

Simplification of Boolean expressions: Formulation of the simplification problem, Prime implicants and irredundant disjunctive expressions, Prime implicants and irredundant conjunctive expressions, Karnaugh Maps, Using K-Maps to obtain minimal expressions for complete Boolean functions, Minimal expressions of incomplete Boolean functions, Five-Variable and Six-variable K-Maps. Quine Mc-clusky method of generating prime implicants. Variable Entered K maps

Text 1: Ch 4.1- 4.8, 4.14

UNIT-3 (11 Hrs)

Logic Design with MSI components and programmable logic devices: Binary adders and Subtractors, Decimal adders. Comparators, Decoders, Encoders, Multiplexers, Programmable Logic

CO2	*	*											
CO3	*		*										
CO4	*			*			*						
CO5	*						*						

NETWORK ANALYSIS				
Course Code	17EC74		Credits	04
Hours/Week(L-T-P)	3-2-0		CIE Marks	50
Total Hours	39(L)+26(T)		SEE Marks	50
Exam Hours	03		Course Type	Core
PRE-REQUISITES				
<ul style="list-style-type: none"> • MATHEMATICS-1 • MATHEMATICS-2 				

COURSE OUTCOMES	
<ul style="list-style-type: none"> • Students will be able to understand and solve the problems related to networks. • Students will be in a position to simplify the complex circuits using network theorems • Students will be able to analyze simple DC circuits and AC circuits and apply the concepts to transient conditions 	

- Students are able to solve the network problems using graphical method.
- Students are able to analyze the network concepts and can apply the same for real time application to solve network related problems

COURSE CONTENTS
UNIT-1 (11Hrs)
Basic circuit analysis concepts: Practical Sources, Source transformation, Network reduction using star delta transformation, Mesh analysis and Node analysis with dependent and Independent sources for DC and AC networks. Concepts of super node and super mesh.
Text1: Ch 1, Ch 2
UNIT-2 (11 Hrs)
Network Theorems: Superposition theorem, Reciprocity theorem, Thevenin's theorem, Norton's theorem Millman's theorem, Maximum power transfer theorem
Text1: Ch 7
UNIT-3 (11 Hrs)
Transient behaviour and initial conditions: Behavior of circuit elements under switching condition and their representation of initial and final conditions in RL,RC and RLC circuits for AC and DC excitations
Laplace transform and it's applications: Laplace transform of periodic functions, Solution of linear differential equation, Solution of network problems.
Text1: Ch 5, Ch 6
UNIT-4 (11 Hrs)
Graph Theory and Network equations: Graph of a network, Trees, Co-trees and Loops, Incidence Matrix, Cut-set Matrix, Tie-set Matrix and loop currents, Number of possible trees of a graph, Analysis of networks, Duality.
Text1: Ch 3
UNIT-5 (11 Hrs)
Two port Network: Characterization of linear time invariant two port network, open circuit impedance parameter, short circuit admittance parameter, transmission parameter, inverse transmission parameter, hybrid parameter, inverse hybrid parameter, relationship between parameters, input and output impedance in terms of two-port parameters.
Text1: Ch 8, Ch 10
TEXT BOOKS

- Van Valkenburg M. E. "Nework Analysis", Prentice Hall of India Pvt Ltd. 3rd Edition, 2002

REFERENCE BOOKS

- D. Roy Choudhury, "Networks and Systems", New Age International Pvt Ltd Publishers (January 30, 2010)
- Franklin F. Kuo, "Network Analysis and Synthesis", John Wiley and Sons 2nd Edition, 2002
- P.M Chandrashekaraiah, "Network analysis" Rajeshwari publication, 2008 edition.
- Network Analysis by Ganesh Rao
- Network Analysis by Ravish R Aradhya

TEACHING METHODOLOGY

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class

COURSE ASSESSMENT METHOD

CIE:

- Tutorials - 10 Marks
- Surprise tests - 10Marks.
- Three mid examinations, 30 Marks each will be conducted and the Average of best of two will be taken.

SEE:

- Two Questions are to be set from each unit, carrying 20 Marks each.
- Students have to answer 5 questions selecting one full question from each unit

CO-PO-PSO MAPPING

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	*	*	*	*										
CO2	*	*	*	*										
CO3	*	*	*	*										
CO4	*	*	*							*				
CO5	*	*	*		*					*				

SIGNALS AND SYSTEMS

Course Code	17EC35	Credits	04
Hours/Week(L-T-P)	3-2-0	CIE Marks	50
Total Hours	39(L)+26(T)	SEE Marks	50
Exam Hours	03	Course Type	Core

PRE-REQUISITES

- MATHEMATICS-1
- MATHEMATICS-2

COURSE OUTCOMES

- Students will analyze types of signals and operations on signals.
- Students will be able to carry out time and frequency domain representation of linear signals and systems.
- Students will be able to analyse the response of LTI system for all possible inputs
- Students will carry out the conversion between time domain and frequency domain signals using Fourier and Z Transforms.
- Students will be able to carry out analysis and characterization of LTI systems using Z transforms.

COURSE CONTENTS

UNIT-1 (11Hrs)

Signals and Systems: Introduction, continuous time and discrete time signals, Transformations of the independent variable, exponential and sinusoidal signals, unit impulse and unit step functions, Continuous time and discrete time systems, Basic System properties.

Ch-1: 1.0-1.6

UNIT-2 (11 Hrs)

Linear Time Invariant Systems

Introduction, Discrete time LTI system: Convolution sum, Representation of discrete time signals in terms of impulses, discrete time unit impulse response and convolution sum Representation of LTI systems.

Continuous Time LTI system: Convolution integral: Representation of continuous time signals in terms of impulses, Continuous time unit impulse response and convolution integral representation of LTI systems, Causal LTI systems described by differential and difference equations.

Ch-2 :2.1-2.4

UNIT-3 (11 Hrs)

Fourier Series Representation: Introduction, Response of LTI systems to complex exponentials, Fourier series representation of Continuous time periodic signals, Convergence of Fourier series, properties of Continuous time Fourier series, Fourier series representation of discrete time periodic signals, properties of discrete time Fourier series, Examples of CT filters described by differential equations, Examples of DT filters described by difference equations,

Representation of aperiodic signals: CTFT, Fourier transform for periodic signals, Systems characterized by linear constant coefficient differential equations

Representation of aperiodic signals: DTFT, Fourier transform for periodic signals, Systems characterized by linear constant coefficient difference equations

Ch-3: 3.2, 3.3, 3.4,3.5,3.6,3.7,3.10,3.11 , Ch-4:4.1,4.2,4.7, Ch-5: 5.1,5.2,5.8

UNIT-4 (11 Hrs)

Sampling: Representation of CT signals by its samples, Sampling Theorem, Reconstruction of a signal from its samples using Interpolation, Effect of under sampling: Aliasing, Sampling of Discrete time signals.

Ch- 7 :7.1, 7.2, 7.3,7.5

UNIT-5 (11 Hrs)

Z-Transform: Introduction, Region of convergence for Z-transform,Inverse Z transform,Properties of Z-transform, Some common Z transform pairs.

Analysis and characterization of LTI systems using Z-transforms, Block diagram Representation, unilateral Z-transform

Ch10: 10.1,10.2,10.3,10.5,10.6,10.7,10.8,10.9

TEXT BOOKS

- Alan V Oppenheim, Alan S, Willsky and A Hamid Nawab, "Signals and Systems", Pearson Education Asia / PHI, 2nd edition, 2002

- Simon Haykin and Barry Van Veen, "Signals and Systems" John Wiley and Sons, Inc., 2002
- Michael J. Roberts, "Signals and Systems - Analysis using transform methods and MATLAB", Tata McGraw-Hill , 1st Edition, 2003.

REFERENCE BOOKS

TEACHING METHODOLOGY

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class

COURSE ASSESSMENT METHOD

CIE:

- Tutorials - 10 Marks
- Surprise tests - 10Marks.
- Three mid examinations, 30 Marks each will be conducted and the Average of best of two will be taken.

SEE:

- Two Questions are to be set from each unit, carrying 20 Marks each.
- Students have to answer 5 questions selecting one full question from each unit

CO-PO-PSO MAPPING

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	*	*	*								*			
CO2	*		*						*					
CO3	*	*	*	*					*		*			
CO4	*	*	*	*	*						*			
CO5	*	*	*		*				*					

MICROCONTROLLER

Course Code	17EC36	Credits	03
-------------	--------	---------	----

Hours/Week(L-T-P)	3-0-0		CIE Marks	50
Total Hours	39(L)		SEE Marks	50
Exam Hours	03		Course Type	Core

PRE-REQUISITES

Programming experience with C and assembly is strongly recommended

COURSE OUTCOMES

- Students will be able to learn the hardware architecture and instruction set of 8051 microcontroller.
- Students will be able to analyze the given problem and write programs in assembly language and C language.
- Students will be able to write programs to develop communication between 8051 and other devices.
- Students will learn to interface 8051 with external hardware.
- Students will be able to design and implement projects based on 8051.

COURSE CONTENTS

UNIT-1 (8Hrs)

The 8051 Architecture: ALU, I/O ports, Special function registers, PSW, internal ROM architecture and addressing Modes.

Data transfer instructions: External data moves, Code Memory data moves, PUSH and POP Instructions, Data Exchanges. Example Programs.

Text 2: Ch 1,3,5

UNIT-2 (7Hrs)

Logical and Arithmetic Instructions: Byte level logical operations, Bit level logical operations, Rotate and swap operations. Incrementing and decrementing, addition, subtraction, multiplication and division, decimal arithmetic, Example Programs. Jump and Call Instructions: Example Programs.
Text 2: Ch 6,7,8

UNIT-3 (8Hrs)

8051 Programming in C: Data types and time delays in 8051C, I/O programming, logic operations, data conversion programs and data serialization.

8051 Timer and counter programming: TMOD, TCON special function registers and programming Examples in C.

Text 1: Ch 7, 9

UNIT-4 (11 Hrs)
8051 Serial Communication: Basics of serial Communication, 8051 connections to RS 232, Serial communication Programming, SBUF, SCON SFRs. Programming examples in C.
Interrupts Programming: 8051 Interrupts, Programming timer interrupts, programming external hardware interrupts, Programming the serial communication interrupts. Programming examples in C.
Text 1: Ch 10,11
UNIT-5 (11 Hrs)
8051 Interfacing and Applications: Interfacing 8051 to LCD, keyboard, parallel and serial ADC, DAC, stepper motor and DC motor. Programming in C.
Text 1: Ch 12, 13, 17
TEXT BOOKS
<ul style="list-style-type: none">• Muhammad Ali Mazidi and Janice Gillespie Mazidi and Rollin D. McKinlay, “The 8051 Microcontroller and embedded systems – using assembly and C”, Prentice Hall India, Pearson, 2006• Kenneth Ayala, “The 8051 Microcontroller”, Thomson Delmar Learning, 3rd Edition
REFERENCE BOOKS
<ul style="list-style-type: none">• Predko, ”Programming and customizing the 8051 micro controller”, Tata McGraw Hill• Frank Vahid& Tony Givargis, “Embedded System design”, John Wiley, 2002.• Michael J. Pont, “Embedded C”, Pearson Education, 2002.

CO2		*		*	*											
CO3		*	*		*											
CO4			*		*											
CO5		*	*	*	*		*		*		*		*			

ANALOG ELECTRONICS LAB				
Course Code	17ECL37		Credits	01
Hours/Week(L-T-P)	0-0-2		CIE Marks	50
Total Hours	13(P)		SEE Marks	50
Exam Hours	03		Course Type	Core

COURSE OUTCOMES	
<ul style="list-style-type: none"> Students will be able to design and test rectifiers, clipping circuits and clamping circuits. Students will be able to understand the operation of the transistors, the concept of biasing, and amplifier topologies. Students will be able to design and test various types of oscillators Students will be able to compute the parameters from the characteristics of JFET and MOSFET 	

devices.

- Students will be able to design and test a power amplifier.

COURSE CONTENTS

LIST OF EXPERIMENTS

- Demonstrate the working of Bridge Rectifier.
- Design and conduct to demonstrate clipping and clamping circuits.
- Realize BJT Darlington Emitter follower with and without Bootstrapping and determine the gain, input and output impedances.
- Design and set up the BJT common emitter amplifier using voltage divider bias with and without feedback and determine the gain-Bandwidth product from its frequency response.
- Plot the transfer and drain characteristics of a JFET and calculate its drain resistance, mutual conductance and amplification factor.
- Design, setup and plot the frequency response of Common Source JFET/MOSFET amplifier and obtain the bandwidth.
- Plot the transfer and drain characteristics of n-channel MOSFET and calculate its parameters, namely; drain resistance, mutual conductance and amplification factor.
- Set-up and study the working of complementary symmetry class B push pull power amplifier and calculate the efficiency.
- Design and set-up the RC-Phase shift Oscillator using FET, and calculate the frequency of output waveform.
- Design and set-up the Hartley Oscillator circuit and determine the frequency of oscillation.
- Design and set-up the Colpitts Oscillator circuits and determine the frequency of oscillation.
- Design crystal oscillator circuit and determine the frequency of oscillation.

DIGITAL ELECTRONICS LAB

Course Code	17ECL38	Credits	01
Hours/Week(L-T-P)	0-0-2	CIE Marks	50
Total Hours	13(P)	SEE Marks	50
Exam Hours	03	Course Type	Core

PREREQUISITES:

- Basic electronics

COURSE OUTCOMES

- Students will be able to construct logic circuits using MSI ICs to realize given function.
- Students will be able to design combinational and sequential circuits for an application.
- Students will be able to analyze and design mini projects based on principles of digital electronics
- Students will be able to develop the ability to understand current applications, trends and new directions in Digital design

COURSE CONTENTS

LIST OF EXPERIMENTS

NOTE: Use discrete components to test and verify the logic gates. Lab View can be used for designing the gates along with the above.

1. Realization of all gates using diodes and Transistors.
2. Simplification, Realization of Booleans Expressions using logic gates/universal gates and verify,
 - (a) De-morgan's Theorem for 2, 3, 4 variables.
 - (b) The sum-of product and product-of- sum expressions using universal gates.
3. Design and implement
 - (a) Full Adder /Full Subtractor using basic logic gates.
 - (b)Full Adder /Full Subtractor using Universal gates.
4. Design and implement 4-bit Parallel Adder/ Subtractor using IC 7483.
5. Design and Implement BCD to EXCESS 3 Conversion and Vice Versa using
 - (a)Logic Gates
 - (b)Parallel Adder/Subtractor IC 7483
- Design and Implement BCD to Gray Conversion and Vice Versa using logic gates.
7. Realize
 - (a) 2:1/4:1 multiplexer using gates.
 - (b)Adders/Subtractors Using IC 74153
 - (c) 1:4 Demux using Gates
 - (d)Adders/Subtractors using IC 74139
8. Design and Implementation of magnitude comparators.
 - (a)One and two bit Comparator using Logic gates
 - (b) 4 bit and 8 bit comparator using IC 7485

9. Realize the following flip-flops using.

(a) JK Flip-Flop Using Nand gates

(b) Clocked SR, JK, D, T Flip Flop using IC 7476

10. Realize the following shift registers using IC7495

(a)SISO

(b) SIPO

(c) PISO

(d) PIPO

11. Design and Implement Asynchronous Mod N up/Down Counter using IC 7476.

12. Design and Implement Synchronous Mod N up/down counter using IC 7476

13. Design and Implement Ring/Johnson counter Using IC 7495

14. Simulate Full- Adder using simulation tool.

15. Simulate Mod-8 Synchronous UP/DOWN Counter using simulation tool.

CO-PO-PSO MAPPING

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	*	*		*							*	*		
CO2	*	*		*	*						*	*		
CO3		*		*	*						*	*		
CO4											*	*		
CO5	*	*		*							*	*		

IV SEMESTER

SEMESTER: IV**ENGINEERING MATHEMATICS-IV**

Course Code	17MAT41		Credits	04
Hours/Week(L-T-P)	3-2-0		CIE Marks	50
Total Hours	39(L)+26(T)		SEE Marks	50
Exam Hours	03		Course Type	Core

PRE-REQUISITES

- Differential and integral calculus
- Matrices, Taylor series

COURSE OUTCOMES

1. Students understand concepts and applications of probability, distributions, sampling.
2. Students understand essentials and applications of linear algebra.
3. Students will be able model physical situations using statistical tools like hypothesis testing
4. Students will be able to understand basics of random processing and apply same
5. Students will be able to understand importance of Markova process

COURSE CONTENTS
UNIT-1 (11Hrs)
<p>Random variable, discrete probability distribution, continuous random variables, continuous probability distribution, cumulative density function, Expectation, variance.</p> <p>Joint distribution- continuous and discrete, expectation, variance, standard deviation, covariance</p> <p>Binomial, Poisson, Exponential, Normal</p>
UNIT-2 (11 Hrs)
<p>Population and sample, sampling with and without replacement, sampling distribution of means, sample variance. Unbiased estimate, reliability, confidence intervals for mean, variance and proportion, statistical hypothesis, testing of hypothesis, Type I and II errors, one tailed, two tailed tests, t - distribution, 2 – test, test for goodness of fit.</p>
UNIT-3 (11 Hrs)
<p>Random process- definition, classification, pdf, cdf, mean, auto correlation, Stationary and Ergodic random process, Poisson process</p> <p>Markov process- Definition, examples, TPM, n – step transitional probabilities, regular, ergodic matrices, stationary distribution, classification of states, Markov chain with absorbing states, periodic, transient and recurrent states.</p>
UNIT-4 (11 Hrs)
<p>Vector spaces- definition, examples, Linear combinations, subspaces, linear dependence, basis and dimension, linear mapping, linear operator, matrix representation of linear operator, change of basis.</p>
UNIT-5 (11 Hrs)
<p>Polynomial of matrices, Characteristic polynomial, Cayley Hamilton theorem, diagonalization, Eigenvalues and eigen vectors, minimal polynomial, inner product space, Jordan canonical form, , Orthogonal vectors and subspaces, Gram Schmidt Orthogonalisation process, Quadratic forms</p>
TEXT BOOKS
<ul style="list-style-type: none"> • Probability and statistics, by Murray R Spiegel, J Schiller, R Alu Srinivasan, Schaum's outline series, second edition • Operations research by Richard Bronson & Govindasami Nadimuthu, Schaum's outline series, second edition • Linear Algebra by Lipschitz, Schaum's outline series, second edition • Probability and random process by S Palaniappan, PHI, 2012
REFERENCE BOOKS
TEACHING METHODOLOGY

SEMESTER: IV**LINEAR INTEGRATED CIRCUITS**

Course Code	17EC42	Credits	04
Hours/Week(L-T-P)	4-0-0	CIE Marks	50
Total Hours	52(L)	SEE Marks	100
Exam Hours	03	Course Type	Core

PRE-REQUISITES

- Basic electronics
- Analog electronic circuits

COURSE OUTCOMES

- Define and describe various parameters of op – amp, its characteristics and specifications
- Discuss the effects of Input and output voltage ranges upon Op-Amp circuits
- Sketch and analyze op- amp circuits to determine input impedances, output impedances and other performance parameters
- Describe and sketch the various switching circuits of Op-Amp and 555 timer and analyze its operations
- Differentiate between various types of DACs and ADCs and evaluate the performance of each with neat circuit diagrams and assuming suitable inputs.

COURSE CONTENTS**UNIT-1 (11Hrs)**

Introduction to operational amplifiers: Operational amplifier description, Basic operational amplifier circuit, OPAMP 741 IC (excluding IC amp circuit), Voltage follower circuit, Non-inverting amplifier, Inverting amplifier.

Operational Amplifier parameters: Input and Output voltage, Common mode and supply rejection ratio, Offset voltages and currents, Input and output impedances, Slew rate and frequency limitations.

OPAMP as DC Amplifiers: Basing OPAMP, Direct coupled voltage follower, Direct coupled non inverting amplifier, Direct coupled inverting amplifier, Summing amplifier, Difference amplifier.

Text1: 1.1, 1.2, 1.3, 1.4, 1.5, 1.6

Text1: 2.1, 2.2, 2.3, 2.4, 2.5

Text 1: 3.1, 3.2, 3.3, 3.4 3.5

UNIT-2 (11 Hrs)

OPAMP as AC Amplifier: Capacitor coupled voltage follower, Capacitor coupled non inverting amplifier, Capacitor coupled inverting amplifier, setting the upper cut off frequency, Capacitor coupled difference amplifier, Use of single polarity supply.

OPAMP's frequency response and compensation: OPAMP circuit stability, Frequency and phase response, Frequency compensating methods

Text 1:4.1,4.3,4.5,4.6,4.7,4.8

Text 1: 5.1, 5.2, 5.3

UNIT-3 (11 Hrs)

Miscellaneous OPAMP linear applications: Voltage sources, Current sources and current sinks, Current amplifiers, Instrumentation amplifier.

Signal Processing Circuits: Precision half wave rectifiers, Precision full wave rectifiers, Limiting circuits, Clamping circuits, Peak detectors, Sample and hold circuits

Text 1:6.1, 6.2, 6.4, 6.8

Text 1: 7.1, 7.2, 7.3, 7.4, 7.5, 7.6

UNIT-4 (11 Hrs)

Differentiating and Integrating Circuits: Differentiating circuit, Differentiator Design, Integrating circuit, Integrator Design,

OPAMP nonlinear circuits: OPAMP in switching circuits, crossing detectors inverting Schmitt trigger circuit, Non-inverting Schmitt circuits, Astablemultivibrator, and Mono stable multivibrator.

Signal Generator: Triangular / Rectangular wave generator, Waveform Generator Design, Phase Shift Oscillator, Wein Bridge Oscillator

Text1: 8.1, 8.2, 8.4, 8.5, 9.1, 9.2, 9.3, 9.4, 9.5, 9.6

Text 1: 10.1, 10.2, 10.3, 10.5

UNIT-5 (11 Hrs)

Active Filters: All Pass shifting Circuits, First order Low Pass active filter, First order high pass filter, Band pass filters, Band Stop filter

DC Voltage Regulators: Voltage Regulator Basics, voltage follower regulator

555 Timer: Description of functional diagram, Monostable operation, Astable operation, Schmitt trigger

Phase Locked Loop: Basic Principles, Phase detector / comparator, Voltage Controlled Oscillator (VCO)

D-A and A-D Converters: Basic DAC techniques, weighted Resistor DAC, R-2R Ladder DAC, A-D Converters, Direct Type ADCs: Parallel Comparator (flash) A/D Converter, Successive Approximation Converter

Text 1: 11.1, 11.2, 11.4, 11.8, 11.10

Text 2: 8.1, 8.2, 8.3, 8.4, 8.5, 9.2, 9.3, 9.4

Text 2: 10.1, 10.2, 10.2.1, 10.2.2, 10.3, 10.3.1, 10.3.4

TEXT BOOKS

- David A. Bell," Operational Amplifiers and Linear IC's", PHI, 2nd edition, 2004.
- D. Roy Choudhury and Shail B. Jain "Linear Integrated Circuits", New Age International, 2nd edition, 2006.

REFERENCE BOOKS

- Allen Holberg : Analog and Mixed mode VLSI"
- Robert. F. Coughlin and Fred.F.Driscoll," Operational amplifiers and Linear Integrated Circuits", Pearson, 2006.
- Ramakant A. Gayakwad, "Op - Amps and Linear Integrated Circuits", PHI, 4th edition, 1999.

TEACHING METHODOLOGY

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class

COURSE ASSESSMENT METHOD

- Two Surprise Tests, 10 Marks each. Average of two tests will be taken.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.
- Course Project(Mini project)
- Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.

CO-PO-PSO MAPPING

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	*	*	*	*	*				*		*			
CO2	*	*	*	*	*				*		*			
CO3	*	*	*	*	*				*		*			
CO4	*	*	*	*	*				*		*			
CO5	*	*	*	*	*				*		*	*		

SEMESTER: IV**DIGITAL SIGNAL PROCESSING**

Course Code	17EC43		Credits	04
Hours/Week(L-T-P)	3-0-0		CIE Marks	50
Total Hours	52		SEE Marks	50
Exam Hours	03		Course Type	Core

PRE-REQUISITES

- Signals and Systems
- Mathematical concepts – Calculus, Matrix operations

COURSE OUTCOMES

- Interpret response of LTI systems using time domain and frequency domain techniques.
- Analyze frequency domain representations of real and complex discrete time signals.
- Design digital filters and solve numerical problems
- Realization of Digital filters using digital computations

COURSE CONTENTS**UNIT-1 (11Hrs)**

Review of Signals and Systems –LTI systems, Fourier representation

Discrete Fourier Transforms (DFT): Frequency domain sampling and reconstruction of discrete time signals. DFT as a linear transformation, its relationship with other transforms. Properties of DFT, multiplication of two DFTs- the circular convolution, Additional DFT properties.

Ref: Text book #1

UNIT-2 (11 Hrs)

Use of DFT in linear filtering, overlap-save and overlap-add method.

Fast-Fourier-Transform (FFT) algorithms: Direct computation of DFT, need for efficient computation of the DFT (FFT algorithms), Radix-2 FFT algorithm for the computation of DFT and IDFT-decimation-in-time and decimation-in-frequency algorithms

Ref: Text book #1

UNIT-3 (11 Hrs)

Applications of FFT Algorithms, Goertzel algorithm, and chirp-z transform.

Ref: Text book #1

Analog filter design: Characteristics of commonly used analog filter – Butterworth and Chebyshev(Type 1) filters, analog to analog frequency transformations.

Ref: Text book #2

Digital Signal processors: Case study based on TMS320C6713 Digital Signal Processor, Programming Examples.

Ref: Reference book #3

UNIT-4 (10 Hrs)

IIR filter design: Approximation of derivative and bilinear transformation method, Matched Z-Transforms, Verification for stability and linearity during mapping.Design of IIR Filters from analog filter (Butterworth and Chebyshev) Impulse invariance, Mapping of transfer functions.

Structure for IIR Systems: Direct forms, Cascade form, Parallel form structures.

Ref: Text book #2

UNIT-5 (10 Hrs)

FIR filter design: Introduction to FIR filters, design of FIR filters using Window based method, Linear phase FIR filter design using frequency sampling and Equiripple filter design. Design of FIR Differentiators. Design of Hilbert Transformers

Structure for FIR Systems: Direct form, Linear Phase, Frequency sampling structure, Lattice structure.

Ref: Text book #2

TEXT BOOKS

- Digital signal processing – Principles Algorithms & Applications, Proakis&Monalakis, Pearson education, 4th Edition, New Delhi, 2007.
- Fundamentals of Digital Signal Processing, Lonnie C. Ludeman,

REFERENCE BOOKS

1. Discrete Time Signal Processing, Oppenheim & Schaffer, PHI, 2003.
2. Digital Signal Processing, S. K. Mitra, Tata Mc-Graw Hill, 3rd Edition, 2010.
3. Digital Signal Processing and Applications with the C6713 and C6416 DSK,RulphChassaing, Wiley Interscience

TEACHING METHODOLOGY

- Blackboard teaching, PowerPoint presentations
- Problem-solving sessions
- Regular review of students by asking questions based on topics covered in the class

COURSE ASSESSMENT METHOD

CIE:

- Two Quiz, 10 Marks each and average of two will be taken.
- Assignment/course project based test. 10 Marks each. Best of two tests will be taken.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.

SEE:

- Final examination, of 100 Marks will be conducted; evaluated for 50 Marks.

CO-PO-PSO MAPPING

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	*		*											
CO2	*	*												
CO3	*		*											
CO4	*			*			*							
CO5	*						*							

SEMESTER: IV

FIELDS AND WAVES

Course Code	17EC44	Credits	04
--------------------	---------------	----------------	-----------

Hours/Week(L-T-P)	3-2-0		CIE Marks	50
Total Hours	39(L)+26(T)		SEE Marks	50
Exam Hours	03		Course Type	Core
PRE-REQUISITES				
<ul style="list-style-type: none"> • Vector Analysis • Mathematics-I and II 				

COURSE OUTCOMES
<ul style="list-style-type: none"> • A basic understanding of electro -and magneto -statics sufficient to enable further study of advanced fields and waves topics. • Formulate potential problems within electrostatics, magneto statics and stationary current distributions in linear, isotropic media and also solve such problems in simple geometries using separation of variables and the method of images. • Define and derive expressions for the energy both for the electrostatic and magneto static fields • AnalysePointing theorem from Maxwell's equations and interpret the same in terms of laws and theorems. • Describe and make calculations of plane electromagnetic waves in homogeneous media, including reflection of such waves in plane boundaries between homogenous media.

COURSE CONTENTS
UNIT-1 (11Hrs)
<p>Vector Analysis: Scalars & vectors, Vector Algebra, the Cartesian coordinate system, vector components & unit vectors, vector field, Dot product & cross product, circular coordinate system, cylindrical coordinate system, spherical coordinate system.</p> <p>Coulomb's Law and Electric Field Intensity: The Experimental law of Coulomb, Electric Field Intensity, and Field due to continuous Volume charge distribution, Field of a line charge, field of a sheet charge.</p> <p>Electric Flux density, Gauss's Law & Divergence: Electric Flux density, Gauss Law, Applications of Gauss' Law: Differential Volume Element, Divergence, Maxwell's First Equation (Electrostatics),The vector operator DEL and Divergence Theorem.</p> <p>Text 1: Ch 1.1, 1.2,1.3,1.4,1.5,1.6,1.7,1.8,1.9, Ch 2.2.1 to 2.5, Ch 3.3.1, 3.2, 3.3, 3.4, 3.5, 3.6, 3.7</p>
UNIT-2 (11 Hrs)
<p>Energy and Potential: Energy & potential in a moving point charge in an Electric Field, The Line Integral, Definition of potential difference & potential, The potential field of a point charge, The potential field of a system of charges: conservative property, Potential Gradient, The Dipole, Energy density in the Electric Field.</p> <p>Conductors, Dielectrics and Potential: Current & current density, continuity of current, metallic conductors, conductor properties & boundary conditions. The method of images, Semiconductors,</p>

Nature of Dielectric materials, Boundary conditions for perfect dielectric materials, Capacitance, several capacitance examples, capacitance of a two wire line.

Poisson's and Laplace Equations: Poisson's & Laplace Equations, Uniqueness theorem, Examples of the solutions of Laplace's equation & Poisson's equation.

Text 1: Ch 4. 4.1, 4.2, 4.3, 4.4, 4.5, 4.6, 4.7, 4.8, Ch 5. 5.1, 5.2, 5.3, 5.4, 5.5, 5.6, Ch 7- 7.1, 7.2, 7.3, 7.4

UNIT-3 (11 Hrs)

The Steady Magnetic Field: Biot-Savart Law, Ampere's Circuital Law, Curl, Stokes' Theorem, Magnetic Flux & Magnetic Flux density, The Scalar & Vector magnetic potentials, Derivation of steady magnetic field Laws.

Magnetic Forces: Force on a moving charge, Force on a Differential current element, Force between differential Current elements, Force & Torque on a closed circuit.

Text 1: Ch 8. 8.1 , 8.2, 8.3, 8.4, 8.5, 8.6, Ch 9. 9.1, 9.2, 9.3, 9.4

UNIT-4 (11 Hrs)

Time- varying fields & Maxwell's Equations: Faraday's Law, Displacement current, Maxwell's equations in point form, Maxwell's equations in Integral form, The Retarded potentials.

UNIT-5 (11 Hrs)

The Uniform Plane wave: Wave propagation in Free space, Wave propagation in Dielectrics, The Poynting vector & power considerations, Propagation in good conductors: Skin Effect, Wave polarization.

Plane waves at Boundaries: Reflection of uniform plane waves at normal Incidence, Standing wave ratio, Wave reflection from multiple interfaces, Plane wave propagation in general Directions.

Text-1: Ch 12, 12.1, 12.2, 12.3, 12.4, 12.5, Ch 13, 13.1, 13.2, 13.3, 13.4

TEXT BOOKS

- William H Hayt Jr. and John A Buck,"Engineering Electromagnetics", Tata McGraw-Hill, 6th Edition 2001

REFERENCE BOOKS

- John Kraus, “Electromagnetics with Applications”, Tata Mc-Graw Hill, 5th Edition 1999.
 - Edward C. Jordan, “Electromagnetic waves & Radiating systems”, Prentice –Hall of India / Pearson education, 2nd edition, 1968

TEACHING METHODOLOGY

- Blackboard teaching
 - PowerPoint presentations (if needed)
 - Regular review of students by asking questions based on topics covered in the class

COURSE ASSESSMENT METHOD

CIE:

- Two Surprise Tests, 10 Marks each. Best of two tests will be taken.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.
- Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.

CO-PO-PSO MAPPING

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	*	*	*	*										
CO2	*	*	*	*										
CO3	*	*	*	*										
CO4	*	*	*							*				
CO5	*	*	*		*					*				

SEMESTER: IV

ADVANCED MICROCONTROLLER (ARM CORTEX M3)

Course Code	17EC45	Credits	04
Hours/Week(L-T-P)	4-0-0	CIE Marks	50
Total Hours	39(L)+26(T)	SEE Marks	100
Exam Hours	03	Course Type	Core

COURSE OUTCOMES

COURSE CONTENTS
UNIT-1 (11Hrs)
<p>ARM Cortex M3: ARM Cortex M3 Processor and ARM Family, Cortex-M3 Processor Applications, Architecture of ARM Cortex M3, Operation Modes, The built-in nested Vectored Interrupt Controller, Memory Map, The Bus Interface, The MPU, Low Power and High Energy Efficiency, Debugging Support</p> <p>Text: 1.1, 1.2, 1.5, 2.1, 2.3, 2.4, 2.5, 2.6, 2.7, 2.9.1, 2.10</p> <p>ARM Cortex M3 Architecture: Registers, Special Registers, Vector Tables, Stack Memory Operation, Reset Sequence</p> <p>Text: 3.1, 3.2, 3.5, 3.6, 3.7</p>
UNIT-2 (11 Hrs)
<p>ARM Cortex M3 Instruction Set: Assembly Basics, Instruction List, Instruction Descriptions, Several Useful Instructions in the Cortex M3</p> <p>Text: 4.1, 4.2, 4.3, 4.4, 4.5, 4.6</p> <p>ARM Cortex M3 Memory Systems: Memory System Features Overview, Memory Map, Memory Access Attributes, Memory Access Permissions, Bit-Band Operations, Unaligned Transfers, Exclusive Access, Endian Mode</p> <p>Text: 5.1, 5.2, 5.3, 5.4, 5.5, 5.6</p>
UNIT-3 (11 Hrs)
<p>ARM Cortex M3 Exceptions: Exception Types, Definition of Priorities, Vector Tables, Interrupt Inputs and Pending Behavior, Fault Exceptions, Supervisor Call and Pendable Service Call</p> <p>Text: 7.1, 7.2, 7.3, 7.4, 7.5, 7.6</p> <p>ARM Cortex M3 NVIC: Nested Vectored Interrupt Controller Overview, The Basic Interrupt Configuration, Example Procedures in Setting Up an Interrupt, Software Interrupts, The SYSTICK Timer</p> <p>Text: 8.1, 8.2, 8.3, 8.4, 8.5, 8.6</p>
UNIT-4 (11 Hrs)
<p>ARM Cortex M3 Programming: Overview, A Typical Development Flow, Using C, CMSIS, Using Assembly, Using Exclusive Access for Semaphores, Using Bit Band for Semaphores, Working with Bit Field Extract and Table Branch</p> <p>Text: 10.1, 10.2, 10.3, 10.4, 10.5, 10.6</p> <p>ARM Cortex M3 Advanced Programming: Running a System with Two Separate Stacks, Double-Word Stack Alignment, Nonbase Thread Enable, Performance Considerations, Lockup Situations, FAULTMASK</p>

Text: 12.1, 12.2, 12.3, 12.4, 12.5, 12.6

UNIT-5 (11 Hrs)

ARM Cortex M3 MPU and Other Features: MPU Registers, Setting Up the MPU, The SYSTICK Timer, Power Management, Multiprocessor Communication, Self-Reset Control

Text: 13.2, 13.3, 14.1, 14.2, 14.3, 14.4

ARM Cortex M3 Debug Architecture: Debugging Features Overview, CoreSight Overview, Debug Modes, Debugging Events, Breakpoint in the Cortex-M3, Accessing Register Content in Debug, Other Core Debugging Features

Text: 15.1, 15.2, 15.3, 15.4, 15.5, 15.6, 15.7

TEXT BOOKS

- Joseph Yiu, "The Definitive Guide to the ARM Cortex-M3, Newnes, (Elsevier), 2008

REFERENCE BOOKS

TEACHING METHODOLOGY

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class

COURSE ASSESSMENT METHOD

CIE:

- Two Surprise Tests, 10 Marks each. Best of two tests will be taken.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.

SEE:

- Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.

CO-PO-PSO MAPPING

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	*	*	*								*			
CO2	*		*						*					
CO3	*	*	*	*					*		*			
CO4	*	*	*	*	*						*			
CO5	*	*	*		*				*					

SEMESTER: IV**DIGITAL SYSTEM DESIGN USING VERILOG**

Course Code	17EC46		Credits	03
Hours/Week(L-T-P)	3-0-0		CIE Marks	50
Total Hours	39(L)		SEE Marks	50
Exam Hours	03		Course Type	Core

PRE-REQUISITES

- Digital Electronics

COURSE OUTCOMES

- Students will understand the basic concepts of Verilog HDL.
- Students will acquire the ability to apply HDL in modeling combinational and sequential circuits.
- Students will develop expertise in coding/modeling of digital circuit.
- Students will gain expertise in development of digital system design.
- Students will gain knowledge of Hardware/Software Co-design for digital system design

COURSE CONTENTS**UNIT-1 (8Hrs)**

Design Concepts: Digital Hardware, The design Process, Design of Digital Hardware, Introduction to CAD tools, standard chips, Programmable Logic Devices, Custom Chips and Gate arrays, Introduction to Verilog, What is Verilog HDL, History, Major capabilities.

Text 1:1.1, 1.2, 1.3, 2.9, 3.5, 3.6, 3.7

Text 2:1.1, 1.2.1.3

UNIT-2 (7Hrs)

Language Elements & Modules and ports:, Identifiers, comments, format, compiler directives, value set, data types, parameters modules and ports

Text2: 3.1-3.8

Text3:4.1,4.2

UNIT-3 (8Hrs)

Gate Level Modelling and Data Flow Modelling: Gate types, Gate delays, Continuous assignments, Delays, Expressions, Operators and Operands, Operator types, Examples.

Text3:5.1-5.3, 6.1-6.6

UNIT-4 (11 Hrs)

Behavioural Modelling and UDP: Structured Procedures, Procedural assignments, Timing controls, Conditional statements, Multi-way branching, Loops, Sequential and Parallel Blocks, Examples, UDP Basics, Combinational UDPs, Sequential UDPs, UDP Table shorthand symbols, Guidelines for UDP designs

Text3: 7.1-7.7,7.9, 12.1-12.5

UNIT-5 (11 Hrs)

Tasks and Functions, Useful Modelling Techniques and Examples: Difference between task-functions, Tasks, Functions, Procedural continues assignments, Overriding assignments, overriding parameters, conditional compilation and execution, timescales, Modelling simple elements, delays, Truth-table, conditional operations, synchronous logic,state machines and examples.

Text 3:8.1-8.3,9.1-9.4 , **Text2:**12.1-12.17

TEXT BOOKS

- Stephen Brown, ZvonkoVransic,” Fundamentals of digital logic with verilog Design”, TMH 2nd Edition.
- J. Bhasker,” A verilog HDL Primer” BS Publications,2nd Edition.
- Samir Palnitkar, “Verilog HDL-A Guide to digital design and synthesis”, 2nd Edition, Pearson education. 2003

REFERENCE BOOKS

NazeihM.Botros, “HDL Programming (VHDL & Verilog)”, John Weily - India & Thomson Learning, 2006

TEACHING METHODOLOGY

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class

COURSE ASSESSMENT METHOD

CIE:

- Two Surprise Tests, 10 Marks each. Best of two tests will be taken.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.

SEE:

- Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.

CO-PO-PSO MAPPING

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1		*	*											
CO2		*		*	*									
CO3		*	*		*									
CO4			*		*									
CO5		*	*	*	*		*		*		*			

SEMESTER: IV		<u>DSD using Verilog Lab</u>		
Course Code	17ECL47		Credits	01
Hours/Week(L-T-P)	0-0-2		CIE Marks	50
Total Hours	13(P)		SEE Marks	50
Exam Hours	03		Course Type	Core

PRE-REQUISITES

- Digital Electronics

COURSE OUTCOMES

- Students will be able to design digital circuits using a Verilog language.
- Students will understand the implementation of digital systems by programmable devices, such as FPGA
- Students will be able to use CAD tools to design and analyze digital systems.
- Students will be familiar with the synthesis of digital circuits.

COURSE CONTENTS

LIST OF EXPERIMENTS

1. Realizing the logic gates using HDL.

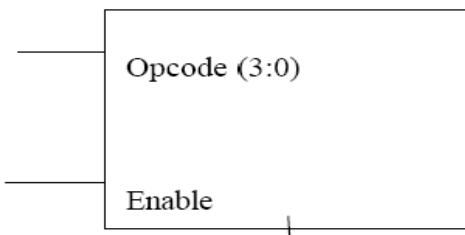
2. Realizing the combinational designs using HDL

- a. 2 to 4 decoder
- b. 8 to 3 (encoder without priority & with priority)
- c. 8 to 1 multiplexer
- d. 4 bit binary to gray converter
- e. Multiplexer, de-multiplexer, comparator.

3. HDL code to describe the functions of a Full Adder Using three Modeling styles.

4. Model for 32 bit ALU using the schematic diagram shown below

A (31:0) B (31:0)



ALU should use combinational logic to calculate an output based on the four bit op-code input.

ALU should pass the result to the out bus when enable line is high, and tri-state the out bus when the enable line is low.

ALU should decode the 4 bit op-code according to the given example below.

OPCODE	ALU OPERATION
1.	$A + B$
2.	$A - B$
3.	A Complement
4.	$A * B$
5.	A AND B
6.	A OR B
7.	A NAND B
8.	A XOR B

- Develop the following flip-flops, (SR, D, JK, T) using HDL
6. Design of 4 bit binary, BCD counters (Synchronous reset and Asynchronous reset) and “any sequence” counters download the programs on a FPGA/CPLD boards such as Apex/Acex/Max/Spartan/Sinfi/TK Base or equivalent and performance testing may be done using 32 channel pattern generator and logic analyzer apart from verification by simulation with tools such as Altera/Modelsim or equivalent.

ADVANCED MICROCONTROLLER LAB

Course Code	17ECL48		Credits	01
Hours/Week(L-T-P)	0-0-2		CIE Marks	50
Total Hours	13(P)		SEE Marks	50
Exam Hours	03		Course Type	Core

PRE-REQUISITES

Programming experience with C and assembly is strongly recommended

COURSE CONTENTS

LIST OF EXPERIMENTS

- **Simulation – with ASM**
 - Introduction / Overview of the IDE – Creation of Project, Editor, Compilation, Debugging / Execution (All with a sample code)
 - ASM Programs – Addition, Multiplication, calling subroutines, multiple source files, writing result(s) to RAM
 - ASM Program – Execution of various special instructions of the processor (such as CMP / TST, LDRD / STRD, UBFX / SBFX, SDIV / UDIV, REV / REVH / REVSH, SXTB / SXTH / UXTB / UXTH, BFC etc.)
 - Simulation – with C Programs
 - Programming the GPIOs
 - Programming the Timer Peripheral
 - Mixed Programming
- **With the Board**
 - Programming blinking of the LED with SW and Timer (use of interrupt)
 - “Hello World” on LCD / UART
 - Programming the PWM / ADC Peripheral
 - Programming the communication UART / SPI / I2C interface
 - Programming the on the board sensor – temperature / accelerometer
 - Programming the special communication interface – CAN

CO-PO-PSO MAPPING

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	*	*		*							*	*		

CO2	*	*		*	*					*	*		
CO3		*		*	*					*	*		
CO4										*	*		
CO5	*	*		*						*	*		

V SEMESTER

DIGITAL SIGNAL PROCESSING				
Course Code	14EC51		Credits	04
Hours/Week(L-T-P)	4-0-0		CIE Marks	50
Total Hours	52		SEE Marks	50
Exam Hours	03		Course Type	Core

COURSE OUTCOMES
<ul style="list-style-type: none"> • Students will be able to analyze signals using the discrete Fourier Transform (DFT). • Students will be able to understand the methods for faster computation of DFT and relating DFT with Convolution • Student will be able to understand IIR and FIR filter design and its implementation • Student will be able to program to perform basic signal, image and video processing tasks using MATLAB/Simulink.

COURSE CONTENTS
UNIT-1 (8Hrs)
Discrete Fourier Transforms (DFT): Frequency domain sampling and reconstruction of discrete time signals. The Discrete Fourier Transform (DFT). DFT as a linear transformation. Properties of DFT. Multiplication of two DFTs- the circular convolution, additional DFT properties, use of DFT in linear filtering, overlap-save and overlap-add method. <i>Text1: Ch 5. 5.1.1, 5.1.2, 5.1.3, 5.2 to 5.3</i>
UNIT-2 (8Hrs)
Fast-Fourier-Transform (FFT) algorithms: Direct computation of DFT, need for efficient

computation of the DFT (FFT algorithms). Radix- 2 FFT algorithms, for the computation of DFT and IDFT. Decimation in time and Decimation in frequency FFT algorithms. Applications of FFT Algorithms. Goertzel algorithm and Chirp Z algorithm *Text1: Ch 6. 6.1.1, 6.1.3, 6.2, 6.3.1, 6.3.2*

UNIT-3 (8Hrs)

FIR filter design: Introduction to FIR filters. Properties of FIR digital filters. Design of Linear FIR filters using - Rectangular, Hanning, Hamming, Blackmann, Bartlett and Kaiser Windows, Linear phase FIR filter design using frequency sampling and Equiripple filter design. Design of FIR Differentiators. Design of Hilbert Transformers. *Text1: Ch 8. 8.2.1 to 8.2.6*

UNIT-4 (8Hrs)

IIR filter design: Characteristics of commonly used IIR filters (Butterworth and Chebyshev). Design of IIR filters from analog filters (Butterworth and Chebyshev) - impulse invariance method. Mapping of transfer functions. Approximation of derivative and bilinear transformation method, Matched Z-Transforms, Verification for stability and linearity during mapping. *Text1:Ch8.8.3.1to8.3.6*

UNIT-5 (7Hrs)

Implementation of discrete-time systems: Basic IIR Filter Structures: Direct Form I and II, Cascade and Parallel Structure. Signal flow graph and Transposed structure. Basic FIR Filter Structure: Direct Form, Cascade structure. Lattice and frequency Sampling Structure *Text1:Ch.7.2,7.3.7.3.1to7.3.4*

TEXT BOOKS

1. Proakis & Monalakis, "Digital signal processing – Principles Algorithms & Applications", Pearson education, 3rd Edition, 2003

REFERENCE BOOKS

1. Oppenheim & Schaffer, "Discrete Time Signal Processing", PHI, 2003
2. S. K. Mitra, "Digital Signal Processing", Tata Mc-Graw Hill, 2nd Edition, 2

TEACHING METHODOLOGY

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class

COURSE ASSESSMENT METHOD

CIE:

- Two Surprise Tests, 10 Marks each. Best of two tests will be taken.
- Assignment/course project based test. 10 Marks each. Best of two tests will be taken.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.

SEE:

- Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.

CO-PO-PSO MAPPING

CO/P O	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO1 0	PO1 1	PO1 2	PSO 1	PS O2	PS O
-----------	---------	---------	---------	---------	---------	---------	---------	---------	---------	----------	----------	----------	----------	----------	---------

CO1	*	*	*	*										*
CO2	*	*		*										*
CO3	*	*	*	*				*						*
CO4	*	*	*	*	*	*			*				*	

ANALOG COMMUNICATION				
Course Code	14EC52		Credits	04
Hours/Week(L-T-P)	4-0-0		CIE Marks	50
Total Hours	52		SEE Marks	50
Exam Hours	03		Course Type	Core
COURSE OUTCOMES				
<ul style="list-style-type: none"> Students will get the fundamental knowledge of analog communication system analysis and design Students will be provided extensive exposure of the concepts related to analog modulation and demodulation techniques. Students will apply concepts and techniques such as Fourier analysis and circuit analysis to the communication systems Students will learn about signal to noise ratio in analog receivers. 				

COURSE CONTENTS
UNIT-1 (8Hrs)
Random process: Random variables: Several random variables. Statistical averages: Function of Random variables, moments, , Mean, Correlation and Covariance function: Principles of autocorrelation function, cross –correlation functions. Central limit theorem, Properties of Gaussian process. <i>Text 1: Ch 4.1-4.6, Ch 8: 8.1,8.2,8.3,8.4,8.5,8.6,8.7,8.8,8.9,8.10,8.11,8.12</i>
UNIT-2 (8Hrs)

Amplitude Modulation: Introduction to AM: Time-Domain description, Frequency – Domain description. Generation of AM wave: square law modulator, switching modulator. Detection of AM waves: square law detector, envelop detector. Double side band suppressed carrier modulation (DSBSC): Time-Domain description, Frequency-Domain representation, Generation of DSBSC waves: balanced modulator, ring modulator. Coherent detection of DSBSC modulated waves. Costas loop. Quadrature carrier multiplexing, Hilbert transform, properties of Hilbert transform, Pre-envelope, Canonical representation of band pass signals. *Text 1: Ch 4: 4.1, 4.2, 4.3, 4.4, 4.5, 4.6 , Text 2: Ch 7: 7.1,7.2*

UNIT-3 (8Hrs)

Single Side-Band Modulation (SSB): Single side-band modulation, Frequency-Domain description of SSB wave, Time-Domain description. Phase discrimination method for generating an SSB modulated wave, Time-Domain description. Phase discrimination method for generating an SSB modulated wave. Demodulation of SSB waves. *Text 2: Ch 7: 7.3, 7.4*

Vestigial Side-Band Modulation (VSB): Frequency – Domain description, Generation of VSB modulated wave, Time - Domain description, Envelop detection of VSB wave plus carrier, Comparison of amplitude modulation techniques, Frequency translation, Frequency division multiplexing. Application: Radio broadcasting, AM radio.

Text 1: Ch 4: 4.1, 4.2, 4.3, 4.4, 4.5, 4.6, text 2: Ch 7: 7.5, 7.6, 7.7, 7.8, 7.9

UNIT-4 (8Hrs)

Angle Modulation (FM): Basic definitions, FM, narrow band FM, wide band FM, transmission bandwidth of FM waves, and generation of FM waves: indirect FM and direct FM.

Demodulation of FM waves: Phase-locked loop, Nonlinear model of the phase – locked loop, Linear model of the phase – locked loop, Nonlinear effects in FM systems.

Text 2: Ch 7: 7.10,7.11,7.12,7.13,7.14.

UNIT-5 (7Hrs)

Noise: Introduction, shot noise, thermal noise, white noise, Noise equivalent bandwidth, Narrow bandwidth, Noise Figure, Equivalent noise temperature, cascade connection of two-port networks.

Noise in Continuous wave modulation systems: Introduction, Receiver model, Noise in DSB-SC receivers, Noise in SSB receivers, Noise in AM receivers, Threshold effect, Noise in FM receivers, FM threshold effect, Pre-emphasis and De-emphasis in FM

Text 2: Ch 9: 9.1, 9.2, Text 1: Ch 5: 5.1, 5.2, 5.3, 5.4, 5.5, 5.6, 5.7

TEXT BOOKS

1. Simon Haykins, Communication Systems, 3rd Edition, John Willey, 1996.
2. Simon Haykins, An Introduction to Analog and Digital Communication, John Wiley, 2003

REFERENCE BOOKS

1. B.P.Lathi, Modern digital and analog Communication systems 3rd ed 2005 Oxford university press.

2. Harold P.E, Stern Samy and A Mahmood, Communication Systems, Pearson Edn, 2004

3. Singh and Sapre: Communication systems: Analog and digital TMH 2nd , Ed 2007

TEACHING METHODOLOGY

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class

COURSE ASSESSMENT METHOD

CIE:

- Two Surprise Tests, 10 Marks each. Best of two tests will be taken.
- Assignment/course project based test. 10 Marks each. Best of two tests will be taken.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.

SEE:

- Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.

CO-PO-PSO MAPPING

CO/P O	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO1 0	PO1 1	PO1 2	PSO 1	PS O 2	PSO 3
CO1	*				*								*	*	
CO2	*	*	*	*										*	
CO3	*	*	*	*										*	*
CO4	*	*		*										*	

MICROWAVE ENGINEERING

Course Code	14EC53	Credits	04
Hours/Week(L-T-P)	4-0-0	CIE Marks	50
Total Hours	52	SEE Marks	50
Exam Hours	03	Course Type	Core

COURSE OUTCOMES

- Students learn about the fundamentals of Transmission lines and waveguides .
- Able to analyze their practical problems and find solutions in establishing a microwave link.
- Students will learn about the construction and working of different types of microwave passive and active devices used in microwave communication.
- Students will be in a position to understand the working of a Radar and will be in a position to calculate maximum range and power levels of Transmitter and receiver.

COURSE CONTENTS
UNIT-1 (8Hrs)
Microwave transmission lines: Introduction, transmission lines equations and solutions, reflection and transmission coefficients, standing waves and SWR, line impedance and line admittance, Microwave coaxial connectors.
Text 1: <i>Ch 3.3.1, 3.2, 3.3, 3.4, 3.5, 3.6, 3.7</i>
UNIT-2 (8Hrs)
Microwave waveguides and Smith Chart: Rectangular waveguides: solutions of wave equations in rectangular co-ordinates,TE modes in rectangular waveguides,TM modes in rectangular waveguides. Smith chart: Introduction to Smith chart,Equations for Generation of Smith chart,.Applications of Smith chart:.Input impedance determination using a known load,Input impedance determination using input Reflection Coefficient,Determination of Admittance from impedance,Determination of value and location of Zmax and Zmin from a known load, Single stub matching.
<i>Text 1: Ch 3: 3.6.1, Ch 4: 4.14.1.1, 4.1.2, 4.1.3, 4.2, 4.3, 4.4, 4.5.</i>
<i>Text 3: Ch 9: 9.1, 9.2,9.3. Ch10: 10.2.1,10.2.2,10.2.3,10.2.4,10.2.5.</i>
UNIT-3 (8Hrs)
Microwave network theory and passive devices: Symmetrical Z and Y parameters for reciprocal Networks, S matrix representation of multi-port networks, Microwave passive devices: coaxial connectors and adapters, Phase shifters, Attenuators, Waveguide Tees, Magic tees.
<i>Text2: 6.1.6.2,6.3,6.4 Text 3:Ch 3. 3.1, 3.2, 3.3, 3.4,Text 1:4.4.1,4.4.2</i>
UNIT-4 (8Hrs)
Strip lines: Introduction, Micro strip lines, Parallel strip lines, Coplanar strip lines, Shielded strip Lines.
Microwave components: Directional couplers: Two hole directional coupler, S matrix of a directional coupler, Circulators and Isolators.
<i>Text1: Ch 11.-11.0,11.1, 11.2, 11.3, 11.4,Ch4: 4.5.1,4.5.2,4.6.1,4.6.2</i>
UNIT-5 (7Hrs)
Microwave solid state devices and circuits: Transfer electron devices: Introduction, GUNN effect diodes – GaAs diode, RWH theory, Modes of operation. Avalanche transit time devices: Introduction, READ diode, IMPATT diode, BARITT diode, Parametric amplifiers.
Text1:Ch 7:7.0,7.1,7.2,7.3 Ch 8:8.0,8.1,8.2,8.4,8.5.
TEXT BOOKS
<ul style="list-style-type: none"> • Liao, "Microwave Devices and circuits", Pearson Education • Annapurna Das, Sisir K Das, "Microwave Engineering", TMH Publication, 2001 • Matthew M.Radmanesh, Radio," Frequency and Microwave Electronics",Pearson Education,2002

REFERENCE BOOKS

--

TEACHING METHODOLOGY

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class

COURSE ASSESSMENT METHOD

CIE:

- Two Surprise Tests, 10 Marks each. Best of two tests will be taken.
- Assignment/course project based test. 10 Marks each. Best of two tests will be taken.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.

SEE:

Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.

CO-PO-PSO MAPPING

CO/P O	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO1 0	PO1 1	PO1 2	PSO 1	PS O 2	PSO 3
CO1	*	*	*			*						*		*	
CO2	*	*	*	*								*	*	*	
CO3														*	
CO4	*	*	*	*								*		*	

FUNDAMENTALS OF VLSI DESIGN

Course Code	14EC54	Credits	04
Hours/Week(L-T-P)	4-0-0	CIE Marks	50
Total Hours	52	SEE Marks	50
Exam Hours	03	Course Type	Core

COURSE OUTCOMES

- Students will learn about fundamentals of VLSI circuits. They would study the theoretical aspects

of CMOS circuit.

- Students will be able to understand the front end and back end in VLSI Design flow.
- They will also be able to sketch stick diagram and layouts of logic gates implemented as CMOS transistors.
- Students will be able to design VLSI circuit.

COURSE CONTENTS

UNIT-1 (8Hrs)

Basic MOS technology: Integrated circuit's era. Enhancement and depletion mode MOS transistors. NMOS fabrication. CMOS Fabrication, p well/ n well/ twin well process, Thermal aspects of processing, BiCMOS technology. Production of E-beam masks. *Text1: Ch 1*

UNIT-2 (8Hrs)

MOS Transistor Theory: Introduction, threshold voltage equation, body effect, MOS Device Design Equations, subthreshold region, channel length modulation, mobility variation, tunnelling, punch through, hot electron effect.

The Complementary CMOS Inverter: DC Characteristics, Static Load MOS Inverters, the Differential Inverter, the Transmission Gate, Tristate Inverter. *Text2: Ch 2*

UNIT-3 (8Hrs)

Circuit design processes: MOS layers. Stick diagrams. Design rules and layout – lambda-based design and other rules. Examples. Layout diagrams, Tutorial exercises. Basic Physical Design of Simple logic gates.

Basic CMOS Technology: Current CMOS enhancement (oxide isolation, LDD, refractory gate, multilayer Interconnect), Circuit elements, resistor, Capacitor, interconnects. *Text1: 3.1, 3.2, 3.3.1, 3.3.2, 3.3.4, 3.4, 3.7. Text2: 3.3.1, 3.3.2*

UNIT-4 (8Hrs)

Basic circuit concepts: Sheet resistance. Area capacitances. Capacitance calculations. The delay unit. Inverter delays. Driving capacitive loads. Propagation delays. Wiring capacitances. Tutorial exercises

Scaling of MOS circuits: Scaling models and factors. *Text1:Ch 4, Ch: 5.1*

UNIT-5 (7Hrs)

CMOS Logic Structures: CMOS Complementary Logic, BICMOS Logic, Pseudo NMOS LOGIC, Dynamic CMOS Logic, Clocked CMOS Logic, Pass Transistor Logic, CMOS Domino Logic, Cascaded Voltage Switch Logic. *Text 2: Ch 5.4.1, 5.4.2, 5.4.3, 5.4.4, 5.4.5, 5.4.6, 5.4.7, 5.4.9*

TEXT BOOKS

- Douglas A. Pucknell & Kamran Eshraghian, "Basic VLSI Design" PHI 3rd Edition (original Edition – 1994), 2005.
- Neil H. E. Weste and K. Eshraghian," Principles of CMOS VLSI Design", A Systems Perspective," Pearson Education (Asia) Pvt. Ltd, 2nd edition, 2000

REFERENCE BOOKS

- M. K. Achuthan and K. N. Bhat, "Fundamentals of Semiconductor Devices", Tata McGraw-Hill Publishing Company Limited, New Delhi, 2007.
- 2. Sung-Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", 3rd Edition, Tata McGraw-Hill Publishing Company Ltd., New Delhi, 2007.

TEACHING METHODOLOGY

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class

COURSE ASSESSMENT METHOD

CIE:

- Two Surprise Tests, 10 Marks each. Best of two tests will be taken.
- Assignment/course project based test. 10 Marks each. Best of two tests will be taken.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.

SEE:

Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.

CO-PO-PSO MAPPING

CO/P O	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO1 0	PO1 1	PO1 2	PSO 1	PS O 2	PSO 3
CO1	*				*					*			*	*	
CO2	*	*	*	*	*								*	*	*
CO3	*	*	*	*	*				*				*	*	
CO4	*	*	*	*	*								*		*

DATA STRUCTURES USING C++

Course Code	14EC55		Credits	04
Hours/Week(L-T-P)	4-0-0		CIE Marks	50
Total Hours	52		SEE Marks	50

Exam Hours	03		Course Type	Core
-------------------	----	--	--------------------	-------------

COURSE OUTCOMES
<ul style="list-style-type: none"> • Students will be able to understand the memory organization and allocation. • Able to understand principle of storage and access of data in computer systems. • Students will be able to understand different individual and collective data types that can be used in computational and programming applications • Students will be able to know the declaration, storage and access of different types of data program applications using C

COURSE CONTENTS
UNIT-1 (8Hrs)
Introduction, Arrays and Structures: Overview, Pointers and Dynamic Memory Allocation, Arrays, Dynamically Allocated arrays, Structures and Unions, Representation of Multidimensional Arrays, Strings, Singly Linked Lists and chains, Representing Chains in C. Chapter 1, 2, 4: 1.1, 1.2, 2.1, 2.2, 2.3, 2.6, 2.7, 4.1, 4.2
UNIT-2 (8Hrs)
Linked List Linked Stacks and Queues, Additional List Operations, Doubly Linked Lists. Chapter 4: 4.3, 4.5, 4.8
UNIT-3 (8Hrs)
Stacks and Queue Using Array, Dynamic Array, Linked List Stacks, Stacks Using Dynamic Arrays, Queues, Circular Queues Using Dynamic Arrays, Evaluation of Expressions. Chapter 3: 3.1, 3.2, 3.3, 3.4, 3.6
UNIT-4 (8Hrs)
Binary Tree & Heaps Introduction, Binary Trees, Binary Tree traversals, Heaps, Binary Search Trees. Chapter 5: 5.1, 5.2, 5.3, 5.6, 5.7
UNIT-5 (7Hrs)
Sorting and Hashing Motivation, Insertion Sort, Quick Sort, How fast can we sort, Merge Sort, Heap Sort, Introduction to hashing, Static hashing, Dynamic hashing. Chapter 7 and 8: 7.1, 7.2, 7.3, 7.4, 7.5, 7.6, 8.1, 8.2, 8.3
TEXT BOOKS
<ul style="list-style-type: none"> • Horowitz, Sahni and Anderson Freed, Fundamentals of Data Structures in C, Universities Press, Second Edition.

REFERENCE BOOKS

- Padma Reddy, Data Structures using C

TEACHING METHODOLOGY

- Blackboard teaching
 - PowerPoint presentations (if needed)
 - Regular review of students by asking questions based on topics covered in the class

COURSE ASSESSMENT METHOD

CIE:

- Two Surprise Tests, 10 Marks each. Best of two tests will be taken.
 - Assignment/course project based test. 10 Marks each. Best of two tests will be taken.
 - Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.

SEE:

Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.

CO-PO-PSO MAPPING

PROGRAM ELECTIVE-1

MICROELECTROMECHANICAL SYSTEMS				
Course Code	14EC551		Credits	03
Hours/Week(L-T-P)	3-0-0		CIE Marks	50
Total Hours	39(L)		SEE Marks	50
Exam Hours	03		Course Type	Program Elective

COURSE OUTCOMES
<ul style="list-style-type: none"> Students will get a basic knowledge of MEMS Applications and Fabrication Process They get hands on experience on MEMS CAD tool. Students will be able to learn the different mathematical modelling. Students learn the analysis of MEMS Devices.

COURSE CONTENTS
UNIT-1 (8Hrs)
Introduction: Why Miniaturization?, Microsystems versus MEMS, Why microfabrication? Smart Materials, Structures and systems, Integrated Microsystems, Applications of smart Materials and Micro Systems
Materials for MEMS: Silicon compatible material System-Silicon, Silicon oxide and Nitride, Thin metal Films, Polymers, Other material and substrates, Important materials properties and Physical effects,
<i>Text book 1: Ch.1: 1.1, 1.2, 1.3, 1.4, 1.5, 1.6 Text book 2: Chapter 2</i>
UNIT-2 (8Hrs)
Micromachining Technologies: Thin Film Deposition, lithography, Etching, Silicon Micromachining, Advanced Process for Microfabrication. <i>Text Book1: Ch 3: 3.1, 3.2, 3.3, 3.4, 3.5, 3.7</i>
UNIT-3 (8Hrs)
Circuits for conditioning sensed signals: Differential charge measurement, switched capacitor circuits for capacitance measurement, circuits for measuring frequency shift,
Implementation of controllers: Design methodology, circuit implementation, digital controllers.
Scaling Effects in Microsystems: Scaling in the mechanical Domain, Scaling in the electrostatic Domain, Scaling in Magnetic Domain, Scaling in the thermal Domain, Scaling in Diffusion, Scaling in Fluids, scaling Effects in the Optical Domain, Scaling in Biochemical Phenomena. <i>Text book1: Ch. 7: 7.4,7.6</i>

Ch. 9: 9.1, 9.2, 9.3, 9.4, 9.5, 9.6, 9.7, 9.8

UNIT-4 (8Hrs)

Integration of Micro and Smart Systems: Integration of Microsystems and Microelectronics, Microsystems Packaging, Case studies of Integrated Microsystems *Text Book 1: Ch 8: 8.1, 8.2, 8.3,*

UNIT-5 (7Hrs)

MEMS Structures and Systems in Industrial and Automotive Applications: General Design methodology, Techniques for sensing and actuation, Passive micromachined Mechanical structures, Sensors and Analysis systems, Actuators and Actuated Microsystems

MEMS Applications in Life Sciences: Microfluidics for Biological applications, DNA Analysis, PCR, Microelectrode arrays, *Text book 2: Chapter 4, Chapter 6*

Simulations of the applications using MEMS tools

TEXT BOOKS

- G.K. Ananthasuresh, K.J. Vinoy, S. Gopalakrishnan, K.N. Bhat, V.K. Aatre, “ Micro and Smart Systems”, Wiley India, 2010
- Nadim Maluf, Kirt Williams “An Introduction to Microelectromechanical Systems Engineering” Second addition

REFERENCE BOOKS

TEACHING METHODOLOGY

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class

COURSE ASSESSMENT METHOD

CIE:

- Two Surprise Tests, 10 Marks each. Best of two tests will be taken.
- Assignment/course project based test. 10 Marks each. Best of two tests will be taken.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.

SEE:

Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.

CO-PO-PSO MAPPING

CO/P O	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO1 0	PO1 1	PO1 2	PSO 1	PS O 2	PSO 3
CO1	*	*	*		*				*	*		*	*	*	
CO2	*	*	*		*				*			*	*		*
CO3		*	*	*					*			*			

CO4		*	*	*					*			*	*	*		*
-----	--	---	---	---	--	--	--	--	---	--	--	---	---	---	--	---

FPGA ARCHITECTURE and APPLICATIONS				
Course Code	14EC555		Credits	03
Hours/Week(L-T-P)	3-0-0		CIE Marks	50
Total Hours	39(L)		SEE Marks	50
Exam Hours	03		Course Type	Program Elective

COURSE OUTCOMES				

COURSE CONTENTS				
UNIT-1 (8Hrs)				
Motivation for advanced microcontrollers – Low Power embedded systems, On-chip peripherals, and low- power RF capabilities. Examples of Applications				
UNIT-2 (8Hrs)				
MSP430 -16-bit Microcontroller family. CPU Architecture. Instruction set, Interrupt mechanism, Clock system, Memory subsystem, bus –architecture The assembly language and 'C' programming for MSP-430 microcontrollers. On-chip peripherals. WDT, Comparator, Op-Amp, Timer, Basic Timer, Real Time Clock (RTC),ADC, DAC, Digital I/O. Using the low-powerfeaturesofMSP430.Clock system, low-power modes, Clock request feature, low-power Programming and interrupts.				
UNIT-3 (8Hrs)				
ARM -32 bit Microcontroller family. Architecture of ARM Cortex M3 -General Purpose Registers, Stack Pointer, Link Register, Program Counter, Special Register, Nested Vector Interrupt Controller. Interrupt behavior of ARM Cortex M3.Exceptions Programming. Advanced Programming features Memory Protection. Debug Architecture.				
UNIT-4 (8Hrs)				
UNIT-5 (7Hrs)				

TEXT BOOKS
REFERENCE BOOKS

- Joseph You, The Definitive Guide to the ARM Cortex-M3, Newness,(Elsevier), 2008.
- John Davies, "MSP430 Microcontroller Basics", Newness' (Elsevier Science), 2008.
- MSP430 Teaching CD-ROM, Texas Instruments, 2008.
- Sample Programs for MSP430 downloadable from msp430.com
- David Patterson and John L. Hennessey, "Computer Organization and Design", (ARM Edition), Morgan Kauffman.

TEACHING METHODOLOGY
<ul style="list-style-type: none"> • Blackboard teaching • PowerPoint presentations (if needed) • Regular review of students by asking questions based on topics covered in the class

COURSE ASSESSMENT METHOD
CIE: <ul style="list-style-type: none"> • Two Surprise Tests, 10 Marks each. Best of two tests will be taken. • Assignment/course project based test. 10 Marks each. Best of two tests will be taken. • Three internals, 30 Marks each will be conducted and the Average of best of two will be taken. SEE: <p>Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.</p>

CO-PO-PSO MAPPING																																																																																
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>CO/P O</th> <th>PO 1</th> <th>PO 2</th> <th>PO 3</th> <th>PO 4</th> <th>PO 5</th> <th>PO 6</th> <th>PO 7</th> <th>PO 8</th> <th>PO 9</th> <th>PO1 0</th> <th>PO1 1</th> <th>PO1 2</th> <th>PSO 1</th> <th>PS O 2</th> <th>PSO 3</th> </tr> </thead> <tbody> <tr> <td>CO1</td> <td>*</td> <td>*</td> <td>*</td> <td></td> <td>*</td> <td></td> <td></td> <td></td> <td>*</td> <td>*</td> <td></td> <td>*</td> <td>*</td> <td>*</td> <td></td> </tr> <tr> <td>CO2</td> <td>*</td> <td>*</td> <td>*</td> <td></td> <td>*</td> <td></td> <td></td> <td></td> <td>*</td> <td></td> <td></td> <td>*</td> <td>*</td> <td></td> <td>*</td> </tr> <tr> <td>CO3</td> <td></td> <td>*</td> <td>*</td> <td>*</td> <td></td> <td></td> <td></td> <td></td> <td>*</td> <td></td> <td></td> <td>*</td> <td></td> <td></td> <td></td> </tr> <tr> <td>CO4</td> <td></td> <td>*</td> <td>*</td> <td>*</td> <td></td> <td></td> <td></td> <td></td> <td>*</td> <td></td> <td></td> <td>*</td> <td>*</td> <td></td> <td>*</td> </tr> </tbody> </table>	CO/P O	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO1 0	PO1 1	PO1 2	PSO 1	PS O 2	PSO 3	CO1	*	*	*		*				*	*		*	*	*		CO2	*	*	*		*				*			*	*		*	CO3		*	*	*					*			*				CO4		*	*	*					*			*	*		*
CO/P O	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO1 0	PO1 1	PO1 2	PSO 1	PS O 2	PSO 3																																																																	
CO1	*	*	*		*				*	*		*	*	*																																																																		
CO2	*	*	*		*				*			*	*		*																																																																	
CO3		*	*	*					*			*																																																																				
CO4		*	*	*					*			*	*		*																																																																	

FPGA ARCHITECTURE and APPLICATIONS				
Course Code	14EC559		Credits	03
Hours/Week(L-T-P)	3-0-0		CIE Marks	50
Total Hours	39(L)		SEE Marks	50
Exam Hours	03		Course Type	Program Elective

COURSE OUTCOMES
<ul style="list-style-type: none"> Students will get a basic knowledge of FPGA design flow They get hands on experience on FPGA EDA tool. Students will be able to learn the design and implementation of digital logic circuits for various applications. Students will be able to design arithmetic circuits

COURSE CONTENTS
UNIT-1 (8Hrs)
Introduction to Programmable logic Device FPGA, FPGA Features, Architectures, Logic blocks, routing architecture, design flow, technology mapping for FPGAs, Programming, Implementation of logic circuits using FPGA.
Xilinx XC4000 & ALTERA's FLEX 8000/10000, AT &T ORCA's (Optimized Reconfigurable Cell Array), ACTEL's ACT-1,2,3 FPGA Architectural features and their speed performance
UNIT-2 (8Hrs)
Finite State Machines (FSM): Top Down Design, State Transition Table, State assignments for FPGAs, Realization of state machine charts using PAL, Alternative realization for state machine charts using microprogramming, linked state machine, encoded state machine.
UNIT-3 (8Hrs)
Architectures Centered around non registered PLDs, Design of state machines centered around shift registers, One-Hot state machine, Petrinets for state machines-Basic concepts and properties, Finite State Machine-Case study.
Design Methods and System Level Design: One –hot design method, Use of ASMs in one-hot

design method, Applications of one hot design method, Extended Petri-nets for parallel controllers, Meta Stability, Synchronization, Complex design using shift registers , data path designing.

UNIT-4 (8Hrs)

Digital front end digital design tools for FPGAs, System level design using EDA tool (FPGA Advantage), Design flow using FPGAs.

Case studies: Design considerations using FPGAs of parallel adder cell, parallel adder sequential circuits, counters, multiplexers, parallel controllers.

UNIT-5 (7Hrs)

On-chip Dual Address ROM Design, Single Address ROM Design.

Arithmetic Circuit Design: Digital Pipelining, Partitioning of a Design, Partition of Data Width, Partition of Functionality, Signed Adder Design, Signed Serial Adder, Parallel Signed Adder Design, Multiplier Design, Verilog Code for Multiplier Design

TEXT BOOKS

- Field Programmable Gate Array Technology - S. Trimberger, Edr, 1994, Kluwer Academic Publications.
- Advanced FPGA Design: Architecture, Implementation, and Optimization **By Steve Kilts**
- Digital VLSI Systems Design, S. Ramachandran, Springer, 2007

REFERENCE BOOKS

- Digital Design Using Field Programmable Gate Array, P.K.Chan & S. Mourad, 1994,Prentice Hall.
- Field programmable gate array, S. Brown, R.J.Francis, J.Rose ,Z.G.Vranesic, 2007, BSP.

TEACHING METHODOLOGY

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class

COURSE ASSESSMENT METHOD

CIE:

- Two Surprise Tests, 10 Marks each. Best of two tests will be taken.
- Assignment/course project based test. 10 Marks each. Best of two tests will be taken.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.

SEE:

Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.

CO-PO-PSO MAPPING

CO/P O	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO1 0	PO1 1	PO1 2	PSO 1	PS O 2	PSO 3
-----------	---------	---------	---------	---------	---------	---------	---------	---------	---------	----------	----------	----------	----------	-----------	----------

CO1	*	*	*		*			*	*		*	*	*	*	
CO2	*	*	*		*			*			*	*	*		*
CO3		*	*	*				*			*				
CO4		*	*	*				*			*	*			*

DIGITAL SIGNAL PROCESSING LAB				
Course Code	14ECL57		Credits	1.5
Hours/Week(L-T-P)	0-0-3		CIE Marks	50
Total Hours	3H/W		SEE Marks	50
Exam Hours	03		Course Type	Regular Lab

COURSE OUTCOMES	
• Students will acquire the knowledge of Matlab/Scilab implementation of DSP algorithm	• Students will acquire the Knowledge of code composer studio usage for DSP application.

COURSE CONTENTS	
LIST OF EXPERIMENTS	
PART- A: <u>LIST OF EXPERIMENTS USING MATLAB</u>	
(4 Lab Sessions of 3Hrs Each)	
<ul style="list-style-type: none"> • Solving a given difference equation and Impulse response of a given system • Computation of N point DFT of a given sequence and to plot magnitude and phase spectrum. • Linear convolution and Circular convolution of two sequences using DFT and IDFT. • Design and implementation of FIR and IIR filter to meet given specifications. • To obtain FFT and IFFT for a given sequence where number of points are 2^n. • Experiments based on Simulink and DSP Block set 	
PART- B: <u>LIST OF EXPERIMENTS USING DSP PROCESSOR</u>	
(8 Lab Sessions of 3Hrs Each)	

(Using TMS320C6713 Processor with DSK and Code Composer Studio - Assembly level coding and C coding).

- Implementation of simple mathematical operations.
- Linear convolution and Circular convolution of two given sequences.
- Computation of N- Point DFT of a given sequence
- (a). Impulse response of first order and second order system
- (b). Solution of differential and difference equations with zero initial conditions for a causal system.
- 5. (a). Realization of an FIR filter (any type) to meet given specifications .The input can be a signal from function generator / speech signal.
- (b) Design of IIR filters of order less than or equal to three.
- 6. Audio applications such as to plot a time and frequency display of Microphone plus a cosine using DSP. Read a wav file and match with their respective spectrograms
- Noise removal: Add noise above 3kHz and then remove ; Interference suppression using 400 Hz tone.

ANALOG COMMUNICATION AND LIC LAB

Course Code	14ECL58	Credits	1.5
Hours/Week(L-T-P)	0-0-3	CIE Marks	50
Total Hours	3H/W	SEE Marks	50
Exam Hours	03	Course Type	Regular Lab

COURSE OUTCOMES

- Upon successful completion of this course, the students will be able to design Opamp related Experiments
- After the modulation task students will be able to plan and implement basic measurement arrangements of modulation system

COURSE CONTENTS

LIST OF EXPERIMENTS

1. Second order active LPF and HPF
2. Second order active BPF and BE
3. Schmitt Trigger Design and test a Schmitt trigger circuit for the given values of UTP and LTP
4. Frequency synthesis using PLL.
5. Design and test R-2R DAC using op-amp

- 6. Design and test the following circuits using IC 555
 - a. Astable multivibrator for given frequency and duty cycle
 - b. Monostable multivibrator for given pulse width W
- 7. Class C Single tuned amplifier
- 8. Amplitude modulation using transistor/FET (Generation and detection)
- 9. Pulse amplitude modulation and detection
- 10. Pulse Width Modulation and Pulse Position Modulation
- 11. Frequency modulation using IC 8038/2206
- 12. Precision rectifiers – both Full Wave and Half Wave.

VI SEMESTER

INFORMATION THEORY AND CODING

Semester: VI

Department: ELECTRONICS AND COMMUNICATION	<i>Regular Course</i>
Course Title ITC	Course Code: 14EC61
L-T-P: 4-0-0	Credits: 04
Total Contact Hours: 45hrs	Duration of SEE: 3 hrs
SEE Marks: 50	CIE Marks: 50

COURSE OUTCOME:-

- Upon completion of this course, students will understand to define and apply the basic concepts of information theory, entropy, mutual information etc
- Students will be able to calculate the capacity of communication channels, sketch Shannon's proof regarding the limits of error free communication
- Students will get to know channel capacity and coding for noisy channels, capacity for different channel models (with emphasis on discrete memory less channels and Gaussian channels).
- Students will be able to design and learn the analysis of error correcting codes with a focus on linear block codes and convolution codes.

PO/PSO	1	2	3	4	5	6	7	8	9	10	11	12	PSO1	PSO2	PSO3
CO1	*	*	*	*							*			*	
CO2	*	*	*	*	*						*			*	*

CO3	*	*	*	*					*	*		*	
CO4	*	*	*						*			*	*

COURSE OUTCOME TO PROGRAM OUTCOME MAPPING:-

Teaching Methodology:

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class

Assessment Methods

- Two Surprise Tests, 10 Marks each. Best of two tests will be taken.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.
- Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.

UNIT I

Information Theory: Introduction, Measure of information, Average information content of symbols in long independent sequences, Average information content of symbols in long dependent sequences. Mark-off statistical model for information source, Entropy and information rate of mark-off source.

Source Coding: Encoding of the source output, Shannon's encoding algorithm. Communication Channels, Discrete communication channels, Continuous channels. *Text 1: Ch 4. 4.1, 4.2, 4.3, 4.4, 4.5, 4.6.* **9Hrs**

UNIT-II

Fundamental Limits on Performance: Source coding theorem, Huffman coding, discrete memory less Channels, Mutual information, Channel Capacity, Channel coding theorem. *Text 2: Ch 2. 2.1, 2.2, 2.3, 2.4, 2.5, 2.6, 2.7, 2.8.* **9Hrs**

UNIT-III

Differential entropy and mutual information for continuous ensembles: Channel capacity Theorem. Introduction to Error Control Coding: Introduction, Types of errors, examples, Types of codes Linear Block Codes: Matrix description, Error detection and correction, Standard arrays and table look up for decoding

*Text 1: Ch 9. 9.1, 9.2**Text 2: Ch 2. 2.8, 2.10* **9Hrs**

UNIT-IV

Binary Cycle Codes, Algebraic structures of cyclic codes, Encoding using an (n-k) bit shift register, Syndrome calculation. BCH codes. RS codes, Golay codes, shortened cyclic codes, Burst error correcting codes.

Text 1: Ch 9. 9.3, 9.4, 9.5. **9Hrs**

UNIT-V

Burst and Random Error correcting codes. Convolution Codes, Time domain approach. Transform domain approach.

Text 1: Ch 9. 9.5, 9.6, 9.7 9.8. **9Hrs**

TEXT BOOKS:

1. K. Sam Shanmugam, “Digital and analog communication systems”, John Wiley, 1996.
2. Simon Haykin, “Digital communication”, John Wiley, 2003.

REFERENCE BOOKS:

1. Ranjan Bose, “ITC and Cryptography”, TMH, II Edition, 2007

DIGITAL COMMUNICATION

Semester: VI

Department: ELECTRONICS AND COMMUNICATION	<i>Regular Course</i>
Course Title Digital communication	Course Code: 14EC62
L-T-P: 4-0-0	Credits: 04
Total Contact Hours: 45hrs	Duration of SEE: 3 hrs
SEE Marks: 50	CIE Marks: 50

PRE-REQUISITES:

Understanding of mathematical tools like Fourier series, Fourier transforms.

Understanding of probability theory, random variables, and linear tie invariant systems.

COURSE OUTCOMES:

1. Students will be able to understand the need for sampling, quantization and encoding
2. Students will be able to use source coding techniques to convert analog signal to digital signal
- 3. Students will be able to use digital modulation techniques for long distance communication.
- 4. Students will be able to understand the basics of spread spectrum modulation

COURSE OUTCOME TO PROGRAM OUTCOME MAPPING:-

PO/PSO	1	2	3	4	5	6	7	8	9	10	11	12	PSO1	PSO2	PSO3
CO1	*	*	*	*			*			*	*			*	*
CO2	*	*	*		*						*			*	*
CO3	*	*									*			*	
CO4	*	*									*	*		*	*

Teaching Methodology:

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class

Assessment Methods

- Two Surprise Tests, 10 Marks each. Best of two tests will be taken.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.

Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.

UNIT-I

Basic signal processing operations in digital communication: Sampling Principles, Sampling Theorem, Quadrature sampling of Band pass signal, Practical aspects of sampling and signal recovery. PAM, TDM.

Text1: Ch 1. 1.2, Ch 4. 4.1, 4.2, 4.5, 4.6, 4.7

9 Hrs

UNIT-II

Waveform Coding Techniques: PCM, Quantization noise and SNR, robust quantization.DPCM, DM, applications. Base-Band Shaping for Data Transmission, Discrete PAM signals, power spectra of discrete PAM signals.

Text 1: Ch 5.5.1, 5.2, 5.3, 5.4, 5.5, 5.6, 5.7, 5.8, Ch 6. 6.1, 6.2

9 Hrs

UNIT-III

Base-Band Shaping for Data Transmission ISI, Nyquist's criterion for distortion less base-band binary transmission, correlative coding, eye pattern, base-band M-ary PAM systems,

adaptive equalization for data transmission. Digital Modulation Techniques: Digital Modulation formats, Coherent binary modulation techniques.

Text 1: Ch 6. 6.3, 6.4, 6.5, 6.6, 6.7, 6.8, Ch 7. 7.1, 7.2, 7.3

9hrs

UNIT-IV

Coherent Quadrature modulation Techniques. Noncoherent binary modulation techniques, Detection and estimation, Model of DCS, Gram-Schmidt Orthogonalization procedure, geometric interpretation of signals, response of bank of correlators to noisy input. *Text 1: Ch 7. 7.3, 7.4, Ch. 3. 3.1, 3.2, 3.3, 3.4*

9hrs

UNIT-V

Detection & Estimation: Detection of known signals in noise, correlation receiver, matched filter receiver, detection of signals with unknown phase in noise, Spread Spectrum Modulation: Pseudo noise sequences, notion of spread spectrum, direct sequence spread spectrum, coherent binary PSK , frequency hop spread spectrum, applications.

Text 1: Ch 3. 3.5, 3.7, 3.8, 3.9, Ch 9. 9.1, 9.2, 9.3, 9.6

9 Hrs

TEXT BOOKS:

1.Simon Haykin, “Digital communications”, JohnWiley, 2003.

REFERENCE BOOKS:

1. K.Sam Shanmugam, “Digital and analog communication systems”, John Wiley, 1996.
2. Simon Hay kin,” An introduction to Analog and Digital Communication”, John Wiley, 2003
3. Bernard Sklar, “Digital communications” Pearson education, 2007

ANTENNA AND WAVE PROPAGATION

Semester: VI

Department: ELECTRONICS AND COMMUNICATION	<i>Regular Course</i>
Course Title Antenna and wave propoagation	Course Code: 14EC63
L-T-P: 4-0-0	Credits: 04
Total Contact Hours: 45hrs	Duration of SEE: 3 hrs

SEE Marks: 50

CIE Marks: 50

PRE-REQUISITES:-

A Fundamental course on Fields & waves and the Maxwell's equations for time varying fields are necessary to understand this subject.

COURSE OUTCOMES:

1. Students learn about the fundamentals of Antenna's and in particular study about the different radiation patterns
2. Students will be able to plot the radiation pattern from the field equations.
3. Students learn to find out the different parameters such as Gain and Directivity.
4. Students will study about the different types of Antennas and propagation mechanisms available, their relative merits and de merits.

COURSE OUTCOME TO PROGRAM OUTCOME MAPPING:-

PO/PSO	1	2	3	4	5	6	7	8	9	10	11	12	PSO1	PSO2	PSO3
CO1	*	*	*	*			*			*				*	
CO2	*	*	*		*									*	*
CO3	*	*												*	
CO4	*	*												*	*

Teaching Methodology:

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class

Assessment Methods

- Two Surprise Tests, 10 Marks each. Best of two tests will be taken.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.
- Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.

UNIT 1

Antenna Basics : Introduction, basic antenna –parameters, patterns, beam area, radiation intensity, beam efficiency, directivity, directivity and gain, antenna aperture, effective aperture, scattering aperture, loss aperture, collecting aperture, effective height, maximum effective aperture of a short dipole, maximum effective aperture of a linear $\lambda/2$ antenna, effective aperture and directivity and Friis transmission formula.

Text 1: Ch 2.2.1 to 2.7, 2.8, 2.9, 2.10, 2.12 to 2.16, 2.19, 2.20, 2.21, 2.22, 2.25 *Text 3: Ch 2.11, 2.14, 2.18.* **9Hrs**

UNIT II

Point Sources and Arrays: Introduction to point source, power patterns, power theorem, radiation intensity, field patterns, phase patterns. Array of two isotropic point sources, two isotropic point sources of same amplitude phase, Two isotropic point sources of same amplitude but opposite phases, two isotropic point sources of same amplitude quadrature phase, non isotropic but similar point sources and the principle of pattern multiplication, examples of pattern synthesis by pattern multiplication, non isotropic & non isotropic point sources. Linear broadside arrays with non uniform amplitude distribution. General considerations. Linear arrays with non uniform amplitude distributions. The Dolph-Tchebychef optimum distribution

Text 1: Ch 3. 3.1 to 3.4, 3.16, 3.17, 4.2a, 4.2b, 4.2c, 4.3, 4.4, 4.5, 4.10, 4.11 **9 Hrs**

UNIT III

Electric dipoles and thin linear antennas: Introduction, short electric dipole, field of a short dipole, radiation resistance of short dipole radiation resistances of lambda/2 Antenna, thin linear antenna, Array of two driven lambda/2 elements end fire case. Micro strip arrays, long wire antenna, folded dipole antenna, patch antennas, rectangular horn antennas. *Text 1: Ch 5. 5.1 to 5.6, and Ch 11. 11.3, Ch 16. 16.12, Ch 13. 13.8* **9 hrs**

UNIT IV

Antenna Types: Helical Antenna, Yagi – Uda array, corner reflectors, parabolic reflectors, log periodic antenna, lens antenna, antenna for special applications-sleeve antenna, turnstile antenna, omni directional antennas, antennas for satellite antennas for ground penetrating radars, embedded antennas, ultra wide band antennas, plasma antenna.

Text 1: Ch 7, Ch 8 , Ch 9,Ch 14 and Ch 17 **9Hrs**

UNIT V

Radio Wave Propagation: Introduction, Ground wave propagation, free space propagation, ground reflection, surface wave, diffraction.

Troposphere Wave Propagation: troposcopich scatter, ionosphere propagation, electrical properties of the ionosphere, effects of earth's magnetic field.

Text 2: Ch 8.1, 8.2 **9Hrs**

TEXT BOOK:

- John D.Krauss, “Antennas”, McGraw- Hill International edition, II edition, 1988.
- Harish and Sachidananda, “Antennas and Wave Propagation”, Oxford Press, 2007
- C.A Balanis, “Antenna Theory Analysis and Design”, John Wiley, 2nd Edition, 2007

REFERENCE BOOKS:

- Sineon R Saunders, “Antennas and Propagation for wireless Communication systems”, John Wiley, 2003

OPERATION RESEARCH

Semester: VI

Department: Electronics and Communication Engineering	<i>Regular Course</i>
Course Title: Operation Research	Course Code: 14ECH64
L-T-P: 4-0-0	Credits: 04
Total Contact Hours: 45 hrs	Duration of SEE: 3 hrs
SEE Marks: 50	CIE Marks: 50

PRE-REQUISITES:

- Students should have knowledge of Matrix multiplication and must be able to solve the problems.
- Students should know basics of mathematical concepts.

COURSE OUTCOMES:

- Students will be well grounded in the mathematical, engineering, and modeling skills that are the basis for operations research.
- On completing this course, students will learn optimization tools, probability, statistics, simulation, and engineering economic analysis.
- Competent with mathematical and computational modeling of real decision-making problems, including the use of modeling tools and computational tools,
- Competent analytic skills to evaluate the problems.

PO/PSO	1	2	3	4	5	6	7	8	9	10	11	12	PSO1	PSO2	PSO3
CO1	*	*	*	*					*		*	*			
CO2	*	*	*		*	*			*		*	*			
CO3	*	*	*				*		*		*	*			
CO4	*	*	*				*		*						

COURSE OUTCOM TO PROGRAM OUTCOME MAPPING:-

Teaching Methodology:

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class.

Assessment Methods

- Three Surprise Tests, 10 Marks each. Average of best of two tests will be taken.
- Three Assignment Tests, 10 Marks each. best of three tests will be taken.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.
- Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.

UNIT I

Introduction: Linear programming, Definition, scope of operations research (O.R) approach and limitations of OR models, characteristics and phases of OR mathematical formulation of L.P. Problems. Graphical solution methods. **Linear Programming Problems:** Introduction, Definitions, simplex method - computational procedure. **9 Hrs**

UNIT II

Artificial Variable Technique: Two phase method. Big-M-method (Charne's penalty method). Degeneracy-Methods to resolve degeneracy. Special cases- Alternative, unbounded & non-existing solution, Concept of duality, primal & dual correspondence, Dual simplex method. **9 Hrs**

UNIT III

Game Theory: Formulations of games, two person-zero sum game, games with and without saddle point, graphical solution ($2 \times n$, $m \times 2$ game), dominance property.

Transportation Problem: Mathematical Formulation; Matrix form, Definitions, Initial basic feasible solution using different methods. Optimality methods. Minimization problem, unbalanced transportation problem, degeneracy in transportation problems. **9 Hrs**

UNIT IV

Assignment Problem: Mathematical Formulation, Hungarian method, Minimal, Maximal & unbalanced assignment problem, traveling salesman (Routing) problem.

Sequencing: Terminology & notations, Johnson's algorithm, processing of: n-jobs to 2 machines, n jobs 3 machines, n jobs m machines without passing sequence. 2 jobs n machines with passing. Graphical solution. **9 Hrs**

UNIT V

PERT-CPM Techniques: Definitions, difference between CPM & PERT. Applications. Network construction, labeling using Fulkerson's '1-J' Rule. Time Estimates and Critical path - Forward & Backward pass computation. Determination of Floats, Slack times & critical path. PERT-critical path, scheduling by project duration, variance under probabilistic models, prediction of date of completion, crashing of simple networks- Optimum duration & Minimum duration cost. **Queuing Theory:** Queuing system and their characteristics. The M/M/1 queuing system, steady state performance and analysis of M/M/1 & MIMIC queuing model. **9hrs**

TEXT BOOKS:-

1. Operation Research, S. D. Sharma - Kedarnath Ramnath and Co, 2002.
2. Problems in Operations Research - P.K.Gupta, Manmohan, Sultan Chand Publications, 2005

REFERENCE BOOKS:-

1. Operations Research - An Introduction, Taha H.A. -Low price Edition, ih Edn, 2006
2. Introduction to Operation Research, Hiller and Liberman, Mc Graw Hill. 5th edition 2001.
3. Operations Research: principles and practice: Ravindran, philiphs and Solberg, Wiley India its 2nd edition 2007.
4. Operation Research, Prem kumar Gupta, 0 SHira, S chand pub,New delhi, 2007.

5. Operation Research, Prem kumar Gupta, 0 SHira, S chand pub, New delhi, 2007.

CORE ELECTIVE-2

ANALOG AND MIXED MODE VLSI DESIGN

Semester: VI

Department: ELECTRONICS AND COMMUNICATION	<i>Core elective</i>
Course Title Analog and mixed mode VLSI	Course Code: 14ECE652
L-T-P: 4-0-0	Credits: 04
Total Contact Hours: 45hrs	Duration of SEE: 3 hrs
SEE Marks: 50	CIE Marks: 50

PREREQUISITES

- Satisfactory completion of understanding of basics of semiconductor theory in physics.
- Satisfactory knowledge of Analog Electronic Circuits.
- Satisfactory knowledge of Digital Electronics

COURSE OUTCOME

- Student will learn about the design of CMOS-VLSI Circuits using hand calculations
- They would study the applications of CMOS circuits, their front end and back end designs
- Students will be able to model the CMOS circuits
- Students will be able simulate them for IC solutions.

COURSE OUTCOME TO PROGRAM OUTCOME MAPPING:-

PO/PSO	1	2	3	4	5	6	7	8	9	10	11	12	PSO1	PSO2	PSO3
CO1	*	*	*	*					*		*		*		
CO2	*	*	*	*	*				*		*		*		*
CO3	*	*	*		*					*	*		*		
CO4	*	*			*					*	*		*		*

Teaching Methodology:

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class

Assessment Methods

- Two Surprise Tests, 10 Marks each. Best of two tests will be taken.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.
- Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.

UNIT I

Introduction to CMOS analog circuits: Second order effects, MOS Device models.

Single Stage Amplifier: Common source stage with resistive load, diode load, triode load, current source load, Source Degeneration, Source follower, Common gate Stage, Cascode amplifier, Folded Cascode,

Text 1: Ch 2: 2.3, 2.4, Ch 3. 3.1, 3.2, 3.3, 3.4, 3.5 **9 Hrs**

UNIT II

Differential amplifier, Single ended and differential operation, Basic Differential pair, Common mode response, Differential pairs with MOS load, Gilbert cell.

Passive current mirrors: Basic current mirrors, cascade current mirrors.

Text 1: Ch 4, Ch 5 **9 Hrs**

UNIT III

Active Current mirrors

Frequency Response of Amplifiers: Miller Effect, Association of poles and nodes, Source Follower, Differential pair.

Text 1: Ch 5; Ch 6. 6.1, 6.3 and 6.6, Ch 9 **9hrs**

UNIT IV

Operational Amplifier: Performance parameters, One stage and two stage op amp, gain boosting, common mode feedback, input range limitations, slew rate, power supply rejection, multi pole systems, phase margin, frequency compensation.

Text 1: Ch 9, Ch 10. 10.1 to 10.4 **9 Hrs**

UNIT V

Data Converter fundamentals: Analog Verses discrete time signals, Converting analog signals to digital signals, sample and hold Characteristics, DAC specifications, ADC specifications, Mixed signal Layout issues.

Data Converter Architecture: DAC Architectures, ADC Architectures.

Text 2:Ch.28, Ch 29 **9Hrs**

TEXT BOOKS:

- Razavi B., “Design of Analog CMOS Integrated Circuits”, McGraw Hill, 2001
- R.Jacob Baker, Harry W.Li & David E.Boyce,“CMOS Circuit Design Layout and Simulation”, PHI, 2002

REFERENCES:

1. Razavi B., “RF Microelectronics”, Prentice Hall, 1998.
2. E. Allen, Douglas R. Holberg, “CMOS Analog circuit Design

OPEN ELECTIVE –A

SENSORS AND ACTUATORS

Semester: VII

Department: ELECTRONICS AND COMMUNICATION	<i>Open elective</i>
Course Title Sensors and Actuators	Course Code: 14ECO661
L-T-P: 3-0-1	Credits: 03
Total Contact Hours: 35hrs	Duration of SEE: 3 hrs
SEE Marks: 50	CIE Marks: 50

Pre-requisites:

- Students are expected to have the basic knowledge of Transducers, signal processing, Elements of Mechanical engineering, Basic Electrical concepts

Course Outcomes:

- Students Will Be Able To Understand The Importance Of Sensors And Actuators
- Students Will be able to understand the state of art different sensors and actuators in electrical and Magnetic domain
- Students Will be able To understand the different sensors and actuators based on mechanical phenomena
- Students will be able to understand the different sensors and actuators based on thermal and Electromagnetic Radiation
- Students Will be To analyze and Interface sensors And actuators in Smart Systems

Course Outcome to Program Outcome Mapping:

PO/P SO	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO1 0	PO1 1	PO1 2	PSO 1	PSO 2	PSO 3
CO1	*	*		*		*	*				*				
CO2	*	*		*		*	*				*	*			
CO3	*	*	*	*		*	*				*	*		*	
CO4	*	*	*	*		*	*				*	*			*
CO5	*	*	*	*		*	*								*

Teaching Methodology:

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class.

Assessment Methods:

- Two Surprise Tests, 10 Marks each. Best of two tests will be taken.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.
- Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.

UNIT 1

Introduction: Motivation ,Definition Of Sensor And Actuator, Domain Of Physical Phenomena, Classification Of Sensors And Actuators ,

Micro And Nano-Technologies : Introduction , Manufacture

Text Book 1: Chapter 1&2 7 Hrs

UNIT 2

Based On The Electric Field: Force, Electric Field And Voltage, Concept Of Capacity ,Capacitive Displacement Sensor, Capacitive Acceleration Sensor , Electrostatic Loudspeaker ,Electrostatic Mems Actuator, Definition Of Electric Resistor, Potentiometric Displacement Sensors, Dependence Of Resistivity With Temperature And Moisture, Resistive Temperature Detector, Thermistor Integrated Temperature Sensor, Dependence Of Resistivity With Deformation ,Strain Gage

Text Book 1: Chapter 3 7 Hrs

UNIT 3

Based On Mechanical Phenomena: Piezoelectric Effect, Accelerometer, Piezoelectric Temperature Sensor , Acoustic Waves, Ultrasound Transducers, Measuring Distance Using Ultrasound (Sonography, Sonar, Etc...), Fluid Actuators

Text Book 1:chapter 5 7 Hrs

UNIT 4

6. Based On Thermal Phenomena: Thomson Effect, Peltier Effect, Seebeck Effect, Thermocouple, Peltier Cell, Joule Effect, Guckel Thermal Actuator , Hot Wire Anemometer

7. Based On Electromagnetic Radiation: Quantities And Units, Electroluminescence, Photovoltaic Effect, Led, Photoresistor , Photodiode, Pyrometers, Source Of X-Rays, Measurement Of The Blood Oxygen Level With A Pulse Meter, Computer Optical Mouse, Wii Game Console, X-Ray Computed Tomography, Multi-Touch Screen, Global Positioning System (Gps)

Text Book1:Chapter 6&7 *7 Hrs*

UNIT 5

8. Based On Chemical Phenomena: Introduction, Reduction And Oxidation Reactions, Galvanic Cell, Potentiometric Sensors, Lambda Probe, Amperometric Sensor, Chemfet, Biosensors

Sensor And Actuator Networks : Introduction, Applications , Network Organization, Energy, Displacement, Temperature, Force, Signal Conditioning

Text Book 2: Chapter 8,9 and 10 *7 Hrs*

TEXT BOOKS:

Text book 1: SMART SENSORS AND ACTUATORS, Francisco Andre Correa Alegria, 2014

Text book 2: Nathan Ida Sensors, Actuators, and their Interfaces: A Multidisciplinary Introduction SciTech Publishing 2013

MICROCONTROLLER

Semester: VI

Department: ELECTRONICS AND COMMUNICATION	<i>Regular Course</i>
Course Title Microcontroller	Course Code: 14ECO662
L-T-P: 4-0-0	Credits: 03
Total Contact Hours: 35hrs	Duration of SEE: 3 hrs
SEE Marks: 50	CIE Marks: 50

PRE-REQUISITES:-

Programming experience with C and assembly is strongly recommended

COURSE OUTCOMES:-

- Students will learn hardware, software and architectural details of 8051 microcontroller.
- Students will learn to program 8051 in assembly language and C, compile, execute .
- Students will be able to embed the code in flash memory for standalone embedded system applications using Keil IDE
- Students will learn to interface 8051 with external devices like LCD, Keyboard, DC Motor, Stepper Motor, ADC and DAC.

COURSE OUTCOME TO PROGRAM OUTCOME MAPPING

PO/PSO	1	2	3	4	5	6	7	8	9	10	11	12	PSO1	PSO2	PSO3
CO1		*	*	*								*	*		*
CO2			*	*			*				*		*		
CO3				*	*		*				*	*	*		*
CO4					*				*	*	*	*	*		

Teaching Methodology:

- Blackboard teaching
- PowerPoint presentations (if needed)

- Regular review of students by conducting objective type quiz based on topics covered in the class.

UNIT-I

Microprocessor and Microcontroller: Introduction, Microprocessor and Microcontrollers, RISC & CISC CPU Architectures, Harvard and Von – Neumann CPU architecture.

The 8051 Architecture: Introduction, 8051 Microcontroller hardware, input / output pins, Ports and circuits, External Memory, Timers, Serial Communication and Interrupts.

Addressing Modes and Operations: Introduction, Addressing modes, External data moves, Code Memory data moves, PUSH and POP Instructions, Data Exchanges, Example Programs.

Text 2: Ch1. 1.0 to 1.1, Text 2: Ch3. 3.0 to 3.6, Text 2. Ch 5 **7Hrs**

UNIT-II

Logical and Arithmetic: Byte level logical operations, Bit level logical operations, Rotate and swap operations, Example Programs. Arithmetic operations: Flags, Incrementing and decrementing, addition, subtraction, multiplication and division, decimal arithmetic, Ex. Prgms.

Jump and Call Instructions: The jump and call Program range, jumps, calls and subroutines. Example Problems. *Text2:Ch 6, Ch7, Ch 8* **7Hrs**

UNIT -III

8051 Programming in C: Data types and time delays in 8051C, I/O programming, logic operations, data conversion programs, accessing code ROM space, data serialization.

Timer / Counter Programming in 8051: Programming 8051 Timers in C, Counter Programming timers 0 and 1 in 8051 C *Text 1: Ch 7, Ch 9* **7Hrs**

UNIT IV

8051 Serial Communication: Basics of serial Communication, 8051 connections to RS 232, 8051 serial communication Programming, Programming the second serial port, Serial programming in C.

Interrupts Programming: 8051 Interrupts, Programming timer interrupts, programming external hardware interrupts, Programming the serial communication interrupts, Interrupts priority in the 8051/52, Interrupt programming in C

Text 1: Ch 10, Ch 11 **7Hrs**

UNIT V

8051 Interfacing and Applications: Interfacing 8051 to LCD, keyboard parallel and serial ADC, DAC, stepper motor interfacing and DC motor interfacing. Programming in C.

Text 1: Ch 12, Ch 13, Ch 17 **7 Hrs**

TEXT BOOKS:

- Muhammad Ali Mazidi and Janice Gillespie Mazidi and Rollin D. McKinlay, “The 8051 Microcontroller and embedded systems – using assembly and C”, Prentice Hall India, Pearson, 2006
- Kenneth Ayala, “The 8051 Microcontroller”, Thomson Delmar Learning, 3rd Edition

REFERENCE BOOKS:

- Predko, ”Programming and customizing the 8051 micro controller”, Tata McGraw Hill
- Frank Vahid & Tony Givargis, “Embedded System design”, John Wiley, 2002.
- Michael J. Pont, “Embedded C”, Pearson Education, 2002.

MICROELECTROMECHANICAL SYSTEMS

Semester: VI

Department: ELECTRONICS AND COMMUNICATION	Core Elective
Course Title:- Micro Electromechanical System	Course Code: 14ECO665
L-T-P: 4-0-0	Credits: 03
Total Contact Hours: 35hrs	Duration of SEE: 3 hrs
SEE Marks: 50	CIE Marks: 50

Pre-requisites:

Students are expected to have the following topical knowledge upon entering this course:

- Satisfactory completion of understanding of basics of semiconductor theory in physics.
- Satisfactory knowledge of Analog Electronic Circuits.
- Satisfactory knowledge of Physics.
- Satisfactory knowledge of Chemistry.
- Fundamentals of Mechanical engineering.

Course Outcomes:

- Students will get a basic knowledge of MEMS Applications and Fabrication Process
- They get hands on experience on MEMS CAD tool.
- Students will be able to learn the scaling and miniaturization effects in microsystems devices.
- Students will be able to understand the integration and packaging of Microsystems.

COURSE OUTCOME TO PROGRAM OUTCOME MAPPING:-

PO/PSO	1	2	3	4	5	6	7	8	9	10	11	12	PSO1	PSO2	PSO3
CO1	*	*	*		*				*	*	*				*
CO2	*	*	*		*				*		*		*		
CO3		*	*	*					*		*				*
CO4		*	*	*					*		*		*		

Teaching Methodology:

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class

Assessment Methods

- Two Surprise Tests, 10 Marks each. Best of two tests will be taken.
- A mini project is given to all students who are asked to give a report on the same and presentation is also given by students based on which the students are evaluated for 10 marks.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.

Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.

UNIT I

Introduction: Why Miniaturization?, Microsystems versus MEMS, Why microfabrication? Smart Materials, Structures and systems, Integrated Microsystems, Applications of smart Materials and Micro Systems

Materials for MEMS: Silicon compatible material System-Silicon, Silicon oxide and Nitride, Thin metal Films, Polymers, Other material and substrates, Important materials properties and Physical effects,

Text book 1: Ch.1: 1.1, 1.2, 1.3, 1.4, 1.5, 1.6 Text book 2: Chapter 2

UNIT II

Micromachining Technologies: Thin Film Deposition, lithography, Etching, Silicon Micromachining, Advanced Process for Microfabrication.

Text Book1: Ch 3: 3.1, 3.2, 3.3, 3.4, 3.5, 3.7

UNIT III

Circuits for conditioning sensed signals: Differential charge measurement, switched capacitor circuits for capacitance measurement, circuits for measuring frequency shift,

Implementation of controllers: Design methodology, circuit implementation, digital controllers.

Scaling Effects in Microsystems: Scaling in the mechanical Domain, Scaling in the electrostatic Domain, Scaling in Magnetic Domain, Scaling in the thermal Domain, Scaling in Diffusion, Scaling in Fluids, scaling Effects in the Optical Domain, Scaling in Biochemical Phenomena.

Text book1: Ch. 7: 7.4,7.6 Ch. 9: 9.1, 9.2, 9.3, 9.4, 9.5, 9.6, 9.7, 9.8

UNIT IV

Integration of Micro and Smart Systems: Integration of Microsystems and Microelectronics, Microsystems Packaging, Case studies of Integrated Microsystems

Text Book 1: Ch 8: 8.1, 8.2, 8.3,

UNIT V

MEMS Structures and Systems in Industrial and Automotive Applications: General Design methodology, Techniques for sensing and actuation, Passive micromachined Mechanical structures, Sensors and Analysis systems, Actuators and Actuated Microsystems

MEMS Applications in Life Sciences: Microfluidics for Biological applications, DNA Analysis, PCR, Microelectrode arrays,

Text book 2: Chapter 4, Chapter 6

Simulations of the applications using MEMS tools

TEXT BOOKS:

Text book 1: G.K. Ananthasuresh, K.J. Vinoy, S. Gopalakrishnan, K.N. Bhat, V.K. Aatre, “Micro and Smart Systems”, Wiley India, 2010

Text book 2: Nadim Maluf, Kirt Williams “An Introduction to Microelectromechanical Systems Engineering” Second addition

VLSI LAB

Department: ELECTRONICS AND COMMUNICATION	<i>Lab</i>
Course Title: VLSI lab	Course Code: 14ECL67
	Credits: 1.5
Total Contact Hours: 3hrs/week	Duration of SEE: 3 hrs
SEE Marks: 50	CIE Marks: 50

PREREQUISITES

- Satisfactory completion of understanding of basics of semiconductor theory in physics.
- Satisfactory knowledge of Analog Electronic Circuits.
- Satisfactory knowledge of Digital Electronics

Course Outcomes

- Students will acquire the knowledge and usage of VLSI CAD tool as required by industry.
- The students will understand the optimization of area in a VLSI chip.

Conduct the DC, AC and Transient Analysis for a given circuit

- Inverter
- Common Source Amplifier
- Common Drain Amplifier
- Current Mirror

- Single Stage
 - Two Stage
 - Differential Amplifier
 - Operational Amplifier
 - Single STage,Two Stage
- Also draw the layout of the above mentioned experiments

ADVANCED COMMUNICATION LAB

Department: ELECTRONICS AND COMMUNICATION	Lab
Course Title:- AC lab	Course Code: 10ECL68
	Credits: 1.5
Total Contact Hours: 3hrs/week	Duration of SEE: 3 hrs
SEE Marks: 50	CIE Marks: 50

PRE-REQUISITE BY TOPIC:

Fundamentals of analog modulation and some exposure to microwave, antenna and wave propagation.

OUTCOME OF THE COURSE:-

The specific course outcomes supporting the program outcome are-

- Students will get a basic knowledge digital modulation techniques ask, fsk, dpsk and qpsk.
- They get hands on experience on micro strips.
- Students get hands on experience to use microwave test branch.
- They get experience to use fiber optic kit

COURSE OUTCOMES:-

- Students get hands on experience on microwave, test bench, microstrips
- Students will be able to design a circuit to implement digital modulation technique

COURSE CONTENTS

- TDM of two band limited signals.
- ASK generation & detection
- FSK generation & detection.
- PSK generation & detection.
- DBSK generation & detection.
- QPSK generation & detection.
- PCM generation & detection using codec chip.
- Measurement of losses in a given optical fiber (propagation loss, bending loss) and numerical aperture.
- Measurement of power & VSWR in a microwave test bench.
- Measurement of guide wavelength and frequency in microwave test bench.
- Measurement of gain & directivity of standard dipole antenna (printed dipole antenna).
- Measurement of gain & directivity of micro strip patch antenna.
- Measurement of gain & directivity of printed YAG antenna.
- Determination of coupling and isolation characteristics of strip line or micro strip line directional coupler.
- Measurement of resonance characteristics of micro strip ring resonator and determination of dielectric constant of the substrate.
- Measurement of power division & isolation characteristics of a micro strip 3 db power divider.

VII SEMESTER

FIBER OPTIC COMMUNICATION				
Course Code	14EC71		Credits	04
Hours/Week(L-T-P)	4-0-0		CIE Marks	50
Total Hours	52(L)		SEE Marks	50
Exam Hours	03		Course Type	Core

COURSE OUTCOMES
<ul style="list-style-type: none">• Students understand the principle of EM waves propagation in fibre• Students will be able to understand the different kind of losses, signal distortion in optical wave guides• Students will learn the different technologies available for optical sources, detectors• They will be able to draw up a power budget for an optical-fibre communication link and use it to

estimate the maximum link distance.

COURSE CONTENTS

UNIT-1 (9Hrs)

Overview of optical fiber communication: Advantages of optical fiber communication, Basic principles, Fiber modes and configuration, step index and graded index structures, Fiber materials, Fiber fabrication, Mechanical properties of fibers, Fiber optic cables.

Signal Degradation in optical fibers: Attenuation, Signal distortion in optical Waveguides, Pulse broadening in graded index in graded index waveguides, Mode Coupling and Design optimization of single mode fibers. *Text 1: Ch 2.2 to 2.10 and 3.1 to 3.5*

UNIT-2 (9Hrs)

Optical sources: Basic characteristics of light sources for communication, LED sources and LASER diodes sources, Hetero junction structure.

Optical Detectors: Physical principles of photo diode, PIN photo diodes and AVALANCHE photo diodes and their responses. *Text 1:Ch 4.1 to 4.3 and 6.1 to 6.3*

UNIT-3 (9Hrs)

Power launching and coupling: Source of fiber power launching, Lensing schemes for Coupling improvement, fiber to fiber joints, LED coupling to single mode fibers, Fiber Splicing, optical fiber connectors.

Optical receiver operation: Fundaments receiver operations, digital receiver Performance calculation, Pre amplifier types, Analog receiver. *Text 1: Ch 5.1 to 5.6 and 7.1 to 7.5*

UNIT-4 (9Hrs)

Analog systems: Overview of analog links, Carrier to noise ratio, Multi-channel Transmission techniques.

Digital Transmission systems: Point to point links, System considerations, Link power Budget, Rise time budget, Line coding for optical fiber links multiplexing, Error Correction.

Text 1:Ch 8.1 to 8.3 and 9.1 to 9.3

UNIT-5 (9Hrs)

Advanced systems and techniques: Operational principles of Wavelength division

Multiplexing, passive components, Optical amplifiers, Local area networks, SONET/SDH Networks, Photonic switching, and non-linear optical effects.

Text 1: Ch 10.1 to 10.2 and 12.1 to 12.5 & Ch 11

TEXT BOOKS
1. Gerd Keiser, "Optical fiber communication", MC Graw Hill, 3Edition, 2000.
REFERENCE BOOKS
1. John Gowar, "Optical communication systems", PHI, 2001 2. D.C Agarwal, Wheeler "Fiber optic communication".

TEACHING METHODOLOGY																
<ul style="list-style-type: none"> • Blackboard teaching • PowerPoint presentations (if needed) • Regular review of students by asking questions based on topics covered in the class 																
COURSE ASSESSMENT METHOD																
CIE:																
<ul style="list-style-type: none"> • Two Surprise Tests, 10 Marks each. Best of two tests will be taken. • Three internals, 30 Marks each will be conducted and the Average of best of two will be taken. 																
SEE:																
<ul style="list-style-type: none"> • Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks. • Two Questions are to be set from each unit, carrying 20 Marks each. • Students have to answer 5 questions selecting one full question from each unit 																
CO-PO-PSO MAPPING																
CO/P O	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO1 0	PO1 1	PO1 2	PSO 1	PSO 2	PSO 3	
CO1	*	*	*			*	*			*			*		*	
CO2	*	*	*	*		*	*			*			*		*	
CO3	*		*										*	*		
CO4	*	*	*			*	*		*				*		*	

COMPUTER COMMUNICATION NETWORK				
Course Code	14EC72		Credits	04
Hours/Week(L-T-P)	4-0-0		CIE Marks	50

Total Hours	52(L)		SEE Marks	50
Exam Hours	03		Course Type	Core

COURSE OUTCOMES

- Student will be able to apply knowledge of mathematics to model and analyze the flow of data on a communication network
- Student will be able to acquire knowledge of layered architecture and interconnecting standards involved in computer networks
- Student will be able to design and implement a local area network of computers
- Student gains knowledge of addressing, routing and protocols involved in building a network of networks.

COURSE CONTENTS

UNIT-1 (9Hrs)

Introduction: Layered tasks, OSI Model, Layers in OSI model, TCP/IP Suite, Addressing, Telephone and cable networks for data transmission, Telephone networks, Dial up modem, DSL, Cable TV for data transmission. *Text1: Ch 2*

UNIT-2 (9Hrs)

Data link control: Framing, Flow and error control, Protocols, Noiseless channels and noisy channels,

HDL Multiple access: Random access, Controlled access, Channelization.

Text 1: Ch.11. 11.1 to 11.6,Ch 12

UNIT-3 (9Hrs)

Wired LAN: Wired LAN, Ethernet, IEEE standards, Standard Ethernet. Changes in the standards, Fast Ethernet, Gigabit Ethernet, Wireless LAN IEEE 802.11

Connecting LANs: Connecting LANs, Backbone and Virtual LANs, Connecting devices, Back bone Networks, Virtual LANs *Text 1: Ch 13, Ch 14. 14.1,Ch 15*

UNIT-4 (9Hrs)

Network Layer: Network Layer, Logical addressing, Ipv4addresses, Ipv6 addresses, Ipv4 and Ipv6Transition from Ipv4 to Ipv6.*Text 1: Ch 19 and 20*

UNIT-5 (9Hrs)

Delivery: Delivery, Forwarding, Unicast Routing Protocols, Multicast Routing protocols.

Transport Layer: Transport layer Process to process Delivery, UDP, TCP, Domain name system, Resolution *Text 1: Ch 22. 22.1 to 22.4, Ch 25. 25.1 to 25.5*

TEXT BOOKS
<ul style="list-style-type: none"> • B Forouzan, "Data communication and networking", TMH, 4th Edition, 2006
REFERENCE BOOKS
<ul style="list-style-type: none"> • James F. Kurose, Keith W. Ross, "Computer networks", Pearson education, 2nd Edition, 2003. • L L Petreson and B S Davie, "Computer Networks a systems approach", Morgan Kauffman/ Elsevier ,4th Edition, 2007.

TEACHING METHODOLOGY
<ul style="list-style-type: none"> • Blackboard teaching • PowerPoint presentations (if needed) • Regular review of students by asking questions based on topics covered in the class
COURSE ASSESSMENT METHOD
<p>CIE:</p> <ul style="list-style-type: none"> • Two Surprise Tests, 10 Marks each. Best of two tests will be taken. • Three internals, 30 Marks each will be conducted and the Average of best of two will be taken. <p>SEE:</p> <ul style="list-style-type: none"> • Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks. • Two Questions are to be set from each unit, carrying 20 Marks each. • Students have to answer 5 questions selecting one full question from each unit

CO-PO-PSO MAPPING																
CO/P O	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO1 0	PO1 1	PO1 2	PSO 1	PSO 2	PSO 3	
CO1	*	*			*								*		*	
CO2	*	*	*	*				*		*		*			*	
CO3	*	*	*					*				*			*	
CO4	*	*	*					*				*				

POWER ELECTRONICS

Course Code	14EC73		Credits	04
Hours/Week(L-T-P)	4-0-0		CIE Marks	50
Total Hours	52(L)		SEE Marks	50
Exam Hours	03		Course Type	Core

COURSE OUTCOMES

- Understand the basic operations of various power semiconductor devices and their applications
- Use appropriate power semiconductor devices for power control and automotive applications
- Study the effect of various switching algorithm on the performance of the converter.
- Understand the effect of the source on the output of the converters
- Design the controllers for power converters and drives to domestic/industrial applications.

COURSE CONTENTS

UNIT-1 (9Hrs)

Introduction: Power semiconductor devices, applications of power electronics, power semiconductor devices, control characteristics, types of power electronic circuits, peripheral effects.

Power BJTs: Switching characteristics, switching limits, base-drive control, and introduction to IGBTs, isolation of gate and base drives.

Text1: Ch1, 1.1, 1.3, 1.4, 1.5, 1.7, Ch 8, 8.2, 8.5, 8.8

UNIT-2 (9Hrs)

Thyristors: Commutation Techniques: Introduction, natural commutation, forced commutation: self-commutation, impulse commutation, resonant pulse commutation and complementary commutation, External Pulse commutation, load side commutation, Line side commutation.

Text 1: Ch 7, 7.1 to 7.3

UNIT-3 (9Hrs)

AC Voltage Controllers: Introduction, principle of ON-OFF and phase control, single-phase bidirectional controllers with resistive loads.

Controlled rectifiers: Introduction, principle of phase controlled converter operation, single-phases, Semi Converters, full converter and dual converters.

Text1: Ch 6, 6.1 to 6.4, Ch 5, 5.1 to 5.5

UNIT-4 (9Hrs)

DC Choppers: Introduction, principle of step-down and step-up choppers, step-down chopper with RL loads, performance parameters. Chopper classification, analysis of impulse commutated thyristor chopper (only qualitative analysis).

Text1: Ch9, 9.1 to 9.6 & 9.8

UNIT-5 (9rs)

Inverters: Introduction, principle of operation, performance parameters, single phase bridge inverters, three phase inverters, voltage control of single phase inverters, current source inverter, variable DC link inverter.

Text 1: Ch10, 10.1 to 10.7 and 10.11

TEXT BOOKS

- M. H. Rashid, “Power Electronics”, Prentice Hall of India Pvt. Ltd., /Pearson (Singapore -Asia) New Delhi, 2nd Edition, 2002

REFERENCE BOOKS

1. G. K. Dubey, S. R. Doradla, A. Joshi& R.M.K. Sinha, “ Thyristorized Power Controllers”, New Age International (P) Ltd. Publishers, 9th Reprint, 1999.
2. M. D. Sing and Khanchandani K. B, “Power Electronics”, TMH Publishing Company Limited, 2001.
3. Cyril W.Lander, “Power Electronics”, McGraw Hill, 3rd Edition.

TEACHING METHODOLOGY

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class

COURSE ASSESSMENT METHOD

CIE:

- Two Surprise Tests, 10 Marks each. Best of two tests will be taken.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.

SEE:

- Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.
- Two Questions are to be set from each unit, carrying 20 Marks each.
- Students have to answer 5 questions selecting one full question from each unit

CO-PO-PSO MAPPING

CO/PO	PO 1	PO2	PO3	PO4	PO5	PO 6	PO 7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PS03
CO1		*		*	*	*							*	*	

CO2		*		*	*							*		
CO3	*				*								*	*
CO4	*		*			*	*					*		

ENTERPRENEURSHIP DEVELOPMENT AND IPR				
Course Code	14ECH74		Credits	03
Hours/Week(L-T-P)	4-0-0		CIE Marks	50
Total Hours	52(L)		SEE Marks	50
Exam Hours	03		Course Type	Core

COURSE OUTCOMES	
<i>Students will be able to</i>	
• Recognize the importance of entrepreneurship and its role in economic development of the Country.	
• Identify various schemes of Central and State Governments and their agencies available to promote MSME and steps in setting up small enterprises, to know the sources of financing and analysing financial statements.	
• Identify and select the projects by conducting feasibility studies with respect to marketing, technical, financial, economic and social.	
• Prepare project report for starting an enterprise in line with planning commission guidelines for appraising to various statutory authorities and financial institutions.	
• Appraise of IP rights like patents, industrial design, trademark, copyrights for effective protection and utilization of innovations.	

COURSE CONTENTS	
UNIT-1 (9Hrs)	
Introduction-meaning and importance of entrepreneurship, entrepreneur, types, characteristics, entrepreneurial process, role of entrepreneurs in economic development, problems faced by entrepreneurs, scope in India, Start ups	
Make in India Concept: Plans and policies, Sectors, Government Initiatives, Investment Opportunities,	

Ease of doing Business.
UNIT-2 (9Hrs)
Micro, Small and medium enterprises, Definition of MSMEs as per MSME act, characteristics of small enterprises, need and advantages of small enterprises, Steps in setting up of small enterprises, Institutional support to MSMEs-State supporting agencies-TECSOK, KIADB, KSSIDC, KSFC, National Schemes-MSME-DI, NSIC, SIDBI Sources of financing: Venture capital, Angel investors, Series A, B and C investors. Financial statements: Balance sheet, Profit and Loss account, Financial ratio analysis.
UNIT-3 (9Hrs)
Preparation of Project reports, control variables in project, project lifecycle, project report, need, project identification, project selection, components of project report, formulation of report, planning commission guidelines, project appraisal, feasibility study-market, financial, technical and economic, PERT and CPM, errors in report.
UNIT-4 (9Hrs)
Introduction to IP, What is Intellectual Property (IP)?, Historical background of IP, Economic value of IP, Motivation to IP development, IP system strategy, Emerging issues, IPR governance, Institutions for administering the IP system, IP rights and marketing regulations, IPR protection, protecting consumers and protecting competition, IP management framework, Drivers of IP management, IP value chain, IP management framework, IP strategies, Strategic considerations, managing trademarks.
UNIT-5 (9Hrs)
Intellectual Property Rights-What are IPRs?, Types of IPRs, Indian IPR scenario, Legal use of IP, Global Vs Indian IPR landscape, TRIPS and its implications Patents-What is a patent, history of patent, Criteria for patent, types of patents, Indian patent act, patents for computer software, business models, incremental innovation, patent infringement Trademarks-role, as a marketing tool, trademark rights, types, use of trademarks, trademark act, trademark registration in India Copyrights-meaning, copyright protection in India, enforcement measures, copyright act.
TEXT BOOKS
<ul style="list-style-type: none"> • Dynamics of Entrepreneurial Development and Management” by Vasanth Desai, Himalaya, “Publishing House. • Entrepreneurship and Management by S Nagendra and Manjunath VS, Pearson Publications • Managing Intellectual Property by Vinod V. Sople, PHI, 3rd Edition, 2012. • Intellectual Property-Copyrights, Trademarks and patent by Richard Stim, Cengage learning 2011.
REFERENCE BOOKS
TEACHING METHODOLOGY

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class

COURSE ASSESSMENT METHOD

CIE:

- Two Surprise Tests, 10 Marks each. Best of two tests will be taken.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.

SEE:

- Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.
- Two Questions are to be set from each unit, carrying 20 Marks each.
- Students have to answer 5 questions selecting one full question from each unit

CO-PO-PSO MAPPING

CO/P O	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO1 0	PO1 1	PO1 2	PSO 1	PSO 2	PSO 3
CO1						*			*				*		
CO2										*			*		
CO3						*	*						*		
CO4									*	*	*	*	*	*	

PROGRAM ELECTIVE -E

SATELLITE COMMUNICATION				
Course Code	14ECE751		Credits	04
Hours/Week(L-T-P)	4-0-0		CIE Marks	50
Total Hours	52(L)		SEE Marks	50
Exam Hours	03		Course Type	Program Elective

COURSE OUTCOMES

- Students will be able to identify the fundamentals of orbital mechanics, the characteristics of common orbits used by communications and other satellites, and be able to discuss launch methods and technologies.
- Students will understand the systems required by a communications satellite to function and the trade-offs and limitations encountered in the design of a communications satellite system.
- Students will be able to understand the radio propagation channel for Earth station to satellite and satellite to satellite communications links, and the basics of designing antenna systems to accommodate the needs of a particular satellite system
- Students will be able to calculate an accurate link budget for a satellite or other wireless communications link.

COURSE CONTENTS
UNIT-1 (9Hrs)
<p>Introduction: History, Overview</p> <p>Orbital Mechanics and Launchers: Orbital mechanics, Look angle Determination, Orbital perturbations, Orbit determination, Launches and Launch Vehicles, Orbital effects in communications Systems performance</p> <p><i>Text: Ch.1:1.1 to 1.4, Ch.2:2.1 to 2.6</i></p>
UNIT-2 (9Hrs)
<p>Satellite: Satellite subsystems, Attitude and orbit control systems(AOCS), Telemetry, Tracking, Tracking, Command and Monitoring, Power Systems, Communications subsystems, Satellite antennas, Equipment Reliability and space qualification tests.</p> <p>VSAT System: Introduction, Overview of VSAT systems, Network Architecture VSAT systems, Network Architecture VSAT Earth Station Engineering</p> <p><i>Text: Ch.3:3.1 to 3.7, Ch.9:9.1 to 9.3, 9.6</i></p>
UNIT-3 (9Hrs)
<p>Satellite Link Design: Introduction, Basic Transmission Theory, System Noise Temperature and G/T Radio, Design of Downlinks, satellite Systems using Small Earth Stations, Uplink Design, Design for Specified C/N: Combining C/N and C/I values in Satellite Links, System Design Examples <i>Text: Ch.4:4.1 to 4.8</i></p>
UNIT-4 (9Hrs)
<p>Multiple Access: Introduction, Frequency Division Multiple Access, Intermodulation, Intermodulation Example, Calculation of C/N with Intermodulation, Time Division multiple access, Demand Access Multiple Access (DAMA), Code Division Multiple Access (CDMA)</p> <p>Error Control for Digital Satellite Links: Implementation of Error Detection on Satellite Links</p>

Text Ch6:6.1, 6.2, 6.3, 6.5, and 6.8 Ch.7:7.6

UNIT-5 (9rs)

Low Earth Orbit and Non-Geo-stationary satellite Systems:

Introduction, Orbit Considerations, Coverage and Frequency Considerations, Delay and Throughput Considerations, Operational NGSO Constellation Design-Iridium, Teledesic

Ch.10:10.1 to 10.4, 10.6

Satellite Navigation and the Global Positioning System

Radio and Satellite Navigation, GPS position Location Principles, GPS receivers and Codes

Text: *Ch.10:10.1 to 10.4, 10.6, Ch 12:12.1, 12.2, 12.3*

TEXT BOOKS

- Charles Bostian, Jeremy Allnutt, Timothy Pratt, “Satellite Communications”, John Wiley & Sons-II Edition.

REFERENCE BOOKS

- Dennis Roody “Satellite Communications”, Mc Graw Hill.

TEACHING METHODOLOGY

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class

COURSE ASSESSMENT METHOD

CIE:

- Two Surprise Tests, 10 Marks each. Best of two tests will be taken.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.

SEE:

- Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.
- Two Questions are to be set from each unit, carrying 20 Marks each.
- Students have to answer 5 questions selecting one full question from each unit

CO-PO-PSO MAPPING

CO/P O	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO1 0	PO1 1	PO1 2	PSO 1	PSO 2	PSO 3
CO1	*			*	*	*							*	*	
CO2		*		*	*								*		
CO3	*				*								*	*	

CO4	*		*			*	*					*		
------------	---	--	---	--	--	---	---	--	--	--	--	---	--	--

LOW POWER VLSI DESIGN

Course Code	14ECE752	Credits	04
Hours/Week(L-T-P)	4-0-0	CIE Marks	50
Total Hours	52(L)	SEE Marks	50
Exam Hours	03	Course Type	Program Elective

COURSE OUTCOMES

- Students will be able to interpret and describe the sources of power dissipation in digital IC systems and study the impact of power on system performance and reliability
- Students will be able to interpret power and performance management techniques in Digital VLSI Design

- Students will be able to analyse the effect of voltage scaling, power gating and other power reduction approaches for different design abstraction levels
- Students will be able to apply probabilistic analysis to characterize dynamic power estimation.

COURSE CONTENTS

UNIT-1 (9Hrs)

Introduction: Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches, Physics of power dissipation in CMOS devices. Degrees of Freedom, Device & Technology Impact on Low Power: Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

UNIT-2 (9Hrs)

Power Optimization at Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic. Low power Clock Distribution: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew.

UNIT-3 (9Hrs)

Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components.

UNIT-4 (9Hrs)

Leakage Power minimization Approaches: Variable-threshold-voltage CMOS (VTCMOS) approach, Multi-threshold-voltage CMOS (MTCMOS) approach, Power gating, Transistor stacking, Dual-Vt assignment approach (DTCMOS).

UNIT-5 (9rs)

Power Estimation: SPICE circuit simulation, Gate level Simulation, Architectural level analysis, Data correlation analysis in DSP systems, Monte-Carlo simulation. Probabilistic power analysis: random signals, probabilistic techniques for signal activity estimation, propagation of static probability in logic circuits, gate level power analysis using transition density.

TEXT BOOKS

- M. H. Rashid, “Power Electronics”, Prentice Hall of India Pvt. Ltd., /Pearson (Singapore -Asia) New Delhi, 2nd Edition, 2002

REFERENCE BOOKS

1. Gary K. Yeap, “Practical Low Power Digital VLSI Design”, KAP, 2002
2. Rabaey, Pedram, “Low Power Design Methodologies” Kluwer Academic, 1997

TEACHING METHODOLOGY

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class

COURSE ASSESSMENT METHOD

CIE:

- Two Surprise Tests, 10 Marks each. Best of two tests will be taken.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.

SEE:

- Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.
- Two Questions are to be set from each unit, carrying 20 Marks each.
- Students have to answer 5 questions selecting one full question from each unit

CO-PO-PSO MAPPING

CO/P O	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO1 0	PO1 1	PO1 2	PSO 1	PSO 2	PSO 3
CO1	*	*	*	*	*	*				*	*	*	*		
CO2	*	*	*	*	*					*	*	*		*	*
CO3	*	*	*		*		*			*	*	*	*		
CO4	*	*	*	*	*	*					*	*	*		*

ASIC DESIGN

Course Code	14ECE753		Credits	04
Hours/Week(L-T-P)	4-0-0		CIE Marks	50
Total Hours	52(L)		SEE Marks	50
Exam Hours	03		Course Type	Program Elective

COURSE OUTCOMES

- Students will get a basic knowledge of ASIC design flow and the overview of VLSI CAD tool.
- Students will learn different CMOS logic cell architectures.
- Students will understand concepts in ASIC library development.
- They will get to know the basic concept of floor planning placement and routing and various algorithm for optimization.

COURSE CONTENTS

UNIT-1 (9Hrs)

Introduction: Full custom with ASIC, Semi customs ASIC'S, Standard cell based ASIC, gate Array based ASIC, channelled gate array, channel less gate array, structured gate array, Programmable logic devices, FPGA Design Flow, ASIC cell libraries.

Data Logic Cells: Data path elements, Adders, Multipliers, arithmetic operator, I/O cell, cell compliers

UNIT-2 (9Hrs)

ASIC library design: Logical effort: Practicing delay, logical area and logical efficiency, logical path, multistage cells, optimum delay, optimum number of stages, library cell design.

UNIT-3 (9Hrs)

Low level design entry: Schematic entry: hierarchical design, the cell library, names, schematics, icons & symbols, nets ,schematic entry for ASIC's, connections, vectored instances & buses, edit in place attributes, netlist, screener, back annotation

UNIT-4 (9Hrs)

Programmable ASIC: Programmable ASIC logic cell, ASIC I/O cell, A brief introduction to low level design language: An introduction to EDIF, PLA tool, An introduction to CFI design representation. Half gate ASIC, Introduction to Synthesis & Simulation

UNIT-5 (9rs)

ASIC construction Floor planning& placement & routing: Physical design, CAD tools, System portioning, Estimating ASIC size, Partitioning methods, floor planning tools, I/O & power planning, clock planning, placement algorithms, iterative placement improvement, time driven placement methods. Physical, design flow: Global routing, local routing, Detailed routing, Special routing, Circuit extraction & DRC

TEXT BOOKS

1. M.J.S Smith-“Application-Specific Integrated Circuits”-Pearson Education 2003.

REFERENCE BOOKS

- | |
|---|
| <ul style="list-style-type: none"> • Jose E France, Yannis Tsividis," Design Of analog-Digital VLSI circuits for Telecommunication & signal processing", Prentice Hall 1994 • Malcolm R Haskard, Lan C May,"Analog VLSI Design-NMOS & PMOS", Prentice Hall 1998 |
|---|

TEACHING METHODOLOGY
<ul style="list-style-type: none"> • Blackboard teaching • PowerPoint presentations (if needed) • Regular review of students by asking questions based on topics covered in the class

COURSE ASSESSMENT METHOD
<p>CIE:</p> <ul style="list-style-type: none"> • Two Surprise Tests, 10 Marks each. Best of two tests will be taken. • Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.
<p>SEE:</p> <ul style="list-style-type: none"> • Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks. • Two Questions are to be set from each unit, carrying 20 Marks each. • Students have to answer 5 questions selecting one full question from each unit

CO-PO-PSO MAPPING																
CO/P O	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO1 0	PO1 1	PO1 2	PSO 1	PSO 2	PSO 3	
CO1	*	*	*	*	*	*					*	*	*			
CO2	*	*	*	*	*					*	*	*		*		*
CO3	*	*	*		*		*			*	*	*	*			
CO4	*	*	*	*	*	*					*	*	*			*

IP NETWORKING				
Course Code	14ECE754		Credits	04
Hours/Week(L-T-P)	4-0-0		CIE Marks	50
Total Hours	52(L)		SEE Marks	50
Exam Hours	03		Course Type	Program Elective

COURSE OUTCOMES
<ul style="list-style-type: none"> • Satisfactory completion of understanding of basics of computer hardware and software • Satisfactory knowledge of C programming • Satisfactory knowledge of Basic Electronics (Analog and digital)

COURSE CONTENTS
UNIT-1 (7Hrs)
Introduction, Topologies, Two approaches to network communication, WAN and LAN, Hardware addressing schemes, Ethernet, Wi-Fi (T2) , T1 Ch2 Properties of the internet, Internet architecture, Interconnection of multiple networks with IP routers, users view T1 Ch3 The conceptual layers of protocol software, Functionality of the layers, ISO 7-layer model, TCP/IP 5-layer model, The Protocol Layering Principle, Two Important Boundaries In The TCP/IP Model, The Basic Idea Behind Multiplexing and Demultiplexing T1 Ch4 Universal host identifiers, IPv4 classful addressing, dotted decimal notation, subnets and masks, IP addresses, hosts, and network connections. Special addresses, An Example IPv4 Address Assignment T1 Ch5
UNIT-2 (7Hrs)
Purpose and importance of IP, IP datagram, IPv4 datagram format, Type of Service and differentiated services, Datagram encapsulation, Fragmentation, Reassembly, TTL, Optional IP Items, Network byte order. T1 Ch7 UDP, message format, Checksum, protocol ports T1 Ch10 Properties of reliable delivery service, Reliability, Sliding window, TCP, Ports, Connections, Endpoints. T1 Ch11
UNIT-3 (7Hrs)
TCP Segments, Streams, Sequence numbers, Variable Window / flow control, segment format, OOB data, TCP options, Checksum, Ack/retransmission/timeouts, Response to congestion, Establishing /closing TCP connection, TCP state machine T1 Ch11 The Client-Server Model, UDP Echo Server, Sequential and Concurrent Servers, Socket API The Socket Abstraction and Socket Operations, Socket options, TCP Connections, Obtaining and Setting

the Host Name, Library Functions Related to Sockets. Examples (Client, Server)
T1 Ch20 and Ch21

UNIT-4 (7Hrs)

World Wide Web, Architectural Components, URL, HTML, HTTP, GET Request, Error messages, Persistent connections, Data length and program output, Length encoding and headers, Negotiation, Conditional requests, proxy servers and caching

T1 Ch25

UNIT-5 (7rs)

Digitizing And Encoding, Audio and Video Transmission and Reproduction, Jitter and Play-back Delay, Real-time Transport Protocol (RTP), Streams, Mixing, And Multicasting, RTP Encapsulations, RTP Control Protocol (RTCP), RTCP Operation, IP Telephony and Signaling, SIP (T2) T1 Ch26

Important Note – This course covers IPv4 protocol only

TEXT BOOKS

- Text book 1 (T1) – Internetworking with TCP/IP Volume One, 6/E Douglas E. Comer
- Text book 2 (T2) –Data and Computer Communications, 10/E William Stallings

REFERENCE BOOKS

TEACHING METHODOLOGY

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class

COURSE ASSESSMENT METHOD

CIE:

- Two Surprise Tests, 10 Marks each. Best of two tests will be taken.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.

SEE:

- Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.
- Two Questions are to be set from each unit, carrying 20 Marks each.
- Students have to answer 5 questions selecting one full question from each unit

CO-PO-PSO MAPPING

CO/P O	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO1 0	PO1 1	PO1 2	PSO 1	PSO 2	PSO 3
CO1		*				*						*		*	
CO2		*	*			*						*			*
CO3	*	*	*	*			*				*	*		*	

CO4				*	*	*								*	*
-----	--	--	--	---	---	---	--	--	--	--	--	--	--	---	---

ARTIFICIAL NEURAL NETWORKS				
Course Code	14ECE759		Credits	04
Hours/Week(L-T-P)	4-0-0		CIE Marks	50
Total Hours	52(L)		SEE Marks	50
Exam Hours	03		Course Type	Program Elective

COURSE OUTCOMES				
<ul style="list-style-type: none"> Understand the fundamentals of artificial neural networks Understand a few applications of artificial neural networks Students will be able to analyze multilayer feed forward neural networks, radial basis function networks and recurrent networks; Students will implement both supervised and unsupervised learning algorithms. 				

COURSE CONTENTS				
UNIT-1 (7Hrs)				
Introduction: What is a neural network? Human brain; models of a neuron; neural networks as directed graphs; feedback; network architectures; knowledge representation.				
Learning Processes: Error-correction learning; memory-based learning; Hebbian learning; competitive learning; Boltzmann learning; credit-assignment problem; learning with and without a teacher.				
UNIT-2 (7Hrs)				
Single-Layer Perceptron: Adaptive filtering problem; unconstrained optimization techniques; linear least-squares filters; least-mean-square algorithm; learning curves; learning rate annealing techniques, Perceptron; perceptron convergence theorem.				
UNIT-3 (7Hrs)				
Multi-Layer Perceptron: Preliminaries, Back-Propagation Algorithm, XOR problem, Heuristics to make Back-Propagation Algorithm perform better, Output representation and Decision rule.				

UNIT-4 (7Hrs)
Support Vector Machines: Optimal Hyperplane for Linearly Separable Patterns, Optimal Hyperplane for Non-separable patterns, How to Build a SVM for Pattern recognition.
UNIT-5 (7rs)
Committee Machines: Ensemble Averaging, Computer experiments, Boosting
TEXT BOOKS
I. "Neural Networks: A Comprehensive Foundation," S. Haykin, 2 nd edition, Prentice Hall of India, 2003.
Unit I : 1.1-1.7, 2.1-2.9
Unit II : 3.1-3.9
Unit III : 4.1-4.7
Unit IV : 6.1-6.4
Unit V: 7.1-7.5
REFERENCE BOOKS

CO2	*	*	*	*	*			*					*		*
CO3	*	*	*	*	*					*				*	
CO4	*	*	*												*

OPEN ELECTIVE – B

ADHOC WIRELESS NETWORKS				
Course Code	14ECO761		Credits	03
Hours/Week(L-T-P)	3-0-0		CIE Marks	50
Total Hours	39(L)		SEE Marks	50
Exam Hours	03		Course Type	Open Elective

COURSE OUTCOMES				
<ul style="list-style-type: none"> Students will be able to understand and explain the concept of ad-hoc wireless networks, their applications Students will be able to understand issues in designing ad-hoc wireless networks Students will be able to apply knowledge of mathematics, probability, and statistics to design, implement ADHOC wireless protocols Students will be able to apply the knowledge of networking to analyse ad hoc wireless networking protocols 				

COURSE CONTENTS				
UNIT-1 (7Hrs)				
Introduction to Avionics				
Importance and role of avionics, avionic environment, Choice of Units Displays –Man Machine Interaction				

Displays and man-machine interaction: Head up displays, helmet mount displays, discussion of HUDs vs. HMDs, Head down displays, data fusion, intelligent displays management, Displays technology, control and data entry, instrument placement. *Text 1: Ch 1.1 to 1.3 and 2.1 to 2.3, 2.5 to 2.10*

UNIT-2 (7Hrs)

Surveillance Systems: Air traffic control, Primary radar, Secondary radar, Replies, Various system modes, error checking, Transponders of ATCCRB & Mode S, Collision avoidance, Lightning detection, Weather radar. *Text 2: Ch 5.1 to 5.18*

UNIT-3 (7Hrs)

Airborne Communications Systems: VHF AM Communications, VHF Communications hardware, High frequency communications, ACARS, SELCAL, Digital Communications and Networking, VHF Digital communications, Data link Modes. *Text 2: Ch 6.1 to 6.10*

UNIT-4 (7Hrs)

On-board Communications: Microphones, Digital communications, Transmission lines, Digital data bus systems ARINC 426, MIL STD 1553, ARINC 629, Commercial standard digital bus, Fiber optic communication. *Text 2: Ch 7.1 to 6.11*

UNIT-5 (7rs)

Avionic Systems Integration: Data bus systems, integrated modular avionics, and commercial off-the shelf (COTS).

Unmanned Air Vehicles: Importance of Unmanned air vehicles, UAV avionics. *Text 1: Ch 9.1 to 9.4 and 10.1 to 10.3*

TEXT BOOKS

1. **Collinson RPG**, Introduction to Avionics, Third Edition, Kluwer Academic Publishers, Chapman & Hall.

2. **Albert Helfrick**, Principles of Avionics 2nd Edition, Avionics Communication Inc.

REFERENCE BOOKS

1. **Moir, I. and Sea bridge**, civil avionics systems, AIAA Education series

2. **Moir, I. and Sea bridge** Military avionics systems (aerospace)

TEACHING METHODOLOGY

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class

COURSE ASSESSMENT METHOD

CIE:

- Two Surprise Tests, 10 Marks each. Best of two tests will be taken.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.

SEE:

- Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.
- Two Questions are to be set from each unit, carrying 20 Marks each.
- Students have to answer 5 questions selecting one full question from each unit

CO-PO-PSO MAPPING

CO/P O	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO1 0	PO1 1	PO1 2	PSO 1	PSO 2	PSO 3
CO1						*	*		*			*			*
CO2	*	*		*	*	*	*					*	*	*	
CO3	*	*	*			*						*	*	*	
CO4	*			*	*	*	*					*	*		*

AVIONICS

Course Code	14ECO764		Credits	03
Hours/Week(L-T-P)	3-0-0		CIE Marks	50
Total Hours	39(L)		SEE Marks	50
Exam Hours	03		Course Type	Open Elective

COURSE OUTCOMES

- Students will understand the need of avionics for both military and civil aviation.
- Students will analyse the communication, surveillance concepts involved in avionics.
- Students will get a summary of avionics which integrates electronics and aviation in both manned and unmanned air vehicles.
- Students will be able to analyse the various electronic systems/subsystems involved in an aircraft.

COURSE CONTENTS

UNIT-1 (7Hrs)

Introduction to Avionics: Importance and role of avionics, avionic environment, Choice of Units

Displays –Man Machine Interaction: Displays and man-machine interaction: Head up displays, helmet mount displays, discussion of HUDs vs. HMDs, Head down displays, data fusion, intelligent displays management, Displays technology, control and data entry, instrument placement. *Text 1: Ch 1.1 to 1.3 and 2.1 to 2.3, 2.5 to 2.10*

UNIT-2 (7Hrs)

Surveillance Systems: Air traffic control, Primary radar, Secondary radar, Replies, Various system modes, error checking, Transponders of ATCCRB & Mode S, Collision avoidance, Lightning detection, Weather radar. *Text 2: Ch 5.1 to 5.18*

UNIT-3 (7Hrs)

Airborne Communications Systems: VHF AM Communications, VHF Communications hardware, High frequency communications, ACARS, SELCAL, Digital Communications and Networking, VHF Digital communications, Data link Modes. *Text 2: Ch 6.1 to 6.10*

UNIT-4 (7Hrs)

On-board Communications: Microphones, Digital communications, Transmission lines, Digital data bus systems ARINC 426, MIL STD 1553, ARINC 629, Commercial standard digital bus, Fiber optic communication. *Text 2: Ch 7.1 to 6.11*

UNIT-5 (7rs)

Avionic Systems Integration: Data bus systems, integrated modular avionics, and commercial off-the shelf (COTS).

Unmanned Air Vehicles: Importance of Unmanned air vehicles, UAV avionics. *Text 1: Ch 9.1 to 9.4 and 10.1 to 10.3*

TEXT BOOKS

Collinson RPG, Introduction to Avionics, Third Edition, Kluwer Academic Publishers, Chapman & Hall.

2. **Albert Helfrick**, Principles of Avionics 2nd Edition, Avionics Communication Inc.

REFERENCE BOOKS

- **Moir, I. and Sea bridge**, civil avionics systems, AIAA Education series
- **Moir, I. and Sea bridge** Military avionics systems (aerospace)

TEACHING METHODOLOGY

- Blackboard teaching
- PowerPoint presentations (if needed)

- Regular review of students by asking questions based on topics covered in the class

COURSE ASSESSMENT METHOD

CIE:

- Two Surprise Tests, 10 Marks each. Best of two tests will be taken.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.

SEE:

- Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.
- Two Questions are to be set from each unit, carrying 20 Marks each.
- Students have to answer 5 questions selecting one full question from each unit

CO-PO-PSO MAPPING

CO/P O	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO1 0	PO1 1	PO1 2	PSO 1	PSO 2	PSO 3
CO1						*	*		*			*			*
CO2	*	*		*	*	*	*					*	*	*	
CO3	*	*	*		*							*	*	*	
CO4	*			*	*	*	*					*	*		*

MICRO SMART SYSTEMS

Course Code	14ECO765		Credits	03
Hours/Week(L-T-P)	3-0-0		CIE Marks	50
Total Hours	39(L)		SEE Marks	50
Exam Hours	03		Course Type	Open Elective

COURSE OUTCOMES

--

COURSE CONTENTS
UNIT-1 (7Hrs)
INTRODUCTION TO MICRO AND SMART SYSTEMS: What are smart-material systems? Evolution of smart materials, structures and systems. Components of a smart system. Application areas. Commercial products. What are microsystems? Feynman's vision. Micro machined transducers. Evolution of micro-manufacturing. Multi-disciplinary aspects. Applications areas. Commercial products.
UNIT-2 (7Hrs)
MICRO AND SMART DEVICES AND SYSTEMS: PRINCIPLES AND MATERIALS: Definitions and salient features of sensors, actuators, and systems. Sensors: silicon capacitive accelerometer, piezo-resistive pressure sensor, blood analyzer, conductometric gas sensor, fiber-optic gyroscope and surface-acoustic-wave based wireless strain sensor. c) Actuators: silicon micro-mirror arrays, piezo-electric based inkjet printhead, electrostatic comb-drive and micro motor, magnetic micro relay, shape memory-alloy based actuator, electro-thermal actuator. d) Systems: micro gas turbine, portable clinical analyzer, active noise control in a helicopter cabin.
UNIT-3 (7Hrs)
MICROMANUFACTURING AND MATERIAL PROCESSING: Silicon wafer processing, lithography, thin-film deposition, etching (wet and dry), wafer-bonding, and metallization. b. Silicon micromachining: surface, bulk, moulding, bonding based process flows. Integration of microelectronics and micro devices at wafer and chip levels.
UNIT-4 (7Hrs)
Smart Objects: The “Things” in IoT, Sensors, Actuators, and Smart Objects, Sensor Networks, Connecting Smart Objects, Communications Criteria, IoT Access Technologies.
UNIT-5 (7rs)
Types of sensors and applications, over view: Trends in sensor Technology and IC Sensors, sensor array's and multi sensor systems, smart sensors, sensor networks in R & D, sensors and networks, industrial network and automation.
TEXT BOOKS
<ul style="list-style-type: none"> • MEMS & Microsystems: Design and Manufacture, Tai-Ran Tsu, Tata Mc-Graw-Hill. • “Micro and Smart Systems” by Dr. A.K.Aatre, Prof. Ananth Suresh, Prof.K.J.Vinoy, Prof. S. Gopalakrishna, Prof. K.N.Bhat., John Wiley Publications. • David Hanes, Gonzalo Salgueiro, Patrick Grosssetete, Robert Barton, Jerome Henry, "IoT Fundamentals: Networking Technologies, Protocols, and Use Cases for the Internet of Things", 1 st Edition, Pearson Education (Cisco Press Indian Reprint). (ISBN: 978- 9386873743) • 4. wireless sensor network:a networking perspective – by jun abas jamalipur. john wiley 2009

REFERENCE BOOKS

--

TEACHING METHODOLOGY

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class

COURSE ASSESSMENT METHOD

CIE:

- Two Surprise Tests, 10 Marks each. Best of two tests will be taken.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.

SEE:

- Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.
- Two Questions are to be set from each unit, carrying 20 Marks each.
- Students have to answer 5 questions selecting one full question from each unit

CO-PO-PSO MAPPING

CO/P O	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO1 0	PO1 1	PO1 2	PSO 1	PSO 2	PSO 3
CO1															
CO2															
CO3															
CO4															

POWER ELECTRONICS LAB

Course Code	14ECL77		Credits	1.5
Hours/Week(L-T-P)	0-0-3		CIE Marks	50
Total Hours	3H/W		SEE Marks	50

Exam Hours	03		Course Type	Regular Lab
-------------------	-----------	--	--------------------	--------------------

COURSE OUTCOMES

- Upon successful completion of this course, the students will be able to design OPAMP related Experiments.
- After the modulation task students will be able to plan and implement basic measurement arrangements of modulation system.

COURSE CONTENTS

LIST OF EXPERIMENTS

- Study of Static Characteristics Of SCR
- Study of Static Characteristics Of DIAC.
- Study of Static Characteristics Of MOSFET
- Study of Static Characteristics Of IGBT
- Half And Full Wave RC Firing Circuits-RC Triggering
- AC voltage Controller
- Universal/Induction Motor Speed Control Unit -0.5hp 220v AC/DC-UMC-2305
- Speed Control Of DC Motor Using 1ph Half Controlled
- Stepper Motor Controller –SMC -305
- Study of SCR Based Voltage Commutated DC – Chopper Circuit.
- RESONANT PULSE CHOPPERS (Current commutated chopper)
- Series Inverter-30V/2A MSI-302
- Forced Commutation Study Unit – FCU
- Auxiliary SCR Commutation (CLASS-D)
- Parallel inverter-30V/2A PI-302
- Half And Full Wave UJT Firing Circuits
- Single phase PWM inverter-IGBT Based
- Design Based Experiment
 1. Design Of DC-Power Supply
 2. Design Based Experiment-1-Phase AC Voltage Controller With R-Load
 3. Design Based Experiment 1-Phase AC Voltage Controller With RL-Load

COMPUTER COMMUNICATION NETWORKS LABORATORY

Course Code	14ECL78		Credits	1.5
Hours/Week(L-T-P)	0-0-3		CIE Marks	50
Total Hours	3H/W		SEE Marks	50
Exam Hours	03		Course Type	Regular Lab

COURSE OUTCOMES	
<ul style="list-style-type: none"> • Student will be able to apply the principles of computer networks • Student will be able to analyse the functionality of layered network architecture. • Student will be able to apply different protocols to design and implement in wired/wireless networks. • Student will be able to compare different routing algorithms • Student will be able to analyze and implement error control coding techniques. 	

COURSE CONTENTS	
LIST OF EXPERIMENTS	
<ul style="list-style-type: none"> • Simulate a three nodes point-to-point network with duplex links between them. Set the queue size vary the bandwidth and find the number of packets dropped • Simulate a four node point-to-point network, and connect the links as follows: n0-n2, n1- n2 and n2-n3. Apply TCP agent between n0-n3 and UDP n1-n3. Apply relevant applications over TCP and UDP agents changing the parameter and determine the number of packets by TCP/UDP • Simulate an Ethernet LAN using N nodes and set multiple traffic nodes and determine collision across different nodes • Simulate an Ethernet LAN using N-nodes(6-10), change error rate and data rate and compare the throughput • Simulate simple BSS and with transmitting nodes in wire-less LAN by simulation and Determine the performance with respect to transmission of packets. • To simulate transmission of ping messages over a network topology using ns-2. • Develop a program that implements dynamic routing algorithm using 6 nodes. • Implement the method of cyclic data transmission using UDP protocol. • Write a program for error detecting code using CRC-CCITT (16-bits). • Write a program for Hamming Code generation for error detection and correction • Write a program for plotting x-graph using exponential traffic • Write a program to create mobile nodes using Destination-Sequenced Distance-Vector Routing (DSDV) protocol. • Write a program to create mobile nodes using Destination-Sequenced Dynamic Source Routing protocol (DSR) protocol. • Write a program to create multicast network in ns2? • Write a program to create mobile nodes using Link State routing protocol? • NS2 simulation for TCP packets in a network • NS2 simulation for UDP packets in a network • Introduction to open source packet capture tool demo of features of Wireshark 	

VIII SEMESTER

WIRELESS COMMUNICATION

Semester: VIII

Department: ELECTRONICS AND COMMUNICATION	<i>Regular Course</i>
Course Title: Wireless communication	Course Code: 14EC81
L-T-P: 4-0-0	Credits: 04
Total Contact Hours: 52hrs	Duration of SEE: 3 hrs
SEE Marks: 50	CIE Marks: 50

COURSE OUTCOME

- Students will acquire the knowledge of frequency reuse concept by making use of allotted bandwidth.
- Students will be able to apply knowledge of mathematics, probability theory, and statistics to model analyze wireless communication
- After completing this course students will have basic understanding of wireless communication systems at the physical layer level.
- Students will be in a position to acquire familiarity with the state of the art technologies like GSM, CDMA and personal communication systems, in addition to an ability to understand the advanced wireless technologies like wireless LAN , wireless MAN, PAN, Bluetooth etc.

Teaching Methodology:

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class

Assessment Methods

- Two Surprise Tests, 10 Marks each. Best of two tests will be taken.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.
- Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.

COURSE OUTCOME TO PROGRAMOUTCOME MAPPING:-

PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO1 0	PO1 1	PO1 2	PSO 1	PSO 2	PSO 3
CO 1	*	*	*	*	*	*							*	

CO 2	*	*	*		*	*		*				*		*
CO 3	*	*	*	*	*	*	*						*	
CO 4	*	*	*	*			*					*	*	

UNIT I

Introduction to Wireless Communication Systems: Evolution of Mobile radio

Communications, Mobile Radiotelephony, Mobile Radio Systems around the World, Examples of Wireless Communication Systems, Paging Systems, Cordless Telephone Systems, Cellular Telephone Systems, Comparison of Common Wireless Communication Systems, Trends in Cellular Radio and Personal Communication Systems.

The Cellular Concept- System Design Fundamental: Introduction, Frequency Reuse, Channel Assignment Strategies, Handoff Strategies, Interference and System capacity, Trunking and Grade of Service, Improving Coverage& capacity in Cellular Systems. *Text1: Ch 1, Ch 3*

9Hrs

UNIT II

Mobile Radio Propagation: Large Scale Path Loss: Introduction to Radio Wave Propagation, Free Space Propagation Model, Relating Power to Electric Field, The Three Basic propagation Mechanisms, Reflection, Ground Reflection (Two-Ray) Model, Diffraction, Scattering, Practical Link Budget Design Using Path Loss Models, Outdoor propagation Models, Indoor Propagation Models, Signals Penetration into Buildings, Ray Tracing and Site Specific Modeling. *Text: Ch 4*

9Hrs

UNIT III

Mobile Radio Propagation: Small –Scale Fading and Multipath: Small-Scale Multipath Propagation, Impulse Response Model of a Multipath Channel, Small-Scale Multipath Measurements, Parameters of Mobile Multipath Channels, Types of Small-scale Fading.

Speech Coding :Characteristics of Speech Signals, Quantization Techniques, Adaptive Differential Pulse Code Modulation, Frequency Domain Coding of Speech, Vcoders, Linear Predictive Coders, Choosing Speech Coders for Mobile Communications, The GSM Codec, The USDC Codec, Performance Evaluation of Speech Coders *Text: Ch 5. 5.1 to 5.5, Ch. 8*

9Hrs

UNIT IV

Modulation Techniques for Mobile Radio: Digital Modulation-an overview, Line Coding, Pulse Shaping Techniques, Geometric Representation of Modulation Techniques, Linear Modulation technique, Constant Envelope Modulation Techniques. *Text: Ch 6.6.1 to 6.9*

9Hrs

UNIT V

Multiple-Access (MA) Schemes: Introduction to FDMA,TDMA,SDMA, Packet radio, capacity of cellular system, Introduction to wireless Networks, Difference between Wireless and Fixed Telephone Networks, Public Switched telephone Networks, Limitations in Wireless networking, Merging Wireless networks and PST

Text: Ch 9, Ch 10, 10.1, 10.2

9Hrs

TEXT BOOKS:

- Theodore S.Rappaport, “Wireless Communications-Principles and practice”, Pearson Education, 2Edition, 2002

REFERENCE BOOKS:

- Dr.Kamilo Fehel , “Wireless digital Communications”, PHI.
- William C.Y.Lee, “Mobile Communications Engineering, - Theory and applications”, McGraw-Hill, 2nd Edition,1995.
- John W.Mark , “Wireless Communications and Networking ”.

PROGRAM ELECTIVE_F

CRYPTOGRAPHY

Semester: VIII

Department: ELECTRONICS AND COMMUNICATION	<i>Open elective</i>
Course Title Cryptography	Course Code: 14ECE821
L-T-P: 4-0-0	Credits: 04
Total Contact Hours: 45hrs	Duration of SEE: 3 hrs
SEE Marks: 50	CIE Marks: 50

Course outcome

- 1.Student will be able to account for the cryptographic theories, principles and techniques that are used to establish security properties
- 2.Students will be able to analyze and use methods for cryptography, the techniques for access control and intrusion detection.
- 3.Student will have an understanding of the themes and challenges of network security, the role of cryptography, reflect about limits and applicability of methods.

Teaching Methodology:

- Blackboard teaching
- PowerPoint presentations (if needed)
- Regular review of students by asking questions based on topics covered in the class

Assessment Methods

- Two Surprise Tests, 10 Marks each. Best of two tests will be taken.
- Three internals, 30 Marks each will be conducted and the Average of best of two will be taken.
- Final examination, of 100 Marks will be conducted and will be evaluated for 50 Marks.

COURSE OUTCOME TO PROGRAM OUTCOME MAPPING:-

PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO1 0	PO1 1	Po1 2	PSO 1	PSO 2	PSO 3
CO 1	S	W	M						S	W			*	
CO 2	S	S	M	S				S			W		*	*
CO 3	S	S	S			M					W		*	

UNIT I

Overview: Services, Mechanisms and attacks, OSI security architecture, Model for network security.

Classical Encryption Techniques: Symmetric cipher model, Substitution techniques, Transposition techniques, Rotor machine, Steganography.

Block Ciphers and DES (Data Encryption Standards): Simplified DES, Block cipher principles, DES, Strength of DES, Block cipher design principles, Block cipher modes of operation.

9hrs

UNIT II

Public Key Cryptography and RSA: Principles of public key cryptosystems, RSA algorithm.

Other Public Key Crypto Systems and Key Management: Key management, Diffie-Hellman key exchange, Elliptic curve arithmetic, Elliptic curve cryptography.

9hrs

UNIT III

Message Authentication and Hash Functions: Authentication requirements, Authentication functions, Message authentication codes, Hash functions, Security of hash functions and MAC's.

Digital Signature and Authentication Protocol: Digital signature, Authentication protocols, Digital signature standard.

Authentication Applications: Kerberos, X.509 authentication service, Kerberos encryption technique. 9hrs

UNIT IV

Electronic Mail Security: Pretty good privacy, S/MIME, Data compression using ZIP, Radix-64 conversion, PGP random number generator.

9hrs

UNIT V

Intruders: Intruders, Intrusion detection, Password management

Firewalls: Firewall design principles; Trusted systems. 9hrs

TEXT BOOK:

William Stallings, “**Cryptography and Network Security**”, 3rd edition, Pearson Education (Asia) Pvt. Ltd./ Prentice Hall of India, 2003.

REFERENCE BOOKS:-

- C. Kaufman, R. Perlman, and M. Speciner, “**Network Security: Private Communication in a Public World**”, 2nd edition, Pearson Education (Asia) Pvt. Ltd., 2002.
- Atul Kahate, “**Cryptography and Network Security**”, Tata McGraw-Hill, 2003.
 - Eric Maiwald, “**Fundamentals of Network Security**”, McGraw-Hill, 2003.

AUTOMOTIVE ELECTRONICS

VIII semester

Department: ECE and EEE	Course Type: Core Elective
Course Title: Automotive Electronics	Course Code: 14ECE822
L-T-P: 4-0-0	Credits: 4
Total Contact Hours: 45 hrs	Duration of SEE: 3 hrs
SEE Marks: 50	CIE Marks: 50

PREREQUISITES:

- Understanding of basics of Electronics
- Basic Knowledge of Microprocessors
- Understanding of working of Mechanical Systems, Sensors and Actuators
- Exposure to basic programming with C

COURSE OUTCOMES:

- Students will understand the concepts of Automotive Electronics systems and subsystems overview.

- Students will be able to understand sensors and sensor monitoring mechanisms aligned to Automotive systems and actuator mechanisms
- Students will be able to understand various communication systems, used in vehicle networking.
- Students will be able to understand Safety standards, advances in towards autonomous vehicles, vehicle on board and off board diagnostics

Teaching Methodology:

- Blackboard Teaching
- Class room presentations, videos and special lectures / sessions by experts from i) Department of Mechanical Engineering and ii) KPIT
- Demo sessions with Matlab / Simulink

Assessment Methods:

- CIE (50 Marks)
- Two surprise tests and two assignments, 10 marks each, average of each for a total of 20 marks
- Three internal tests, 30 marks each, average of best two would be taken for 30 marks
- SEE (50 Marks)
- An end-semester exam for 100 marks will be conducted and half of these marks would be taken into consideration.

COURSE OUTCOME TO PROGRAM OUTCOME MAPPING:-

CO / PO	Po 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	Po 9	PO1 0	PO1 1	PO1 2	PSO 1	PSO 2	PSO 3
CO 1	*			*		*	*	*	*			*	*	*	
CO 2	*	*	*	*	*	*						*		*	
CO 3	*	*	*	*	*	*						*	*	*	*
CO 4	*		*						*	*	*	*		*	

UNIT 1

Automotive Systems, Design cycle and automotive industry overview

9 hrs

Automotive Systems :

Overview of Automotive industry. Role of technology in Automotive Electronics and interdisciplinary design. Tools and Processes.

Introduction to modern automotive systems and need for electronics in automobiles and application areas of electronic systems in modern automobiles

Spark and Compression Ignition Engines: Ignition

systems, Fuel delivery systems, Engine control functions, Fuel control, Electronic systems in Engines

Automotive transmissions: Transmission fundamentals

Vehicle braking fundamentals: Vehicle dynamics during braking, hydraulic brake system components, Introduction to antilock braking systems

Steering Control: Steering system basics, Fundamentals of electronically controlled power steering: type, electronically controlled hydraulic systems and Electric power

steering systems. Passenger Safety and Convenience occupant protection systems, Overview of Hybrid Vehicles,

ECU Design Cycle : V-Model development cycle , Components of ECU, Examples of ECU on Chassis, Infotainment, Body Electronics and cluster

UNIT 2**Automotive Sensors and Actuators****9 hrs**

Systems approach to control and instrumentation: Concept of a system, Analog and Digital systems, Basic measurements systems, Analog and digital signal processing, Sensors, Sensor characteristics, Sensor response, Sensor error, Redundancy of sensors in ECUs, Smart Nodes , Examples of sensors : Accelerometers, wheel speed sensors, brake pressure sensors, Steering wheel angle, Vehicle speed sensor, Throttle position sensor, Temperature sensor, Exhaust gas oxygen concentration sensor RPM sensor, , Actuators used : Solenoids, various types of electric motors, and piezoelectric force generators, Examples for actuators: Relays, solenoids and motors. Sensors in Airbag system

UNIT 3**Microcontrollers/Microprocessors in Automotive domain, Communication protocols, Infotainment systems****Microcontrollers/Microprocessors in Automotive domain**

Critical review of microprocessor, microcontroller and digital signal processor development (overview of development within the automotive context (Architecture of 8/16 bit microcontrollers with emphasis on Ports, Timer/Counters, Interrupts. Watchdog timers, PWM)

Criteria to choose the right microcontroller/processor for various automotive applications

Understanding various architectural attributes relevant to automotive applications

Automotive grade processors ex: Renesas, Quorivva, Infineon

Understanding and working on tool chains for different processors

Development of control algorithm for different automotive subsystems Look-up tables and maps, Need of maps, Procedure to generate maps, Fuel maps/tables, Engine calibration, Torque table,

Communication protocols

Overview of Automotive communication protocols : CAN, LIN , Flex Ray, MOST, Ethernet
Communication interface with ECUs Interfacing techniques and interfacing with infotainment gadgets

Relevance of Protocols such as TCP/IP for automotive applications

Wireless LANs standards such as Bluetooth, IEE802. 11x communication protocols for automotive applications.

Infotainment Systems: Application of Telematics in Automotive domain, Global Positioning Systems (GPS)

UNIT 4

Automotive Control Systems and Model Based Development: **9hrs**

Automotive Control System & Model Based development: Control system approach in Automotive: Analog and Digital control methods, modelling of linear systems, System responses. Modeling of Automotive Systems simple examples.

Model based Development: Introduction to MATLAB, Simulink and SIMSCAPE tool boxes. Model-Based Design for a small system - Motor Model, Generator Model, Controller Model, SimDriveline Intro Simulink Simulations, Explore the system response using different control methods.

UNIT 5

Safety Systems in Automobiles and Diagnostic Systems **9 hrs**

Active Safety Systems: ABS, TCS, ESP, Brake assist etc

Passive Safety Systems: Airbag systems, Advanced Driver Assistance Systems (ADAS): Combining computer vision techniques as pattern recognition, feature extraction, learning, tracking, 3D vision, etc. to develop real-time algorithms able to assist the driving activity. Examples of assistance applications: Lane Departure Warning, Collision Warning, Automatic Cruise Control, Headlights Control, Connected Cars technology and trends towards Autonomous vehicles.

Functional Safety: Need for safety systems, safety concept, safety process for product life cycle

Diagnostics: Fundamentals of Diagnostics: Basic wiring system and Multiplex wiring system, Preliminary checks and adjustments, Self-diagnostic system. Fault finding and corrective measures, Diagnostic procedures and sequence, On board and off board diagnostics in Automobiles, OBDII, Concept of DTCs, DLC, MIL, Freeze Frames, History memory, Diagnostic tools, Diagnostic protocols : KWP2000 and UD

TEXT BOOKS:

- William Ribbens, "Understanding Automotive Electronics", 6th Edition, Elsevier
- Tom Denton: "Advanced Automotive Diagnosis", 2nd Edition, Elsevier, 2006

REFERENCE BOOKS

- Ronald K Jurgen: "Automotive Electronics Handbook, 2nd Edition, McGraw-Hill, 1999
- James D Halderman: -Automotive electricity and Electronics", PHI Publication
- Terence Rybak. Mark Stefika: Automotive Electromagnetic Compatibility (EMC), Springer. 2004
- Allan Bonnick.: "Automotive Computer Controlled Systems" Diagnostic Tools and Techniques". Elsevier Science, 2001
- Uwe Kieneke and Lars Nielsen: Automotive Control Systems Engine, Driveline and Vehicle, 2nd Edition Springer Verlag, 2005
- David Alciatore, Michael Histand: "Introduction to Mechatronics and Measurement Systems (SIE) TMH, 2007
- Iqbal Husain: "Electric and Hybrid Vehicles: Design fundamentals" CRC Press, 2003.
- G. Meyer, J. Valldorf and W. Gessner: "Advanced Microsystems for Automotive Applications", Springer. 2009
- Tracy Martin: "How to Diagnose and Repair Automotive Electrical Systems" Motor Books/MBI Publishing Company. 2005.
- Mehrdad Ebsani. Ali Emadi, Yimin Gao: - "Modern electronic. Hybrid Electric and Fuel Cell Vehicles: Fundamentals. Theory and Design". 2nd CRC Press. 2009
- Marc Herniter: "Introduction to Model Based System Design – Rose Hulman Institute of Technology

ERROR CONTROL CODING**VIII semester**

Department: ECE and EEE	Course Type: Core Elective
Course Title: Error Control Coding	Course Code: 14EC823
L-T-P: 4-0-0	Credits: 4
Total Contact Hours: 45 hrs	Duration of SEE: 3 hrs
SEE Marks: 50	CIE Marks: 50

COURSE OUTCOMES

- Students will be able to study the mathematical fundamentals required to understand the design of error control codes.
 - Students will be able to understand and analyze the basics of error control codes.
 - Students will be able to design the encoder and decoder circuit of error control codes.
 - Students will be able to understand the characteristic features and capability of different error control

COURSE OUTCOME TO PROGRAM OUTCOME MAPPING:-

UNIT I

9hrs

Introduction to linear algebra: Groups, Fields ,Binary Field Arithmetic, Construction of Galois Field GF (2^m) and its basic Properties, Computation using Galois Field GF (2^m) Arithmetic, Vector spaces and Matrices.

Linear Block Codes: Reed – Muller codes, The (24, 12) Golay code, Product codes and Interleaved codes.

UNIT-II

9 hrs

Cyclic Codes: Introduction, Generator and Parity check Polynomials, Encoding using Multiplication circuits, Systematic Cyclic codes, Encoding using Feed back shift register circuits, Generator matrix for Cyclic codes, Syndrome computation and Error detection, Meggitt decoder, Error trapping decoding, Cyclic Hamming codes, The (23, 12) Golay code, Shortened cyclic codes

UNIT III

9hrs

BCH codes: Binary primitive BCH codes, Decoding procedures, Implementation of Galois field Arithmetic, Implementation of Error correction, Non – binary BCH codes, q – ary Linear Block Codes, Primitive BCH codes over GF (q), Reed – Solomon Codes, Decoding of Non – Binary BCH and RS codes: The Berlekamp – Massey algorithm **9hrs**

UNIT IV

Majority logic decodable codes: One – Step Majority logic decoding, one – step Majority logic decodable Codes, Two – step Majority logic decoding, Multiple – step Majority logic decoding. Encoding of Convolutional codes, Structural properties, Distance properties ,Viterbi Decoding Algorithm for decoding Convolutional codes Viterbi Decoding Algorithm for decoding, Soft – output Viterbi Algorithm, Stack and Fano sequential decoding Algorithms, Majority logic decoding

UNIT-V

9hrs

Burst Error correcting Codes: Burst and Random error correcting codes, Concept of Inter – leaving, cyclic codes for Burst Error correction – Fire codes, Convolutional codes for Burst Error correction.

REFERENCE BOOKS:

- “Error Control Coding” Shu Lin & Daniel J. Costello, Jr. Pearson / Prentice Hall, Second Edition, 2004.
 Unit I- 2, 4.3 – 4.8
 Unit II- 5.1-5.10
 Unit III- 6.1, 6.2. 6.8, 7.1-7.4
 Unit IV- 8.1-8.4, 12.1-12.5
 Unit V- 20 & 21

- 2. “The theory of error correcting codes” F.J. Mac Williams and N.J.A. Sloane, North Holland, 1977

MULTIMEDIA COMMUNICATION

Semester - VIII

Department: ELECTRONICS AND COMMUNICATION	<i>Core elective</i>
Course Title MULTIMEDIA COMMUNICATION	Course Code: 14ECE824
L-T-P: 4-0-0	Credits: 04
Total Contact Hours: 45hrs	Duration of SEE: 3 hrs

SEE Marks: 50	CIE Marks: 50
----------------------	----------------------

PREREQUISITE:

Basics of Digital Communication

COURSE OUTCOMES:

1. This subject helps the students to understand the basics of multimedia communications
2. Students understand Graphics and Image Representation, Fundamental Concepts in Video,
- 3 .Students understand basics of Digital Audio, Lossless Compression Algorithms, Lossey Compression Algorithm, Image Compression Standards
4. Students will be able perform MPEG Video Coding.

COURSE OUTCOME TO PROGRAM OUTCOME MAPPING:-

PO	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO1 0	PO1 1	PO1 2	PSO 1	PSO 2	PSO 3
CO 1	*	*	*	*	*	*								*	*
CO 2	*	*	*		*	*							*		*
CO 3	*	*	*	*	*	*								*	
CO 4	*	*	*	*										*	*

UNIT-I

Introduction to Multimedia: What is multimedia, Multimedia and Hypermedia, WWW

Graphics and Image Representation: Graphics/ Image data types, popular file formats.

Fundamental Concepts in Video: Types of video Signals, Analog video, Digital video.

Basics of Digital Audio: Digitization of sound, MIDI, Quantization and Transmission of Audio.

9 Hours

UNIT II

Lossless Compression Algorithms: Introduction, Run-length coding, variable- length coding, Dictionary-Based coding, Arithmetic coding, lossless image compression. **9 Hours**

UNIT III

Lossy Compression Algorithm: Introduction, Distortion measures, rate distortion theory, Quantization, Transform coding, Wavelet-Based coding, embedded zero tree wavelet coefficients, SPIHT. **9 Hours**

UNITIV

Image Compression Standards: The JPEG standard, The JPEG2000 standard, JPEG LS standard, JBIG. **9Hours**

UNITV

MPEG Video Coding: Basic video compression techniques-H.261, MPEG-1, MPEG-2, MPEG-4. **9Hours**

TEXT BOOKS:

1. "Fundamentals of Multimedia" – Ze-Nian Li and Mark S. Drew. Pearson Education 2004.
 - Unit - I : 1.1, 1.2, 1.3, 3.1, 3.2, 5.1, 5.2, and 5.3
 - Unit - II : 7.1, 7.3, 7.4, 7.5, 7.6, 7.7
 - Unit – III: 8.1 - 8.9
 - Unit – IV: 9.1 - 9.4
- Unit- V : 10.1 - 10.4, 11.2, 11.3, 12.1, 12.2, 12.3, 12.4