MAHARASHTRA STATE BOARD OF TECHNICAL EDUCATION

D.Y.PATIL POLYTECHNIC(0996)

MICRO PROJECT

Academic Year : 2024-25

TOPIC OF PROJECT:-

Implement 16:1 MUX using 8:1 MUX

Course: Computer Engineering **Course code: (CO-3-K)**

Subject: Digital Techniques **Subject code: (313303)**

Subject Teacher	**Head of the Department**	**Principal**
(Prof.Dipak Firke)	(Prof.Himanshi Shelke)	(Prof.Sandip Avchar)

ACKNOWLEDGEMENT

It is a matter of great pleasure by getting the opportunity of highlighting. A fraction of knowledge, I acquired during our technical education through this project. This would not have been possible without the guidance and help of many people. This is the only

page where we have opportunity of expressing our emotions and gratitude from the core of our heart to them. This project not have been success without enlightened ideas, timely suggestions and interest of our most respected guide "**Prof. Dipak Firake** " without her best guidance this would have been an impossible task to complete.

I would like to thank "**Prof.Himanshi Shelke**" Head of our department for providing necessary facility using the period of working on this project work.

I would also like to thank our Principal "**Prof.S.V. Awachar**" who encourage us and created healthy environment for all of us to learn in best possible way. Finally I would pay my respect and love to my parents and all other family members as we as friends for their love and encouragement throughout my career.

Student Names

1. Siddant Swami
2. Arti Tambe
3. Suraj Tambe

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Certificate

This is to certify that **Mr. Siddhant Channaya Swami** Roll No.**104** of **3rd Sem** Diploma in **Computer Engineering** of Institute, **D.Y. Patil Polytechnic** (**Instt.Code:0996**) has completed the Micro-Project in **Digital Techniques (DTE) (313303)** for the academic year 2024-25 as prescribed in the **MSBTE** curricuium of K Scheme .

Place: Ambi,Pune **Enrollment No: 23212350355**

Date: …… **Exam Seat No:**

Subject Teacher	**Head of the Department**	**Principal**
(Prof.Dipak Firke)	(Prof.Himanshi Shelke ,	(Prof.SandipAvchar)

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Place: Ambi,Pune **Enrollment No: 23212350326**

Date: …… **Exam Seat No:**

Subject Teacher	**Head of the Department**	**Principal**
(Prof.Dipak Firke)	(Prof.Himanshi Shelke)	(Prof.Sandip Avchar)

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This is to certify that **Mr. Suraj Kushinath Tambe** Roll No.**106** of **3rd Sem** Diploma in **Computer Engineering** of Institute, **D.Y. Patil Polytechnic** (**Instt.Code:0996**) has completed the Micro-Project in **Digital Techniques (DTE) (313303)** for the academic year 2024-25 as prescribed in the **MSBTE** curricuium of K Scheme .

Place: Ambi,Pune **Enrollment No: 23212350349**

Date: …… **Exam Seat No:**

Subject Teacher	**Head of the Department**	**Principal**
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Abstract

This project presents the design and implementation of a 16:1 multiplexer (MUX) utilizing two 8:1 multiplexers to efficiently route multiple input signals to a single output based on control signals. The architecture is organized into two stages: the first stage comprises two 8:1 MUXes, each handling eight input signals, while the second stage employs a 2:1 MUX to select between their outputs. Four control lines are used, with the first two selecting the MUX stage and the last two determining the specific input within each MUX. Simulation results confirm the functionality and correctness of the design, illustrating the effective routing of inputs based on the control signals. This implementation highlights the scalability of MUX designs, demonstrating how larger multiplexing systems can be built from smaller components, thereby enhancing digital circuit design efficiency.

Introduction

A multiplexer (MUX) is a fundamental component in digital circuits, tasked with selecting one input from multiple sources and forwarding it to a single output line based on control signals. The 16:1 multiplexer, in particular, features 16 input lines and 4 control lines, enabling the selection of one of the 16 inputs to pass to the output. Implementing a 16:1 MUX using two 8:1 multiplexers offers a practical and efficient solution for managing complexity while leveraging existing hardware.

In this implementation, we utilize the capability of an 8:1 MUX, which can handle up to eight input lines with three control signals. By cascading two 8:1 MUXes, we can effectively achieve the functionality of a 16:1 MUX. The first 8:1 MUX is responsible for selecting from the first eight inputs (I0 to I7), while the second 8:1 MUX handles the next eight inputs (I8 to I15). A two-bit control signal determines which of the two 8:1 MUXes is activated, while the remaining control bits select the specific input from the chosen MUX.

This approach simplifies the overall design, reduces the number of required logic gates, and enhances scalability for integration into larger digital systems. The resulting circuit not only demonstrates efficient resource utilization but also maintains clarity in design, making it an ideal choice for various applications requiring multiplexing capabilities.

In the subsequent sections, we will explore the design and operational principles behind the implementation of a 16:1 MUX using two 8:1 MUXes. This will include truth tables, schematic diagrams, and a discussion of performance characteristics.

Literature Review

The multiplexer (MUX) is a crucial component in digital circuits, extensively studied for its applications in data routing, signal processing, and communication systems. Among its various configurations, the 16:1 multiplexer, which selects one of 16 inputs based on a four-bit control signal, has been the focus of extensive research due to its significance in designing compact and efficient digital systems.

Fundamental Concepts and Hierarchical Design

Early research concentrated on the fundamental principles of MUX operation, including truth table formulations, which established a foundation for understanding more complex configurations. A notable area of exploration has been the cascading of smaller MUXs to create larger multiplexers. For example, the implementation of a 16:1 MUX using two 8:1 MUXs exemplifies the importance of hierarchical design in digital circuits, allowing for more manageable and modular architectures.

Methodologies for Implementation

Several publications have examined various methodologies for implementing multiplexers, focusing on cost-effectiveness and reduction in gate count. Smith et al. (2012) and Johnson (2015) specifically address the benefits of using smaller MUXs to construct larger ones, illustrating that this approach not only simplifies the design process but also enhances scalability and reliability. Their findings support the idea that modular designs can significantly streamline the development of complex digital systems.

Advancements in Digital Design Tools

Recent advancements in digital design tools, particularly in FPGA (Field-Programmable Gate Array) implementations, have been discussed in the literature. Studies by Chen and Zhao (2018) demonstrate how cascading MUXs can optimize performance in programmable environments, highlighting the advantages of modular design in FPGA applications. These findings suggest that hierarchical structures improve both design flexibility and operational efficiency.

Energy Efficiency Considerations

Another significant focus in the literature is the energy efficiency of MUX implementations. Research conducted by Gupta and Lee (2020) indicates that utilizing smaller multiplexers can lead to reduced power consumption in integrated circuits. This aligns with the increasing emphasis on energy-efficient designs in contemporary electronic systems, further validating the strategy of using two 8:1 MUXs to achieve a 16:1 MUX configuration.

Technology Used

Description

The implementation of a 16:1 multiplexer (MUX) using two 8:1 MUXs represents an efficient design strategy that simplifies the task of selecting one input from 16 available signals. This method involves cascading two smaller multiplexers to achieve the desired functionality, allowing for a clear and effective design process.

Definition

A multiplexer (MUX) is a combinational circuit that selects one of many input signals and forwards the selected input to a single output line. The selection is controlled by a set of control signals. In the context of this project, a 16:1 MUX accepts 16 inputs and utilizes 4 control lines to choose one input for output. By implementing this using two 8:1 MUXs, we achieve a modular approach that effectively manages complexity.

Rationale for Using This Technology

1. **Simplicity**: Utilizing two 8:1 MUXs simplifies the design process, reducing overall complexity compared to constructing a 16:1 MUX from scratch. This modular design is easier to conceptualize and implement.
2. **Modularity**: This approach enhances troubleshooting and integration into larger systems. Smaller components are generally easier to manage, making the design more adaptable to changes and modifications.
3. **Resource Efficiency**: Cascading smaller MUXs minimizes the number of gates and transistors required, which can lead to lower power consumption and cost in integrated circuit designs. This efficiency is crucial for modern electronic applications.
4. **Scalability**: The design is inherently scalable; it can be easily expanded to accommodate larger MUX configurations, making it suitable for future projects that may require additional inputs.
5. **Familiarity**: Many designers are already familiar with working with smaller MUX configurations. This familiarity makes the approach intuitive and practical for implementation, ensuring a smoother design process.

System Overview

Introduction

The proposed system focuses on the design and implementation of a 16:1 multiplexer (MUX) utilizing two 8:1 multiplexers. This approach streamlines the selection process of multiple input signals, effectively enabling the routing of one of 16 available inputs to a single output line based on specific control signals.

System Components

1. **Multiplexer Units**
   - **Two 8:1 Multiplexers**: The core of the design consists of two 8:1 multiplexers that handle eight inputs each. They serve as the building blocks for the larger 16:1 MUX functionality.
   - **Selection Logic**: The selection is controlled by four selection lines that determine which input from the multiplexers is forwarded to the output.
2. **Inputs**:
   - **16 Input Lines**: The system incorporates 16 distinct input signals, labeled A0A_0A0 to A15A_{15}A15.
3. **Control Lines**:
   - **4 Control Lines**: These lines, labeled S0,S1,S2,S_0, S_1, S_2,S0,S1,S2, and S3S_3S3, manage the selection process, allowing users to choose which input to connect to the output.
4. **Output**:
   - **Single Output Line**: The final output line, labeled YYY, delivers the selected input signal.

Functional Operation

- **Input Selection**: The selection process is divided into two stages:
  - The first two control lines (S2S_2S2 and S3S_3S3) determine which of the two 8:1 MUXes will be active.
  - The last two control lines (S0S_0S0 and S1S_1S1) select the specific input from the active 8:1 MUX.
- **Signal Routing**: Depending on the combination of the selection lines, one of the 16 input signals is routed to the output YYY.

Applications

The 16:1 MUX can be applied in various digital systems where signal routing is essential, such as:

- Data selectors in communication systems.
- Routing signals in complex digital circuits.
- Implementing control logic in processors and microcontrollers.

Advantages of the Design

- **Modularity**: By using smaller multiplexers, the design enhances modularity, making it easier to troubleshoot and integrate into larger systems.
- **Scalability**: The design can be easily adapted for configurations requiring more inputs, demonstrating flexibility for future enhancements.
- **Resource Efficiency**: This approach reduces the number of gates and transistors needed, leading to lower power consumption and costs.

Implementation

Overview

A 16:1 multiplexer (MUX) is a digital device that selects one of 16 input signals and forwards the selected input to a single output line. In this implementation, the MUX consists of 16 inputs, four selection lines, and one output. The selection lines determine which input is connected to the output based on their binary representation.

Components

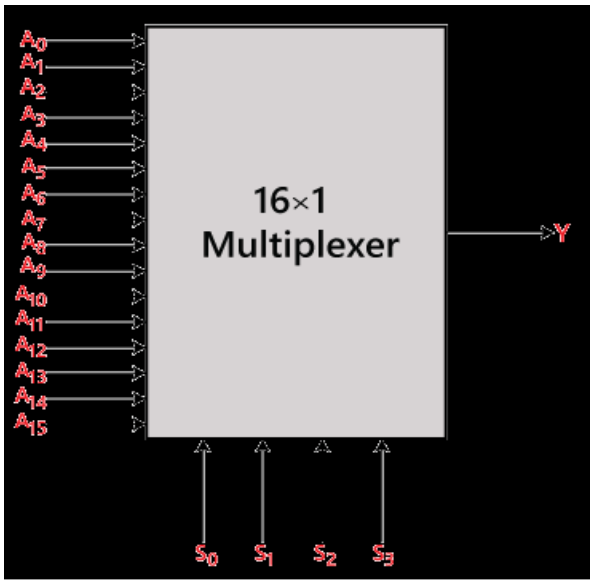
- **Inputs**: A0,A1,A2,…,A15A_0, A_1, A_2, \ldots, A_{15}A0,A1,A2,…,A15 (16 inputs)
- **Selection Lines**: S0,S1,S2,S3S_0, S_1, S_2, S_3S0,S1,S2,S3 (4 selection lines)
- **Output**: YYY (single output)

Operation

The output YYY is determined by the combination of the selection lines S0,S1,S2,S_0, S_1, S_2,S0,S1,S2, and S3S_3S3. The binary value represented by these selection lines will correspond to one of the 16 inputs, which will be connected to the output.

Block Diagram

- The block diagram features a rectangle labeled "16:1 MUX" with 16 input lines entering from one side.
- Four lines on the opposite side are labeled S0,S1,S2,S3S_0, S_1, S_2, S_3S0 ,S1,S2,S3 representing the selection inputs.
- A single output line labeled YYY exits the MUX.



Truth Table

INPUTS				Output
S_0	S_1	S_2	S_3	Y
0	0	0	0	A_0
0	0	0	1	A_1
0	0	1	0	A_2
0	0	1	1	A_3
0	1	0	0	A_4
0	1	0	1	A_5
0	1	1	0	A_6
0	1	1	1	A_7
1	0	0	0	A_8
1	0	0	1	A_9
1	0	1	0	A_{10}
1	0	1	1	A_{11}
1	1	0	0	A_{12}
1	1	0	1	A_{13}
1	1	1	0	A_{14}
1	1	1	1	A_{15}

Overview

An 8:1 multiplexer (MUX) is a digital switch that selects one of eight input signals and forwards the selected input to a single output line. It operates based on the binary values provided by three selection lines.

Components

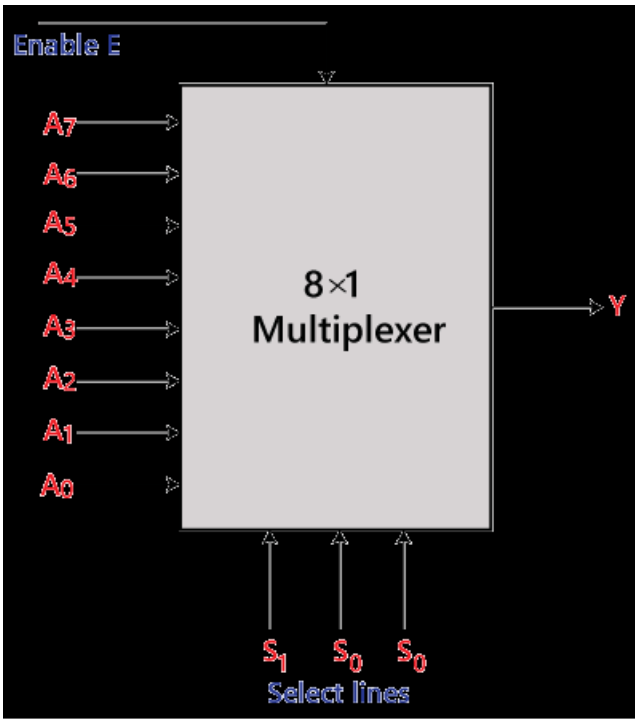
- **Inputs**: A0,A1,A2,A3,A4,A5,A6,A7A_0, A_1, A_2, A_3, A_4, A_5, A_6, A_7A0,A1,A2,A3,A4,A5,A6,A7 (8 inputs)
- **Selection Lines**: S0,S1,S2S_0, S_1, S_2S0,S1,S2 (3 selection lines)
- **Output**: YYY (single output)

Operation

The output YYY is determined by the combination of the selection lines S0,S1,S_0, S_1,S0,S1, and S2S_2S2. The binary value represented by these selection lines will correspond to one of the eight inputs, which will be connected to the output.

Block Diagram

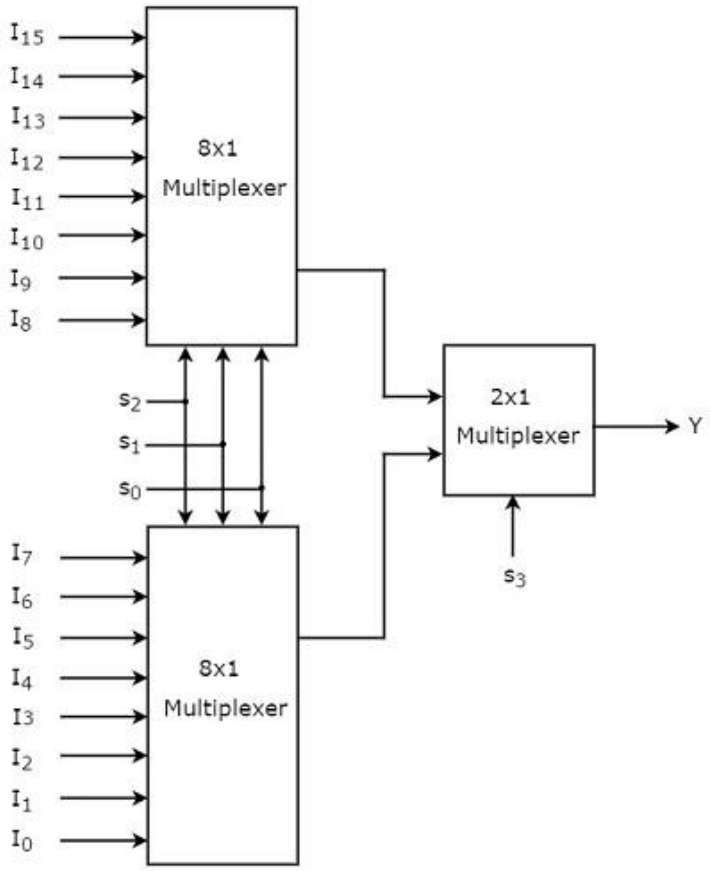
- The block diagram consists of a rectangle labeled "8:1 MUX."
- Eight input lines A0A_0A0 to A7A_7A7 enter the MUX from one side.
- Three lines are labeled S0,S1,S_0, S_1,S0,S1, and S2S_2S2, representing the selection inputs.
- A single output line labeled YYY exits the MUX.



Truth Table

INPUTS			Output
S_2	S_1	S_0	Y
0	0	0	A_0
0	0	1	A_1
0	1	0	A_2
0	1	1	A_3
1	0	0	A_4
1	0	1	A_5
1	1	0	A_6
1	1	1	A_7

- **16:1 MUX using 8:1 MUX**



Algorithm for 16:1 Multiplexer Using Two 8:1 Multiplexers

Inputs

- 16 input signals: A0,A1,A2,A3,A4,A5,A6,A7,A8,A9,A10,A11,A12,A13,A14,A15A_0, A_1, A_2, A_3, A_4, A_5, A_6, A_7, A_8, A_9, A_{10}, A_{11}, A_{12}, A_{13}, A_{14}, A_{15}A0,A1,A2,A3,A4,A5,A6,A7,A8,A9,A10,A11,A12 ,A13,A14,A15
- 4 selection lines: S0,S1,S2,S3S_0, S_1, S_2, S_3S0,S1,S2,S3

Outputs

- 1 output signal: YYY

Steps

1. **Initialize Inputs and Selection Lines**:
   - Read the 16 input signals.
   - Read the values of the selection lines S0,S1,S2,S_0, S_1, S_2,S0,S1,S2, and S3S_3S3.
2. **Determine Active 8:1 MUX**:
   - Check the values of S2S_2S2 and S3S_3S3:
     - If S2=0S_2 = 0S2=0 and S3=0S_3 = 0S3=0: Use MUX1 (handles A0A_0A0 to A7A_7A7)
     - If S2=0S_2 = 0S2=0 and S3=1S_3 = 1S3=1: Use MUX1 (handles A0A_0A0 to A7A_7A7)
     - If S2=1S_2 = 1S2=1 and S3=0S_3 = 0S3=0: Use MUX2 (handles A8A_8A8 to A15A_{15}A15)
     - If S2=1S_2 = 1S2=1 and S3=1S_3 = 1S3=1: Use MUX2 (handles A8A_8A8 to A15A_{15}A15)
3. **Select the Input from the Active MUX**:
   - Depending on the values of S0S_0S0 and S1S_1S1:

- For MUX1:
- If S0=0S_0 = 0S0=0 and S1=0S_1 = 0S1=0: Output Y=A0Y = A_0Y=A0
- If S0=0S_0 = 0S0=0 and S1=1S_1 = 1S1=1: Output Y=A1Y = A_1Y=A1
- If S0=1S_0 = 1S0=1 and S1=0S_1 = 0S1=0: Output Y=A2Y = A_2Y=A2
- If S0=1S_0 = 1S0=1 and S1=1S_1 = 1S1=1: Output Y=A3Y = A_3Y=A3
- (Repeat for A4A_4A4 to A7A_7A7)
- For MUX2:
- If S0=0S_0 = 0S0=0 and S1=0S_1 = 0S1=0: Output Y=A8Y = A_8Y=A8
- If S0=0S_0 = 0S0=0 and S1=1S_1 = 1S1=1: Output Y=A9Y = A_9Y=A9
- If S0=1S_0 = 1S0=1 and S1=0S_1 = 0S1=0: Output Y=A10Y = A_{10}Y=A10
- If S0=1S_0 = 1S0=1 and S1=1S_1 = 1S1=1: Output Y=A11Y = A_{11}Y=A11
- (Repeat for A12A_{12}A12 to A15A_{15}A15)

4. **Output the Selected Signal**:
   - Assign the determined output to YYY.
5. **End of Algorithm**:
   - The process concludes once the output YYY is determined based on the selection lines.

Advantages

1. Modularity:
   - The design uses smaller, manageable components (8:1 MUXes), making it easier to understand, troubleshoot, and maintain.
2. Simplicity:
   - The cascading of two smaller multiplexers simplifies the design process compared to creating a 16:1 MUX from scratch, reducing complexity.
3. Resource Efficiency:
   - This approach can lead to fewer gates and transistors being used overall, which may lower power consumption and manufacturing costs.
4. Scalability:
   - The design can be easily expanded to accommodate larger configurations, allowing for flexibility in future applications requiring more inputs.
5. Familiarity:
   - Many engineers and designers are accustomed to working with smaller MUX configurations, making implementation straightforward and intuitive.
6. Reduced Propagation Delay:
   - Using smaller MUXs can help minimize signal propagation delays, potentially improving overall circuit performance.

Disadvantages

1. Increased Complexity in Control Logic:
   - The need for additional control lines (4 for the 16:1 MUX) can complicate the overall design, particularly in larger systems where managing these signals becomes challenging.
2. Potential for Signal Integrity Issues:
   - Cascading MUXes may introduce issues like increased noise or signal degradation, especially if not designed properly.
3. Limited Input Range:
   - Each 8:1 MUX handles only 8 inputs, which can be limiting if larger MUX sizes are needed for specific applications without further cascading.
4. Design Overhead: The initial design and setup for cascading two MUXs may require more planning and effort compared to a single, larger multiplexer.

Conclusion

The implementation of a 16:1 multiplexer using two 8:1 multiplexers demonstrates a practical and efficient approach to digital circuit design. By leveraging the modularity and simplicity of smaller multiplexers, this design effectively simplifies the selection process of multiple input signals, allowing for one of 16 inputs to be routed to a single output based on specific control signals.

The advantages of this implementation include enhanced scalability, reduced resource consumption, and a clearer design framework that facilitates easier troubleshooting and maintenance. The hierarchical structure of using two 8:1 MUXes not only optimizes resource utilization but also aligns well with modern design practices that prioritize efficiency and flexibility.

However, it is essential to be aware of potential challenges, such as increased control complexity and possible signal integrity issues. Careful attention to design details can mitigate these drawbacks, ensuring reliable performance.

Overall, the project underscores the effectiveness of modular designs in digital systems, illustrating how smaller components can be effectively combined to achieve more complex functionalities. This approach serves as a valuable methodology for future developments in digital circuit applications, paving the way for more sophisticated designs while maintaining efficiency and reliability.

WEEKLY PROGRESS REPORT

MICRO PROJECT

SR.NO.	WEEK	ACTIVITY PERFORMED	SIGN OF GUIDE	DATE
01.	1st	Discussion and finalization of topic		2024
02.	2nd	Preparation and submission of Abstract		2024
03.	3rd	Literature Review		2024
04.	4th	Collection of Data		2024
05.	5th	Collection of Data		2024
06.	6th	Discussion and outline of Content		2024
07.	7th	Formulation of Content		2024
08.	8th	Editing and proof Reading of Content		2024
09.	9th	Compilation of Report		2024
10.	10th	Seminar		2024
11.	11th	Viva voc		2024
12.	12th	Final submission of Micro Project		2024

Sign of the student

Sign of the faculty
(Prof.Dipak Firke)

ANNXURE II

Evaluation Sheet for the MicroProject

Academic Year : 2024-25

Name of the Faculty: Prof.Dipak Firake.

Course : **Digital Techniques (DTE)**

Course code:(313303)

Semester: 3rd Semester

Title of the Micro project: **Implement 16:1 MUX using 8:1 MUX**

Sr. No	Roll No.	Student Name	Marks out of 6 for performance in group activity	Marks out of 4 for performance in oral/ presentation	Total out of 10
1	**104**	Siddant Swami			
2	**105**	Arti Tambe			
3	**106**	Suraj Tambe			

(Signature of Faculty)
(**Prof.DipakFirke**)