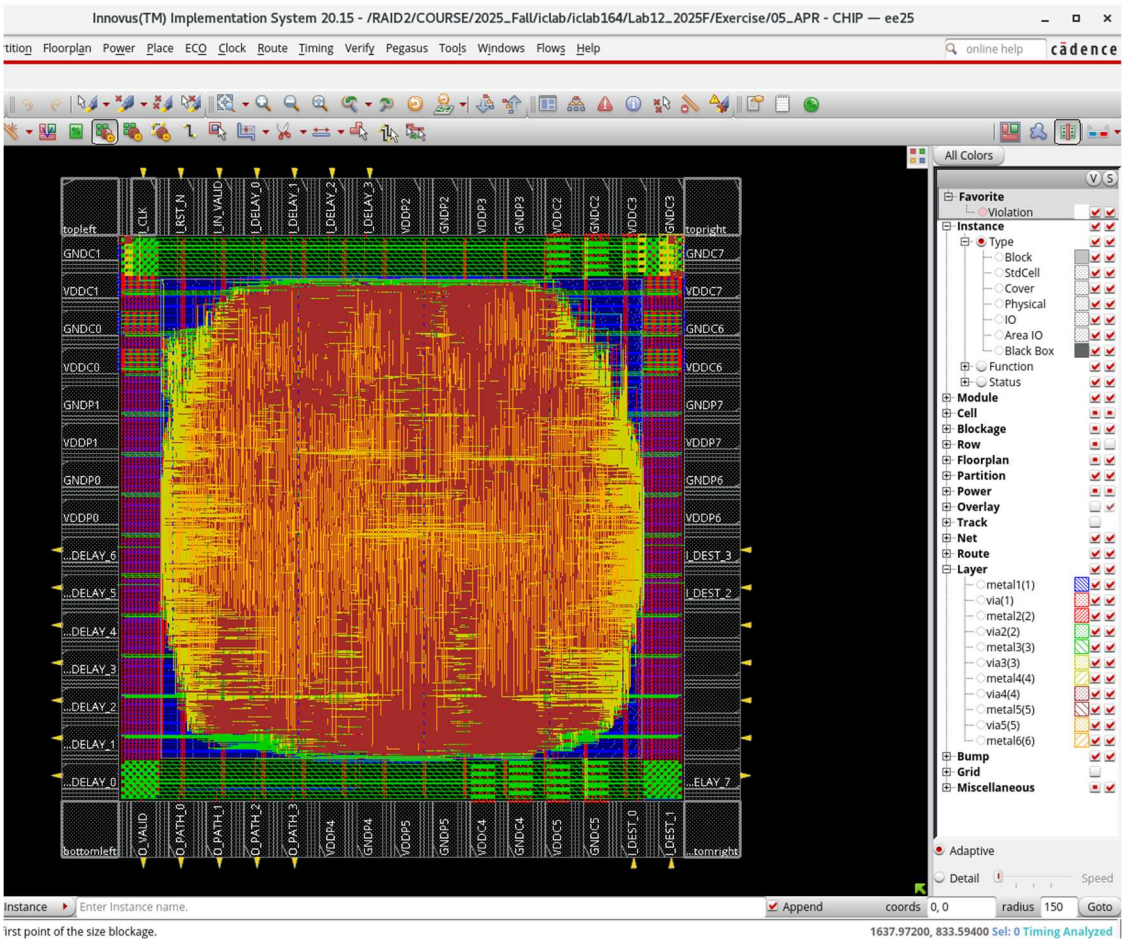
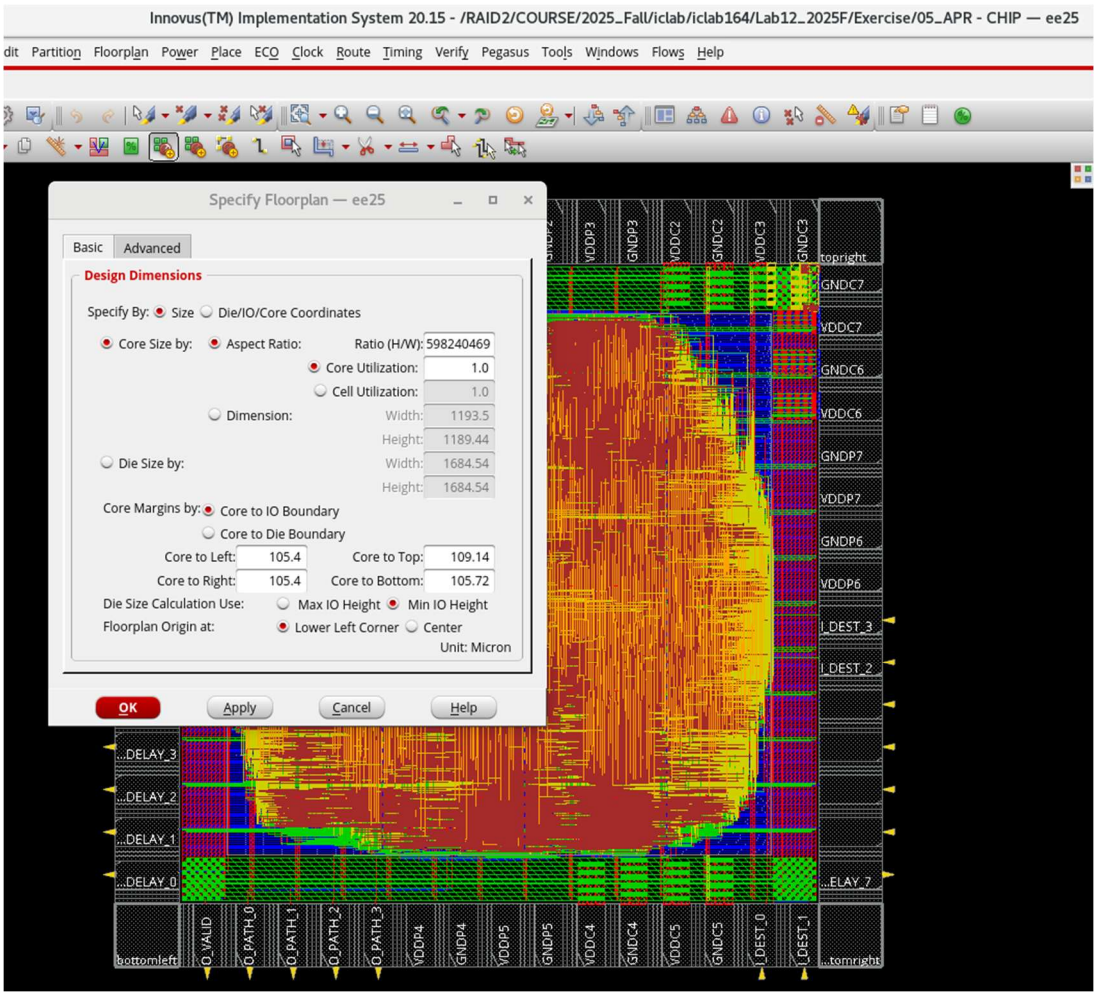
Report

iclab164

1. Chip Layout View :



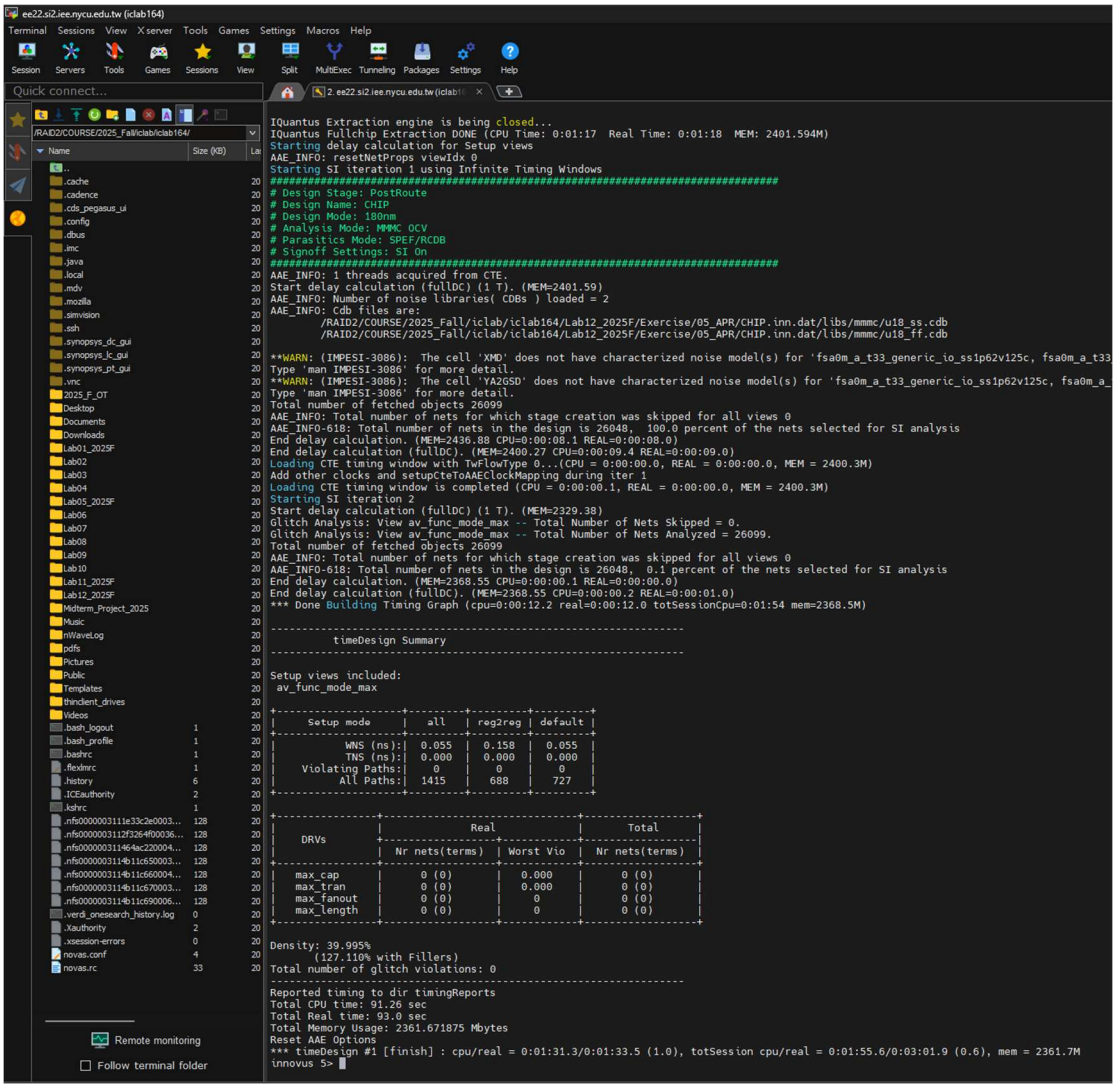
2. Core to IO boundary :



3. Core Ring :

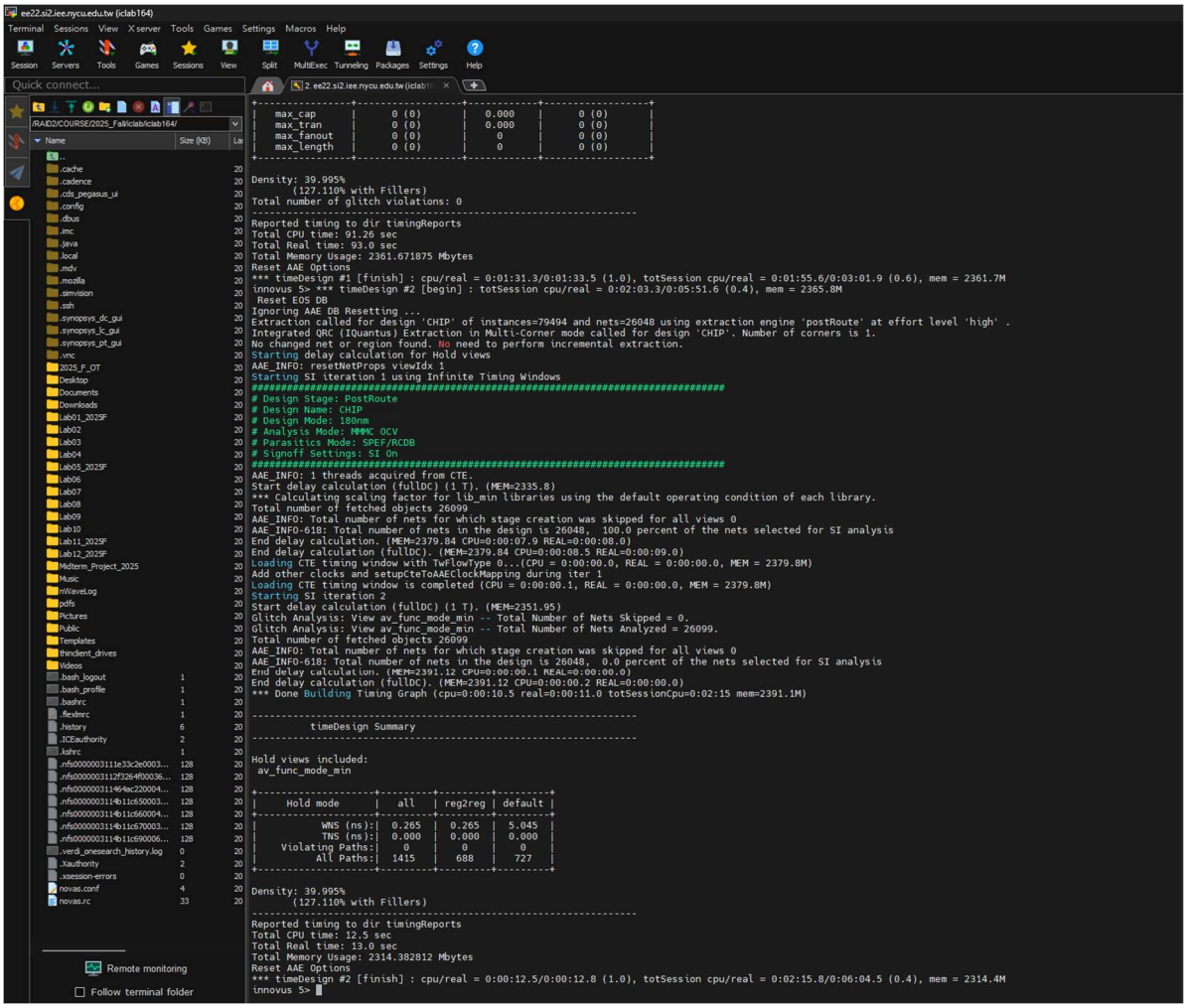

Innovus(TM) Implementation System 20.15 - /RAID2/COURSE/2025_Fall/iclab/iclab164/Lab12_2025F/Exercise/05_APR - CHIP — ee25
Floorplan Power Place ECO Clock Route Timing Verify Pegasus Tools Windows Flows Help
GND
VCC
total=9.00
Enter Instance name.
Append
coords

4. Post-Route setup time analysis :

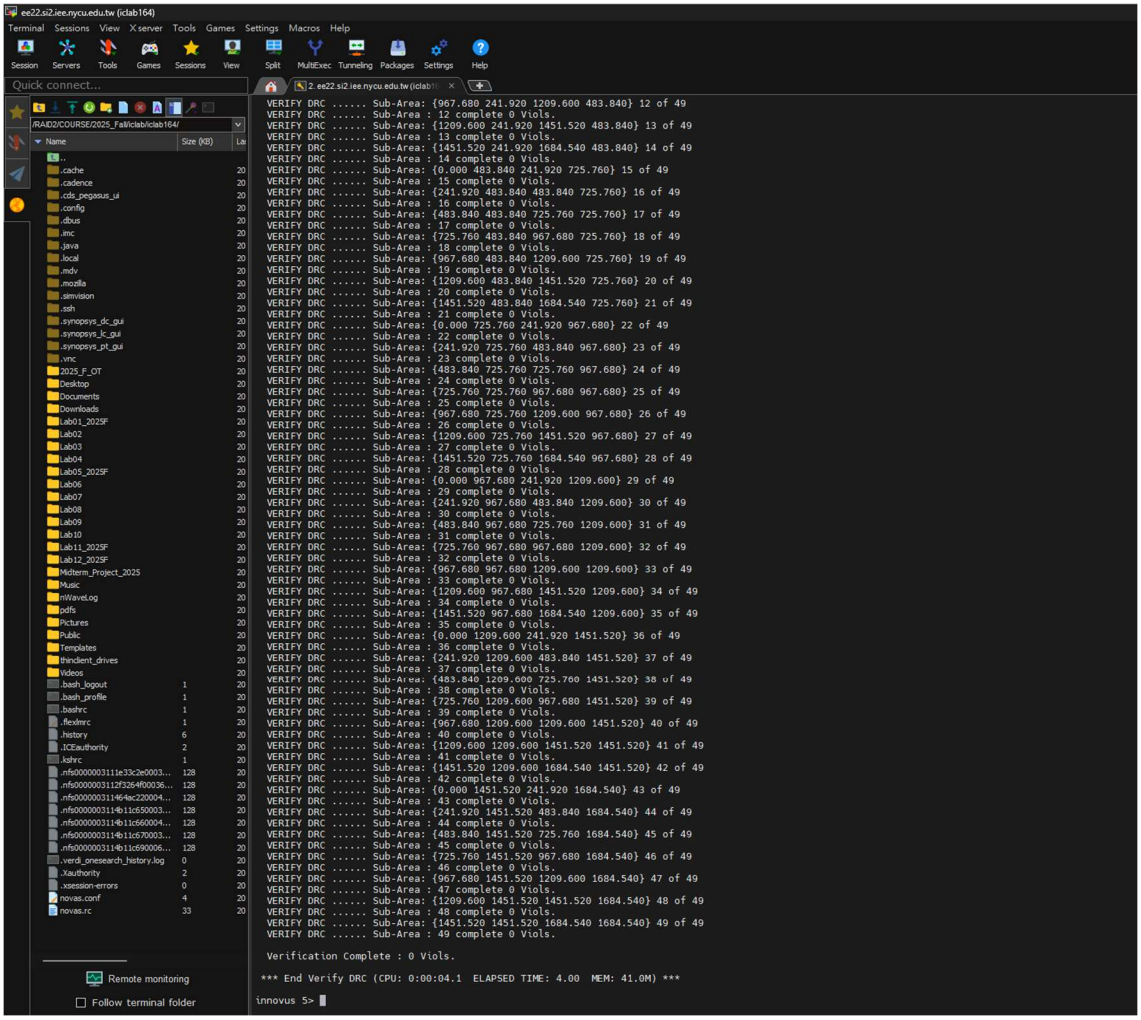


5. Post-Route hold time analysis :

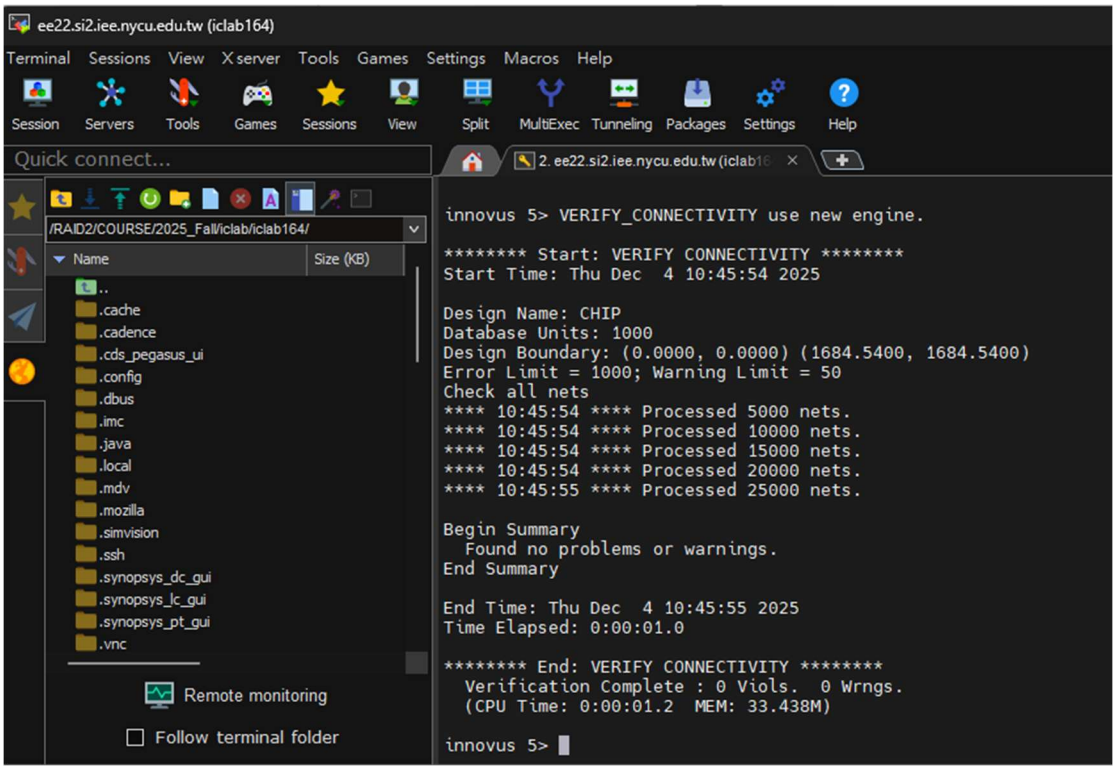
Instructions: After completing the analysis, capture a screenshot of the results displayed in the terminal (including the timeDesign Summary).



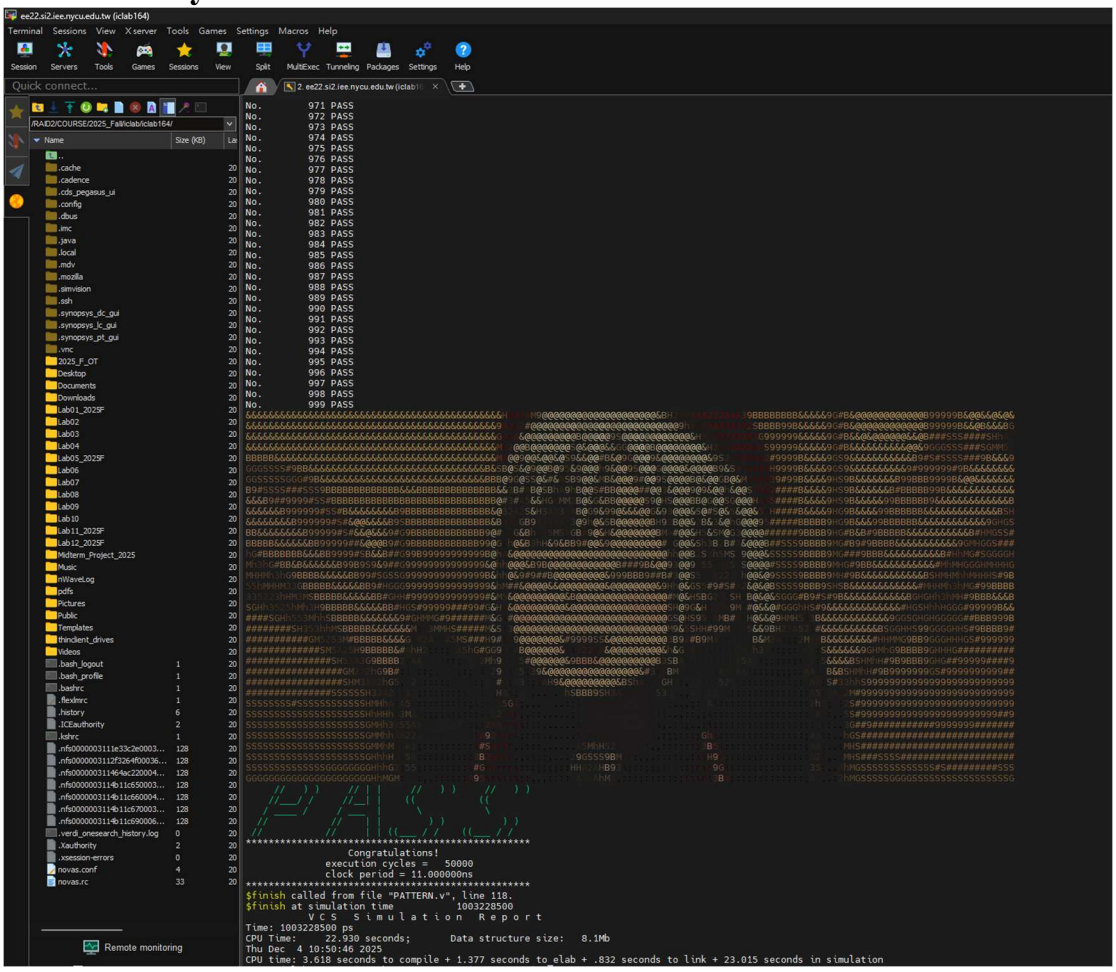
6. DRC result :


ee22.si2.iee.nycu.edu.tw (iclab164)
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
Quick connect...
/RAID2/COURSE/2025_Fall/iclab/iclab164/
Name Size (KB)
Remote monitoring
Follow terminal folder
VERIFY DRC ..... Sub-Area: {967.680 241.920 1209.600 483.840} 12 of 49
VERIFY DRC ..... Sub-Area : 12 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1209.600 241.920 1451.520 483.840} 13 of 49
VERIFY DRC ..... Sub-Area : 13 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1451.520 241.920 1684.540 483.840} 14 of 49
VERIFY DRC ..... Sub-Area : 14 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 483.840 241.920 725.760} 15 of 49
VERIFY DRC ..... Sub-Area : 15 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {241.920 483.840 483.840 725.760} 16 of 49
VERIFY DRC ..... Sub-Area : 16 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {483.840 483.840 725.760 725.760} 17 of 49
VERIFY DRC ..... Sub-Area : 17 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {725.760 483.840 967.680 725.760} 18 of 49
VERIFY DRC ..... Sub-Area : 18 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {967.680 483.840 1209.600 725.760} 19 of 49
VERIFY DRC ..... Sub-Area : 19 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1209.600 483.840 1451.520 725.760} 20 of 49
VERIFY DRC ..... Sub-Area : 20 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1451.520 483.840 1684.540 725.760} 21 of 49
VERIFY DRC ..... Sub-Area : 21 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 725.760 241.920 967.680} 22 of 49
VERIFY DRC ..... Sub-Area : 22 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {241.920 725.760 483.840 967.680} 23 of 49
VERIFY DRC ..... Sub-Area : 23 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {483.840 725.760 725.760 967.680} 24 of 49
VERIFY DRC ..... Sub-Area : 24 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {725.760 725.760 967.680 967.680} 25 of 49
VERIFY DRC ..... Sub-Area : 25 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {967.680 725.760 1209.600 967.680} 26 of 49
VERIFY DRC ..... Sub-Area : 26 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1209.600 725.760 1451.520 967.680} 27 of 49
VERIFY DRC ..... Sub-Area : 27 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1451.520 725.760 1684.540 967.680} 28 of 49
VERIFY DRC ..... Sub-Area : 28 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 967.680 241.920 1209.600} 29 of 49
VERIFY DRC ..... Sub-Area : 29 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {241.920 967.680 483.840 1209.600} 30 of 49
VERIFY DRC ..... Sub-Area : 30 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {483.840 967.680 725.760 1209.600} 31 of 49
VERIFY DRC ..... Sub-Area : 31 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {725.760 967.680 967.680 1209.600} 32 of 49
VERIFY DRC ..... Sub-Area : 32 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {967.680 967.680 1209.600 1209.600} 33 of 49
VERIFY DRC ..... Sub-Area : 33 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1209.600 967.680 1451.520 1209.600} 34 of 49
VERIFY DRC ..... Sub-Area : 34 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1451.520 967.680 1684.540 1209.600} 35 of 49
VERIFY DRC ..... Sub-Area : 35 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 1209.600 241.920 1451.520} 36 of 49
VERIFY DRC ..... Sub-Area : 36 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {241.920 1209.600 483.840 1451.520} 37 of 49
VERIFY DRC ..... Sub-Area : 37 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {483.840 1209.600 725.760 1451.520} 38 of 49
VERIFY DRC ..... Sub-Area : 38 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {725.760 1209.600 967.680 1451.520} 39 of 49
VERIFY DRC ..... Sub-Area : 39 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {967.680 1209.600 1209.600 1451.520} 40 of 49
VERIFY DRC ..... Sub-Area : 40 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1209.600 1209.600 1451.520 1451.520} 41 of 49
VERIFY DRC ..... Sub-Area : 41 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1451.520 1209.600 1684.540 1451.520} 42 of 49
VERIFY DRC ..... Sub-Area : 42 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 1451.520 241.920 1684.540} 43 of 49
VERIFY DRC ..... Sub-Area : 43 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {241.920 1451.520 483.840 1684.540} 44 of 49
VERIFY DRC ..... Sub-Area : 44 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {483.840 1451.520 725.760 1684.540} 45 of 49
VERIFY DRC ..... Sub-Area : 45 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {725.760 1451.520 967.680 1684.540} 46 of 49
VERIFY DRC ..... Sub-Area : 46 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {967.680 1451.520 1209.600 1684.540} 47 of 49
VERIFY DRC ..... Sub-Area : 47 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1209.600 1451.520 1451.520 1684.540} 48 of 49
VERIFY DRC ..... Sub-Area : 48 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1451.520 1451.520 1684.540 1684.540} 49 of 49
VERIFY DRC ..... Sub-Area : 49 complete 0 Viols.
Verification Complete : 0 Viols.
*** End Verify DRC (CPU: 0:00:04.1 ELAPSED TIME: 4.00 MEM: 41.0M) ***
innovus 5>

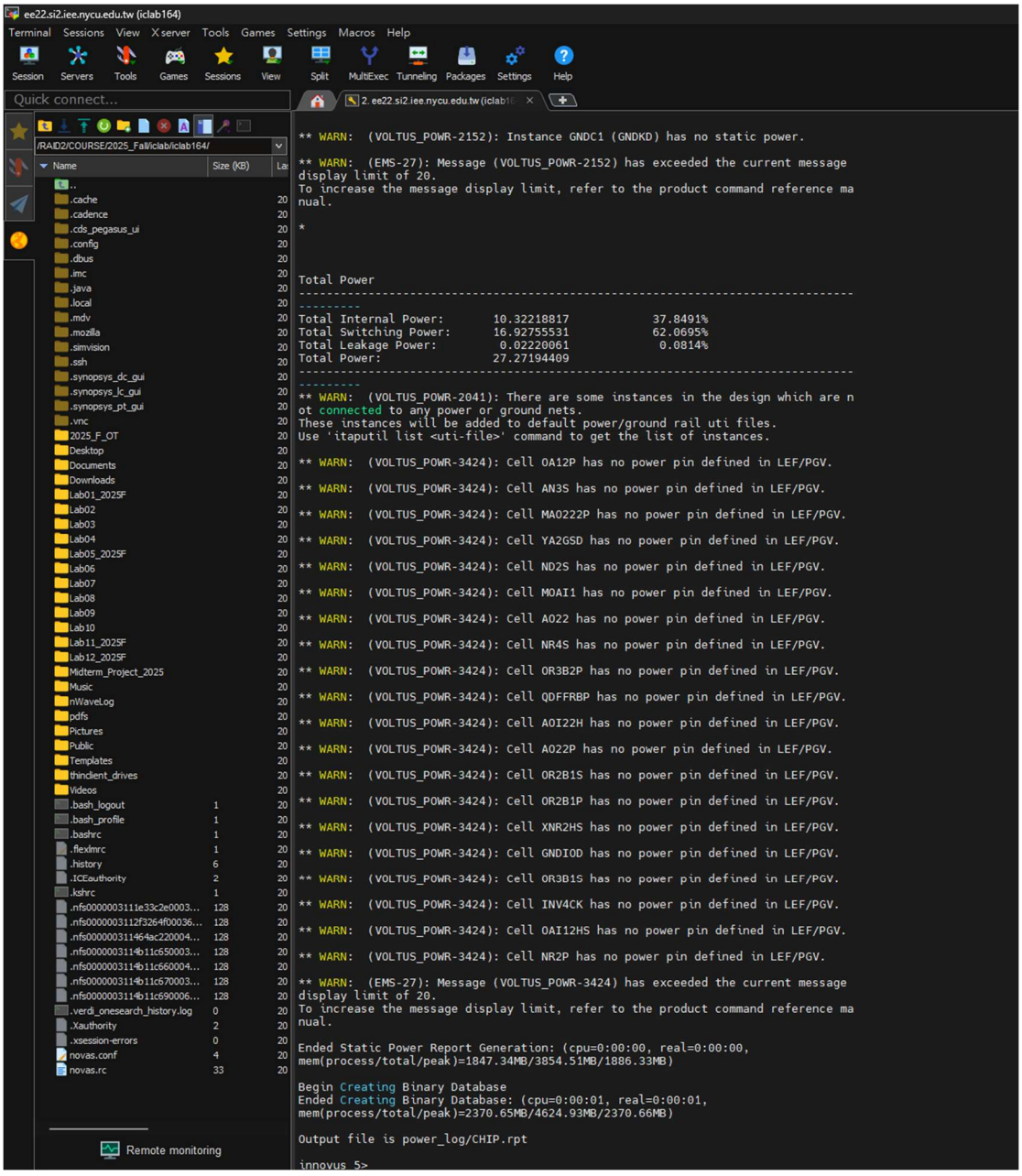
7. LVS result :


ee22.si2.iee.nycu.edu.tw (iclab164)
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
Quick connect...
2. ee22.si2.iee.nycu.edu.tw (iclab16
/RAID2/COURSE/2025_Fall/iclab/iclab164/
Name
Size (KB)
..
.cache
.cadence
.cds_pegasus_ui
.config
.dbus
.imc
.java
.local
.mdv
.mozilla
.simvision
.ssh
.synopsys_dc_gui
.synopsys_lc_gui
.synopsys_pt_gui
.vnc
Remote monitoring
Follow terminal folder
innovus 5> VERIFY_CONNECTIVITY use new engine.
******** Start: VERIFY CONNECTIVITY ********
Start Time: Thu Dec 4 10:45:54 2025
Design Name: CHIP
Database Units: 1000
Design Boundary: (0.0000, 0.0000) (1684.5400, 1684.5400)
Error Limit = 1000; Warning Limit = 50
Check all nets
**** 10:45:54 **** Processed 5000 nets.
**** 10:45:54 **** Processed 10000 nets.
**** 10:45:54 **** Processed 15000 nets.
**** 10:45:54 **** Processed 20000 nets.
**** 10:45:55 **** Processed 25000 nets.
Begin Summary
Found no problems or warnings.
End Summary
End Time: Thu Dec 4 10:45:55 2025
Time Elapsed: 0:00:01.0
******** End: VERIFY CONNECTIVITY ********
Verification Complete : 0 Viols. 0 Wrngs.
(CPU Time: 0:00:01.2 MEM: 33.438M)
innovus 5>

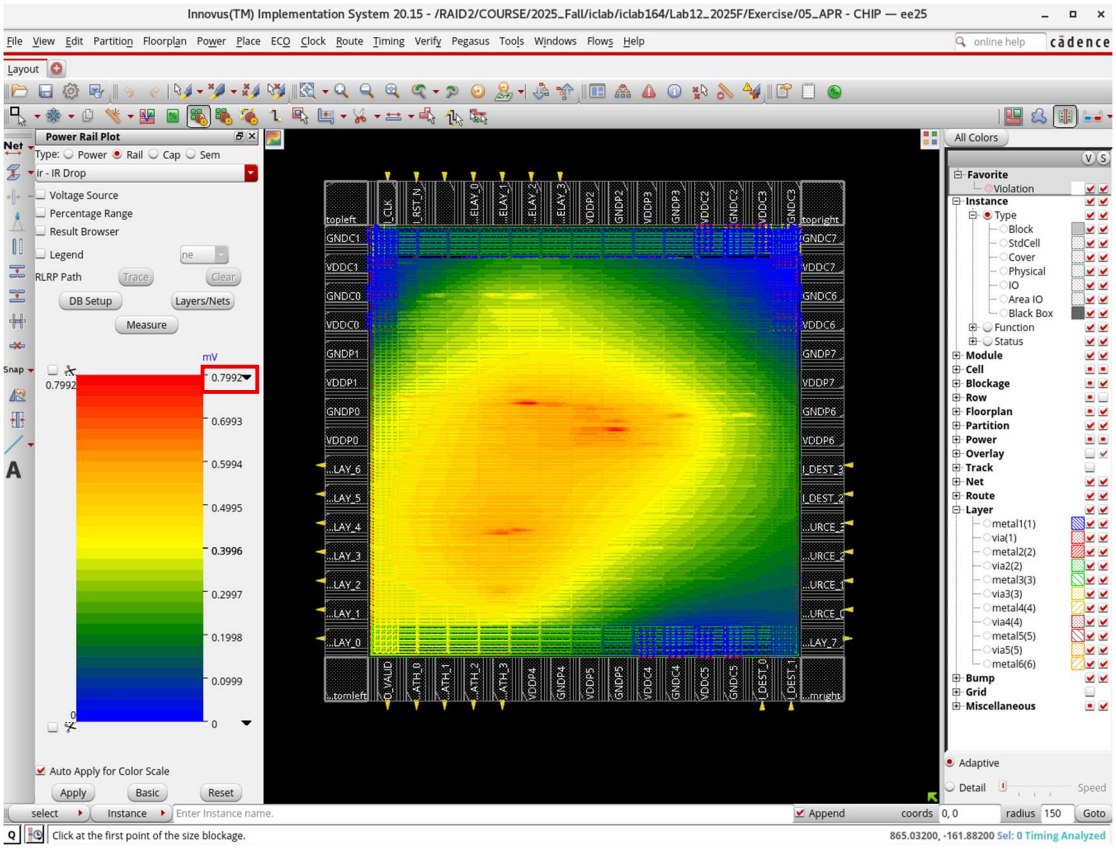
8. Post Layout simulation result :



9. Power result :



10. IR Drop Results :



IR drop 最大值為 **0.7992 mV** < 1 mV < 0.1 V

增加更多 power pad / ring / stripe 等可以改善 IR drop。
跟 Lab11 相比，在 Lab 12 我用了兩倍的 power pad。