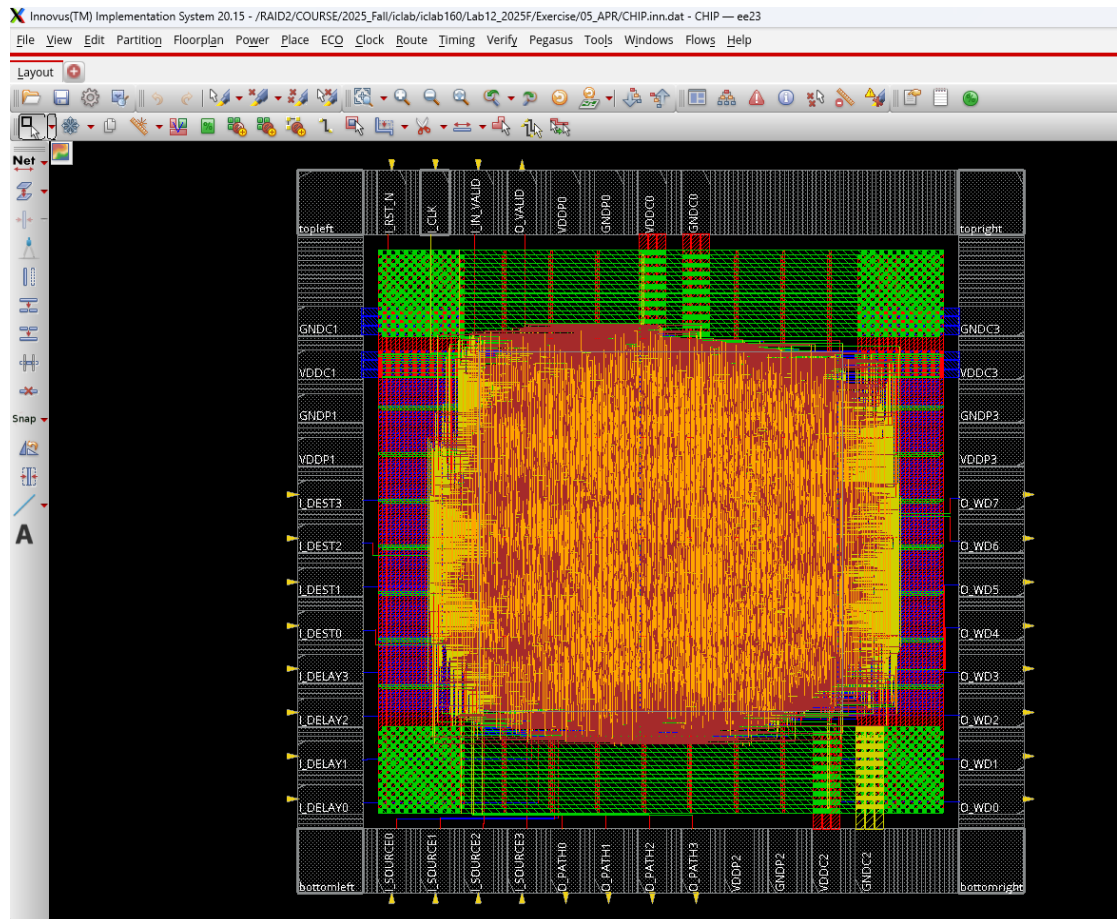


# Report

## Iclab160

### 1. Chip Layout View :

Instructions: After completing the final layout, capture a screenshot of the entire chip layout.



### 2. Core to IO boundary :



```
RAID2/COURSE/2025_Fall/iclab/iclab160/Lab12_2025F/Exercise05_APR/
Name Size (KB) Last modified
..
cadence 2025-12-03 14:05
CellC 2025-05-28 01:25
CHP_arn.dat 2025-12-03 16:03
CHP_placement.arn.dat 2025-12-03 15:33
CHP_postCTS.arn.dat 2025-12-03 15:37
CHP_pp.arn.dat 2025-12-03 15:24
client_log 2025-12-03 15:57
dnd 2025-05-28 01:25
DSS 2025-12-03 15:36
extlogDir 2025-12-03 15:51
layermap 2025-05-28 01:25
LEF 2025-05-28 01:25
LIB 2025-05-28 01:25
log 2025-05-28 01:25
PD_25C_avg_1 2025-12-03 16:22
power_log 2025-12-03 16:26
RC 2025-05-28 01:25
SummaryReport 2025-12-03 15:59
TimingReports 2025-12-03 15:59
work 2025-12-03 16:26
iclab160_launch_209905_0 13 2025-12-03 16:22
iclab160_launch_209905_1 13 2025-12-03 16:22
iclab160_launch_215025_0 13 2025-12-03 16:26
iclab160_launch_215025_1 13 2025-12-03 16:26
nano_eco_dedolist 1 2025-12-03 15:48
qor_metric.tcl 1 2025-12-03 16:26
timing_file_64003.tff.gz 1 889 2025-12-03 15:42
00_combine 1 2025-05-28 01:25
01_setupenv 1 2025-05-28 01:25
09_clean_up 1 2025-05-28 01:25
2_cellIDMap 1 2025-12-03 16:26
CHP.COOPT.spec 2 2025-12-03 15:33
CHP.comn.rpt 1 2025-12-03 16:00
CHP.comn.rpt.old 1 2025-12-03 15:24
CHP.drc.rpt 1 2025-12-03 16:00
CHP.drc.rpt.old 1 2025-12-03 15:24
CHP.globals 134 2025-12-03 15:08
CHP.inn 1 2025-12-03 16:03
CHP.ip 3 2025-12-03 15:12
CHP.sdc 8 2025-05-28 01:25
CHP.ssf 22 313 2025-12-03 16:00
CHP.v 2 771 2025-12-03 16:00

Total Leakage Power: 0.02248542 0.6776%
Total Power: 28.98173933
-----
Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00,
mem(process/total/peak)=2094.6GB/4099.51MB/2094.73MB)

Output file is power_log/CHIP.rpt
innovus > pvd
/RAID2/COURSE/2025_Fall/iclab/iclab160/Lab12_2025F/Exercise05_APR
innovus > *** timeDesign #2 [begin] : totSession cpu/real = 0:03:43.7/0:30:16.1 (0.1), mem = 2901.8M
Reset EOS DB
Ignoring AAE DB Resetting ...
Extraction called for design 'CHIP' of instances=33918 and nets=26135 using extraction engine 'postRoute' at effort level 'high'.
Integrated QRC (IQuantus) Extraction in Multi-Corner mode called for design 'CHIP'. Number of corners is 1.
No changed net or region found. No need to perform incremental extraction.

-----
timeDesign Summary
-----
Setup views included:
av_func_mode_max
-----
| Setup mode | all | reg2reg | default |
|-----|-----|-----|-----|
| WNS (ns): | 0.023 | 0.023 | 0.043 |
| TNS (ns): | 0.000 | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 | 0 |
| All Paths: | 1415 | 688 | 727 |
-----

|-----|-----|-----|-----|
| DRVs | | Real | | Total |
|-----|-----|-----|-----|
| | Nr nets (terms) | Worst Vio | Nr nets (terms) |
|-----|-----|-----|-----|
| max_cap | 0 (0) | 0.000 | 0 (0) |
| max_tran | 0 (0) | 0.000 | 0 (0) |
| max_fanout | 0 (0) | 0 | 0 (0) |
| max_length | 0 (0) | 0 | 0 (0) |
|-----|-----|-----|-----|

Density: 94.730%
(128.354% with Fillers)
Total number of glitch violations: 0
-----
Reported timing to dir timingReports
Total CPU time: 2.93 sec
Total Real time: 4.0 sec
Total Memory Usage: 2841.109375 Mbytes
Reset AAE Options
*** timeDesign #2 [finish] : cpu/real = 0:00:02.9/0:00:04.6 (0.6), totSession cpu/real = 0:03:46.6/0:30:20.7 (0.1), mem = 2841.1M
innovus >
```

## 5. Post-Route hold time analysis :

```
RAID2/COURSE/2025_Fall/iclab/iclab160/Lab12_2025F/Exercise05_APR/
Name Size (KB) Last modified
..
cadence 2025-12-03 14:05
CellC 2025-05-28 01:25
CHP_arn.dat 2025-12-03 16:03
CHP_placement.arn.dat 2025-12-03 15:33
CHP_postCTS.arn.dat 2025-12-03 15:37
CHP_pp.arn.dat 2025-12-03 15:24
client_log 2025-12-03 15:57
dnd 2025-05-28 01:25
DSS 2025-12-03 15:36
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LEF 2025-05-28 01:25
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log 2025-05-28 01:25
PD_25C_avg_1 2025-12-03 16:22
power_log 2025-12-03 16:26
RC 2025-05-28 01:25
SummaryReport 2025-12-03 15:59
TimingReports 2025-12-03 15:59
work 2025-12-03 16:26
iclab160_launch_209905_0 13 2025-12-03 16:22
iclab160_launch_209905_1 13 2025-12-03 16:22
iclab160_launch_215025_0 13 2025-12-03 16:26
iclab160_launch_215025_1 13 2025-12-03 16:26
nano_eco_dedolist 1 2025-12-03 15:48
qor_metric.tcl 1 2025-12-03 16:26
timing_file_64003.tff.gz 1 889 2025-12-03 15:42
00_combine 1 2025-05-28 01:25
01_setupenv 1 2025-05-28 01:25
09_clean_up 1 2025-05-28 01:25
2_cellIDMap 1 2025-12-03 16:26
CHP.COOPT.spec 2 2025-12-03 15:33
CHP.comn.rpt 1 2025-12-03 16:00
CHP.comn.rpt.old 1 2025-12-03 15:24
CHP.drc.rpt 1 2025-12-03 16:00
CHP.drc.rpt.old 1 2025-12-03 15:24
CHP.globals 134 2025-12-03 15:08
CHP.inn 1 2025-12-03 16:03
CHP.ip 3 2025-12-03 15:12
CHP.sdc 8 2025-05-28 01:25
CHP.ssf 22 313 2025-12-03 16:00
CHP.v 2 771 2025-12-03 16:00

Starting SI iteration 1 using Infinite Timing Windows
#####
# Design Stage: PostRoute
# Design Name: CHIP
# Design Mode: 180nm
# Analysis Mode: MMWC_OCV
# Parasitics Mode: SPEF/RCDB
# Signoff Settings: SI On
#####
AAE_INFO: 1 threads acquired from CTE.
Start delay calculation (fullDC) (1 T). (MEM=2813.28)
*** Calculating scaling factor for lib_min libraries using the default operating condition of each library.
Total number of fetched objects 26179
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
AAE_INFO-618: Total number of nets in the design is 26135, 100.0 percent of the nets selected for SI analysis
End delay calculation (fullDC). (MEM=2833.3 CPU=0:00:07.0 REAL=0:00:07.0)
Loading CTE timing window with TwFlowType 0... (CPU = 0:00:00.0, REAL = 0:00:00.0, MEM = 2833.3M)
Add other clocks and setup to the AEClockMapping during iter 1
Loading CTE timing window is completed (CPU = 0:00:00.1, REAL = 0:00:00.0, MEM = 2833.3M)
Starting SI iteration 2
Start delay calculation (fullDC) (1 T). (MEM=2805.42)
Glitch Analysis: View av_func_mode_min -- Total Number of Nets Skipped = 0.
Glitch Analysis: View av_func_mode_min -- Total Number of Nets Analyzed = 26179.
Total number of fetched objects 26179
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
AAE_INFO-618: Total number of nets in the design is 26135, 0.0 percent of the nets selected for SI analysis
End delay calculation (fullDC). (MEM=2845.59 CPU=0:00:00.1 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=2845.59 CPU=0:00:00.1 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:10.5 real=0:00:10.0 totSessionCpu=0:04:00 mem=2845.6M)

-----
timeDesign Summary
-----
Hold views included:
av_func_mode_min
-----
| Hold mode | all | reg2reg | default |
|-----|-----|-----|-----|
| WNS (ns): | 0.260 | 0.260 | 5.046 |
| TNS (ns): | 0.000 | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 | 0 |
| All Paths: | 1415 | 688 | 727 |
-----

Density: 94.730%
(128.354% with Fillers)
-----
Reported timing to dir timingReports
Total CPU time: 12.68 sec
Total Real time: 15.0 sec
Total Memory Usage: 2768.859375 Mbytes
Reset AAE Options
*** timeDesign #3 [finish] : cpu/real = 0:00:12.7/0:00:13.1 (1.0), totSession cpu/real = 0:04:00.7/0:31:06.2 (0.1), mem = 2768.9M
```

## 6. DRC result :





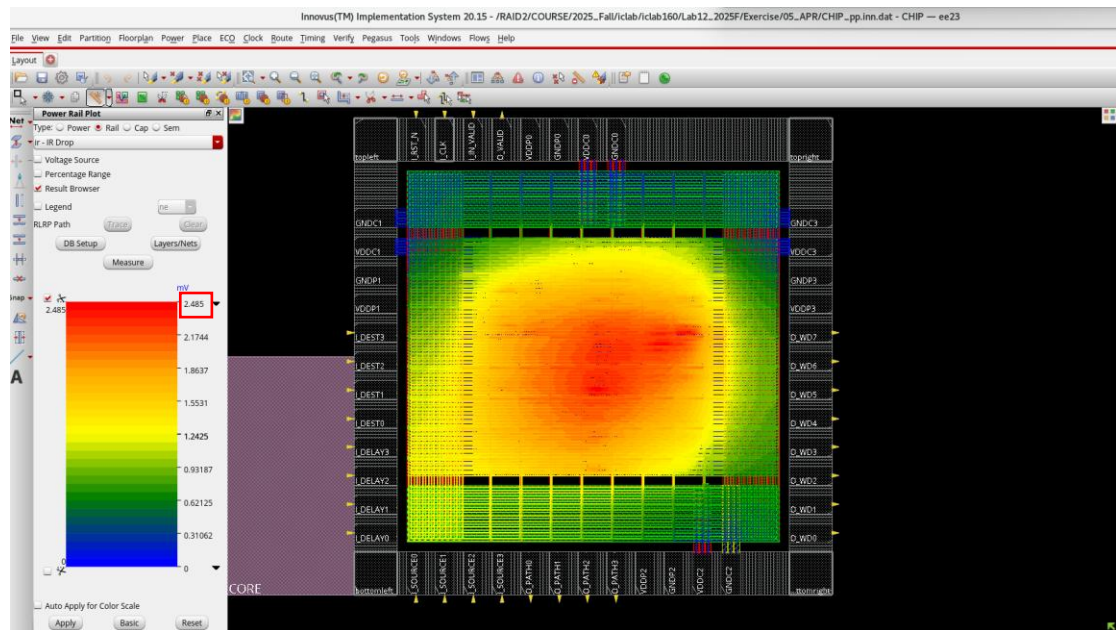
## 8. Post Layout simulation result :

8. Post Layout simulation result :

## 9. Power result :

9. Power result :

## 10. IR Drop Results :



I use more power pads, and more power rails to reduce the IR drop issue.