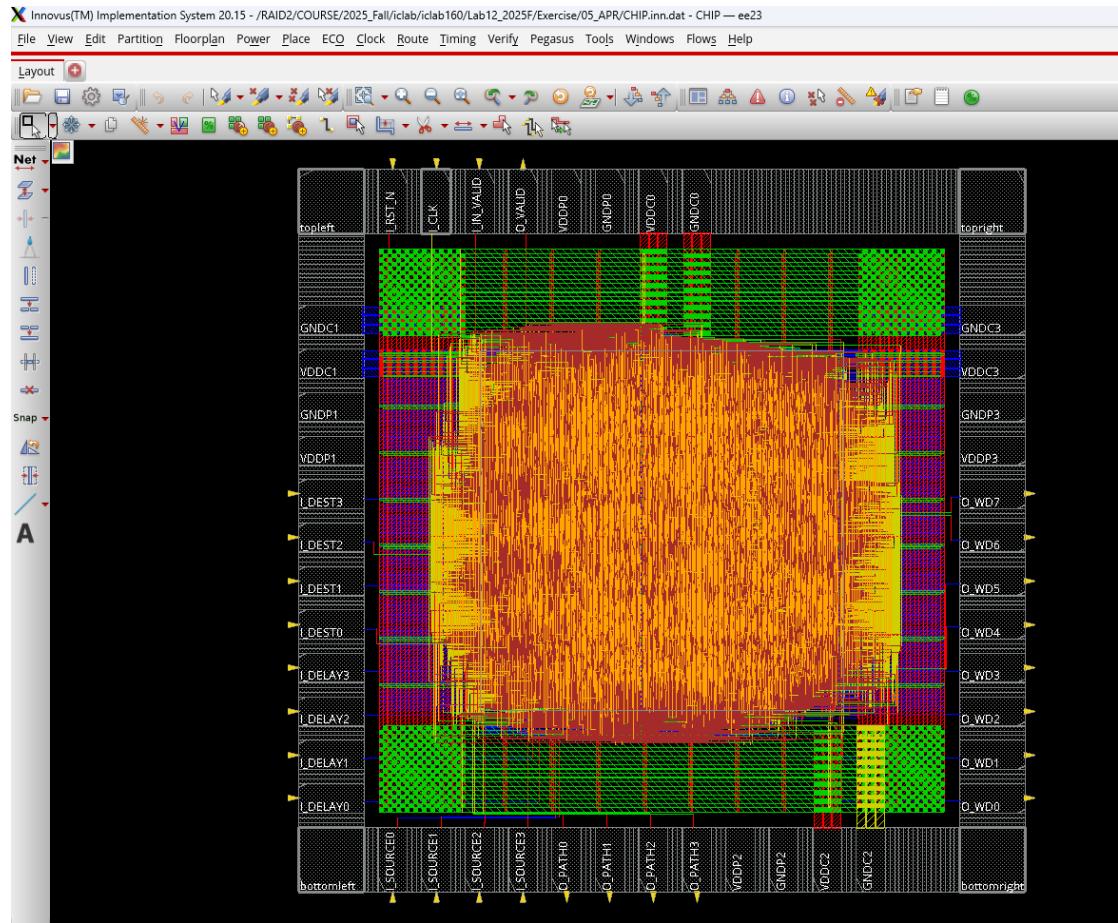


# Report

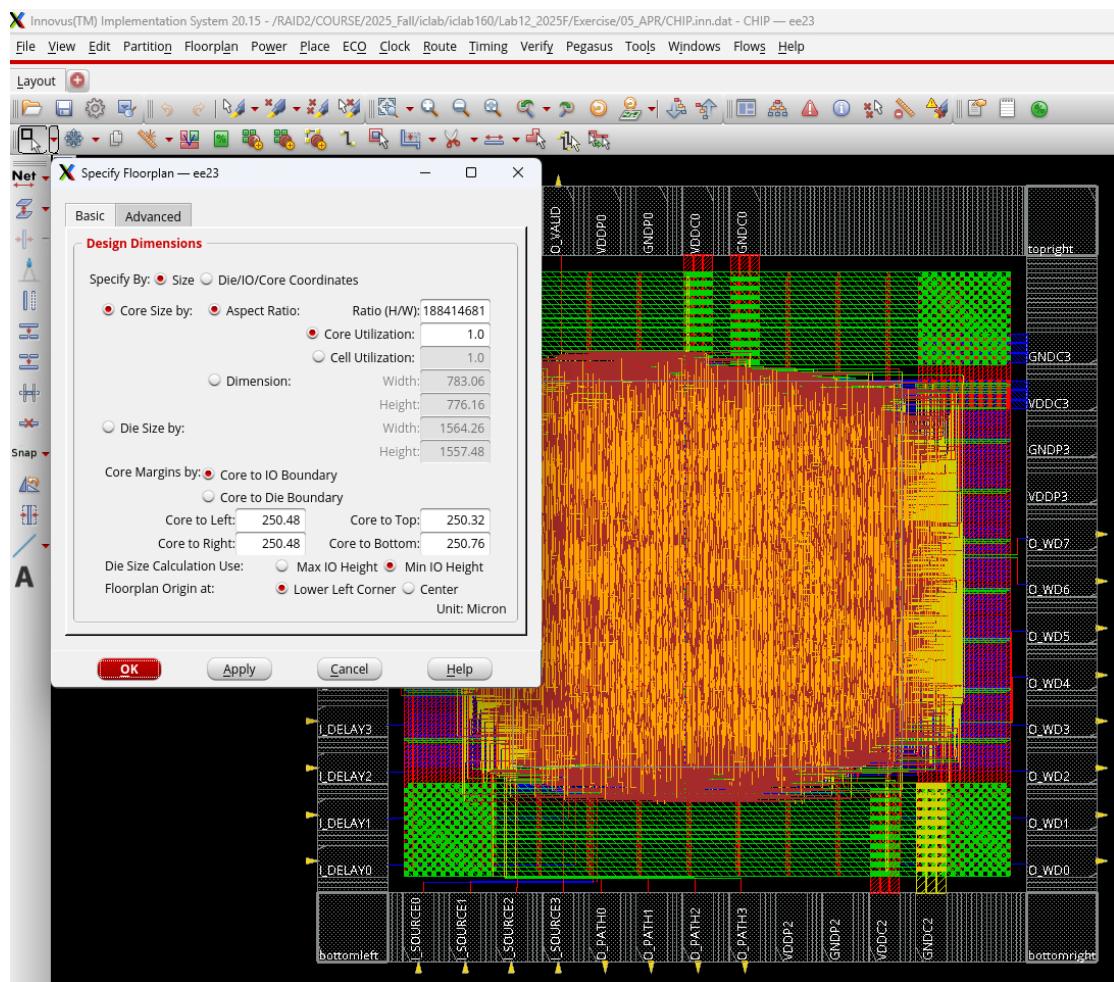
## Iclab160

### 1. Chip Layout View :

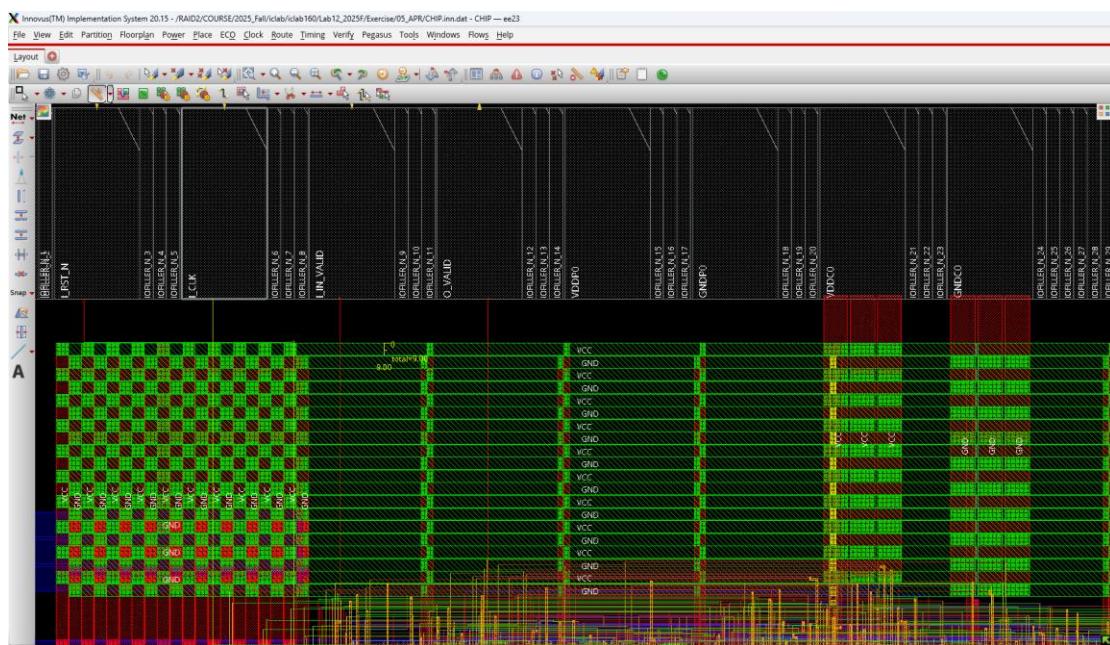
Instructions: After completing the final layout, capture a screenshot of the entire chip layout.



### 2. Core to IO boundary :



### 3. Core Ring :



### 4. Post-Route setup time analysis :

```

Total Leakage Power: 0.02248542 0.0776%
Total Power: 28.98173033

Endled Static Power Report Generation: (cpu=0:00:00, real=0:00:00, mem/process/total/peak)=2094.66MB/4099.61MB/2094.73MB

Output file is power_log/CHIP.rpt

innovus >
innovus > pwd
/RAID2/COURSE/2025_Fall/iclab/iclab160/Lab12_2025F/Exercise/05_APR

innovus > timeDesign #2 [begin] : totSession cpu/real = 0:03:43.7/0:38:16.1 (0.1), mem = 2901.8M
innovus > report EOS DB
Ignoring AAE DB Respecting ...
Extraction called for design 'CHIP' of instances=33918 and nets=26135 using extraction engine 'postRoute' at effort level 'high'.
Integrated QRE (IQunrats) Extraction in Multi-Corner mode called for design 'CHIP'. Number of corners is 1.
No changed net or region found. No need to perform incremental extraction.

-----
timeDesign Summary
-----

Setup views included:
av_func_mode_max

+-----+-----+-----+-----+
| Setup mode | all | reg2reg | default |
+-----+-----+-----+-----+
| MNS (ns) | 0.023 | 0.023 | 0.043 |
| TNS (ns) | 0.000 | 0.000 | 0.000 |
Violating Paths: 9 0 0
All Paths: 1415 688 727
+-----+-----+-----+-----+

+-----+-----+-----+-----+
| DRVs | Real | Total |
+-----+-----+-----+-----+
| Nr nets(terms) | Worst Vio | Nr nets(terms) |
+-----+-----+-----+-----+
| max_cap | 0 (0) | 0.000 | 0 (0) |
| max_ftran | 0 (0) | 0.000 | 0 (0) |
| max_Fanout | 0 (0) | 0 | 0 (0) |
| max_length | 0 (0) | 0 | 0 (0) |
+-----+-----+-----+-----+

Density: 94.730%  

(128.354% with Fillers)
Total number of glitch violations: 0
-----
Reported timing to dir timingReports
Total CPU time: 0.193 sec
Total real time: 4.0 sec
Total Memory Usage: 2841.109375 Mbytes
Reset AAE Options
*** timeDesign #2 [finish] : cpu/real = 0:00:02.9/0:00:04.6 (0.6), totSession cpu/real = 0:03:46.6/0:30:20.7 (0.1), mem = 2841.1M
innovus > 

```

## 5. Post-Route hold time analysis :

Starting SI iteration 1 using Infinite Timing Windows

```
#####
# Design Stage: PostRoute
# Design Name: CH12
# Design Mode: 180nm
# Device: XC2V1000-10CQV
# Parasitics Mode: SPEF/RCDB
# Signoff Settings: SI On
#####
#####threads from CTE
AAE INFO: 3 threads acquired from CTE
Start delay calculation [fullDC] (1 T), (MEM=2813.28)
*** calculating scaling factor for lib_min libraries using the default operating condition of each library.
Total number of fetched objects 26179
AAE INFO: Total number of nets for which stage creation was skipped for all views 0
End delay calculation [fullDC] (MEM=2833.3 CPU=0:00:00.0 REAL=0:00:00.0)
End delay calculation [fullDC] (MEM=2833.3 CPU=0:00:00.0 REAL=0:00:00.0)
Loading CTE timing window with TwFlowType 0, (CPU = 0:00:00.0, REAL = 0:00:00.0, MEM = 2833.3M)
Add other clocks and setupToAEClockMapping during iter 1
Loading CTE timing window is completed (CPU = 0:00:00.1, REAL = 0:00:00.0, MEM = 2833.3M)
Add other clocks and setupToAEClockMapping during iter 1
Starting SI iteration 2
Start delay calculation [fullDC] (1 T), (MEM=2805.42)
Glitch Analysis: View av_func_mode_min -- Total Number of Nets Skipped = 0,
Glitch Analysis: View av_func_mode_min -- Total Number of Nets Analyzed = 26179.
Total number of fetched objects 26179
AAE INFO: Total number of nets for which stage creation was skipped for all views 0
End delay calculation [fullDC] (MEM=2845.59 CPU=0:00:00.1 REAL=0:00:00.0)
End delay calculation [fullDC] (MEM=2845.59 CPU=0:00:00.1 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:10.5 real=0:00:10.0 totSessionCpu=0:04:00 mem=2845.6M)

-----
timeDesign Summary

Hold views included:
av_func_mode_min

+-----+-----+-----+
| Hold mode | all | req2req | default |
+-----+-----+-----+
| WNS (ns) | 0.260 | 0.260 | 5.046 |
| TNS (ns) | 0.000 | 0.000 | 0.000 |
| Violation Paths | 0 | 0 | 0 |
| All Paths | 1415 | 688 | 727 |
+-----+-----+-----+-----+
```

Density: 94.728% (128.354% with fillers)

Reported timing to dir timingReports

Total CPU time: 12.68 sec

Total Real time: 13.0 sec

Total memory usage: 2768.859375 Mbytes

Report EAE Options

\*\*\* timeDesign #3 [finish] : cpu:real = 0:00:12.7/0:00:13.1 (1.0), totSession cpu/real = 0:04:00.7/0:31:06.2 (0.1), mem = 2768.9M

## **6. DRC result :**

```

/RAID2/COURSE/2025_Fall/iclab/iclab160/Lab12_2025F/Exercise/05_pwdA
Name           Size (KB) Last modified
..              2025-12-03 14:0!
.cadence        2025-05-28 01:2!
.CeltIC          2025-05-28 01:2!
CHIP.inn.dat    2025-12-03 16:0!
CHIP_placement.inn.dat 2025-12-03 15:3!
CHIP_postTS.inn.dat 2025-12-03 15:3!
CHIP_pp.inn.dat 2025-12-03 15:2!
client_log       2025-12-03 15:5!
cmd              2025-05-28 01:2!
DBS              2025-12-03 15:3!
extLogDir        2025-12-03 15:5!
layermap         2025-05-28 01:2!
LEF              2025-05-28 01:2!
LIB              2025-05-28 01:2!
log              2025-05-28 01:2!
PD_25C_avg_1    2025-12-03 16:2!
power_log        2025-12-03 16:2!
RC               2025-05-28 01:2!
summaryReport    2025-05-28 01:2!
timingReports   2025-12-03 15:5!
work             2025-12-03 16:2!
.idlab160_launch_209905_0 13 2025-12-03 16:2!
.idlab160_launch_209905_1 13 2025-12-03 16:2!
.idlab160_launch_215025_0 13 2025-12-03 16:2!
.idlab160_launch_215025_1 13 2025-12-03 16:2!
.nano_eco_diode.list 1 2025-12-03 15:4!
.qor_metric.td  1 2025-12-03 16:2!
.timing_file_64003.tif.gz 1 889 2025-12-03 15:4!
00_combine      1 2025-05-28 01:2!
01_setenv       1 2025-05-28 01:2!
09_clean_up    1 2025-05-28 01:2!
cellIDMap       1 2025-12-03 16:2!
CHIP.CCOPT.spec 2 2025-12-03 15:3!
CHIP.conn.rpt   1 2025-12-03 16:0!
CHIP.conn.rpt.old 1 2025-12-03 15:2!
CHIP.drc.rpt    1 2025-12-03 16:0!
CHIP.drc.rpt.old 1 2025-12-03 15:2!
CHIP.globals    134 2025-12-03 15:0!
CHIP.inn        1 2025-12-03 16:0!
CHIP.io         3 2025-12-03 15:1!
CHIP.sdc        8 2025-05-28 01:2!
CHIP.sdf        22 313 2025-12-03 16:0!
CHIP.v          2 771 2025-12-03 16:0!

VERIFY DRC ..... Sub-Area : {0..000 522..240 261..120 783..360} 13 of 36
VERIFY DRC ..... Sub-Area : 13 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {261..120 522..240 522..240 783..360} 14 of 36
VERIFY DRC ..... Sub-Area : 14 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {522..240 522..240 783..360 783..360} 15 of 36
VERIFY DRC ..... Sub-Area : 15 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {783..360 522..240 1044..480 783..360} 16 of 36
VERIFY DRC ..... Sub-Area : 16 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1044..480 522..240 1305..600 783..360} 17 of 36
VERIFY DRC ..... Sub-Area : 17 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1305..600 522..240 1564..260 783..360} 18 of 36
VERIFY DRC ..... Sub-Area : 18 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0..000 783..360 261..120 1044..480} 19 of 36
VERIFY DRC ..... Sub-Area : 19 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {261..120 783..360 522..240 1044..480} 20 of 36
VERIFY DRC ..... Sub-Area : 20 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {522..240 783..360 783..360 1044..480} 21 of 36
VERIFY DRC ..... Sub-Area : 21 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {783..360 783..360 1044..480 1044..480} 22 of 36
VERIFY DRC ..... Sub-Area : 22 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1044..480 783..360 1305..600 1044..480} 23 of 36
VERIFY DRC ..... Sub-Area : 23 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1305..600 783..360 1564..260 1044..480} 24 of 36
VERIFY DRC ..... Sub-Area : 24 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0..000 1044..480 261..120 1305..600} 25 of 36
VERIFY DRC ..... Sub-Area : 25 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {261..120 1044..480 522..240 1305..600} 26 of 36
VERIFY DRC ..... Sub-Area : 26 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {522..240 1044..480 783..360 1305..600} 27 of 36
VERIFY DRC ..... Sub-Area : 27 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {783..360 1044..480 1044..480 1305..600} 28 of 36
VERIFY DRC ..... Sub-Area : 28 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1044..480 1044..480 1305..600 1305..600} 29 of 36
VERIFY DRC ..... Sub-Area : 29 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1305..600 1044..480 1564..260 1305..600} 30 of 36
VERIFY DRC ..... Sub-Area : 30 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0..000 1305..600 261..120 1557..480} 31 of 36
VERIFY DRC ..... Sub-Area : 31 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {261..120 1305..600 522..240 1557..480} 32 of 36
VERIFY DRC ..... Sub-Area : 32 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {522..240 1305..600 783..360 1557..480} 33 of 36
VERIFY DRC ..... Sub-Area : 33 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {783..360 1305..600 1044..480 1557..480} 34 of 36
VERIFY DRC ..... Sub-Area : 34 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1044..480 1305..600 1305..600 1557..480} 35 of 36
VERIFY DRC ..... Sub-Area : 35 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1305..600 1305..600 1564..260 1557..480} 36 of 36
VERIFY DRC ..... Sub-Area : 36 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:04.3 ELAPSED TIME: 4.00 MEM: 92.0M) ***

```

innovus 2>  
innovus 2> pwd  
/RAID2/COURSE/2025\_Fall/iclab/iclab160/Lab12\_2025F/Exercise/05\_AP

## 7. LVS result :

```

/RAID2/COURSE/2025_Fall/iclab/iclab160/Lab12_2025F/Exercise/05_pwdA
Name           Size (KB) Last modified
..              2025-12-03 14:0!
.cadence        2025-05-28 01:2!
.CeltIC          2025-05-28 01:2!
CHIP.inn.dat    2025-12-03 16:0!
CHIP_placement.inn.dat 2025-12-03 15:3!
CHIP_postTS.inn.dat 2025-12-03 15:3!
CHIP_pp.inn.dat 2025-12-03 15:2!
client_log       2025-12-03 15:5!
cmd              2025-05-28 01:2!
DBS              2025-12-03 15:3!
extLogDir        2025-12-03 15:5!
layermap         2025-05-28 01:2!
LEF              2025-12-03 16:2!
LIB              2025-05-28 01:2!
log              2025-05-28 01:2!
PD_25C_avg_1    2025-12-03 16:2!
power_log        2025-12-03 16:2!
RC               2025-05-28 01:2!
summaryReport    2025-05-28 01:2!
timingReports   2025-12-03 15:5!
work             2025-12-03 16:2!
.idlab160_launch_209905_0 13 2025-12-03 16:2!
.idlab160_launch_209905_1 13 2025-12-03 16:2!
.idlab160_launch_215025_0 13 2025-12-03 16:2!
.idlab160_launch_215025_1 13 2025-12-03 16:2!
.nano_eco_diode.list 1 2025-12-03 15:4!
.qor_metric.td  1 2025-12-03 16:2!
.timing_file_64003.tif.gz 1 889 2025-12-03 15:4!
00_combine      1 2025-05-28 01:2!
01_setenv       1 2025-05-28 01:2!
09_clean_up    1 2025-12-03 16:2!
cellIDMap       1 2025-12-03 16:2!
CHIP.CCOPT.spec 2 2025-12-03 15:3!
CHIP.conn.rpt   1 2025-12-03 16:0!
CHIP.conn.rpt.old 1 2025-12-03 15:2!
CHIP.drc.rpt    1 2025-12-03 16:0!
CHIP.drc.rpt.old 1 2025-12-03 15:2!
CHIP.globals    134 2025-12-03 15:0!
CHIP.inn        1 2025-12-03 16:0!
CHIP.io         3 2025-12-03 15:1!
CHIP.sdc        8 2025-05-28 01:2!
CHIP.sdf        22 313 2025-12-03 16:0!
CHIP.v          2 771 2025-12-03 16:0!

VERIFY DRC ..... Sub-Area : 26 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {522..240 1044..480 783..360 1305..600} 27 of 36
VERIFY DRC ..... Sub-Area : 27 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {783..360 1044..480 1044..480 1305..600} 28 of 36
VERIFY DRC ..... Sub-Area : 28 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1044..480 1044..480 1305..600 1305..600} 29 of 36
VERIFY DRC ..... Sub-Area : 29 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1305..600 1044..480 1564..260 1305..600} 30 of 36
VERIFY DRC ..... Sub-Area : 30 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0..000 1305..600 261..120 1557..480} 31 of 36
VERIFY DRC ..... Sub-Area : 31 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {261..120 1305..600 522..240 1557..480} 32 of 36
VERIFY DRC ..... Sub-Area : 32 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {522..240 1305..600 783..360 1557..480} 33 of 36
VERIFY DRC ..... Sub-Area : 33 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {783..360 1305..600 1044..480 1557..480} 34 of 36
VERIFY DRC ..... Sub-Area : 34 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1044..480 1305..600 1305..600 1557..480} 35 of 36
VERIFY DRC ..... Sub-Area : 35 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1305..600 1305..600 1564..260 1557..480} 36 of 36
VERIFY DRC ..... Sub-Area : 36 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:04.3 ELAPSED TIME: 4.00 MEM: 92.0M) ***

```

innovus 2>  
innovus 2> pwd  
/RAID2/COURSE/2025\_Fall/iclab/iclab160/Lab12\_2025F/Exercise/05\_AP  
innovus 3> VERIFY\_CONNECTIVITY use new engine.

\*\*\*\*\* Start: VERIFY CONNECTIVITY \*\*\*\*\*  
Start Time: Thu Dec 4 01:24:51 2025

Design Name: CHIP  
Database Units: 1000  
Design Boundary: (0.0000, 0.0000) (1564.2600, 1557.4800)  
Error Limit = 1000; Warning Limit = 50  
Check all nets  
\*\*\*\* 01:24:51 \*\*\*\* Processed 5000 nets.  
\*\*\*\* 01:24:51 \*\*\*\* Processed 10000 nets.  
\*\*\*\* 01:24:52 \*\*\*\* Processed 15000 nets.  
\*\*\*\* 01:24:52 \*\*\*\* Processed 20000 nets.  
\*\*\*\* 01:24:52 \*\*\*\* Processed 25000 nets.

Begin Summary  
Found no problems or warnings.  
End Summary

End Time: Thu Dec 4 01:24:52 2025  
Time Elapsed: 0:00:01.0

\*\*\*\*\* End: VERIFY CONNECTIVITY \*\*\*\*\*  
Verification Complete : 0 Viols. 0 Wrngs.  
(CPU Time: 0:00:01.2 MEM: 14.000M)

## 8. Post Layout simulation result :

```

No. 996 PASS
No. 997 PASS
No. 998 PASS
No. 999 PASS

***** Congratulations!
executed cycles: 50000
clock period: 11.000000ns
*****$finish called from file "PATTERN.v", line 118.
$finish at simulation time 1003228500
VCS Simulation Report
Time: 1003228500 ns
CPU Time: 23.750 seconds; Data structure size: 8.1MB
Thu Dec 01 28:21:2025
CPU time: 3.820 seconds to compile + 1.426 seconds to elab + .971 seconds to link + 23.829 seconds in simulation
1:23 /Lab160@ee231-Lab12_2025F/Exercise/06_POST]$ 

```

## 9. Power result :

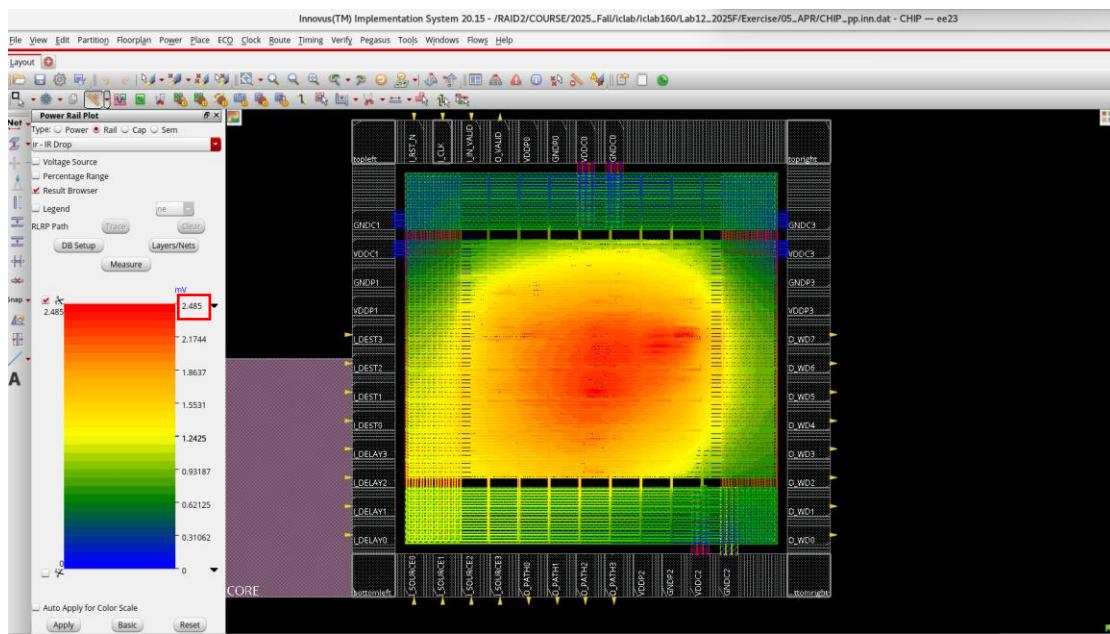
```

Quick connect...
(raid2/course/2025_fall/iclab/iclab160/lab12_2025f/exercise/05_apr)
Name Size (KB) Last modified
.. 2025-12-03 14:05
cadence 2025-05-28 01:25
CeltIC 2025-12-03 16:03
CHIP.inn.dat 2025-12-03 15:33
CHIP_placement.inn.dat 2025-12-03 15:37
CHIP_postCTS.inn.dat 2025-12-03 15:24
CHIP_pp.inn.dat 2025-12-03 15:27
client_log 2025-05-28 01:25
cmd 2025-12-03 15:36
DBS 2025-12-03 15:51
extLogDir 2025-05-28 01:25
layermap 2025-05-28 01:25
LEF 2025-12-03 16:26
LIB 2025-05-28 01:25
log 2025-05-28 01:25
PD_2SC_avg_1 2025-12-03 16:22
power_log 2025-12-03 16:26
RC 2025-05-28 01:25
summaryReport 2025-05-28 01:25
timingReports 2025-12-03 15:59
work 2025-12-03 16:26
.idab160_launch_209905_0 13
.idab160_launch_209905_1 13
.idab160_launch_215025_0 13
.idab160_launch_215025_1 13
.nano_eco_diode.lst 1
.qor_metric.td 1
.timing_file_54003.tif.gz 1889
00_combine 1
01_seternv 1
09_clean_up 1
.cellIDMap 1
CHIP_COOPT.spec 2
CHIP_conn.rpt 1
CHIP_conn.rpt.old 1
CHIP_drc.rpt 1
CHIP_drc.rpt.old 1
CHIP_globals 134
CHIP_inn 1
CHIP_io 3
CHIP_sd 8
CHIP_sdc 22313
CHIP_sdf 2025-12-03 16:00
CHIP.v 2771
2025-12-03 16:00

***** Ended Boundary Leakage Calculation: (cpu=0:00:00, real=0:00:00, mem(process/total/peak)=2092.98MB/4099.61MB/2093.55MB)
Begin Static Power Report Generation
16 instances have no static power
** WARN: (VOLTUS_POWR-2152): Instance VDDP0 (VCC3IOD) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance VDP1 (VCC3IOD) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance VDDP2 (VCC3IOD) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance VDDP3 (VCC3IOD) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance GNDP0 (GNDIOD) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance GNDP1 (GNDIOD) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance GNDP2 (GNDIOD) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance GNDP3 (GNDIOD) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance VDDC0 (VCCKD) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance VDDC1 (VCCKD) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance VDDC2 (VCCKD) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance VDDC3 (VCCKD) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance GNDCK0 (GNDKD) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance GNDCK1 (GNDKD) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance GNDCK2 (GNDKD) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance GNDCK3 (GNDKD) has no static power.
*
Total Power
-----
Total Internal Power: 10.57343142 36.4831%
Total Switching Power: 18.38581349 63.4393%
Total Leakage Power: 0.02248542 0.0776%
Total Power: 28.9817033
----- Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00, mem(process/total/peak)=2094.66MB/4099.61MB/2094.73MB)
Output file is power_log/CHIP.rpt
innovus 3>
innovus 3> pwd
/RAID2/COURSE/2025_Fall/iclab/iclab160/Lab12_2025F/Exercise/05_APR
innovus 4>

```

## 10. IR Drop Results :



I use more power pads, and more power rails to reduce the IR drop issue.