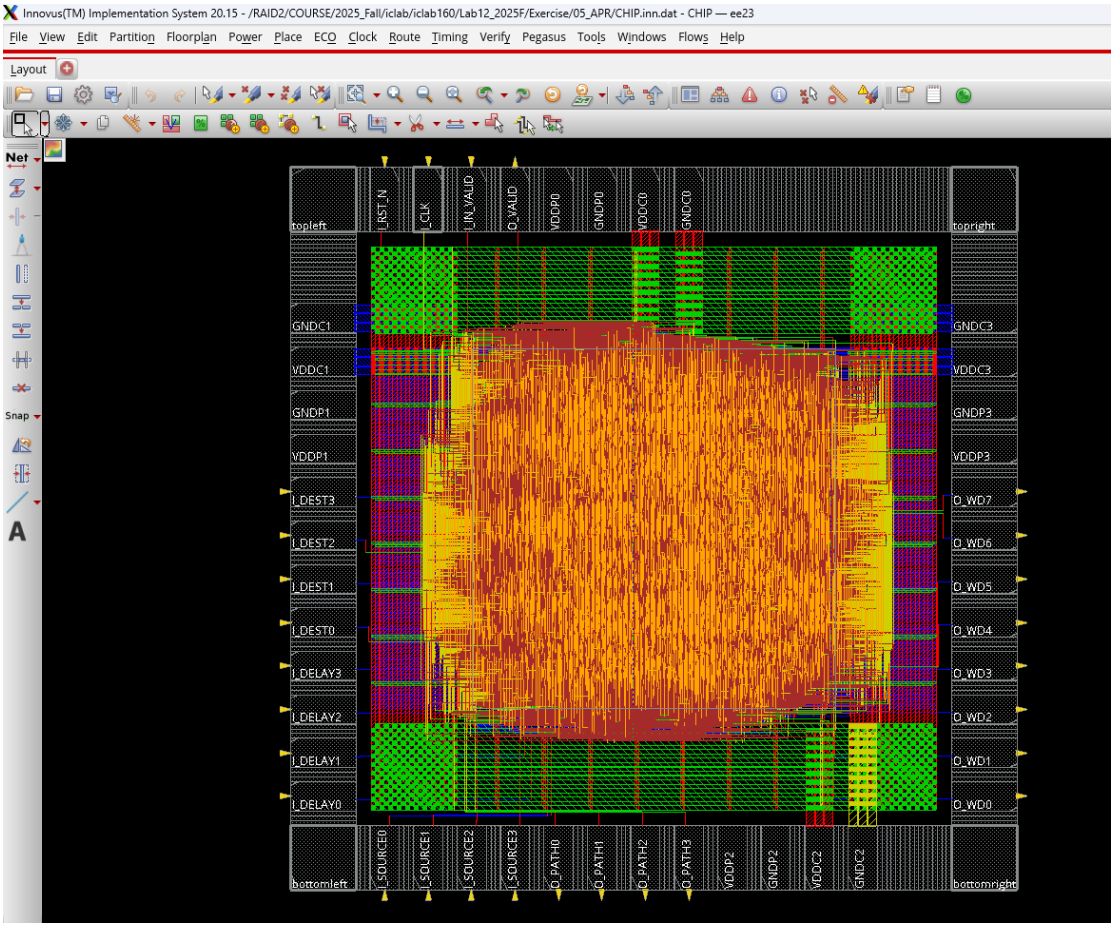
Report

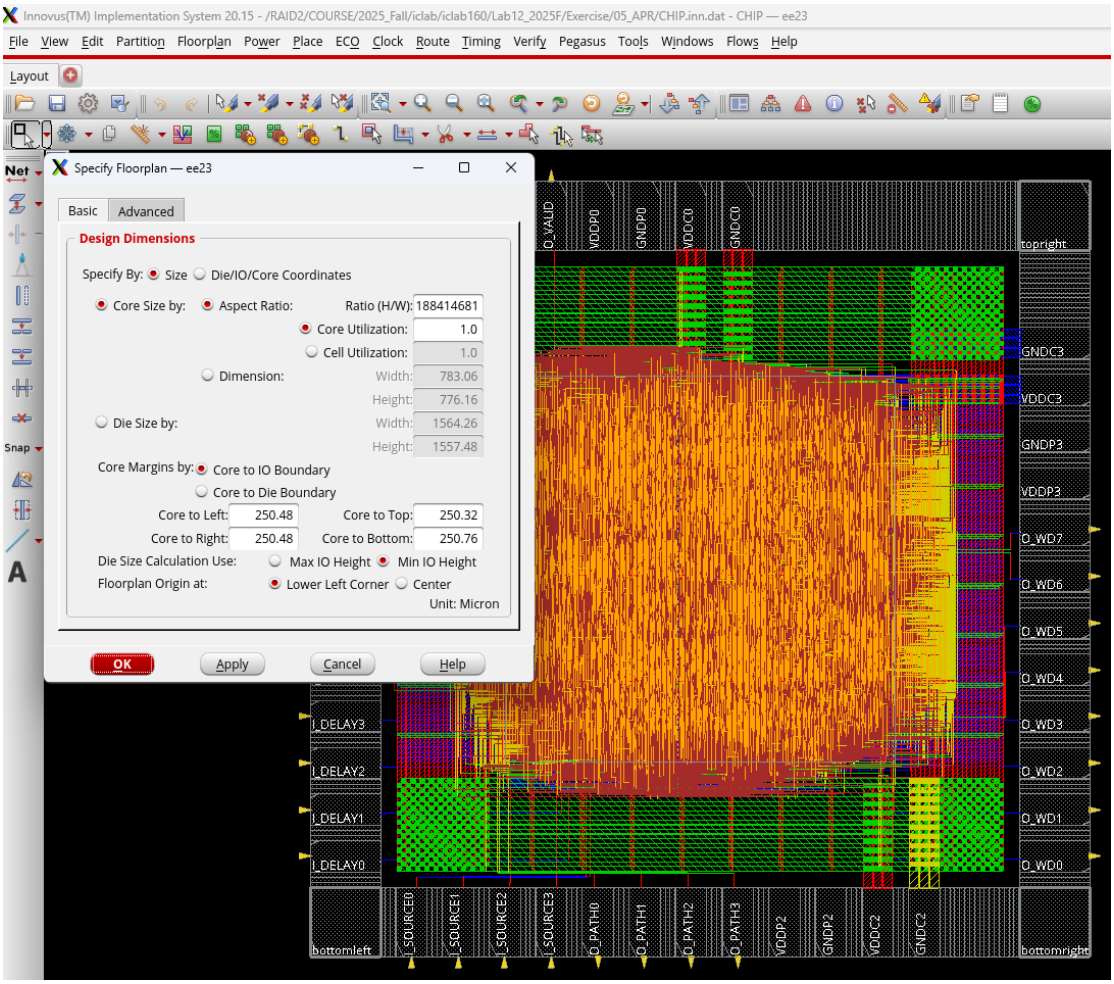
Iclab160

1. Chip Layout View :

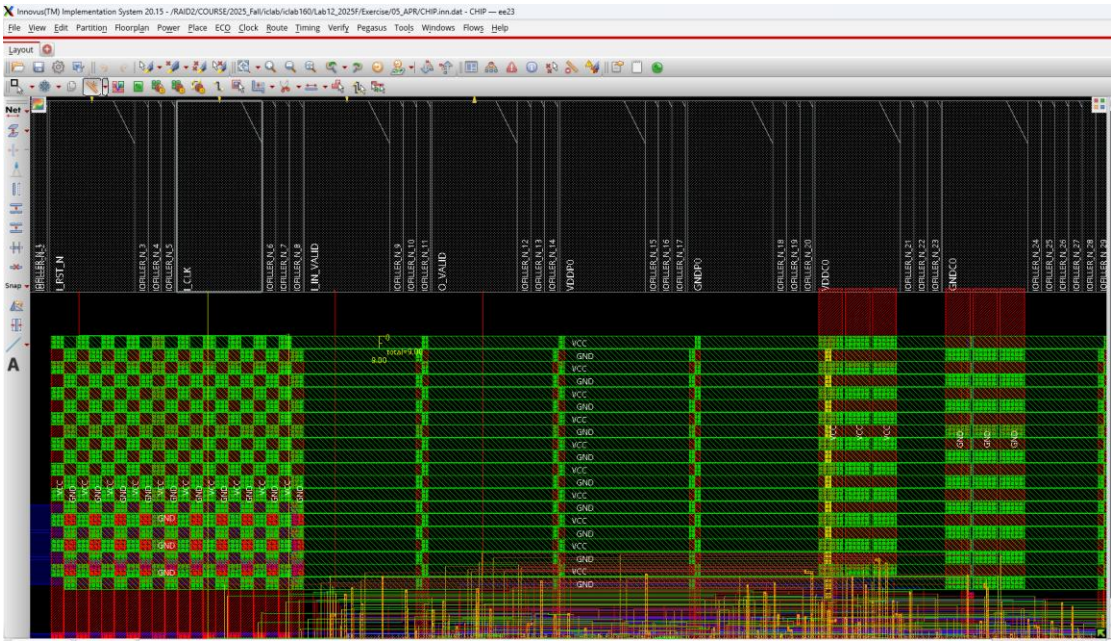
Instructions: After completing the final layout, capture a screenshot of the entire chip layout.



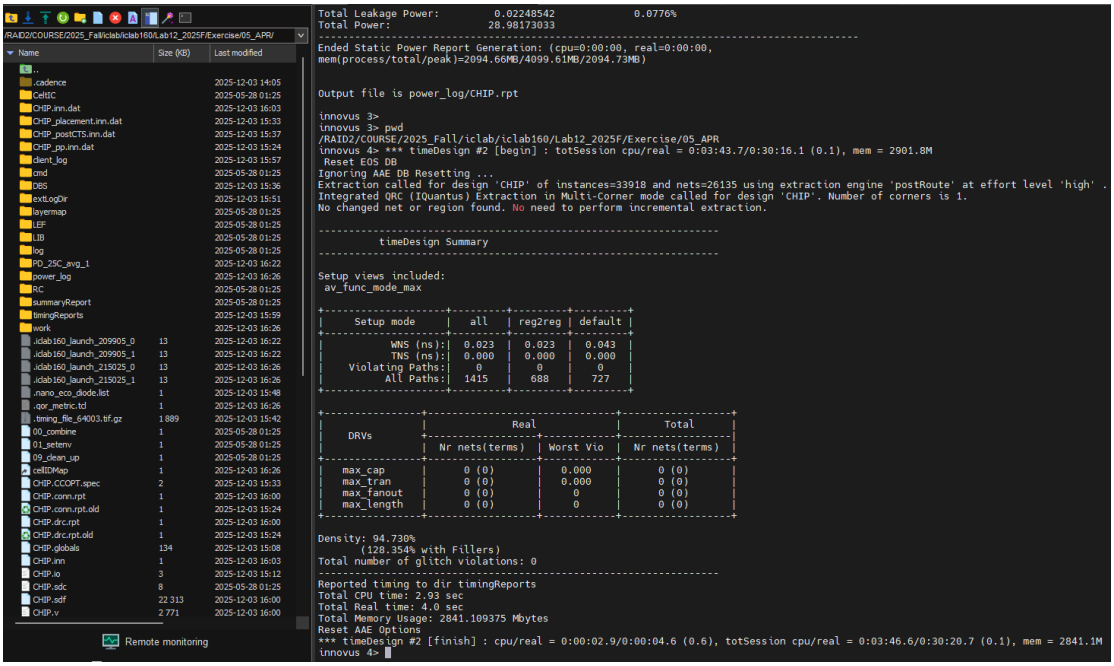
2. Core to IO boundary :



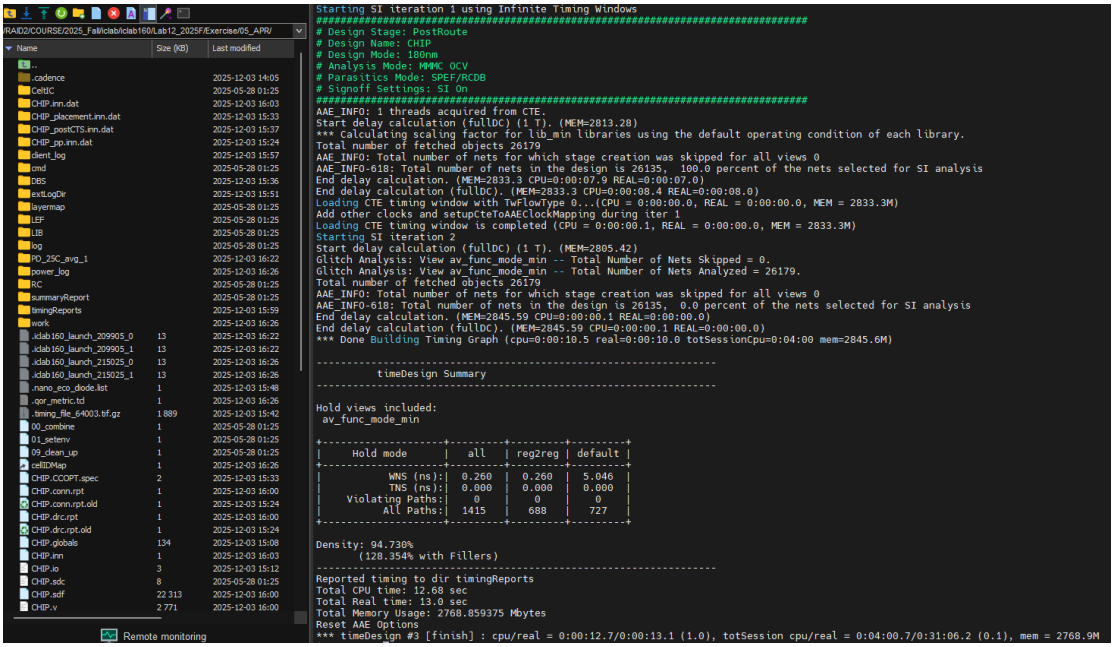
3. Core Ring :



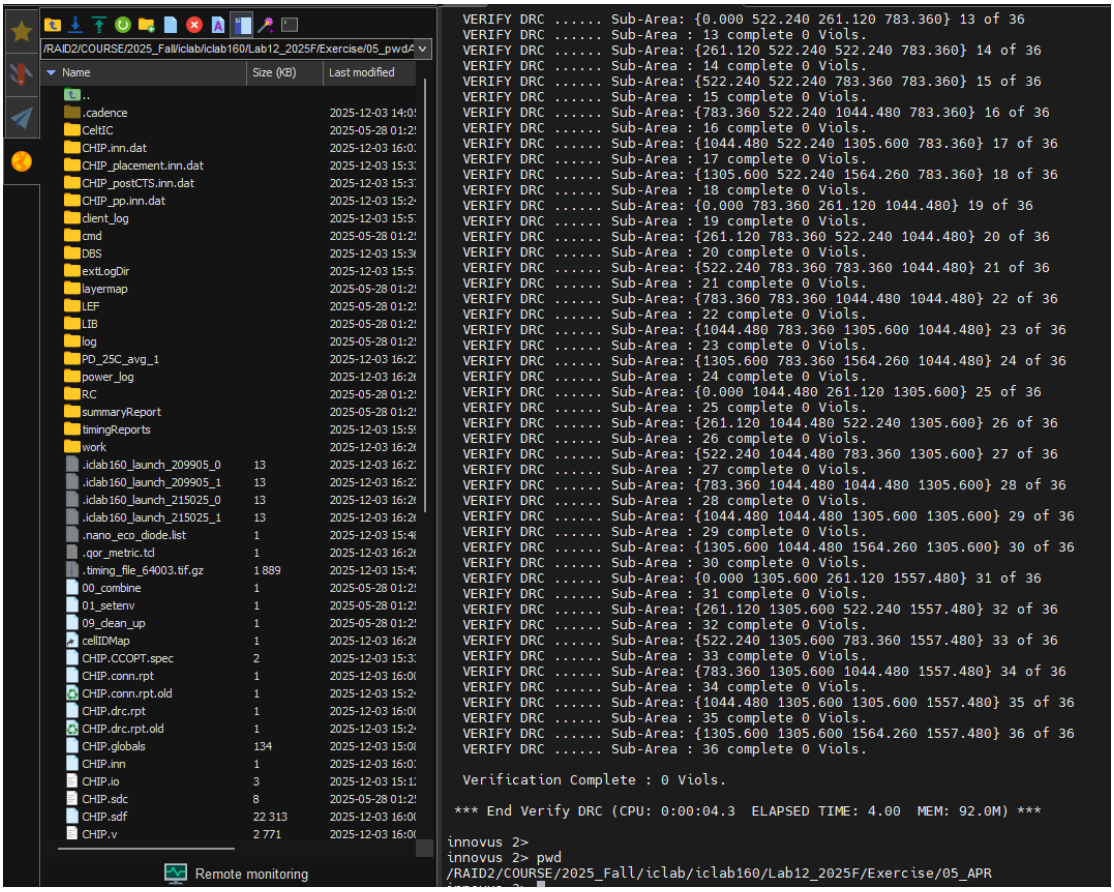
4. Post-Route setup time analysis :



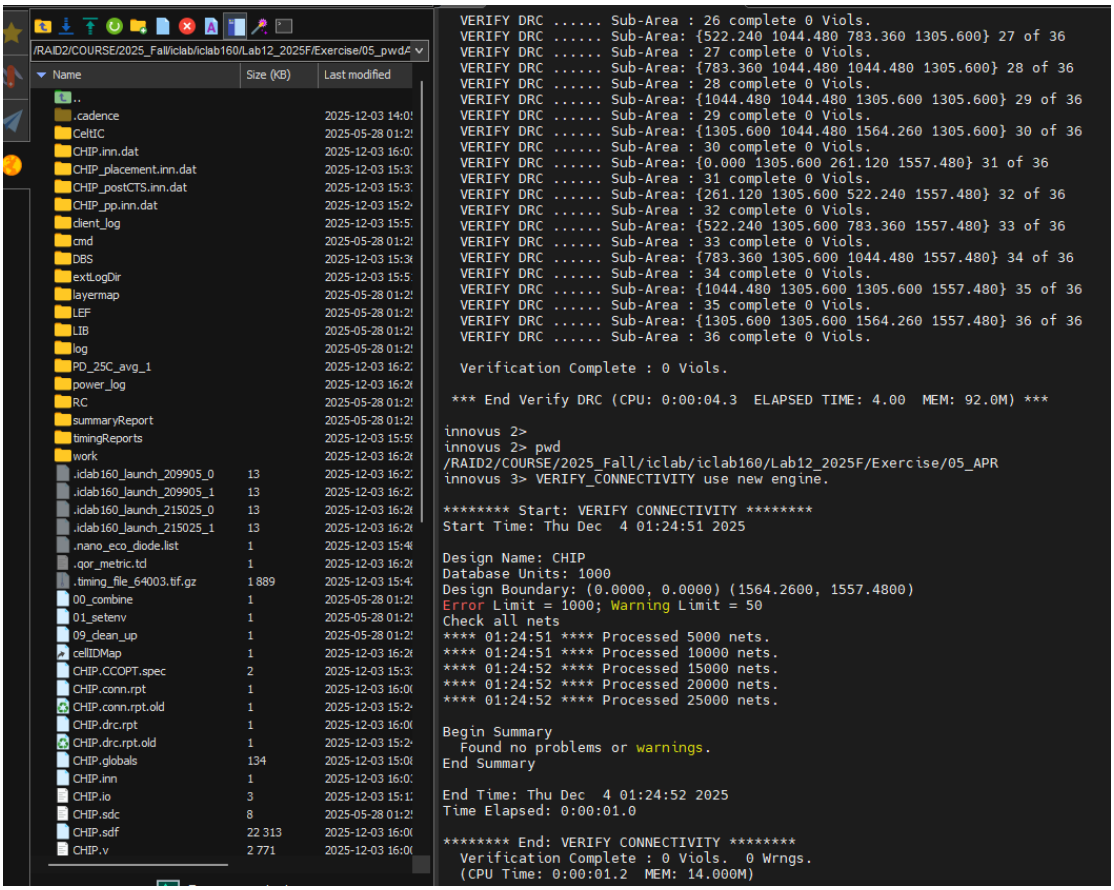
5. Post-Route hold time analysis :



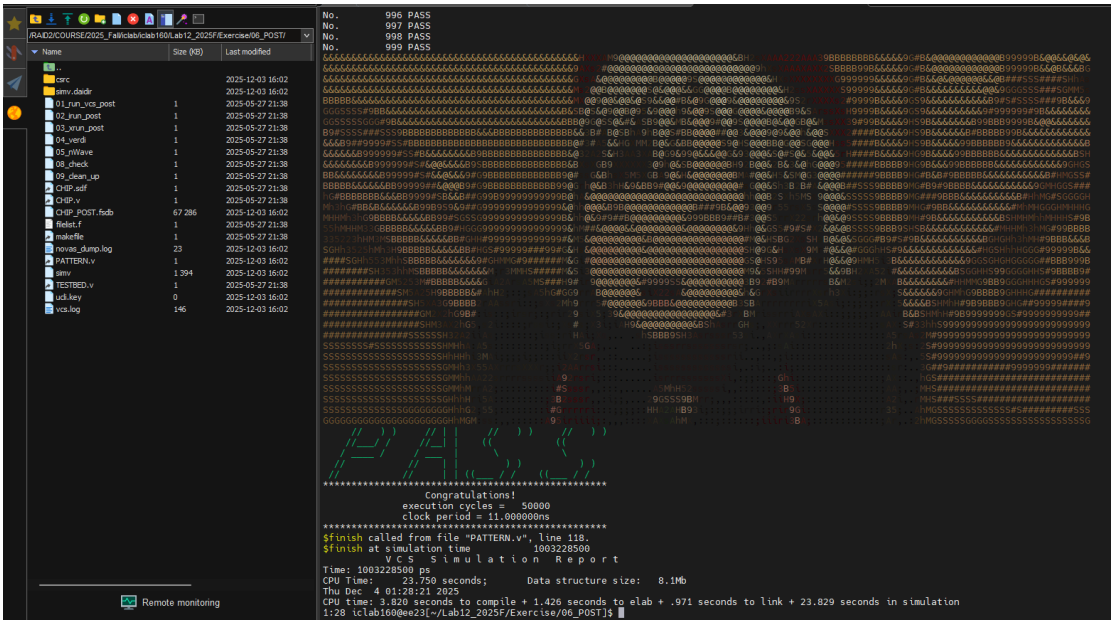
6. DRC result :


/RAID2/COURSE/2025_Fall/iclab/iclab160/Lab12_2025F/Exercise/05_pwd
Name
Size (KB)
Last modified
Remote monitoring
VERIFY DRC ..... Sub-Area: {0.000 522.240 261.120 783.360} 13 of 36
VERIFY DRC ..... Sub-Area : 13 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {261.120 522.240 522.240 783.360} 14 of 36
VERIFY DRC ..... Sub-Area : 14 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {522.240 522.240 783.360 783.360} 15 of 36
VERIFY DRC ..... Sub-Area : 15 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {783.360 522.240 1044.480 783.360} 16 of 36
VERIFY DRC ..... Sub-Area : 16 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1044.480 522.240 1305.600 783.360} 17 of 36
VERIFY DRC ..... Sub-Area : 17 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1305.600 522.240 1564.260 783.360} 18 of 36
VERIFY DRC ..... Sub-Area : 18 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 783.360 261.120 1044.480} 19 of 36
VERIFY DRC ..... Sub-Area : 19 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {261.120 783.360 522.240 1044.480} 20 of 36
VERIFY DRC ..... Sub-Area : 20 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {522.240 783.360 783.360 1044.480} 21 of 36
VERIFY DRC ..... Sub-Area : 21 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {783.360 783.360 1044.480 1044.480} 22 of 36
VERIFY DRC ..... Sub-Area : 22 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1044.480 783.360 1305.600 1044.480} 23 of 36
VERIFY DRC ..... Sub-Area : 23 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1305.600 783.360 1564.260 1044.480} 24 of 36
VERIFY DRC ..... Sub-Area : 24 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 1044.480 261.120 1305.600} 25 of 36
VERIFY DRC ..... Sub-Area : 25 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {261.120 1044.480 522.240 1305.600} 26 of 36
VERIFY DRC ..... Sub-Area : 26 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {522.240 1044.480 783.360 1305.600} 27 of 36
VERIFY DRC ..... Sub-Area : 27 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {783.360 1044.480 1044.480 1305.600} 28 of 36
VERIFY DRC ..... Sub-Area : 28 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1044.480 1044.480 1305.600 1305.600} 29 of 36
VERIFY DRC ..... Sub-Area : 29 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1305.600 1044.480 1564.260 1305.600} 30 of 36
VERIFY DRC ..... Sub-Area : 30 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 1305.600 261.120 1557.480} 31 of 36
VERIFY DRC ..... Sub-Area : 31 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {261.120 1305.600 522.240 1557.480} 32 of 36
VERIFY DRC ..... Sub-Area : 32 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {522.240 1305.600 783.360 1557.480} 33 of 36
VERIFY DRC ..... Sub-Area : 33 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {783.360 1305.600 1044.480 1557.480} 34 of 36
VERIFY DRC ..... Sub-Area : 34 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1044.480 1305.600 1305.600 1557.480} 35 of 36
VERIFY DRC ..... Sub-Area : 35 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1305.600 1305.600 1564.260 1557.480} 36 of 36
VERIFY DRC ..... Sub-Area : 36 complete 0 Viols.
Verification Complete : 0 Viols.
*** End Verify DRC (CPU: 0:00:04.3 ELAPSED TIME: 4.00 MEM: 92.0M) ***
innovus 2>
innovus 2> pwd
/RAID2/COURSE/2025_Fall/iclab/iclab160/Lab12_2025F/Exercise/05_APR

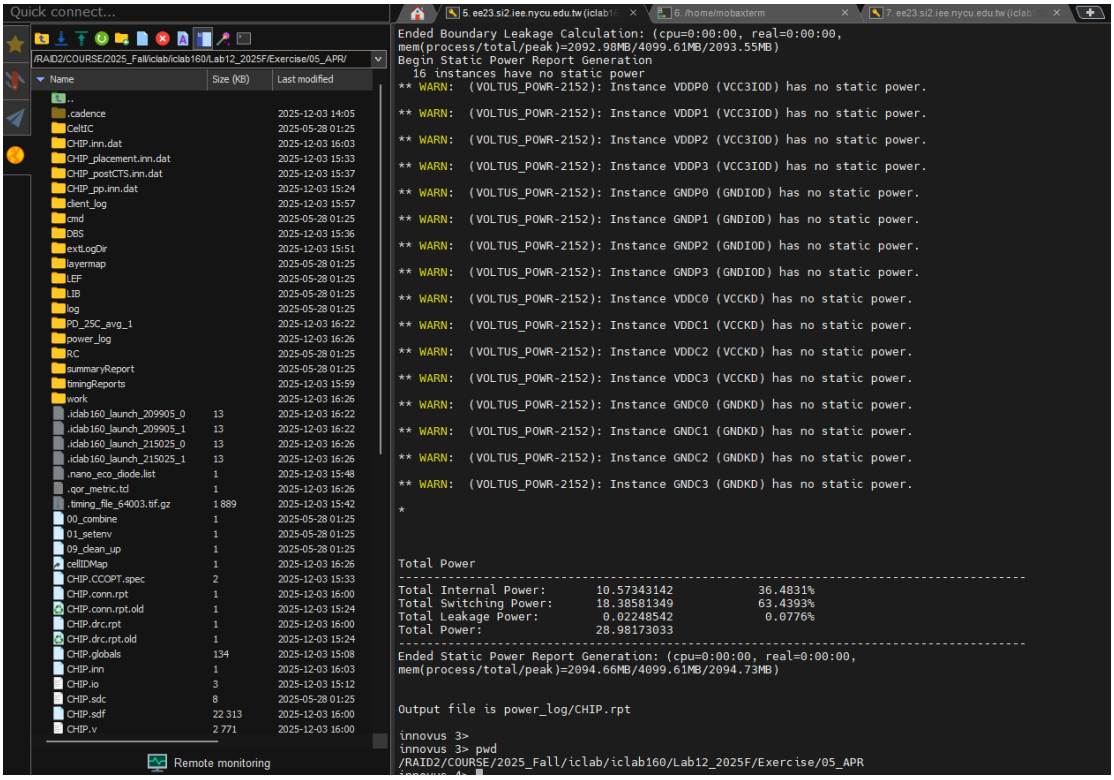
7. LVS result :


/RAID2/COURSE/2025_Fall/iclab/iclab160/Lab12_2025F/Exercise/05_pwd
Name
Size (KB)
Last modified
VERIFY DRC ..... Sub-Area : 26 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {522.240 1044.480 783.360 1305.600} 27 of 36
VERIFY DRC ..... Sub-Area : 27 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {783.360 1044.480 1044.480 1305.600} 28 of 36
VERIFY DRC ..... Sub-Area : 28 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1044.480 1044.480 1305.600 1305.600} 29 of 36
VERIFY DRC ..... Sub-Area : 29 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1305.600 1044.480 1564.260 1305.600} 30 of 36
VERIFY DRC ..... Sub-Area : 30 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 1305.600 261.120 1557.480} 31 of 36
VERIFY DRC ..... Sub-Area : 31 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {261.120 1305.600 522.240 1557.480} 32 of 36
VERIFY DRC ..... Sub-Area : 32 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {522.240 1305.600 783.360 1557.480} 33 of 36
VERIFY DRC ..... Sub-Area : 33 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {783.360 1305.600 1044.480 1557.480} 34 of 36
VERIFY DRC ..... Sub-Area : 34 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1044.480 1305.600 1305.600 1557.480} 35 of 36
VERIFY DRC ..... Sub-Area : 35 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1305.600 1305.600 1564.260 1557.480} 36 of 36
VERIFY DRC ..... Sub-Area : 36 complete 0 Viols.
Verification Complete : 0 Viols.
*** End Verify DRC (CPU: 0:00:04.3 ELAPSED TIME: 4.00 MEM: 92.0M) ***
innovus 2>
innovus 2> pwd
/RAID2/COURSE/2025_Fall/iclab/iclab160/Lab12_2025F/Exercise/05_APR
innovus 3> VERIFY_CONNECTIVITY use new engine.
******** Start: VERIFY CONNECTIVITY ********
Start Time: Thu Dec 4 01:24:51 2025
Design Name: CHIP
Database Units: 1000
Design Boundary: (0.0000, 0.0000) (1564.2600, 1557.4800)
Error Limit = 1000; Warning Limit = 50
Check all nets
**** 01:24:51 **** Processed 5000 nets.
**** 01:24:51 **** Processed 10000 nets.
**** 01:24:52 **** Processed 15000 nets.
**** 01:24:52 **** Processed 20000 nets.
**** 01:24:52 **** Processed 25000 nets.
Begin Summary
Found no problems or warnings.
End Summary
End Time: Thu Dec 4 01:24:52 2025
Time Elapsed: 0:00:01.0
******** End: VERIFY CONNECTIVITY ********
Verification Complete : 0 Viols. 0 Wrngs.
(CPU Time: 0:00:01.2 MEM: 14.000M)

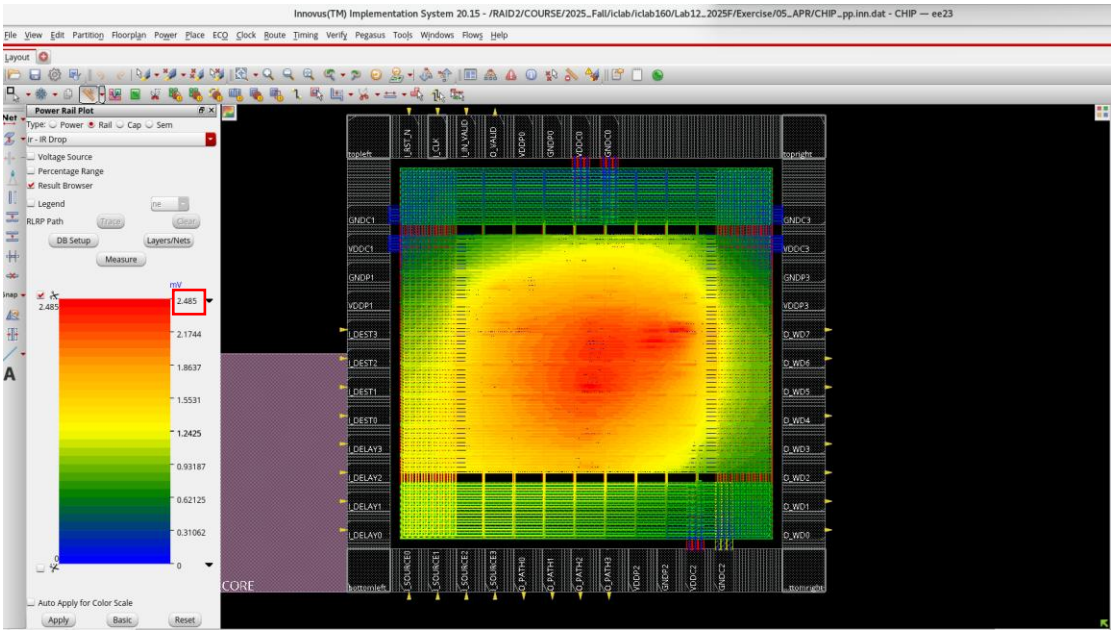
8. Post Layout simulation result :



9. Power result :



10. IR Drop Results :



I use more power pads, and more power rails to reduce the IR drop issue.