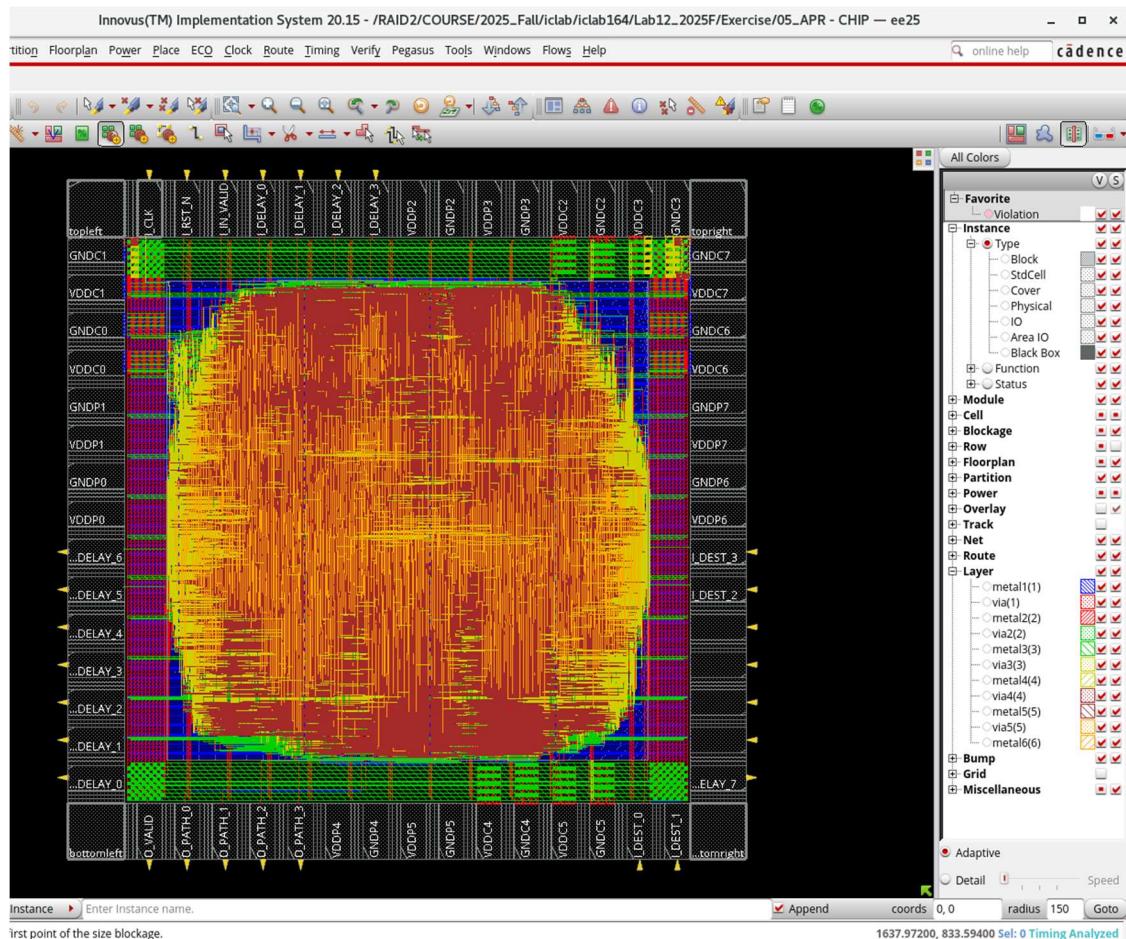


# Report

iclab164

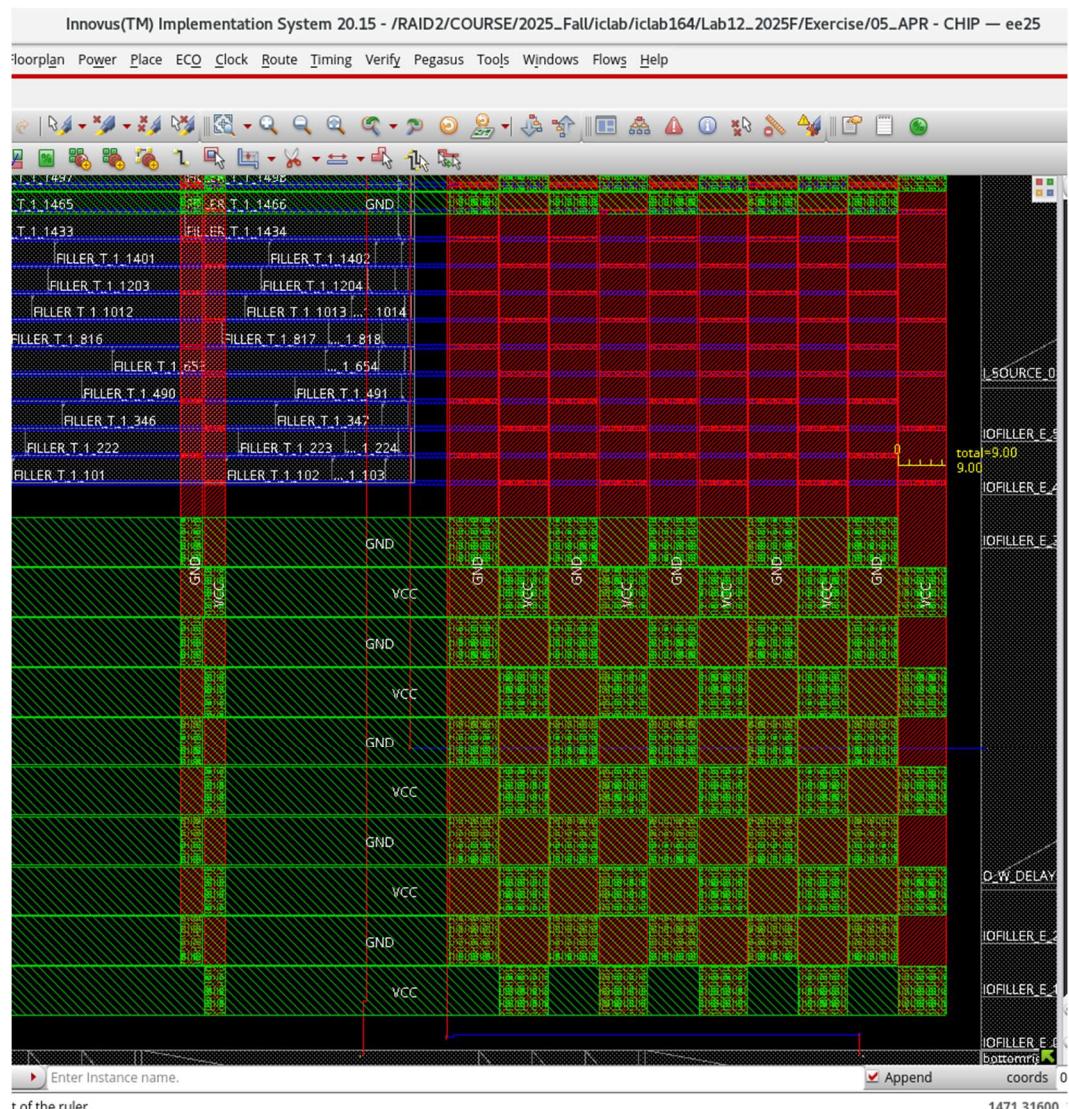
## 1. Chip Layout View :



## 2. Core to IO boundary :



### 3. Core Ring :



## 4. Post-Route setup time analysis :

```

IQuantum Extraction engine is being closed...
IQuantum Fullchip Extraction DONE (CPU Time: 0:01:17  Real Time: 0:01:18  MEM: 2401.594M)
Starting delay calculation for Setup views
AAE_INFO: resetNetProps viewIdx 0
Starting SI iteration 1 using Infinite Timing Windows
#####
# Design Stage: PostRoute
# Design Name: CHIP
# Design Mode: 180nm
# Analysis Mode: MMC OCY
# Parasitics Mode: SEDNRCDB
# Power Staff: Sednrcdb ST On
#####
#####
AAE_INFO: 1 threads acquired from CTE.
Start delay calculation (fullDC) (1 T). (MEM=2401.59)
AAE_INFO: Number of noise libraries( CDBs ) loaded = 2
AAE_INFO: Cdb files are:
          /RAID2/COURSE/2025_Fall/iclab/iclab164/Lab12_2025F/Exercise/05_APR/CHIP.inn.dat/libs/mmmc/u18_ss.cdb
          /RAID2/COURSE/2025_Fall/iclab/iclab164/Lab12_2025F/Exercise/05_APR/CHIP.inn.dat/libs/mmmc/u18_ff.cdb
AAE_INFO: **WARN: (IMPESI-3086): The cell 'XMD' does not have characterized noise model(s) for 'fsa0m_a_t33_generic_io_ss1p62v125c, fsa0m_a_t33
Type 'man IMPESI-3086' for more detail.
AAE_WARN: (IMPESI-3086): The cell 't2g265D' does not have characterized noise model(s) for 'fsa0m_a_t33_generic_io_ss1p62v125c, fsa0m_a_
Type 'man IMPESI-3086' for more detail.
Total number of fetched objects 26099
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
AAE_INFO-618: Total number of nets in the design is 26048, 100.0 percent of the nets selected for SI analysis
End delay calculation. (MEM=2436.88 CPU=0:00:08.1 REAL=0:00:08.0)
End delay calculation (fullDC). (MEM=2401.59 CPU=0:00:08.1 REAL=0:00:08.0)
Reported timing window with Tw=0.000 sec, Td=0.000 sec, TC=0.000 sec, REAL = 0:00:00.0, MEM = 2400.3M
Add other clocks and setupToAmeClockMapping during iter 1
Loading CTE timing window is completed (CPU = 0:00:09.1, REAL = 0:00:00.0, MEM = 2400.3M)
Starting SI iteration 2
Start delay calculation (fullDC) (1 T). (MEM=2329.38)
Glitch Analysis: View av_func_mode_max -- Total Number of Nets Skipped = 0.
Glitch Analysis: View av_func_min -- Total Number of Nets Analyzed = 26099.
Total number of fetched objects 26099
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
AAE_INFO-618: Total number of nets in the design is 26048, 0.1 percent of the nets selected for SI analysis
End delay calculation. (MEM=2368.55 CPU=0:00:09.1 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=2368.55 CPU=0:00:09.2 REAL=0:00:01.0)
*** Done Building timing Graph (cpu=0:00:12.2 real=0:00:12.0 totSessionCpu=0:01:54 mem=2368.5M)

-----timeDesign Summary-----
-----Setup views included:
av_func_mode_max
-----Setup mode +-----+-----+-----+
|      Setup mode |      all |      reg2reg |      default |
+-----+-----+-----+
|      MWS (ns) | 0.055 | 0.158 | 0.055 |
|      TNS (ns) | 0.000 | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 | 0 |
| All Paths: | 1415 | 688 | 727 |
+-----+-----+-----+
-----DRVs +-----+-----+-----+
|      DRVs |      Real |      Total |
+-----+-----+-----+
|      Nr nets(terms) |      Worst Vio |      Nr nets(terms) |
+-----+-----+-----+
|      max_cap | 0 (0) | 0.000 | 0 (0) |
|      max_tran | 0 (0) | 0.000 | 0 (0) |
|      max_fanout | 0 (0) | 0 | 0 (0) |
|      max_length | 0 (0) | 0 | 0 (0) |
+-----+-----+-----+
Density: 39.995%
(127.11% with Fillers)
Reported timing to dir timingReports
Total CPU time: 91.26 sec
Total Real time: 93.0 sec
Total Memory Usage: 2361.671875 Mbytes
Reset AAE Options
**INFO: timeDesign #1 [finish] : cpu/real = 0:01:31.3/0:01:33.5 (1.0), totSession cpu/real = 0:01:55.6/0:03:01.9 (0.6), mem = 2361.7M
innovus 5> ■

```

The terminal window displays the IQuantum Extraction engine log for a Post-Route setup time analysis. It starts with the extraction being closed and the fullchip extraction being done. It then begins a delay calculation for setup views, starting with SI iteration 1 using infinite timing windows. The log shows various noise library and CDB files being loaded. It includes several warning messages about cells like 'XMD' and 't2g265D' not having characterized noise models. The log continues through multiple iterations of delay calculations, reporting on the number of nets, memory usage, and total execution time. It ends with a summary of the timing design, including setup views, driver statistics, and density information.

## 5. Post-Route hold time analysis :

Instructions: After completing the analysis, capture a screenshot of the results displayed in the terminal (including the timeDesign Summary).

```
ee22.sj.ice.nycu.edu.tw (kclab164)
Terminal Sessions View Xserver Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
Quick connect...
+-----+-----+-----+-----+
| max_cap | 0 (0) | 0.000 | 0 (0) |
| max_tran | 0 (0) | 0.000 | 0 (0) |
| max_fanout | 0 (0) | 0 | 0 (0) |
| max_length | 0 (0) | 0 | 0 (0) |
+-----+-----+-----+-----+
20 Density: 39.995%
(127.110% with Fillers)
Total number of glitch violations: 0
Reported timing to dir timingReports
Total CPU time: 12.5 sec
Total real time: 13.0 sec
Total Memory Usage: 2314.382812 Mbytes
Reset AAE Options
*** timeDesign #1 [finish] : cpu/real = 0:00:13.1:00:01:33.5 (1.0), totSession.cpu/real = 0:01:55.6:0/03:01.9 (0.6), mem = 2361.7M
*** timeDesign #2 [begin] : totSession.cpu/real = 0:02:03.3:0/05:1.6 (0.4), mem = 2365.8M
Reset EOS DB
Ignoring AAE DB Resetting ...
Extraction called for design 'CHIP' of instances=79494 and nets=26048 using extraction engine 'postRoute' at effort level 'high' .
No corner found or region found. No need to perform incremental extraction.
Starting delay calculation for Hold views
AAE INFO: resetNetProps viewIdx 1
Starting SI iteration 1 using Instantaneous Timing Windows
#####
# Design Stage Postroute
# Design Name: CHIP
# Design Mode: 18nm
# Analysis Mode: MMEC QV
# Extraction Engine: PPE/RCOB
# Signoff Settings: SI On
#####
20 AAE INFO: 1 threads acquired from CTE
Start calculating objects (1), (MEM=2335.8)
Start calculating scaling factor for lib_min libraries using the default operating condition of each library.
Total number of fetched objects 26099
20 AAE INFO: Total number of nets for which stage creation was skipped for all views 0
20 AAE INFO: 618: Total number of nets in the design is 26048. 100.0 percent of the nets selected for SI analysis
20 AAE INFO: Total number of nets for which stage creation was skipped for all views 0
End delay calculation (fullDC) (MEM=2379.84 CPU=0:00:08.5 REAL=0:00:09.0)
20 Loading CTE timing window with TwFlowType 0... (CPU = 0:00:00.0, REAL = 0:00:00.0, MEM = 2379.8M)
20 Add other clocks and setupctet0AEClockMapping during iter 1
20 Loading CTE timing window is completed (CPU = 0:00:00.1, REAL = 0:00:00.0, MEM = 2379.8M)
20 Start delay calculation (fullDC) (1), (MEM=2351.95)
20 Glitch Analysis: View av_func_mode_min -- Total Number of Nets Skipped = 0.
20 Glitch Analysis: View av_func_mode_min -- Total Number of Nets Analyzed = 26099.
20 AAE INFO: Total number of nets for which stage creation was skipped for all views 0
20 AAE INFO: Total number of nets in the design is 26048. 100.0 percent of the nets selected for SI analysis
20 End delay calculation. (MEM=2391.12 CPU=0:00:00.1 REAL=0:00:00.0)
20 End delay calculation (fullDC). (MEM=2391.12 CPU=0:00:00.2 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:10.5 real=0:00:11.0 totSessionCpu=0:02:15 mem=2391.1M)
20
timeDesign Summary
20
Hold views included:
av_func_mode_min
20
+-----+-----+-----+-----+
| Hold mode | all | regreg | default |
+-----+-----+-----+-----+
| WNS (ns): | 0.265 | 0.265 | 5.045 |
| TNS (ns): | 0.000 | 0.000 | 0.000 |
| Violations (Paths): | 0 | 0 | 0 |
| All Paths: | 1415 | 688 | 727 |
+-----+-----+-----+-----+
20 Density: 39.995%
(127.110% with Fillers)
Reported timing to dir timingReports
Total CPU time: 12.5 sec
Total real time: 13.0 sec
Total Memory Usage: 2314.382812 Mbytes
Reset AAE Options
*** timeDesign #2 [finish] : cpu/real = 0:00:12.5:0/00:12.8 (1.0), totSession cpu/real = 0:02:15.8:0/06:04.5 (0.4), mem = 2314.4M
innovus> 
```

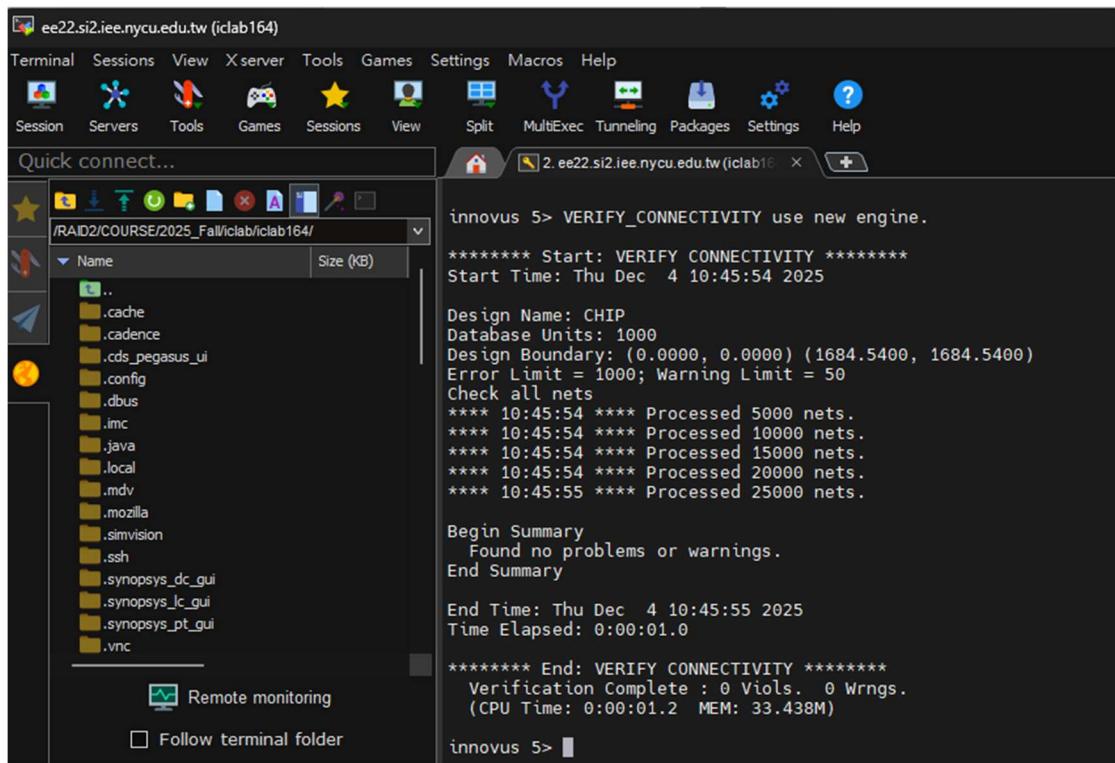
## 6. DRC result:

```
ee22.ee22.sie.ncyu.edu.tw (lab164)
Terminal Sessions View Xserver Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
Quick connect...
[2. ee22.ee22.sie.ncyu.edu.tw (lab164)]
RAD25COURSE/2025_Fall/lab164/
Name Size (kB) Le
.. 20
.cache 20
.cadence 20
.cds_pegasus_id 20
.config 20
.dv 20
.jnc 20
.java 20
.local 20
.mdv 20
.mozilla 20
.senvision 20
.ash 20
synopsys_dc_dsl 20
synopsys_lc_dsl 20
synopsys_pc_gsl 20
.vnc 20
2025_F_OF 20
Desktop 20
Documents 20
Downloads 20
Lab01_2025P 20
Lab02 20
Lab03 20
Lab04 20
Lab05_2025P 20
Lab06 20
Lab07 20
Lab08 20
Lab09 20
Lab11_2025P 20
Lab11_2025R 20
Lab12_2025R 20
Midterm_Project_2025 20
Music - 20
mWaveLog 20
pdfs 20
Pictures 20
Public 20
Templates 20
Transient_drives 20
Video 20
.bash 1
.bash_profile 1
.bashrc 1
.flexhrc 1
.history 6
.iCAuthentity 2
.iCache 1
.inf00000000311e33c2e0003... 128
.inf00000000311e4ec4000... 128
.inf00000000311e4ec20004... 128
.inf00000000311e5650003... 128
.inf00000000311e5660004... 128
.inf00000000311e5670003... 128
.inf00000000311e5690006... 128
.verd_oresearch_history.log 0
.Jauthrc 2
.kerberos-errors 0
.novice.conf 4
.novice.rc 33
VERIFY DRC ..... Sub-Area: {967,680 241,920 1209,600 483,840} 12 of 49
VERIFY DRC ..... Sub-Area: {1209,600 241,920 1451,520 483,840} 13 of 49
VERIFY DRC ..... Sub-Area: {1451,520 241,920 1684,540 483,840} 14 of 49
VERIFY DRC ..... Sub-Area: {14 complete 0 Viols.}
VERIFY DRC ..... Sub-Area: {0,000 483,840 241,920 725,760} 15 of 49
VERIFY DRC ..... Sub-Area: {241,920 483,840 493,840 725,760} 16 of 49
VERIFY DRC ..... Sub-Area: {16 complete 0 Viols.}
VERIFY DRC ..... Sub-Area: {483,840 483,840 725,760 725,760} 17 of 49
VERIFY DRC ..... Sub-Area: {18 complete 0 Viols.}
VERIFY DRC ..... Sub-Area: {567,680 483,840 1209,600 725,760} 18 of 49
VERIFY DRC ..... Sub-Area: {19 complete 0 Viols.}
VERIFY DRC ..... Sub-Area: {1209,600 483,840 1451,520 725,760} 19 of 49
VERIFY DRC ..... Sub-Area: {20 complete 0 Viols.}
VERIFY DRC ..... Sub-Area: {1451,520 483,840 1684,540 725,760} 20 of 49
VERIFY DRC ..... Sub-Area: {21 complete 0 Viols.}
VERIFY DRC ..... Sub-Area: {0,000 725,760 241,920 967,680} 22 of 49
VERIFY DRC ..... Sub-Area: {241,920 725,760 493,840 967,680} 23 of 49
VERIFY DRC ..... Sub-Area: {23 complete 0 Viols.}
VERIFY DRC ..... Sub-Area: {483,840 725,760 725,760 967,680} 24 of 49
VERIFY DRC ..... Sub-Area: {24 complete 0 Viols.}
VERIFY DRC ..... Sub-Area: {1451,520 725,760 967,680 967,680} 25 of 49
VERIFY DRC ..... Sub-Area: {567,680 725,760 1209,600 967,680} 26 of 49
VERIFY DRC ..... Sub-Area: {25 complete 0 Viols.}
VERIFY DRC ..... Sub-Area: {1209,600 725,760 1451,520 967,680} 27 of 49
VERIFY DRC ..... Sub-Area: {1451,520 725,760 1684,540 967,680} 28 of 49
VERIFY DRC ..... Sub-Area: {26 complete 0 Viols.}
VERIFY DRC ..... Sub-Area: {0,000 967,680 241,920 1209,600} 29 of 49
VERIFY DRC ..... Sub-Area: {241,920 967,680 483,840 1209,600} 30 of 49
VERIFY DRC ..... Sub-Area: {30 complete 0 Viols.}
VERIFY DRC ..... Sub-Area: {483,840 967,680 725,760 1209,600} 31 of 49
VERIFY DRC ..... Sub-Area: {31 complete 0 Viols.}
VERIFY DRC ..... Sub-Area: {1209,600 967,680 1451,520 1209,600} 32 of 49
VERIFY DRC ..... Sub-Area: {32 complete 0 Viols.}
VERIFY DRC ..... Sub-Area: {567,680 967,680 1209,600 1209,600} 33 of 49
VERIFY DRC ..... Sub-Area: {33 complete 0 Viols.}
VERIFY DRC ..... Sub-Area: {1209,600 967,680 1451,520 1209,600} 34 of 49
VERIFY DRC ..... Sub-Area: {34 complete 0 Viols.}
VERIFY DRC ..... Sub-Area: {1451,520 967,680 1684,540 1209,600} 35 of 49
VERIFY DRC ..... Sub-Area: {35 complete 0 Viols.}
VERIFY DRC ..... Sub-Area: {0,000 1209,600 241,920 1451,520} 36 of 49
VERIFY DRC ..... Sub-Area: {241,920 1209,600 483,840 1451,520} 37 of 49
VERIFY DRC ..... Sub-Area: {37 complete 0 Viols.}
VERIFY DRC ..... Sub-Area: {483,840 1209,600 725,760 1451,520} 38 of 49
VERIFY DRC ..... Sub-Area: {1209,600 1209,600 967,680 1451,520} 39 of 49
VERIFY DRC ..... Sub-Area: {39 complete 0 Viols.}
VERIFY DRC ..... Sub-Area: {567,680 1209,600 1209,600 1451,520} 40 of 49
VERIFY DRC ..... Sub-Area: {40 complete 0 Viols.}
VERIFY DRC ..... Sub-Area: {1209,600 1209,600 1451,520 1451,520} 41 of 49
VERIFY DRC ..... Sub-Area: {41 complete 0 Viols.}
VERIFY DRC ..... Sub-Area: {1451,520 1209,600 1684,540 1451,520} 42 of 49
VERIFY DRC ..... Sub-Area: {42 complete 0 Viols.}
VERIFY DRC ..... Sub-Area: {0,000 1684,540 241,920 1684,540} 43 of 49
VERIFY DRC ..... Sub-Area: {241,920 1684,540 483,840 1684,540} 44 of 49
VERIFY DRC ..... Sub-Area: {44 complete 0 Viols.}
VERIFY DRC ..... Sub-Area: {483,840 1684,540 725,760 1684,540} 45 of 49
VERIFY DRC ..... Sub-Area: {725,760 1684,540 1451,520 1684,540} 46 of 49
VERIFY DRC ..... Sub-Area: {46 complete 0 Viols.}
VERIFY DRC ..... Sub-Area: {567,680 1684,540 1451,520 1684,540} 47 of 49
VERIFY DRC ..... Sub-Area: {47 complete 0 Viols.}
VERIFY DRC ..... Sub-Area: {1209,600 1684,540 1451,520 1684,540} 48 of 49
VERIFY DRC ..... Sub-Area: {1451,520 1451,520 1684,540 1684,540} 49 of 49
VERIFY DRC ..... Sub-Area: {49 complete 0 Viols.}

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:04.1 ELAPSED TIME: 4.00 MEM: 41.0M) ***
innovus 5> 
```

## 7. LVS result :



The screenshot shows a terminal window titled "innovus 5> VERIFY\_CONNECTIVITY use new engine." The window displays the output of a "VERIFY CONNECTIVITY" command. The output includes the start time (Thu Dec 4 10:45:54 2025), design name (CHIP), database units (1000), and boundary coordinates (0.0000, 0.0000) to (1684.5400, 1684.5400). It also shows error and warning limits (Error Limit = 1000; Warning Limit = 50), and a log of processed nets from 10:45:54 to 10:45:55. The summary indicates no problems or warnings found. The end time is Thu Dec 4 10:45:55 2025, and the total time elapsed is 0:00:01.0. The verification was complete with 0 violations and 0 wrongs, using 33.438M of memory.

```
innovus 5> VERIFY_CONNECTIVITY use new engine.

***** Start: VERIFY CONNECTIVITY *****
Start Time: Thu Dec 4 10:45:54 2025

Design Name: CHIP
Database Units: 1000
Design Boundary: (0.0000, 0.0000) (1684.5400, 1684.5400)
Error Limit = 1000; Warning Limit = 50
Check all nets
**** 10:45:54 **** Processed 5000 nets.
**** 10:45:54 **** Processed 10000 nets.
**** 10:45:54 **** Processed 15000 nets.
**** 10:45:54 **** Processed 20000 nets.
**** 10:45:55 **** Processed 25000 nets.

Begin Summary
    Found no problems or warnings.
End Summary

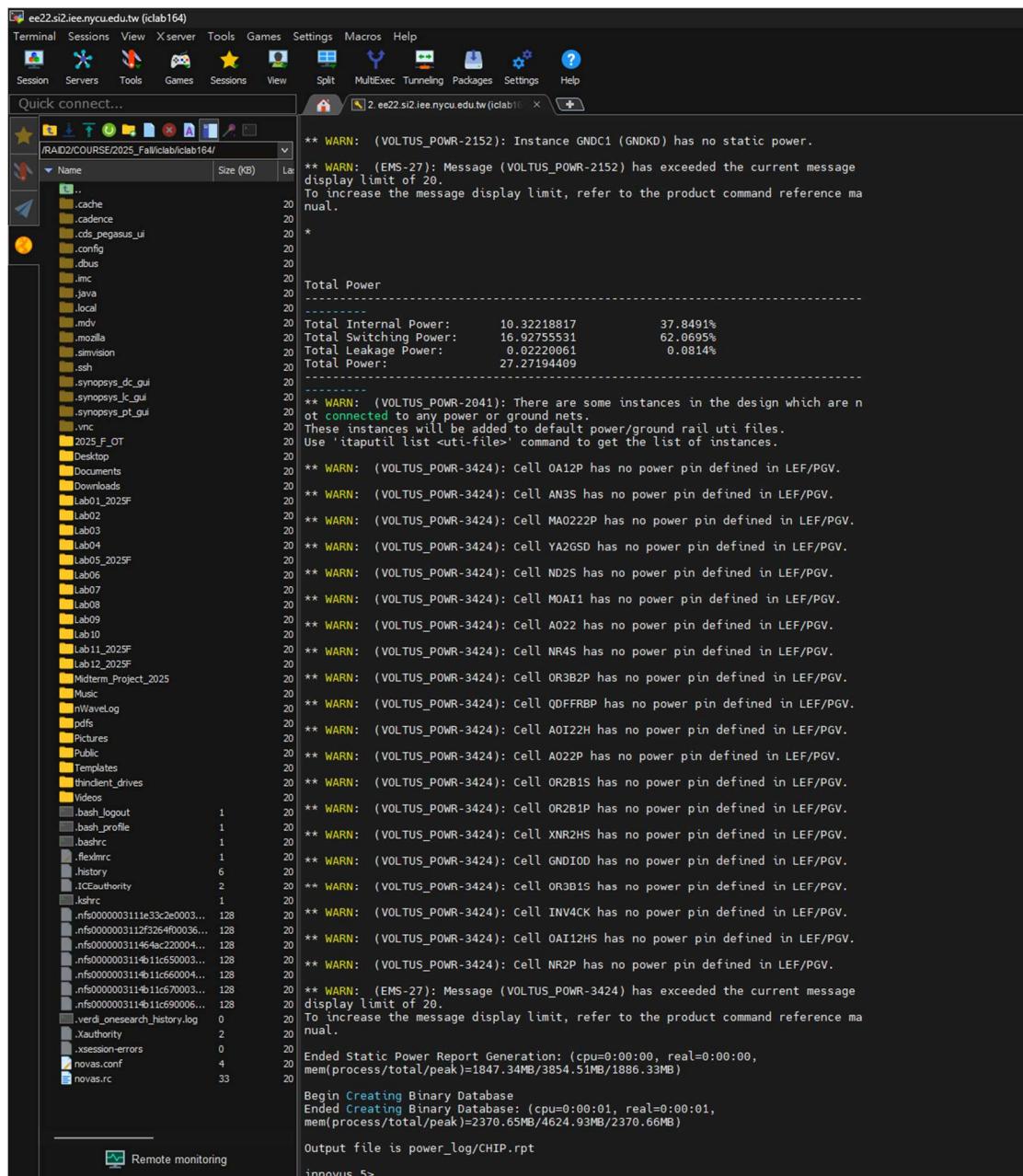
End Time: Thu Dec 4 10:45:55 2025
Time Elapsed: 0:00:01.0

***** End: VERIFY CONNECTIVITY *****
Verification Complete : 0 Viols. 0 Wrngs.
(CPU Time: 0:00:01.2 MEM: 33.438M)

innovus 5>
```

## **8. Post Layout simulation result :**

## 9. Power result :



The screenshot shows a terminal window titled "ee22.si2.iee.nycu.edu.tw (iclab164)" with the following content:

```

Terminal Sessions View Xserver Tools Games Settings Macros Help
Session Servers Tools Games Sessions View
Split MultiExec Tunneling Packages Settings Help

Quick connect...
2. ee22.si2.iee.nycu.edu.tw (iclab164)

RAID2/COURSE/2025_Fall/iclab/iclab164/
Name Size (KB) Last modified
.t...
.cache 20
.cadence 20
.cds_pegasus_ui 20
.config 20
.dbus 20
.lmc 20
.java 20
.local 20
.mdv 20
.mozilla 20
.simvision 20
.vnc 20
.ssh 20
.synopsys_dc_gui 20
.synopsys_lc_gui 20
.synopsys_pt_gui 20
.vnc 20
2025_F_OT 20
Desktop 20
Documents 20
Downloads 20
Lab01_2025F 20
Lab02 20
Lab03 20
Lab04 20
Lab05_2025F 20
Lab06 20
Lab07 20
Lab08 20
Lab09 20
Lab10 20
Lab11_2025F 20
Lab12_2025F 20
Midterm_Project_2025 20
Music 20
nvWaveLog 20
pdfs 20
Pictures 20
Public 20
Templates 20
thirdclient_drives 20
Videos 20
.bash_logout 1
.bash_profile 1
.bashrc 1
.flexlmc 1
.history 6
.tCEauthority 2
.kshrc 1
.nfs000000311e33c2e0003... 128
.nfs000000312f324f00036... 128
.nfs000000311e33c2e0004... 128
.nfs000000311e33c2e0005... 128
.nfs000000311e33c2e0006... 128
.verdi_onsearch_history.log 0
.xauthority 2
.xsession-errors 0
.novas.conf 4
.novas.rc 33

** WARN: (VOLTUS_POWR-2152): Instance GNDKD has no static power.
** WARN: (EMS-27): Message (VOLTUS_POWR-2152) has exceeded the current message display limit of 20.
To increase the message display limit, refer to the product command reference manual.

Total Power
-----
Total Internal Power: 10.32218817 37.8491%
Total Switching Power: 16.92755531 62.0695%
Total Leakage Power: 0.02220061 0.0814%
Total Power: 27.27194409

** WARN: (VOLTUS_POWR-2041): There are some instances in the design which are not connected to any power or ground nets.
These instances will be added to default power/ground rail uti files.
Use 'itaputil list <uti-file>' command to get the list of instances.

** WARN: (VOLTUS_POWR-3424): Cell OA12P has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell AN3S has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell MA022P has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell YA2GSD has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell ND2S has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell MOAI1 has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell A022 has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell NR4S has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): cell OR3B2P has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): cell QDFFRBP has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): cell A0I22H has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): cell A022P has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): cell OR2B1S has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): cell OR2B1P has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): cell XNR2HS has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): cell GNDIOD has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): cell OR3B1S has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell INV4CK has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell OAI12HS has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell NR2P has no power pin defined in LEF/PGV.

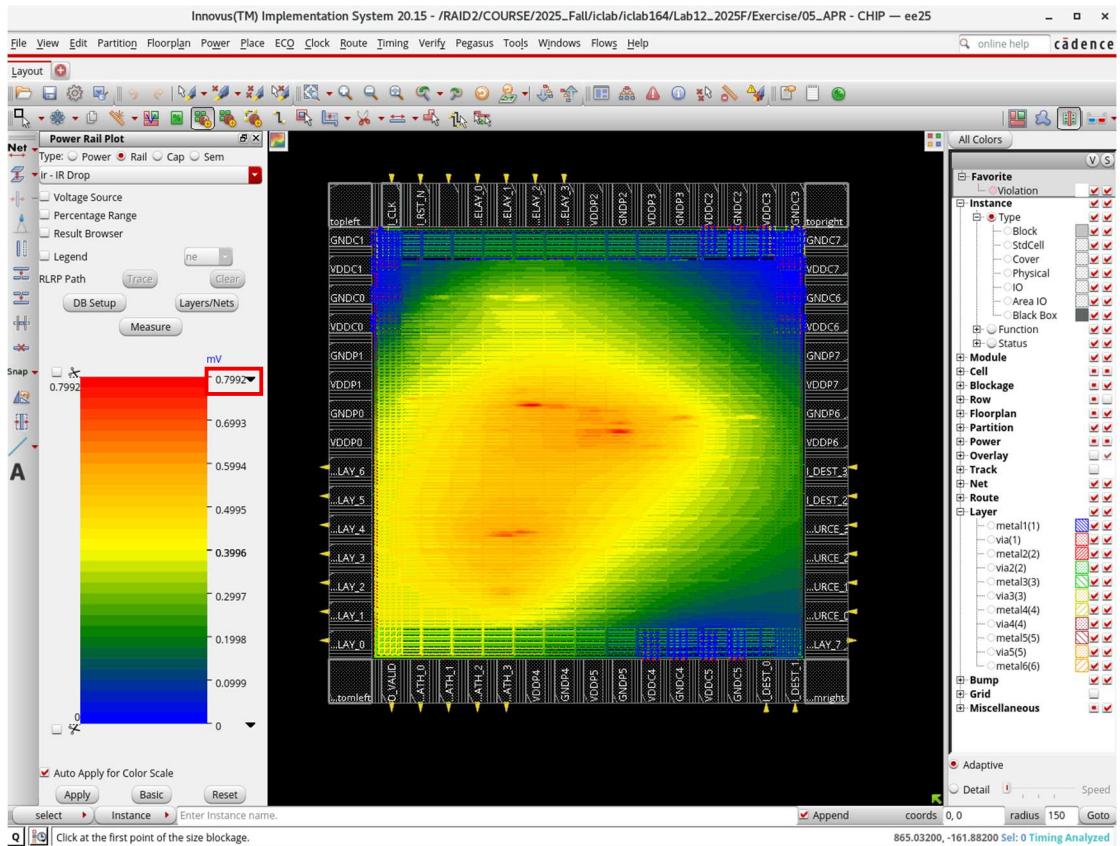
** WARN: (EMS-27): Message (VOLTUS_POWR-3424) has exceeded the current message display limit of 20.
To increase the message display limit, refer to the product command reference manual.

Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00,
mem(process/total/peak)=1847.34MB/3854.51MB/1886.33MB)
Begin Creating Binary Database
Ended Creating Binary Database: (cpu=0:00:01, real=0:00:01,
mem(process/total/peak)=2370.65MB/4624.93MB/2370.66MB)
Output file is power_log/CHIP.rpt
innovus 5>

```

The terminal also displays a "Remote monitoring" icon at the bottom.

## 10. IR Drop Results :



IR drop 最大值為 **0.7992 mV** < 1 mV < 0.1 V

增加更多 power pad / ring / stripe 等可以改善 IR drop。  
跟 Lab11 相比，在 Lab 12 我用了兩倍的 power pad。