

Compal Confidential

Schematics Document

PAW20

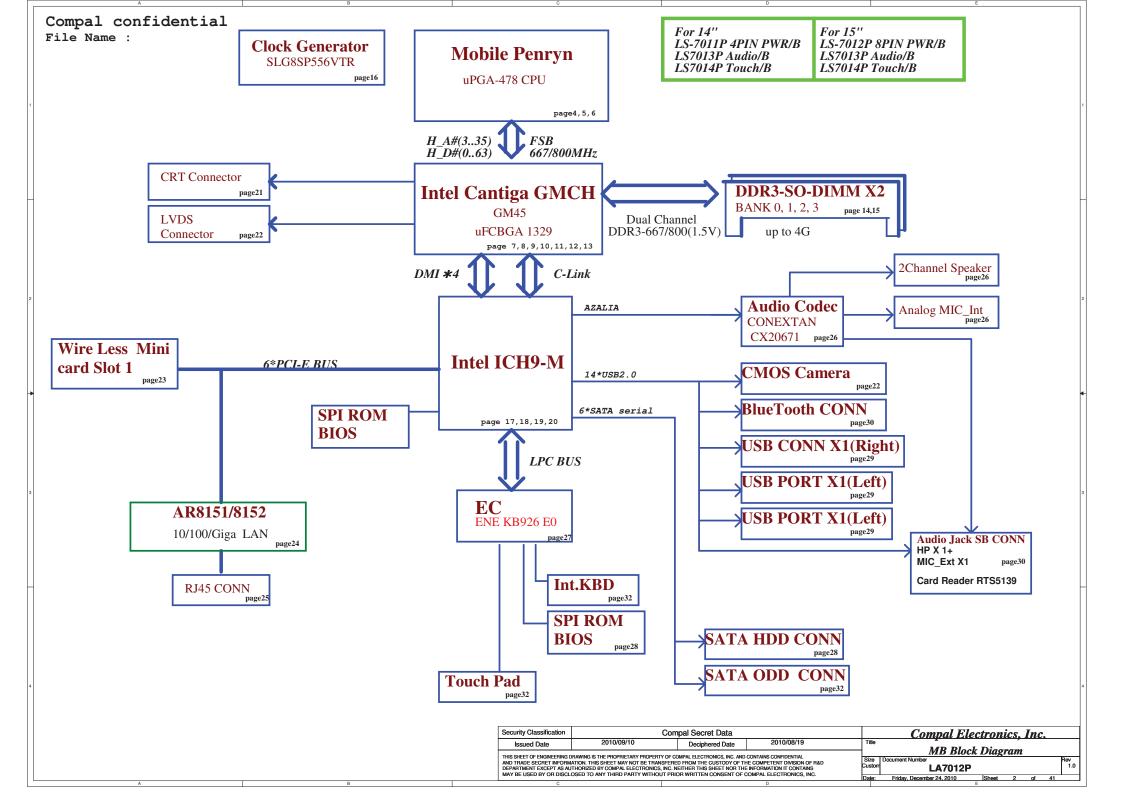
Montevina

with Intel Cantiga + ICH9 core logic

REV: 1.0A

2010-12-24

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DDR3 Voltage Rails

power plane	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +CPU_CORE +VGA_CORE +1.8VS
State				+1.05VS
so	0	0	0	0
s3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	х	X	х	х

SMBUS Control Table

	SOURCE	BATT	KB926	SODIMM	CLK CHIP	WLAN WWAN	ICH9	Therml
EC_SMB_CK1 EC_SMB_DA1	KB926 + 3VALW	V +3VALW	Х	Х	Х	Х	Х	Х
EC_SMB_CK2 EC_SMB_DA2	KB926 + 3VALW	Х	Х	Х	Х	Χ	Х	+3VS
ICH_SMBCLK ICH_SMBDATA	ICH +3VALW	Х	Х	V +3VS	+3VS	+ 3VALW	Х	Х

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM	A0	10100000
BDR SO-DIMM	A4	10100100
€LOCK GENERATOR (EXT.)	D2	11010010

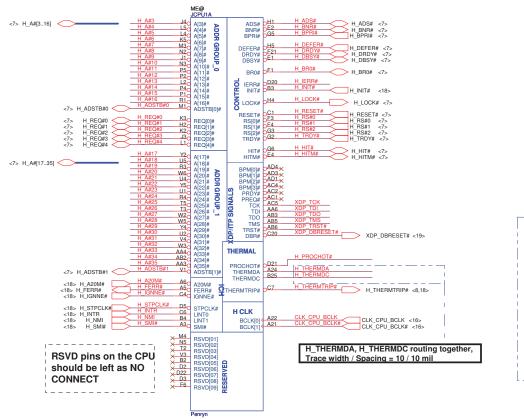
@ FUNCTION

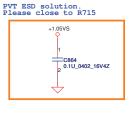
Structure	Description	NON-USE
45@	45 BOM	
BT@	Blue Tooth function	
CMOS@	CMOS CAMERA function	

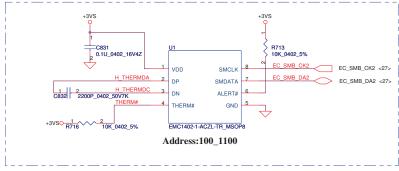
PCIE PORT LIST PORT DEVICE 1 LAN 2 3 3 WLAN 4 5 6 7 8 8

USB	PORT LIST
PORT	DEVICE
0	RIGHT SIDE
1	LEFT SIDE
2	CMOS
3	
4	CARD READER
5	WIRELESS
6	BT
7	USB PORT(ESATA)
8	
9	
10	
11	
12	
13	

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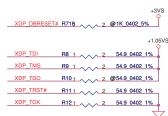


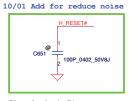
+1.05VS

H_IERR# R714 1 2 56 0402 5%

H_PROCHOT# R715 1 _____ 2 68 0402 5%

XDP Reserve for debug , Please close to CPU side $\,$





XDP_DBRESET#

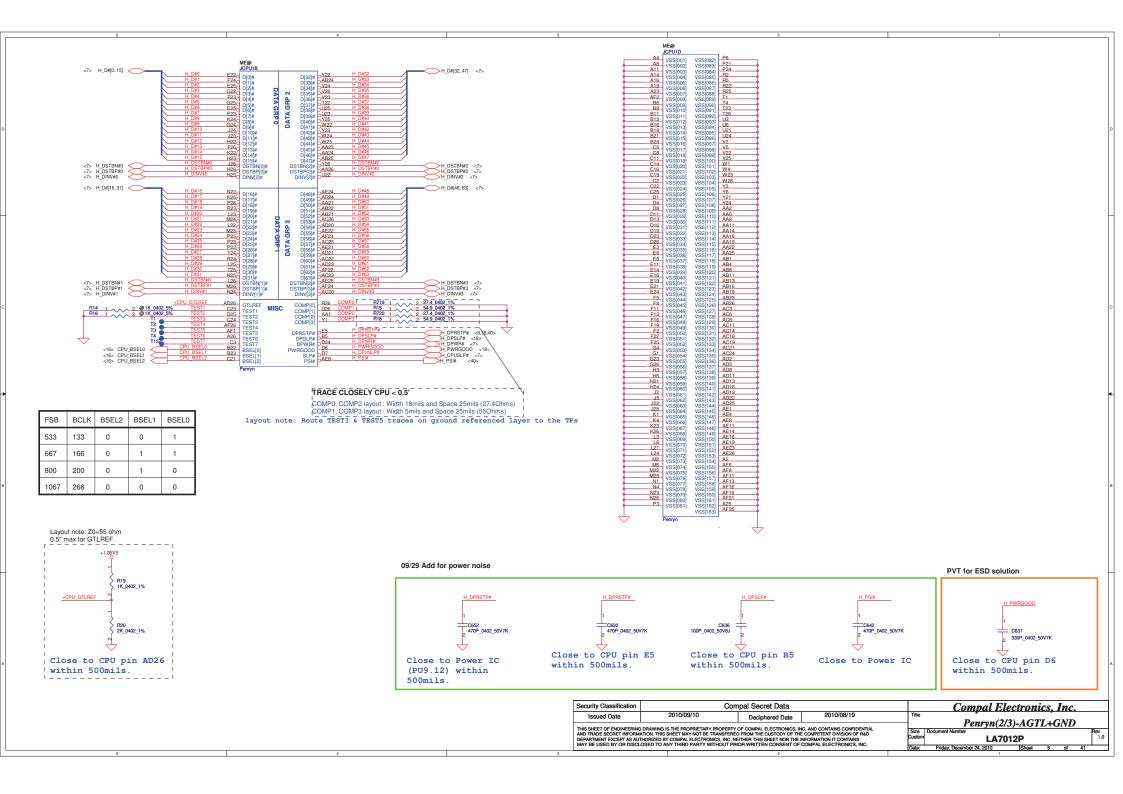
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C834
0.1U_0402_16V4Z

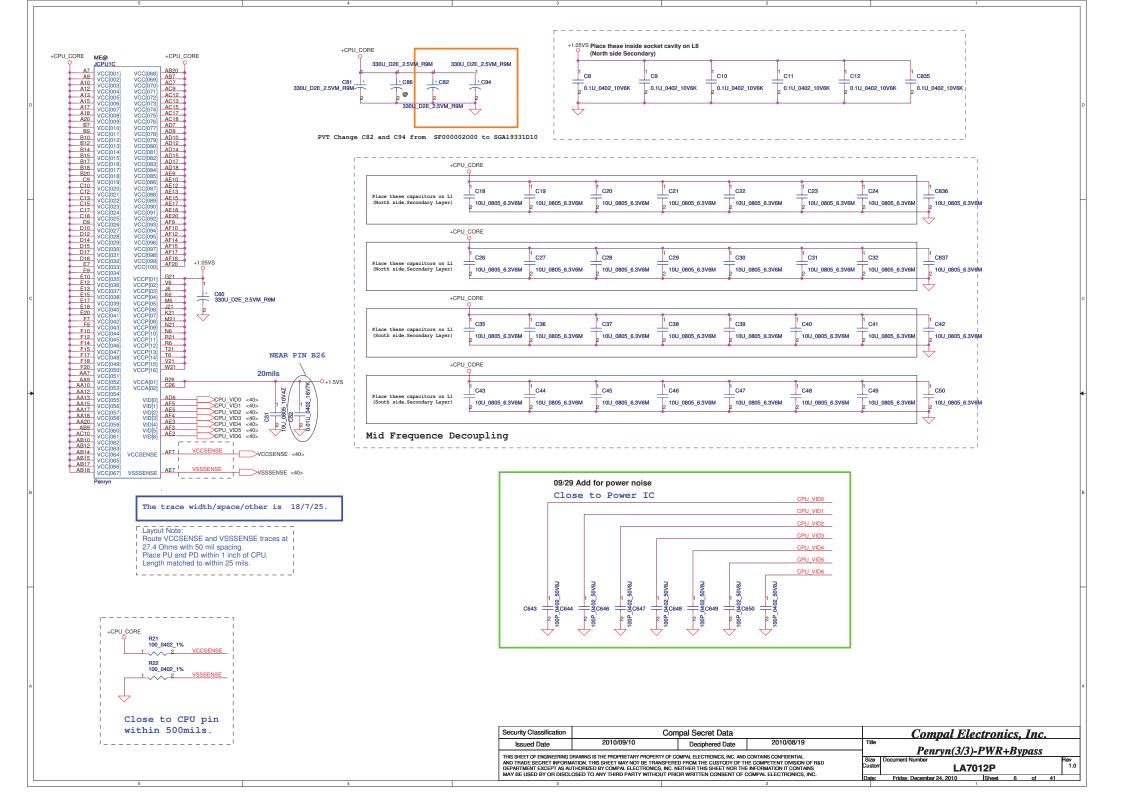
09/16 Add C834 For ESD

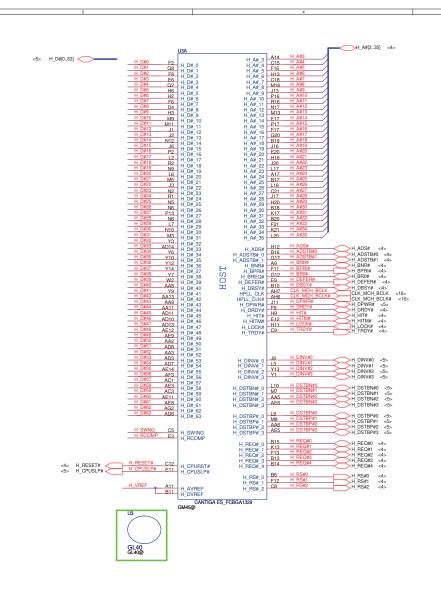
Place closely pin C1

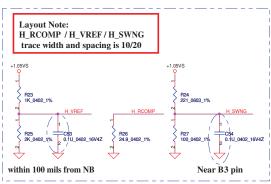
Place closely pin C20

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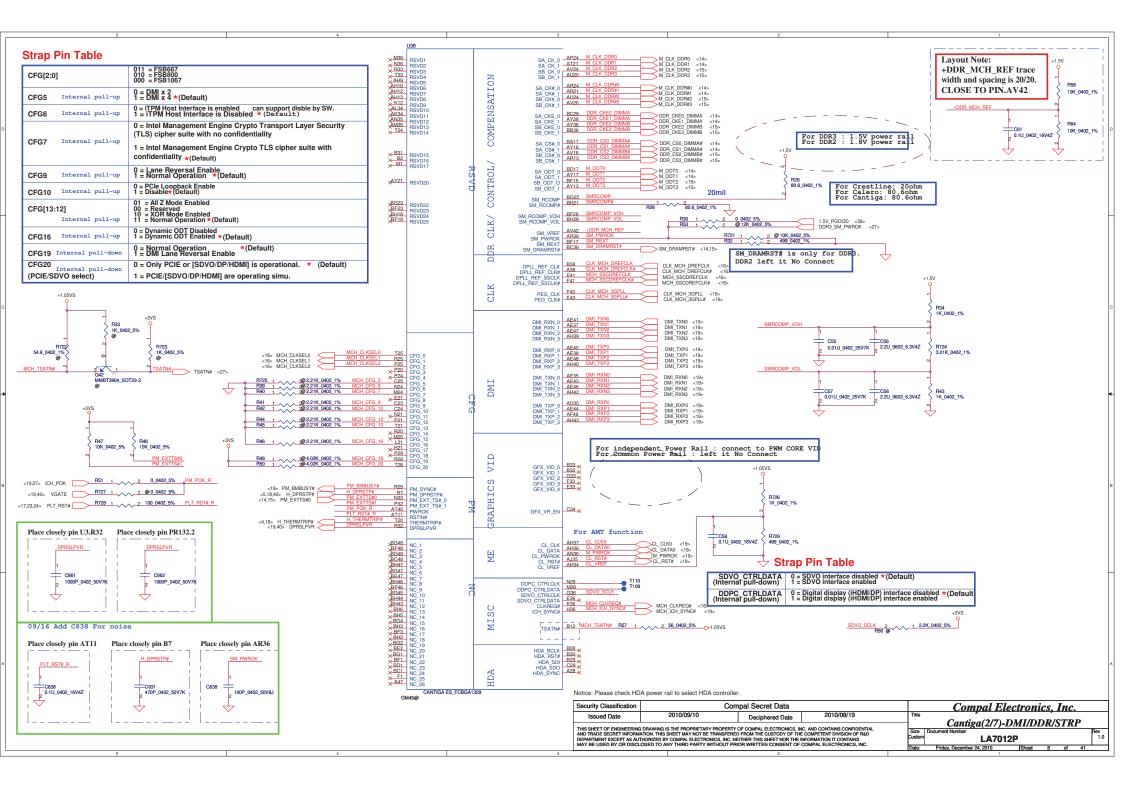


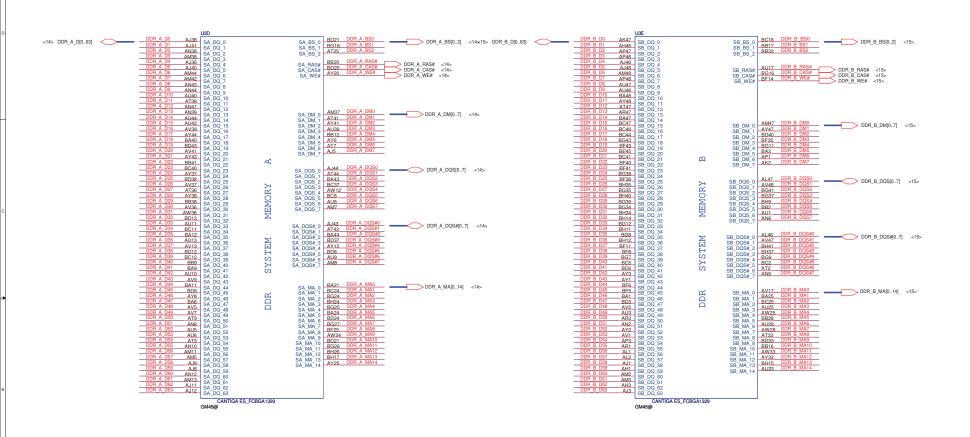
PVT ESD solution.

Please close to R23

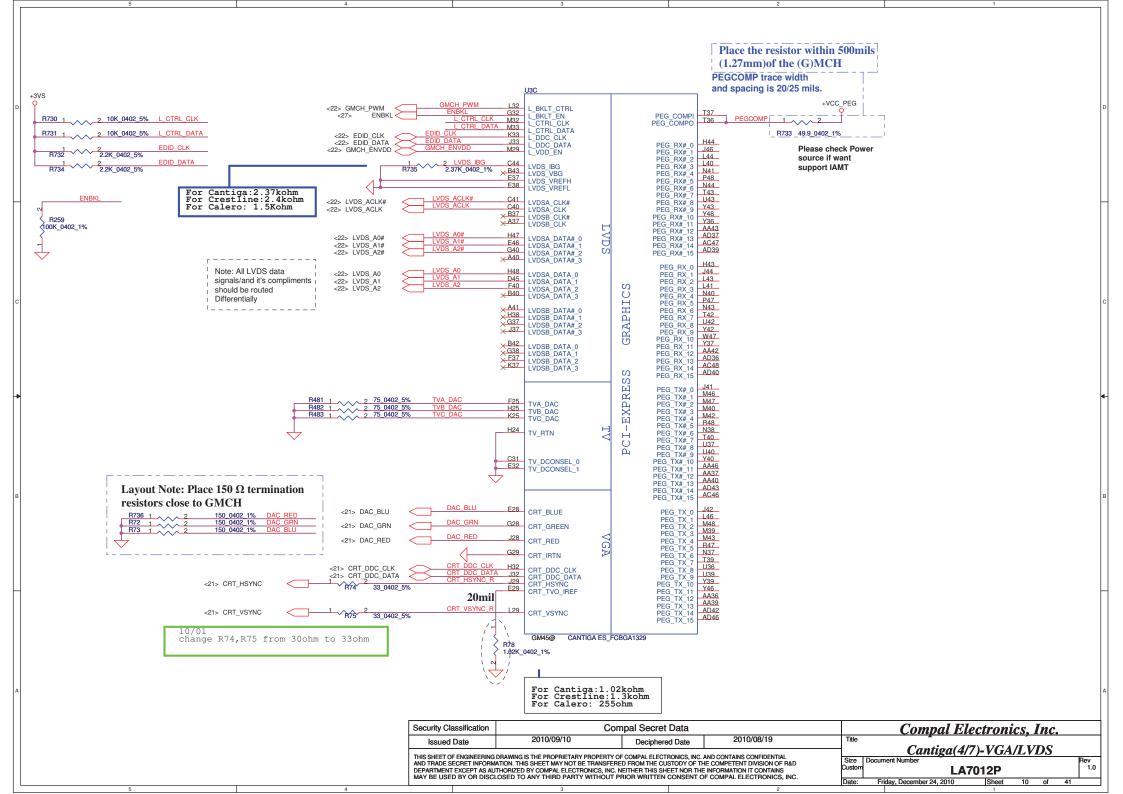


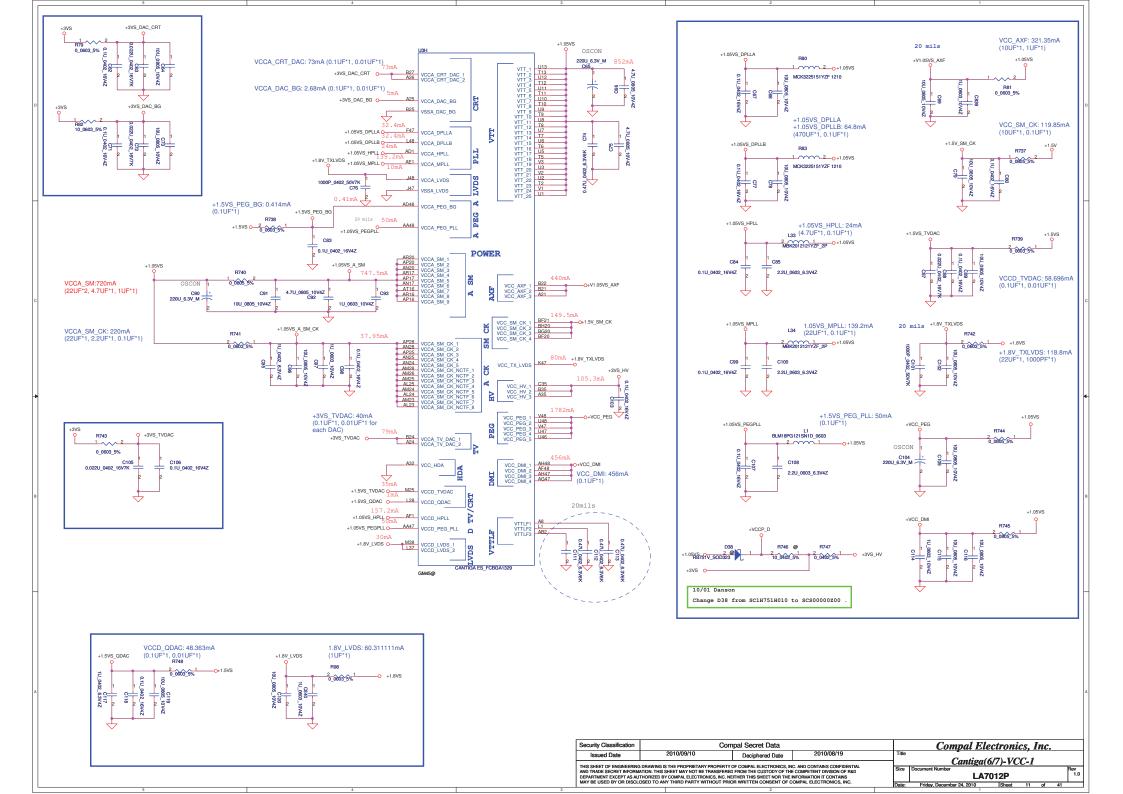
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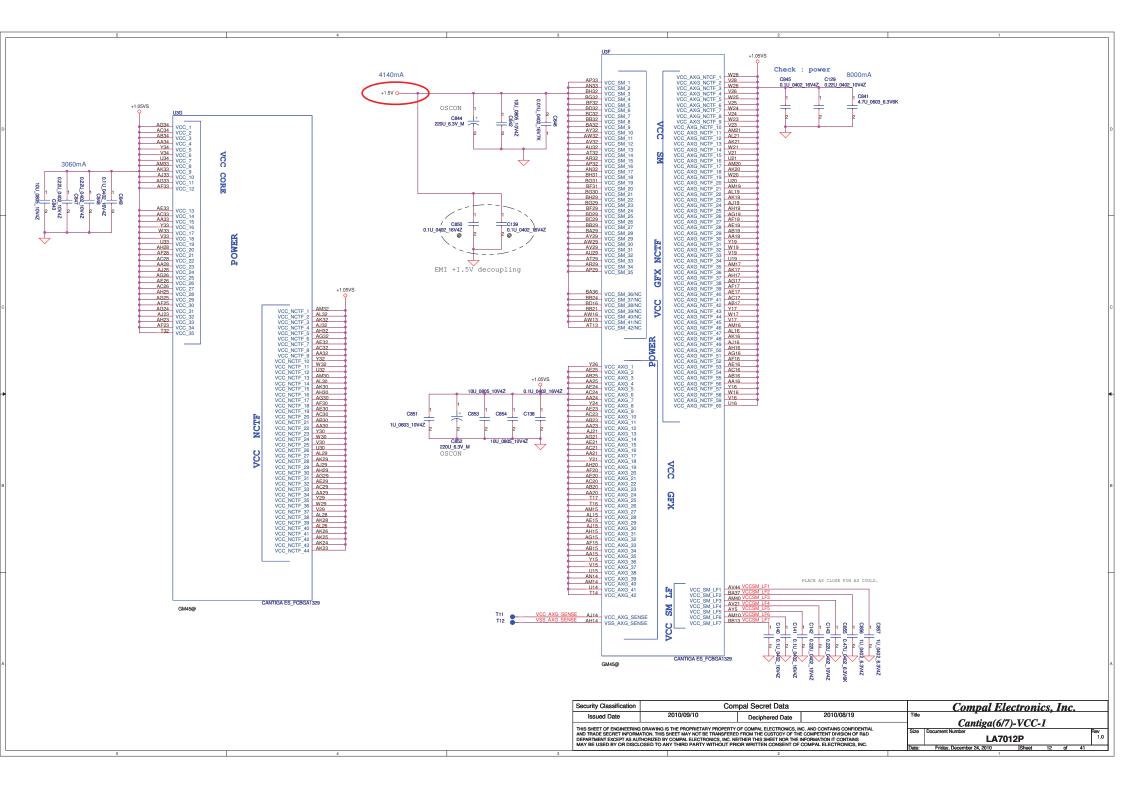


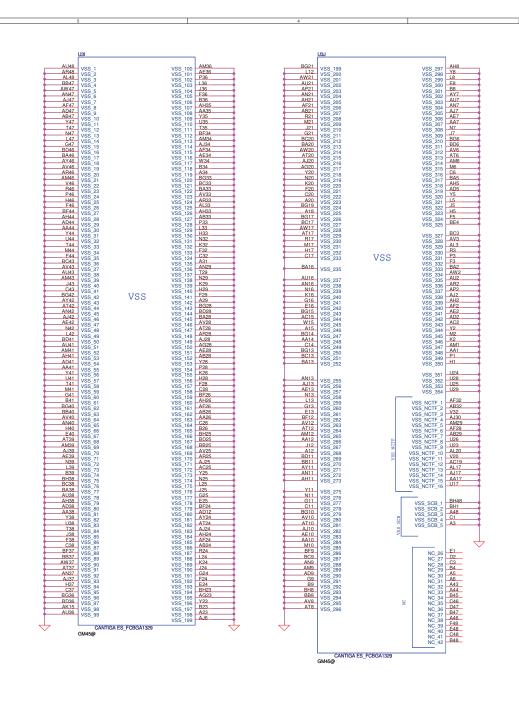


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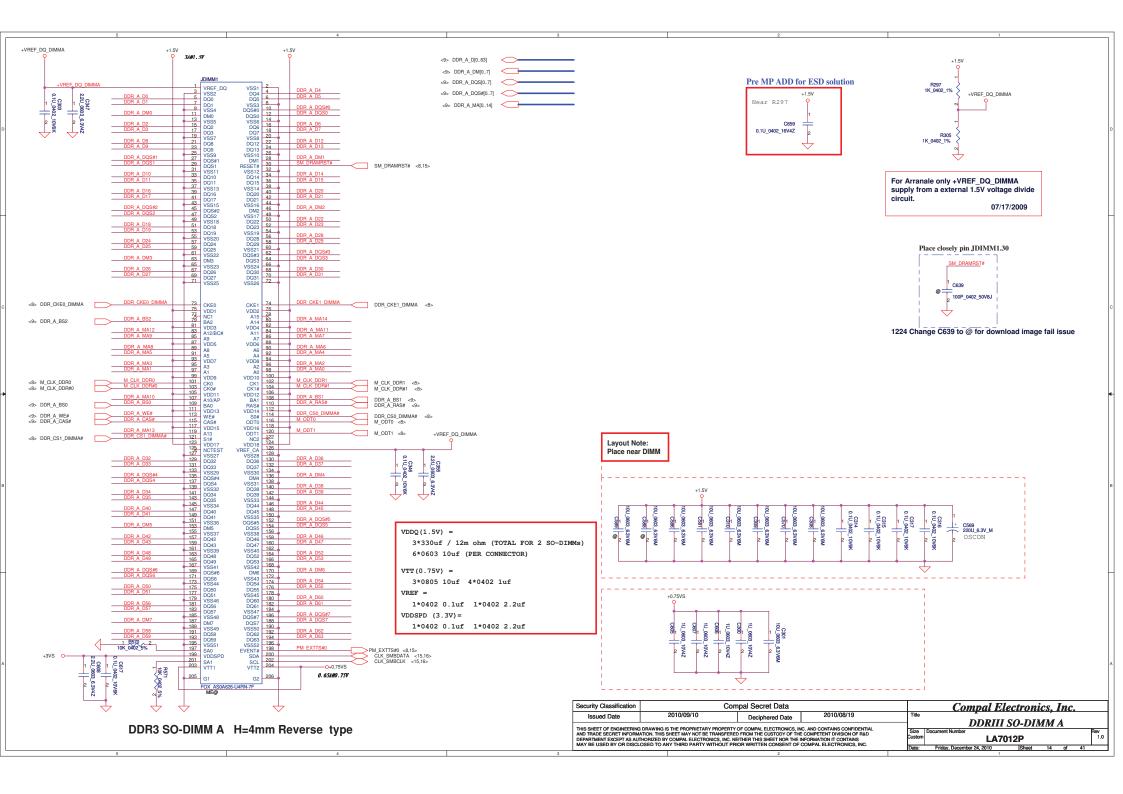


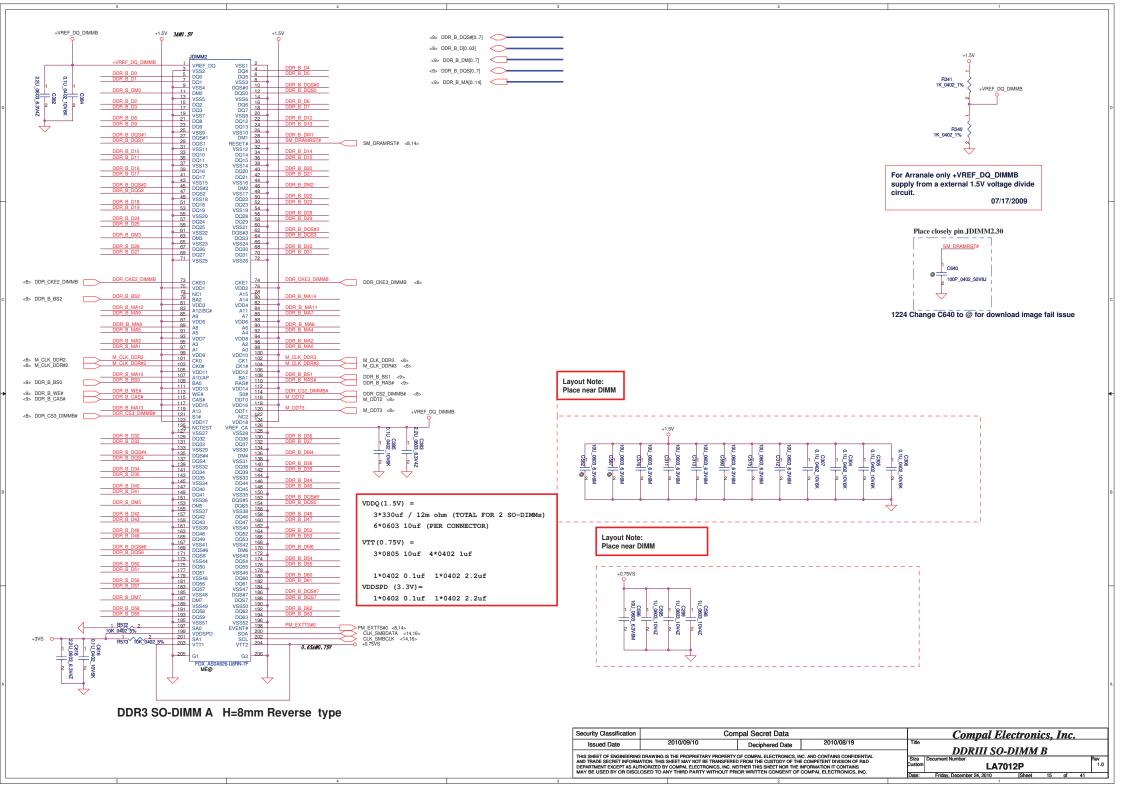


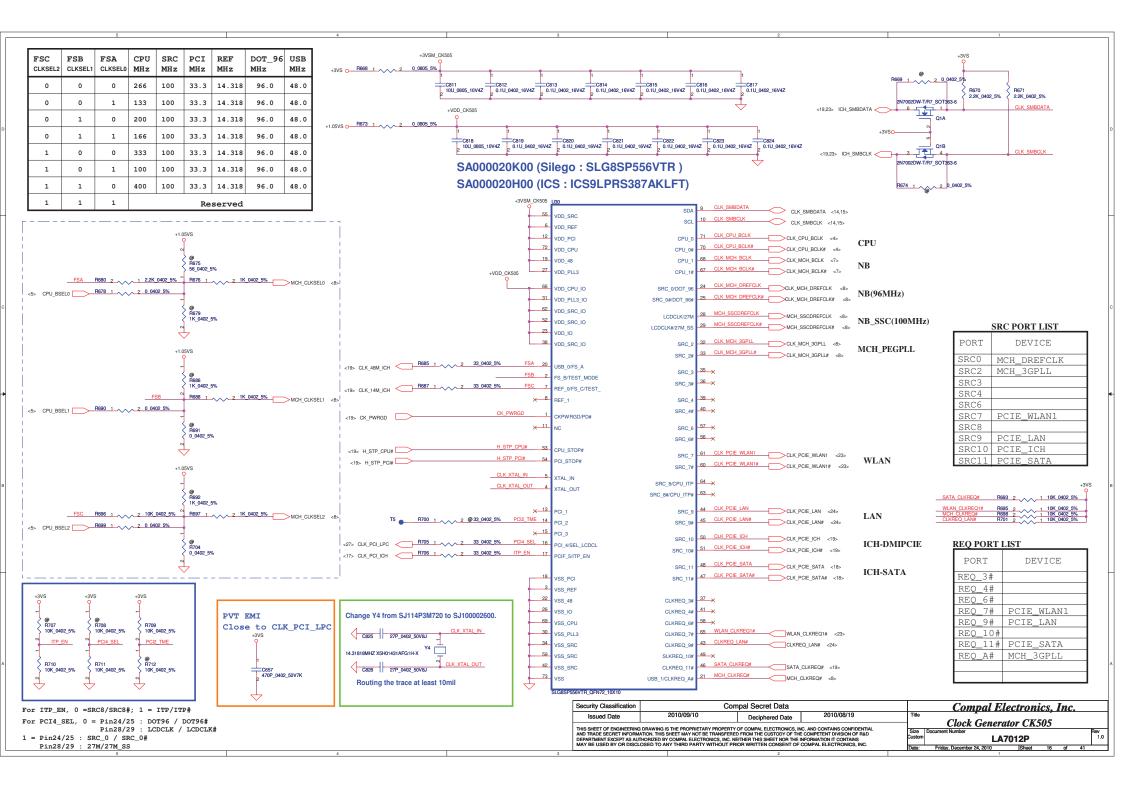


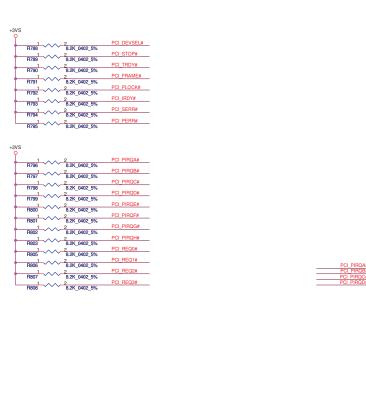


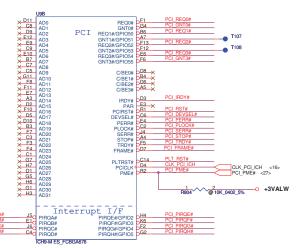
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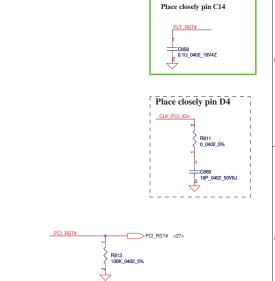












PLT_RST# <8,23,24>

R814 100K_0402_5%

PLT_RST#

09/16 Add C858 For ESD

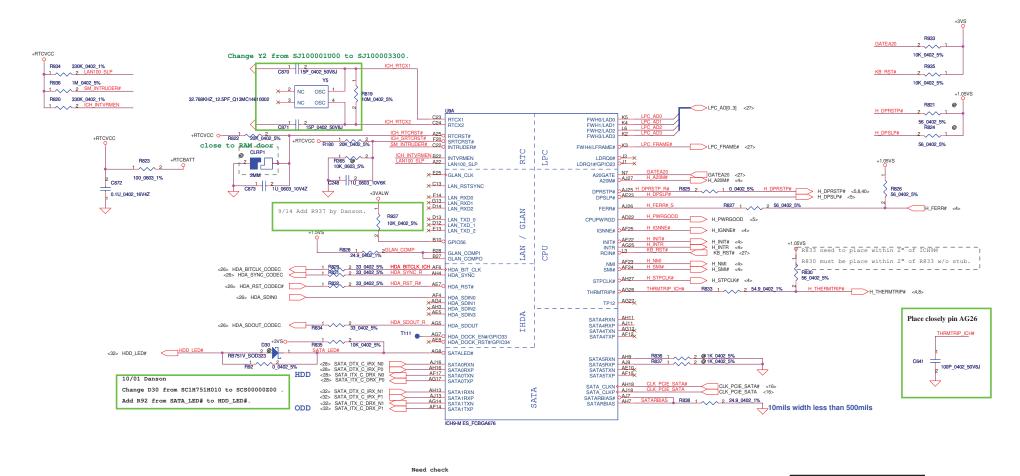


Boot BIOS Strap					
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction			
0	1	SPI			
1	0	PCI			
1	1	LPC*			

	1 0 0 0 2	PCI_GNT3#
	R812 2 0 1K_0402_5%	
\rightarrow		

A16 Swap Override Strap							
PCI_GNT#3	Low= A16 swap override Enable High= Default*						

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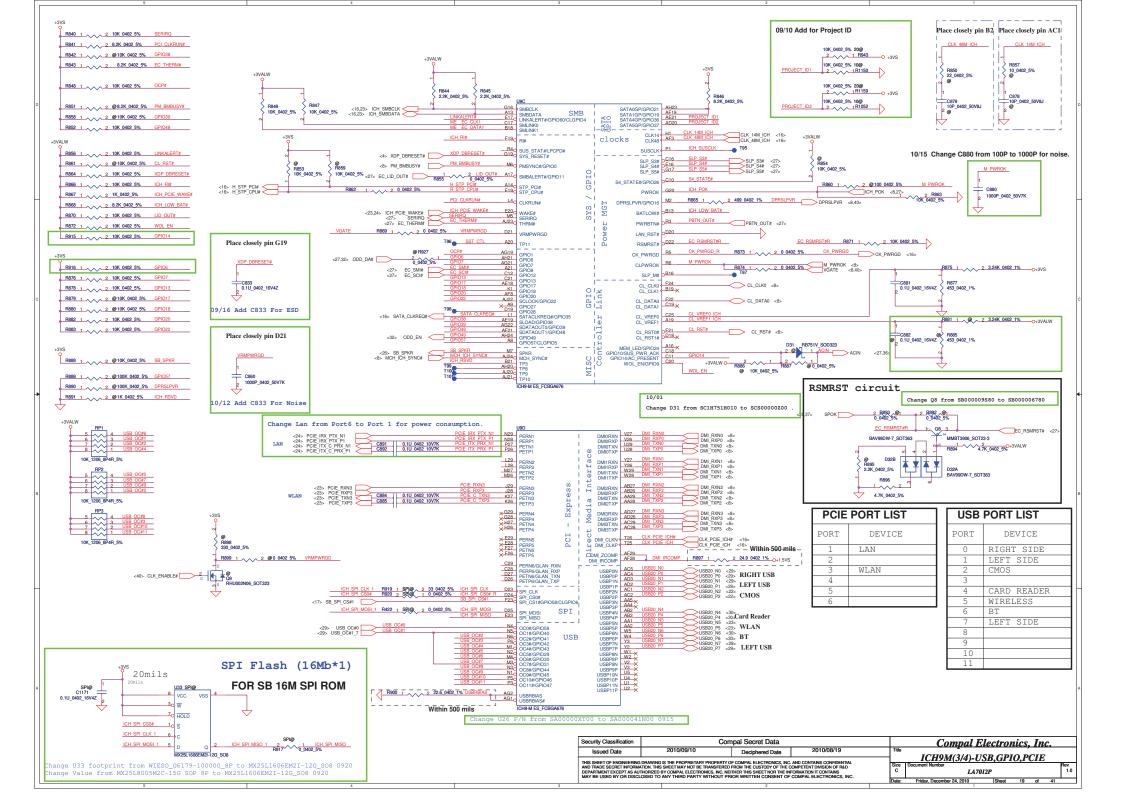


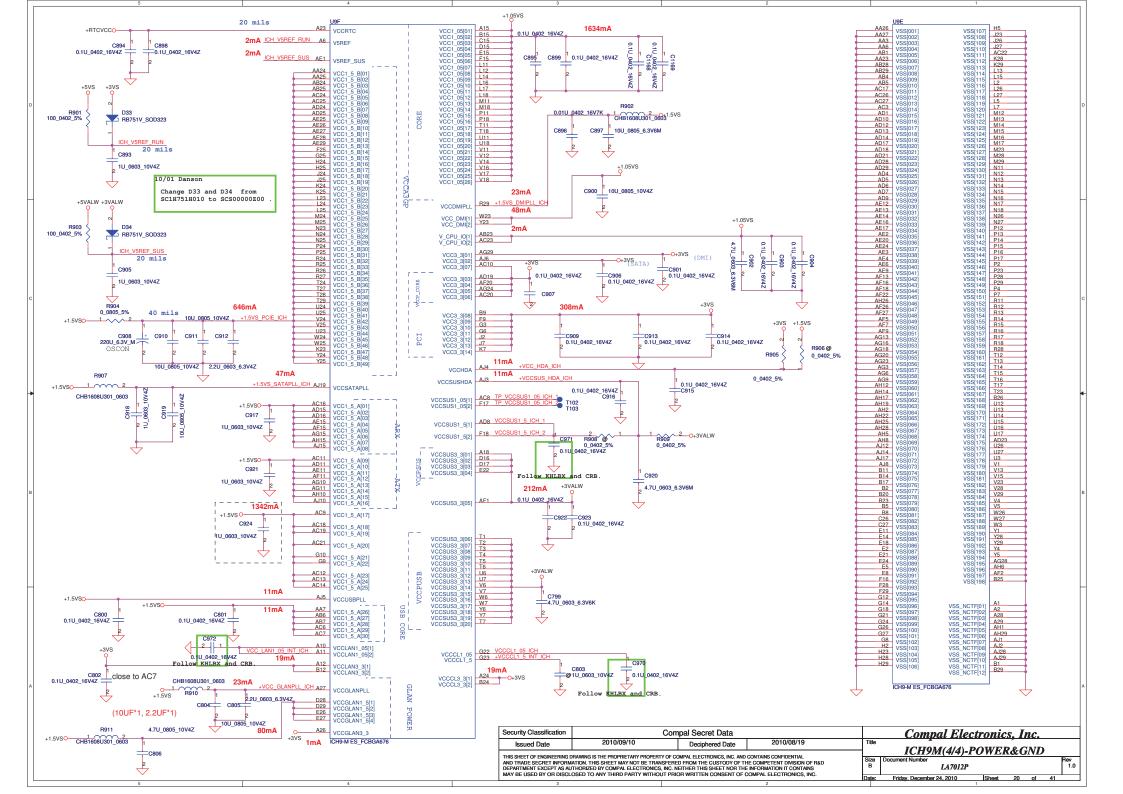
XOR Chain Entrance Strap							
ICH_TP3	HDA_SDOUT	Description					
0	0	RSVD					
0	1	Enter XOR Chain					
1	0	Normal Operation					
1	1	Set PCIE port config bit 1					

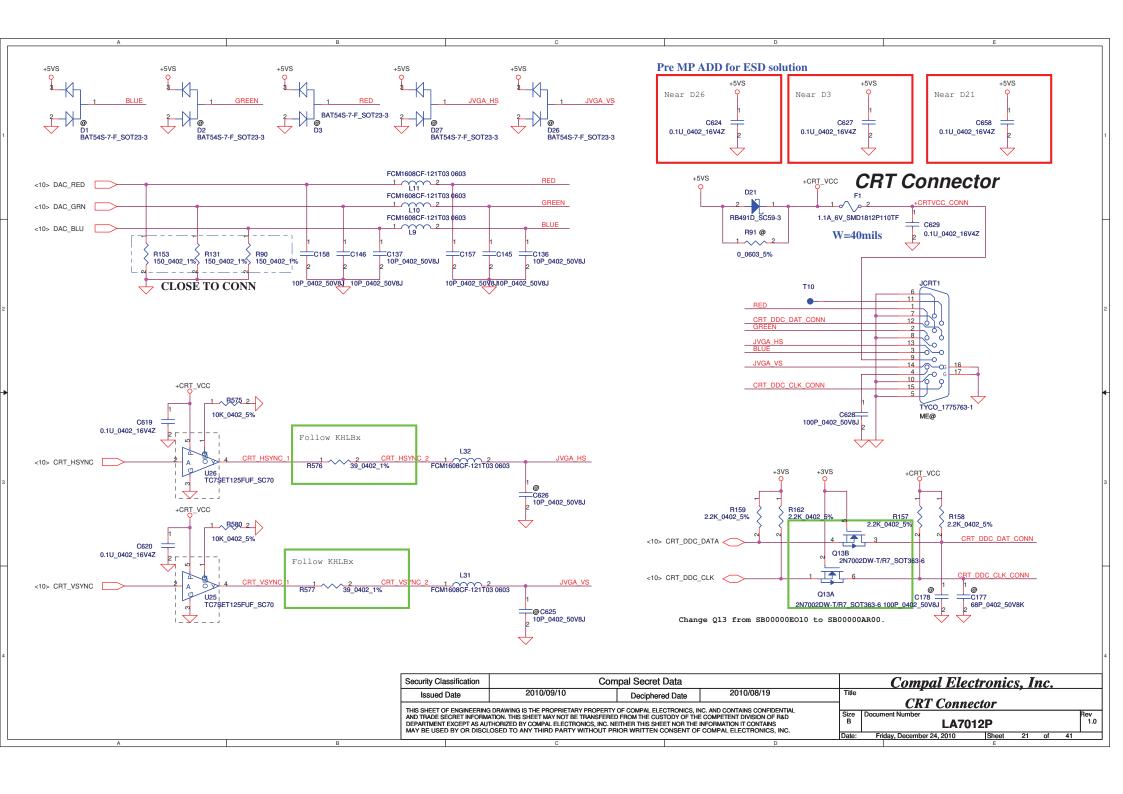
SAT	SATA PORT LIST						
PORT	DEVICE						
0	HDD						
1	ODD						
4							
5							

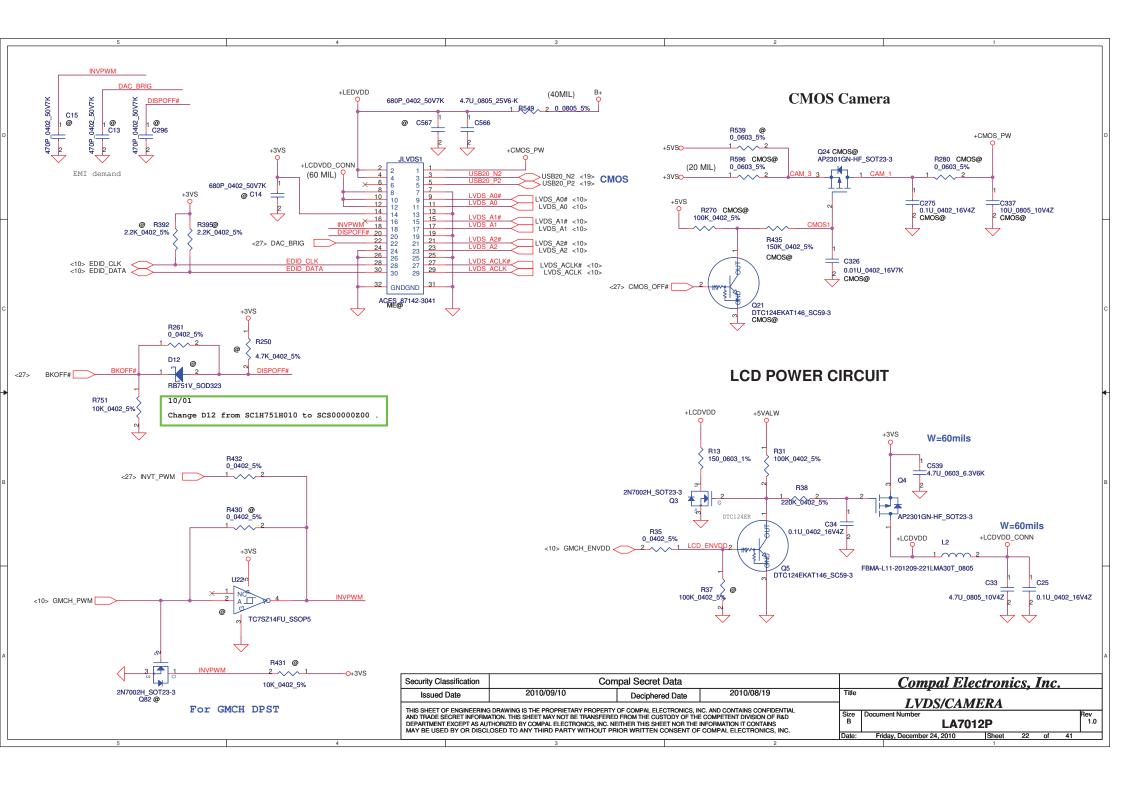
	Flash Descriptor Security Override Strap						
	GPIO33	Low= Descriptor Security override					
- 1		High= Default* (Internal pull-up)					

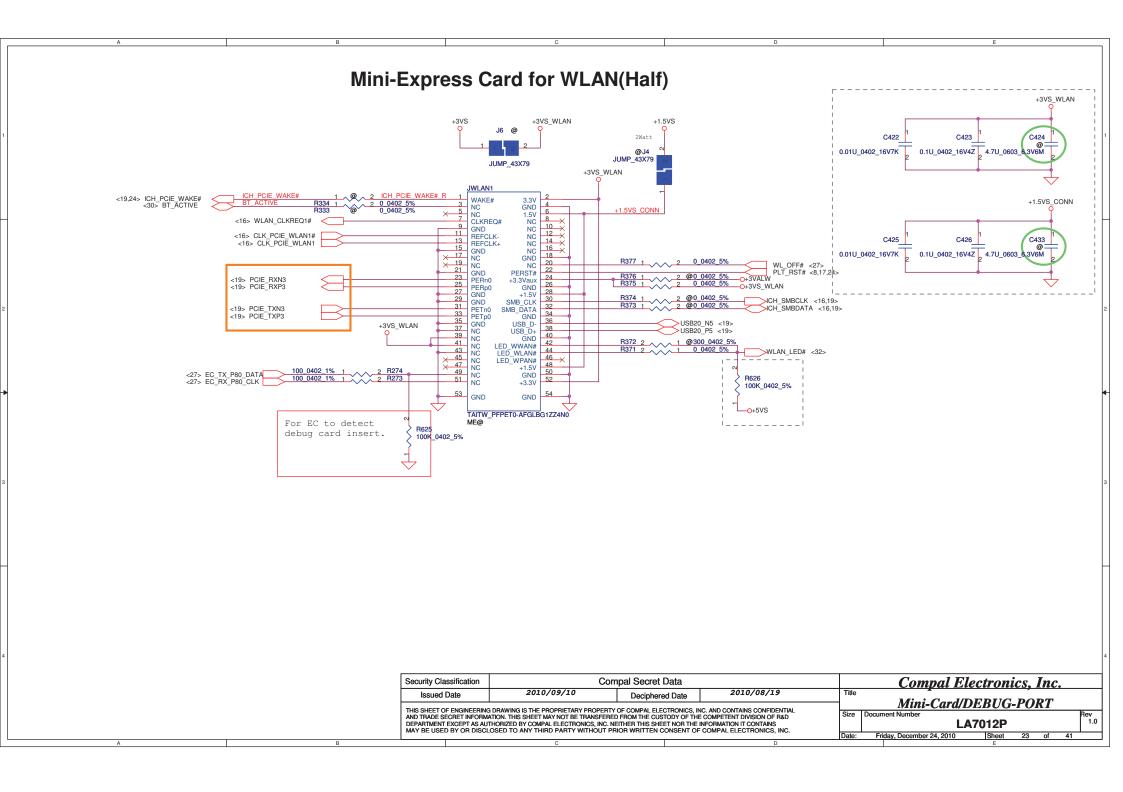
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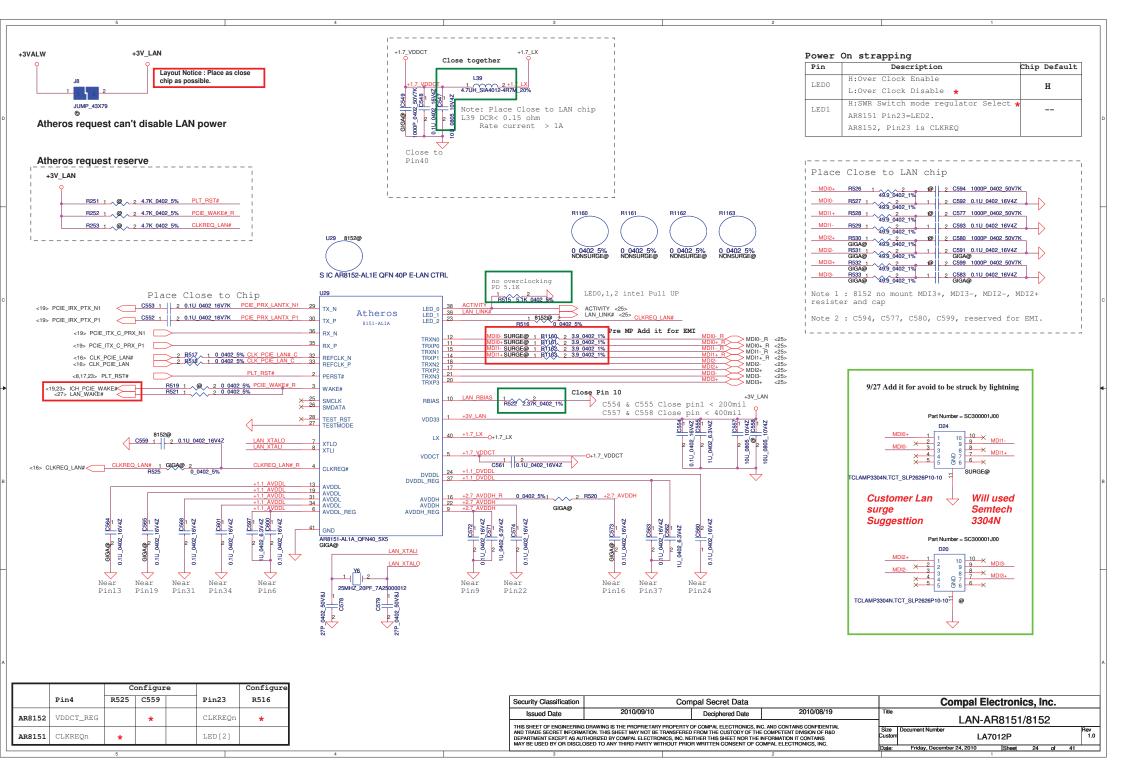


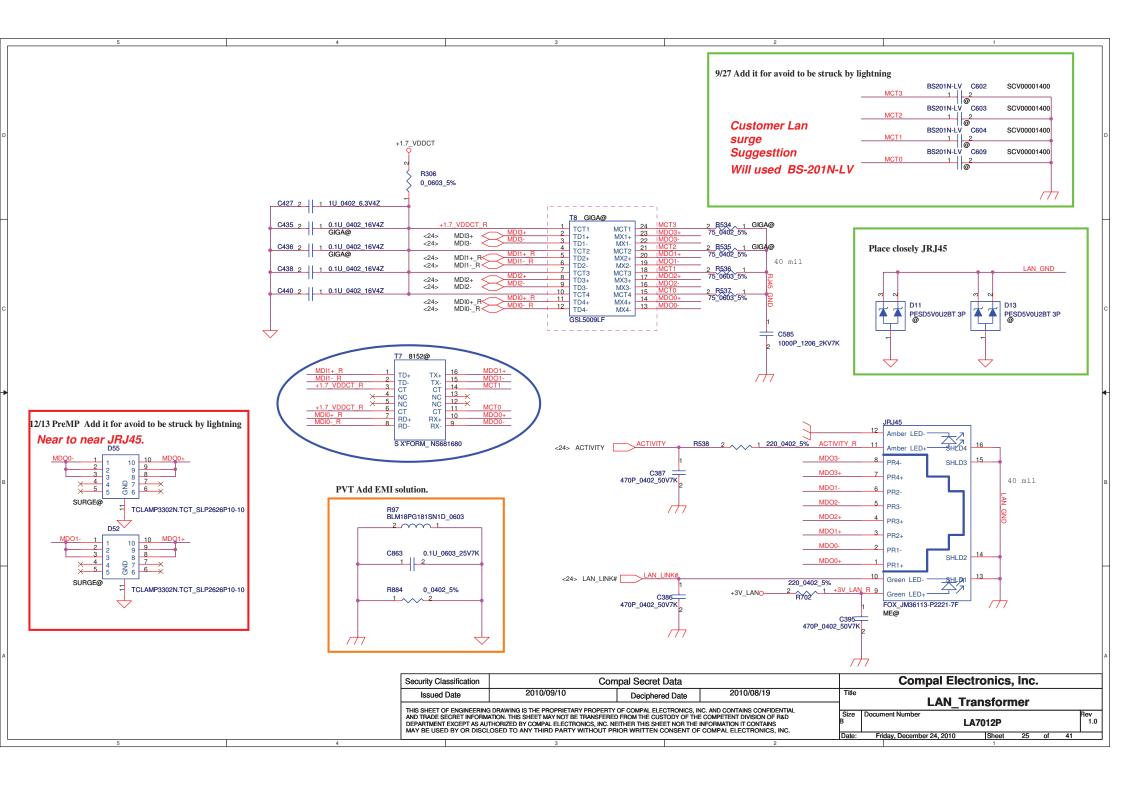


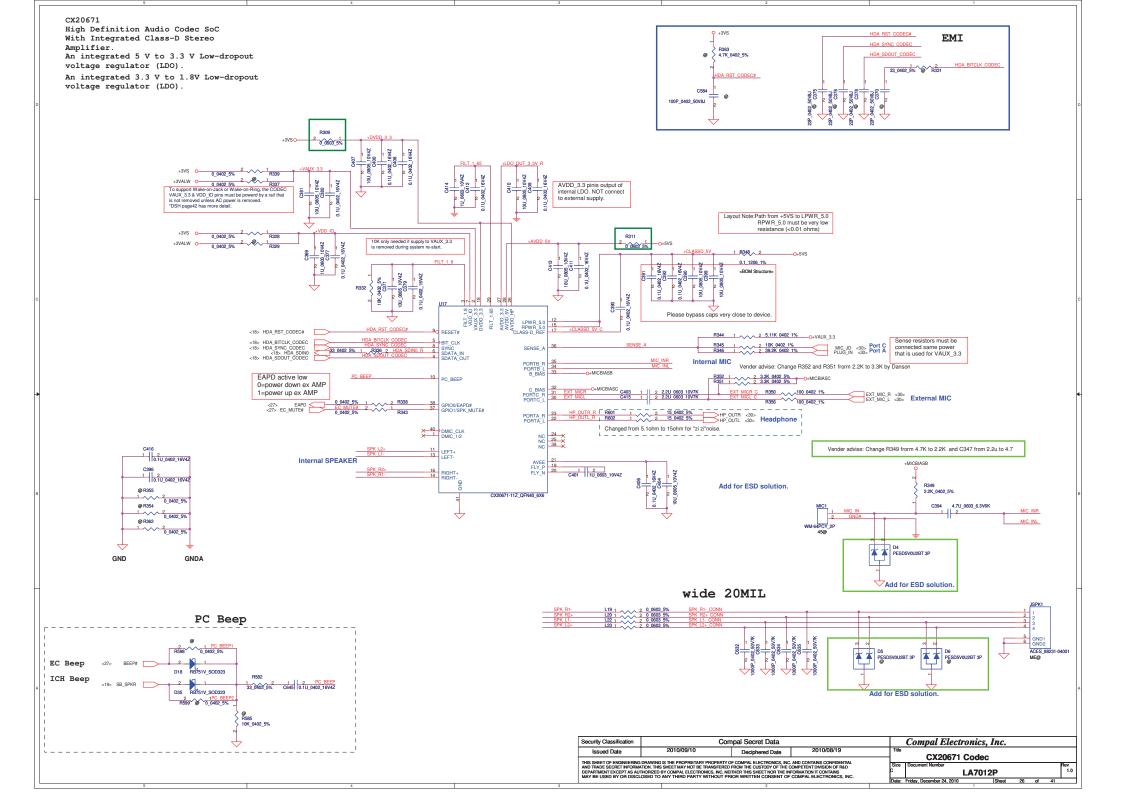


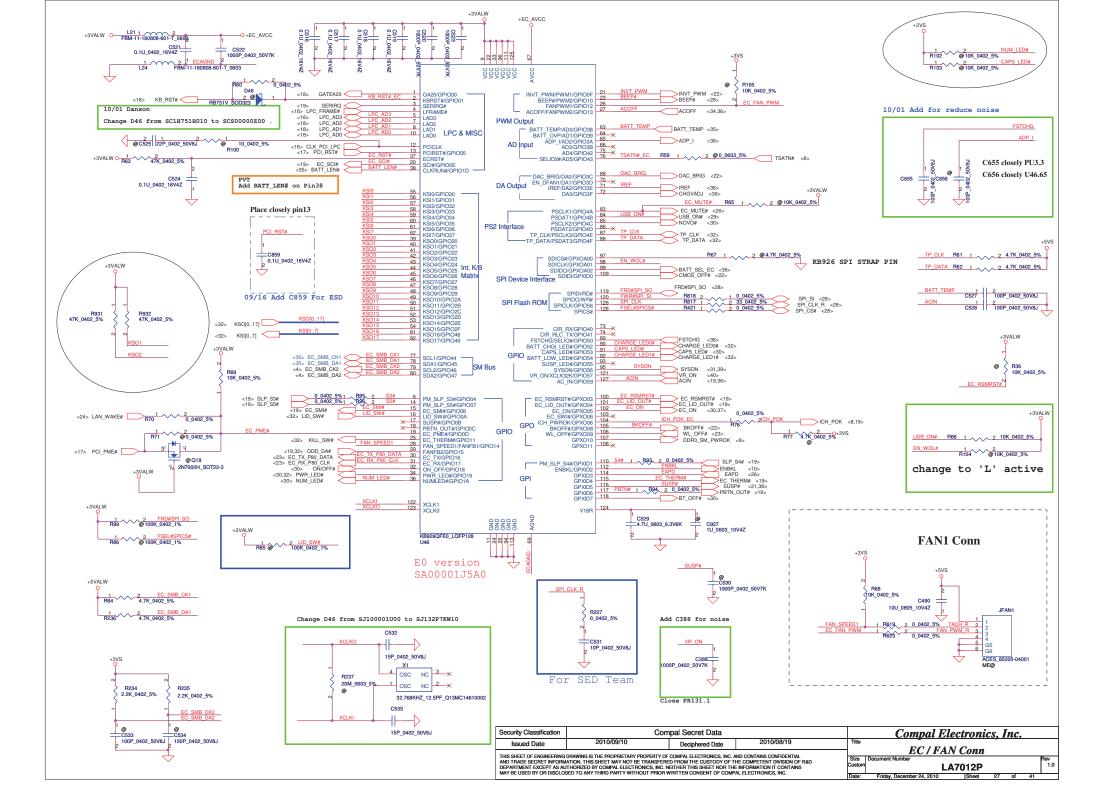






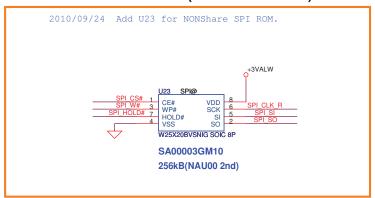






FOR EC 16M SPI ROM SPI Flash (16Mb*1) Change U31 P/N from SA00000XT00 to SA000041N00 0915 +3VALW Change U31 footprint from WIESO_G6179-100000_8P to 20mils MX25L1606EM2I-12G_S08 0920 U31 LPC@ C1170 0.1U_0402_16V4Z VCC VSS 0 0402 5% 1SPI_HOLD#_7 0_0402_5% HOLD <27> SPI CLK R FRD#SPI_SO <27> R816 0_0402_5% MX25L1606EM2I-12G_SO8

FOR EC 256K SPI ROM (NONShare ROM)



HDD / SPI ROM / Hold

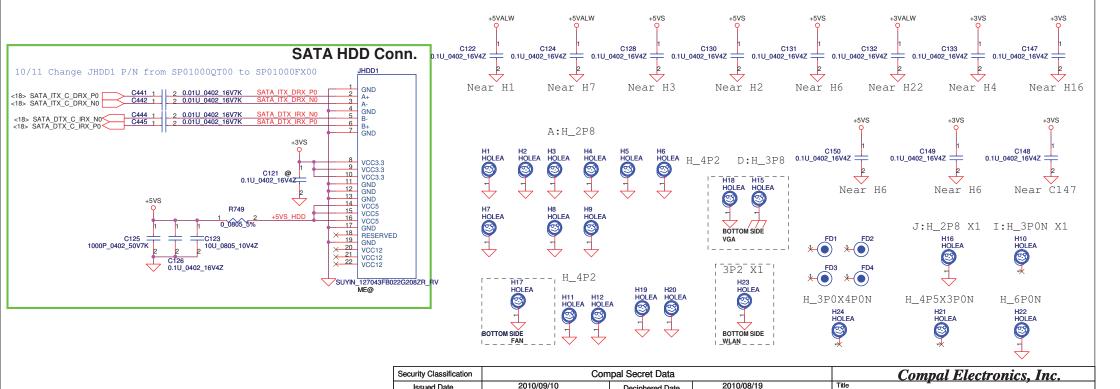
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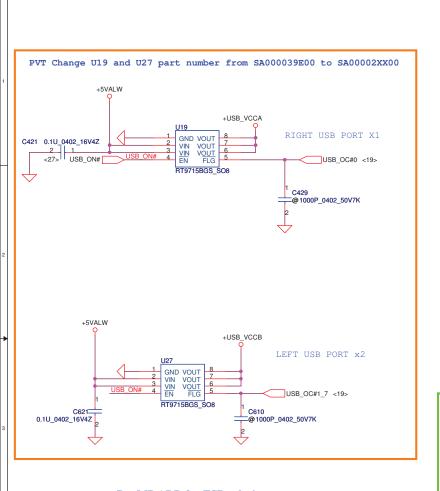


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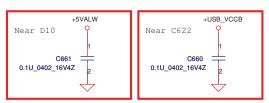
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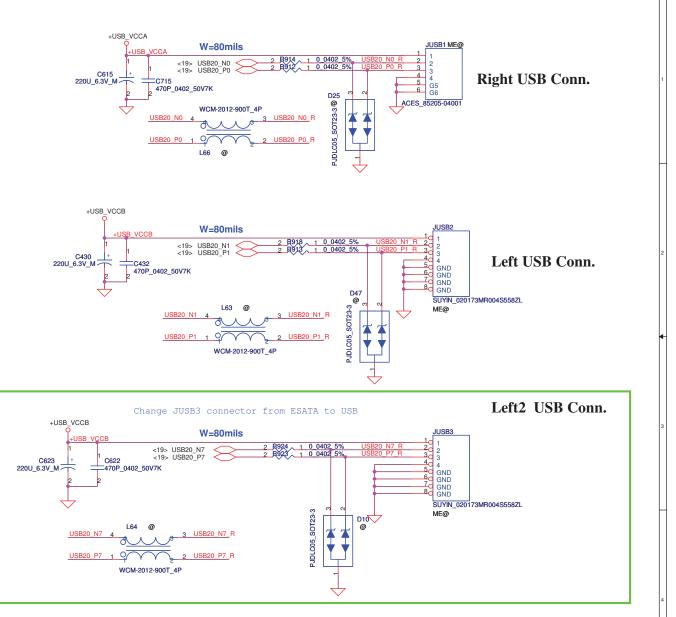
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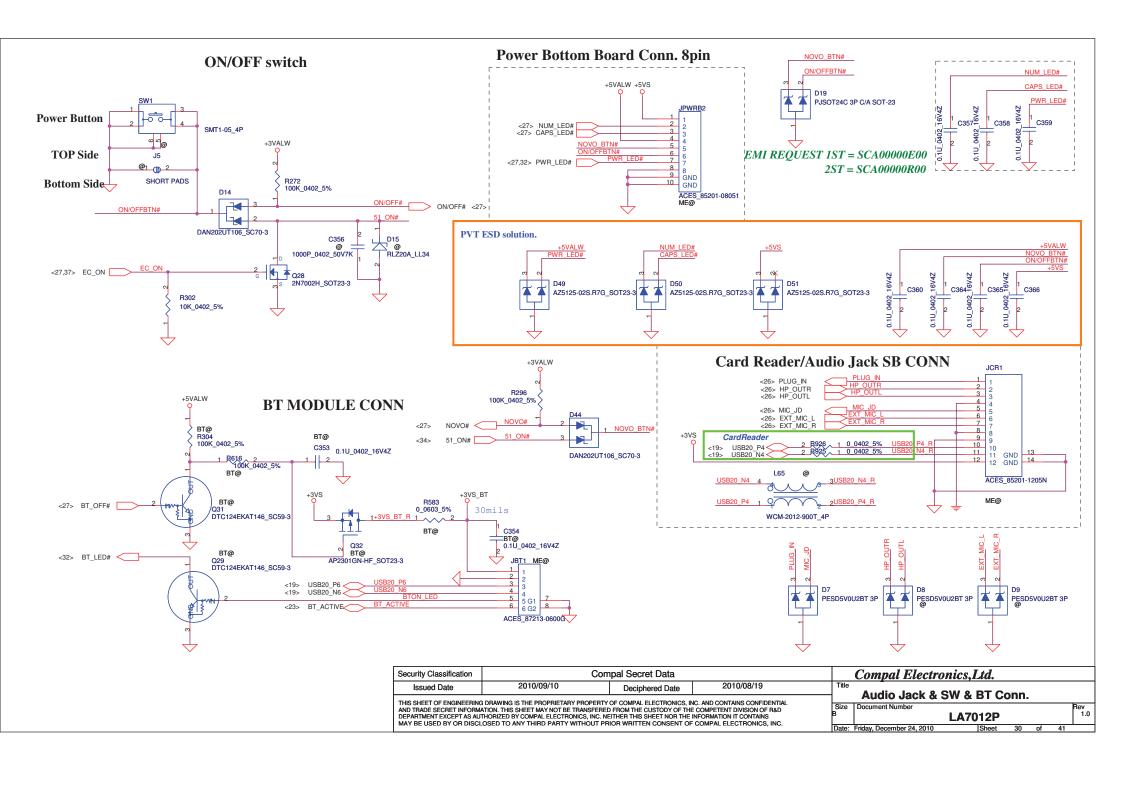


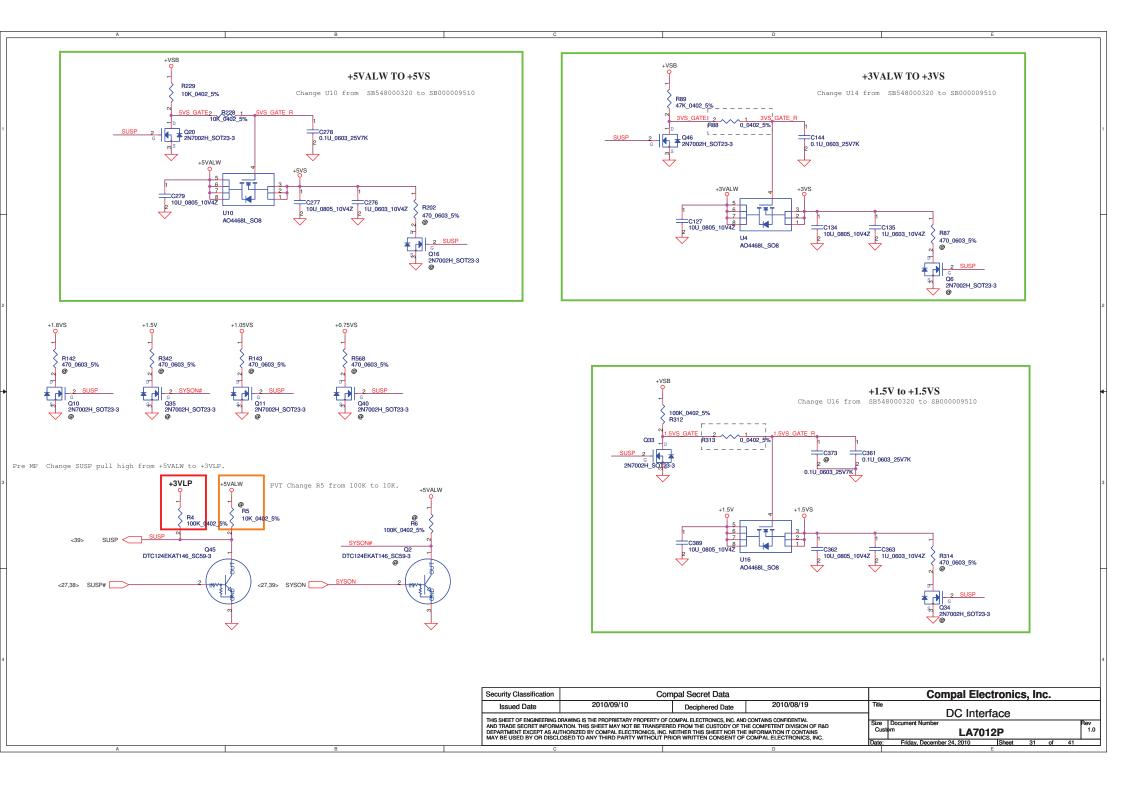
Pre MP ADD for ESD solution

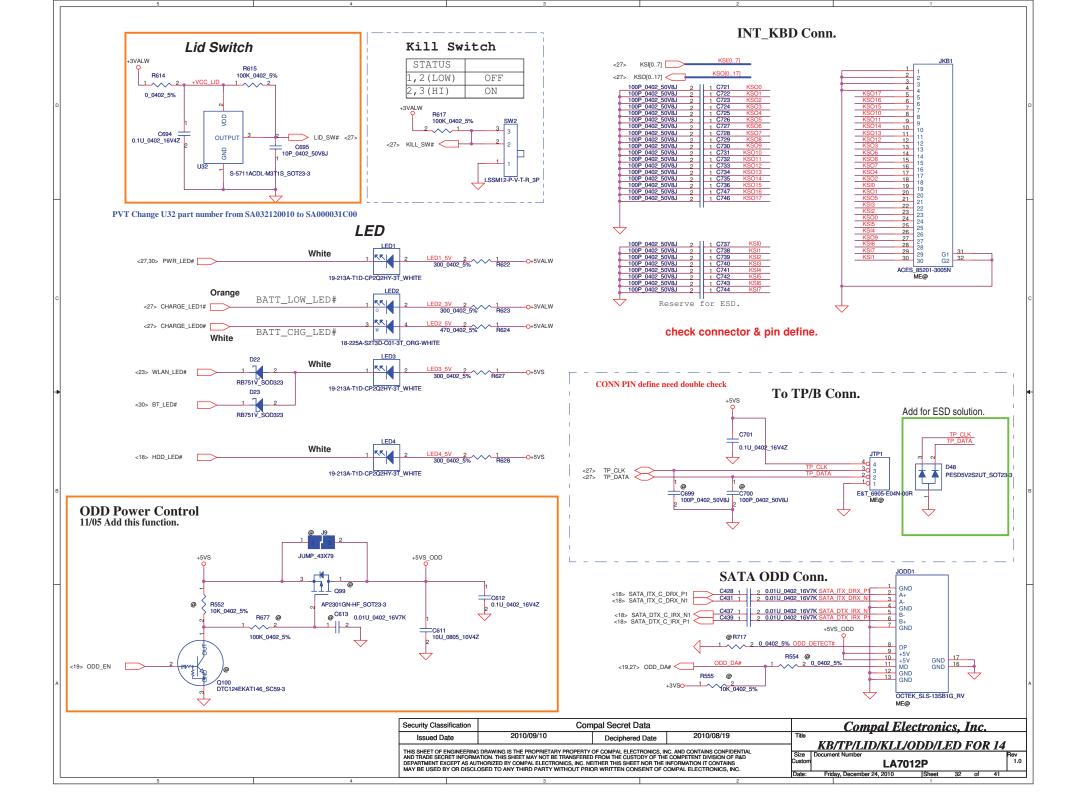




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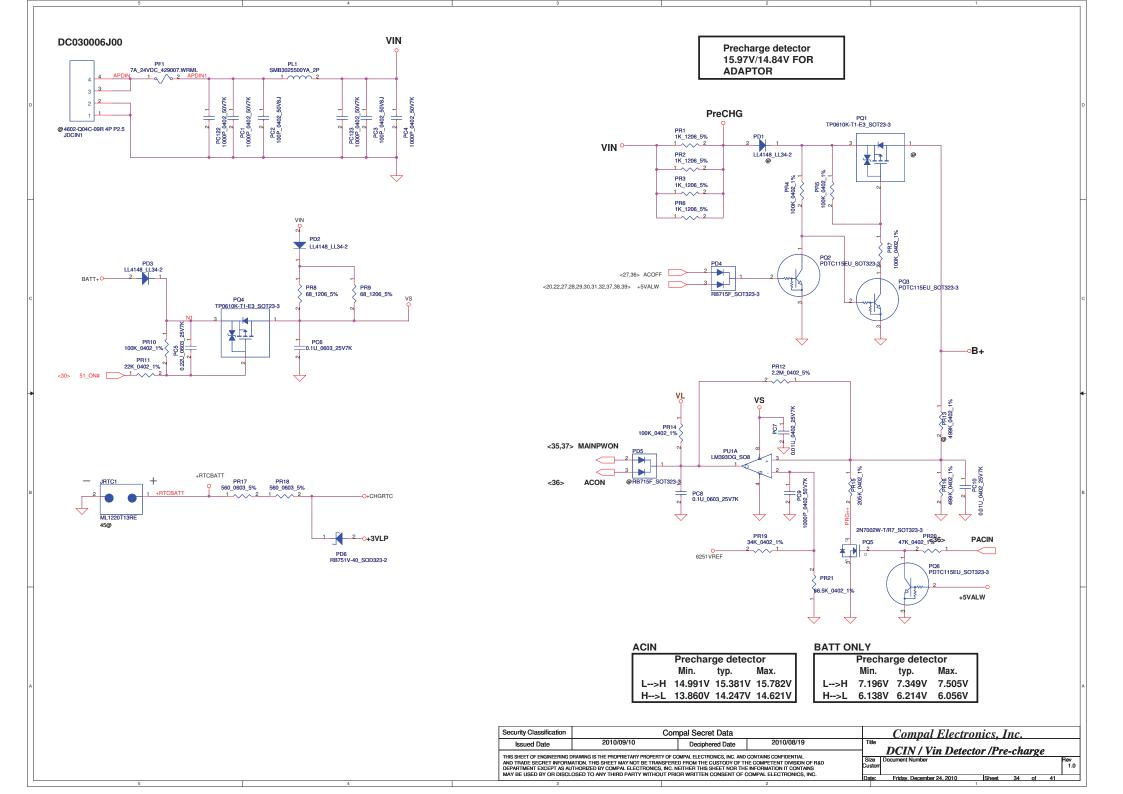


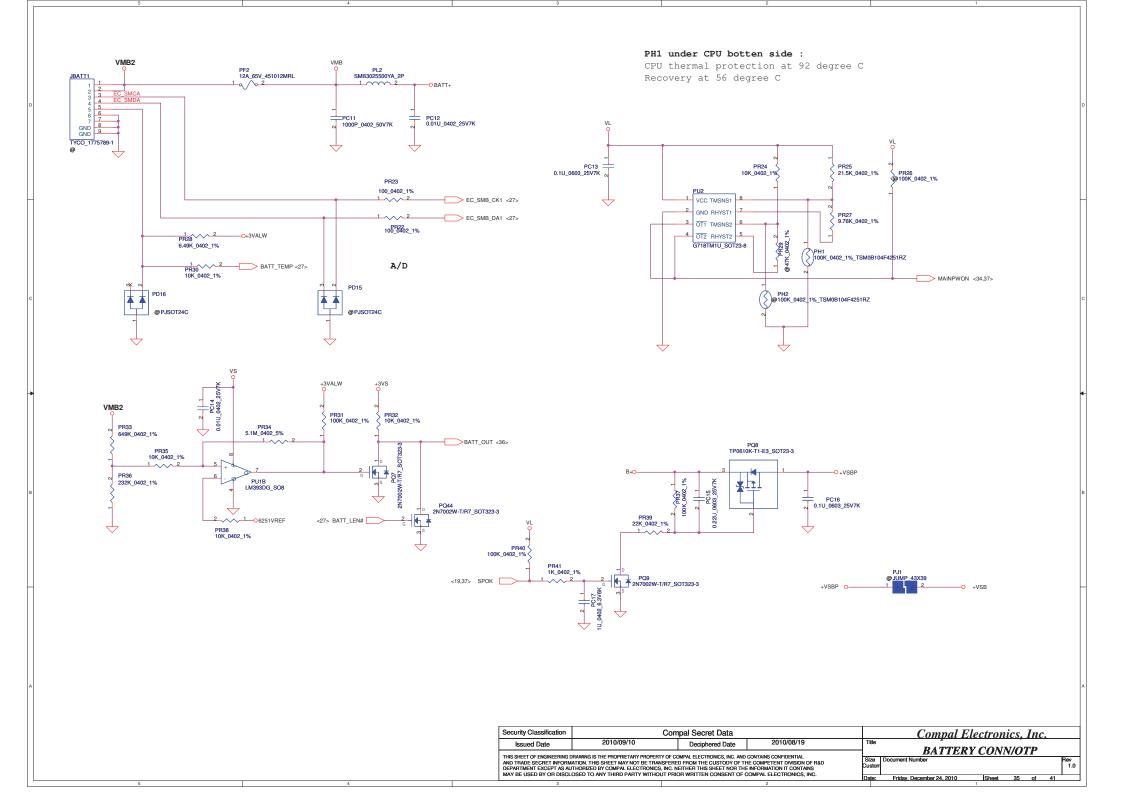


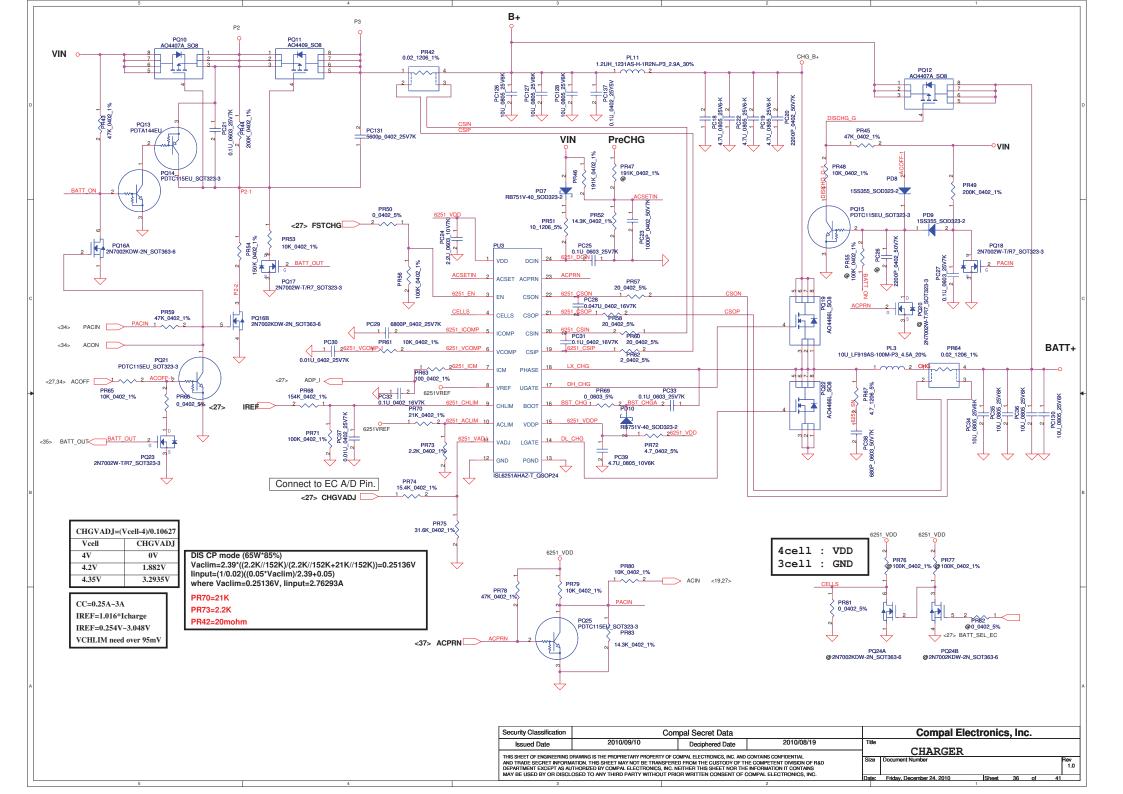


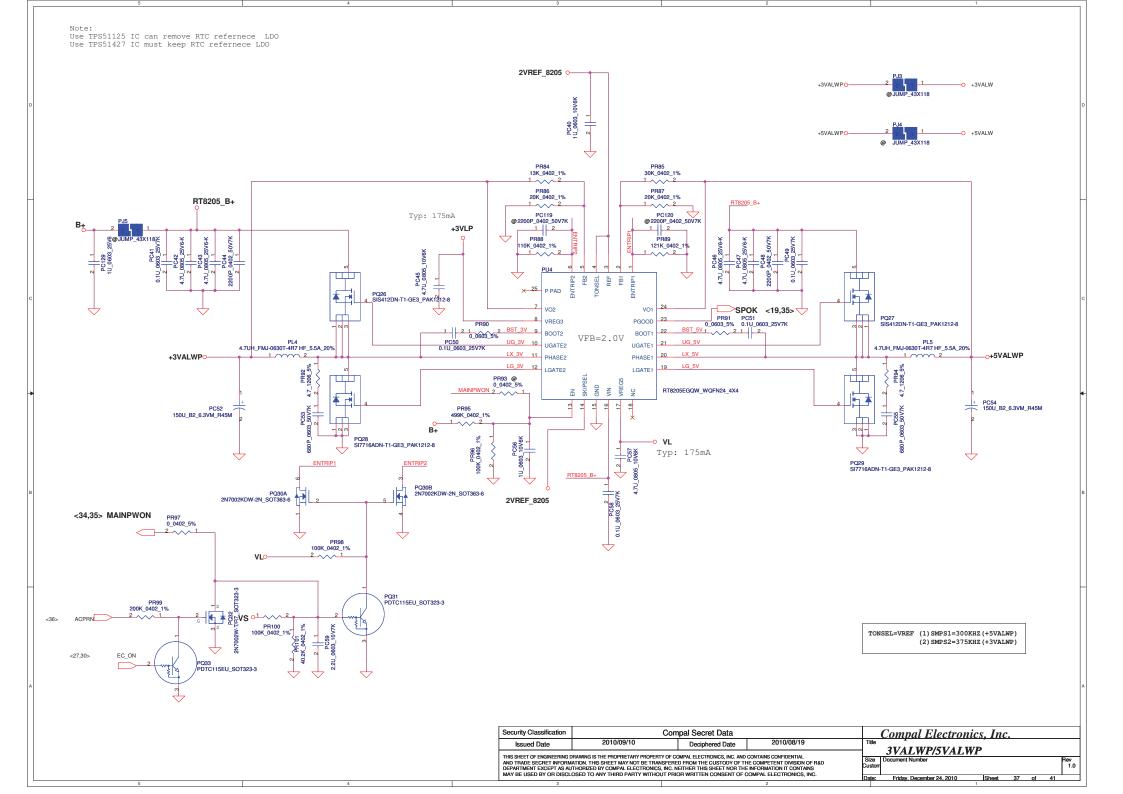
Page 1 of 1 for HW Version change list (P.I.R. List) Item Fixed Issue Reason for change PG# Modify List Rev. Date Phase 24

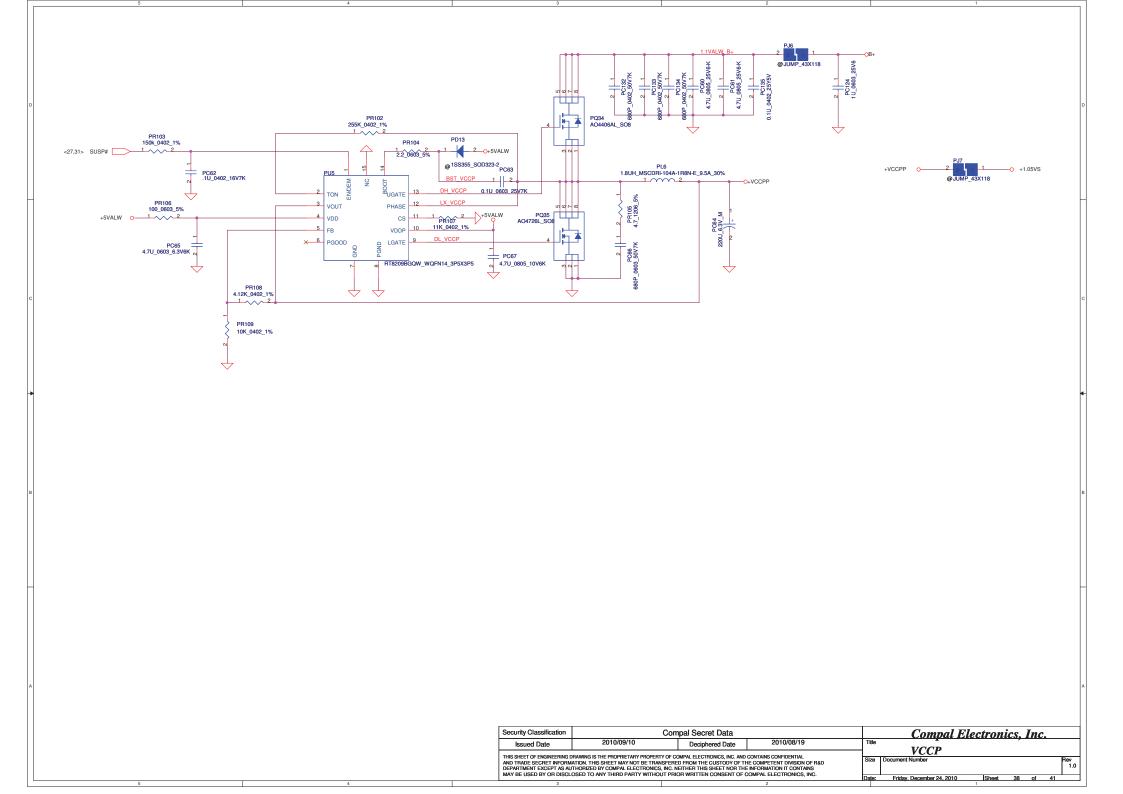
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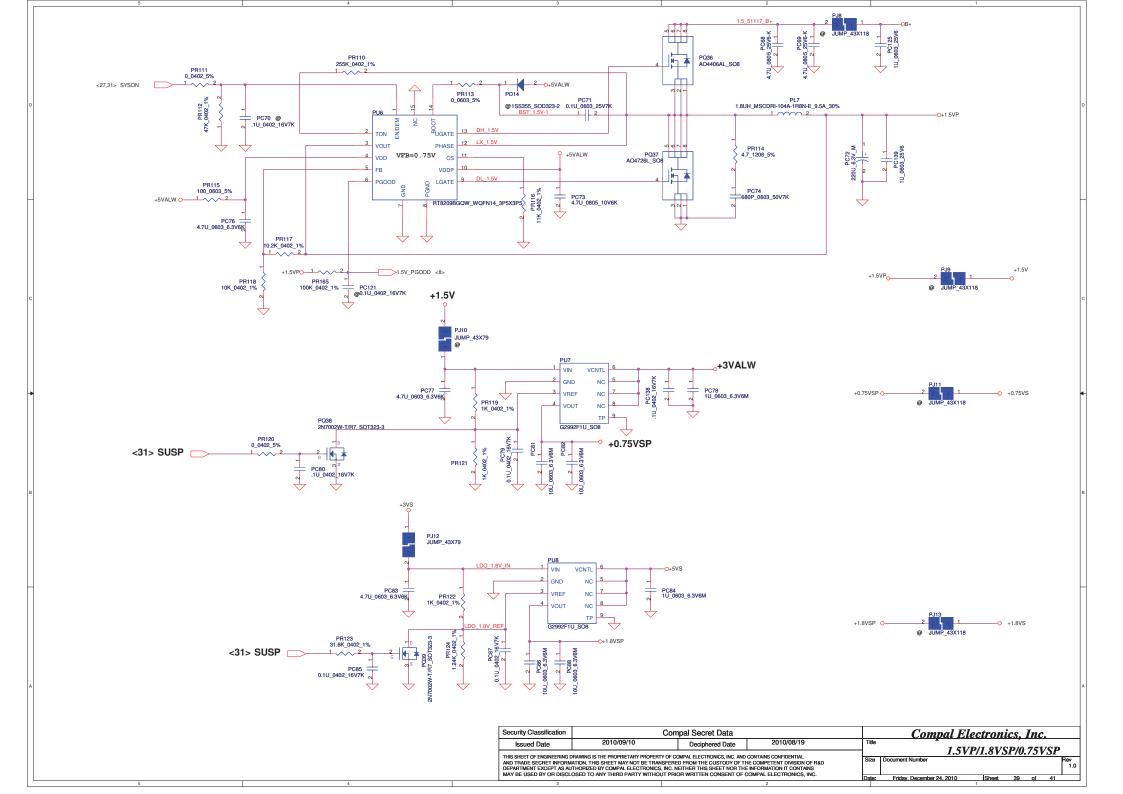


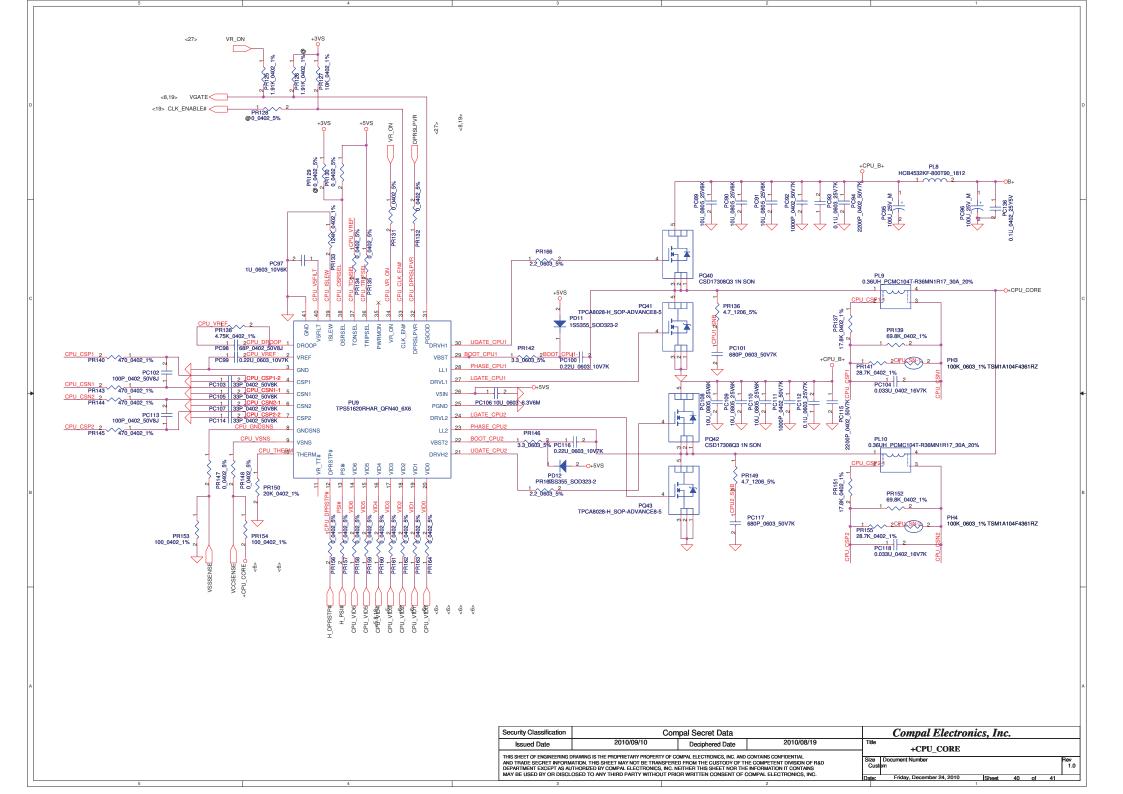












Version Change List (P. I. R. List) for Power Circuit

Page#	Title	Date	Request Owner	Issue Description	Solution Description
P35,37,39	Add capacities for EMI request	2010.11.12	EMI	EMI test fail	Add PC132,PC133,PC134,PC135,PC136,PC137
P37	Change resistance for EMI request	2010.11.12	EMI	EMI test fail	Change PR104 from 0 ohm to 2.2ohm
P35	Add one capacitor for prevent inrush current too large	2010.11.12	PWR	If there isn't add capacity, the MOS of PQ11 have damged risk.	Add PC131 which value is 5600PF
P34	Add one transistor for improve design margin	2010.11.12	PWR	If there isn't add transitor, the design margin of PQ11 is not enough.	Add PQ44
P39	Change resistance for CPU loadline fine tuning	2010.11.12	PWR	For meet the load line of intel spec	Change PR138 from 4.3k to 4.75k
P35	Add one capacitor for improve ripple current	2010.11.12	PWR	For meet the ripple current spec of Compal	Add PC130
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В					
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