Problem 1: How Many Memory Accesses?

Assuming our cache can fit infinitely many blocks and is initially empty, how many memory accesses will be required to perform reads at the following addresses? The addresses are 16 bits, block size is 16, and the cache is fully associative. (Hint: Start by finding which addresses are in the same block)

Address	Tag Bits	Block Offset Bits
0x000F	0x000	0xF
0xBEA7	0xBEA	0x7
0xDEAD	0xDEA	0xD
0xDEA0	0xDEA	0x0
0x1337	0x133	0x7
0xDEA1	0xDEA	0x1
0x0000	0x000	0x0
0xBEEF	0xBEE	0xF

memory accesses: _____5_____

Problem 2: Keeping Track of LRU Blocks

Use the same accesses as the previous question, but now assume our cache holds only 4 blocks.

- How many LRU bits do we need for each block?
- Walk through the accesses. What does our cache look like after we have performed each one? Which block is LRU? 2nd most? Etc. Use the caches below to store your work.

LRU bits: _____2_____

After 1st read

Tag	LRU
0x000	LRU

After 2nd read

Tag	LRU
0x000	LRU
0xBEA	MRU

After 3rd read

Tag	LRU
0x000	LRU
0xBEA	2LRU
0xDEA	MRU

After 4th

Tag	LRU
0x000	LRU
0xBEA	2LRU
0xDEA	MRU

After 5th read

Tag	LRU
0x000	LRU
0xBEA	2LRU
0xDEA	2MRU
0x133	MRU

After 6th read

Tag	LRU
0x000	LRU
0xBEA	2LRU
0xDEA	MRU
0x133	2MRU

After 7th read

Tag	LRU
0x000	MRU
0xBEA	LRU
0xDEA	2MRU
0x133	2LRU

After 8th

Tag	LRU
0x000	2MRU
0xBEE	MRU
0xDEA	2LRU
0x133	LRU