

Upcoming Assignments

- Lab 3 due Wednesday 9/18
- Project 1s & 1m due Thursday 9/19
- Homework 1 due Monday 9/23

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Lab 3: **ARM Assembly**

LC2K Instructions Compared to ARM

LC2K

add (R-type

nor (R-type)

lw (I-type)

sw (I-type)

beq (I-type)

jalr (J-type)

halt (O-type)

noop (O-type)

addr

addr+1

addr+2

addr+3

about

ARM

Load #-1 then EOR/SUB

CMP then B.EQ

BR (branch reg)

LDURSW

STURW

End of file

Big Endian Memory

ВА

AD

FØ

0D

address is the MSB.

Big Endian builds the word so the smallest

NOP

ADD



Also ADDI for constants, and SUB/SUBI for subtraction. (LC2K Subtraction: nor the 2nd with itself, add 1, add result to 1st one). MOVZ #0 zeros out reg. We use LSL, LSR for shifts. (Pseudo-instructions: MUL)

Much easier to use ORR/ORRI, ADD/ADDI, EOR/EORI. (Note: a NOT instruction exists in pseudocode for ARM overall, but not LEGv8)

CBZ branch if zero (beq 0 regB offset), B for unconditional (beq 0 0 offset)

This is for 32 bits. Also LDUR, LDURH, LDURB

This is for 32 bits. Also STUR, STURH, STURB

Using BL with #0 right before BR stores return address

Technically not in LEGv8, but present in ARM overall



Data is Stored in Memory in Chunks



Each chunk is (typically) the size of a single byte

Think of each chunk like a wooden letter block:

To interpret the word, we can rearrange the blocks, but can't change the letters.







In memory, data is aligned to the size of its type









Endianness in Byte-Addressable Systems

32-bit Integer

0×BAADF00D

This can be more natural for humans to think Faster for a computer to read, as int ops can

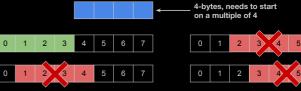


Memory Alignment



This makes it more efficient to access within memory

and is important for caching (we'll see why later in the course)



Typical Size of Data Types



Little Endian Memory

FØ

Little Endian builds the word so the largest

start after reading the first byte.

address is the MSB.

0D addr

addr+1

AD addr+2

BA addr+3



Aligning Data within a struct



	Data Type	Size / Alignment	
char		1 Byte	
short		2 Bytes	
int, float		4 Bytes	
double		8 Bytes	
long	(32-bit Architecture)	4 Bytes	
long	(64-bit Architecture)	8 Bytes	
pointer	(32-bit Architecture)	4 Bytes	
pointer	(64-bit Architecture)	8 Bytes	

Since a struct can contain multiple different data types, we must align the struct using the largest primitive type within it

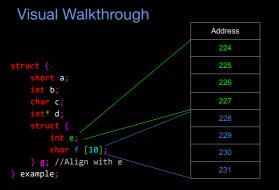
Furthermore, we may need to pad the **struct** to keep everything aligned, even padding the end in case we have an array of structs

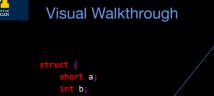


Notice the padding

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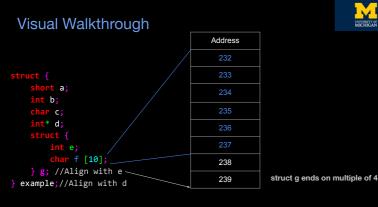








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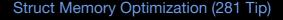


Visual Walkthrough Address f [10] 238 } g; //Align with e 239 example;//Align with d

struct example ends on multiple of 8

Grid View







f [10];

} example;

- offset +2 +3 +6 +7 base а +8 +16 +24 +32 g g
- We can rearrange the variables in a struct to use as little padding as possible for BOTH 32-bit and 64-bit systems.
- Greedy yet optimal algorithm: start with the largest size primitives, then go down.
 - o This also works by starting with the smallest, and working up.
 - o And there might be more solutions for a given struct.
- Count structs as multiples of their largest member, as with alignment.

ARM's LEGv8 ABI





Application Binary Interface (ABI) defines convention of how registers should be used

Ex: LEGv8 Register X0-X7 are used for arguments/results

See here for full LEGv8 ABI

REC	REGISTER NAME, NUMBER, USE, CALL CONVENTION					
	NAME	NUMBER	USE	PRESERVED ACROSS A CALL?		
	X0 - X7	0-7	Arguments / Results	No		
	X8	8	Indirect result location register	No		
	X9 - X15	9-15	Temporaries	No		
	X16 (IP0)	16	May be used by linker as a scratch register; other times used as temporary register	No		
	X17 (IP1)	17	May be used by linker as a scratch register; other times used as temporary register	No		
	X18	18	Platform register for platform independent code; otherwise a temporary register	No		
- 1	X19-X27	19-27	Saved	Yes		
- [X28 (SP)	28	Stack Pointer	Yes		
- 1	X29 (FP)	29	Frame Pointer	Yes		
	X30 (LR)	30	Return Address	Yes		
ı	XZR	31	The Constant Value 0	N.A.		

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