

Faculty of Computing, Online Examinations 2021

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MODULE LECTURER	Mr. Gayan Perera	DATE SUBMITTED	6 – Sep – 2021

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GRADE/MARK	
COMMENTS	

Declaration

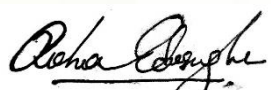
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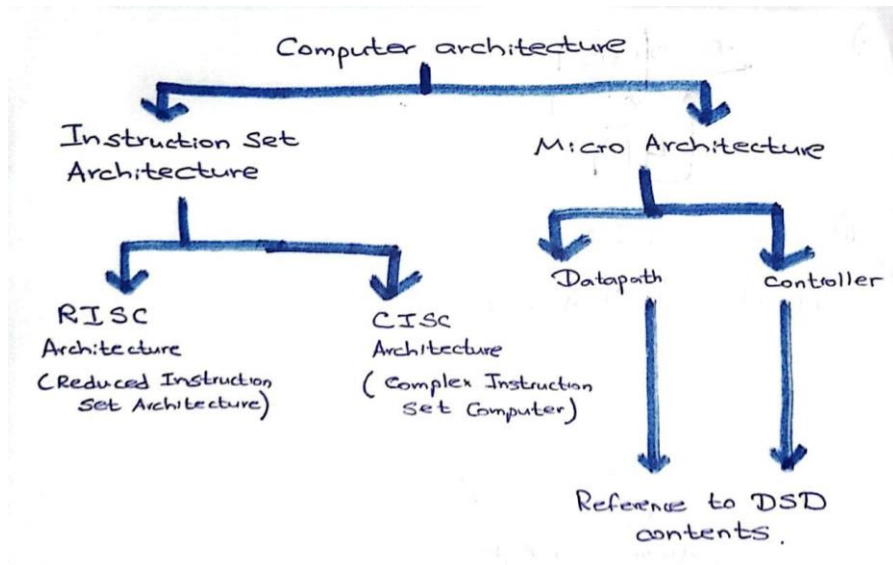
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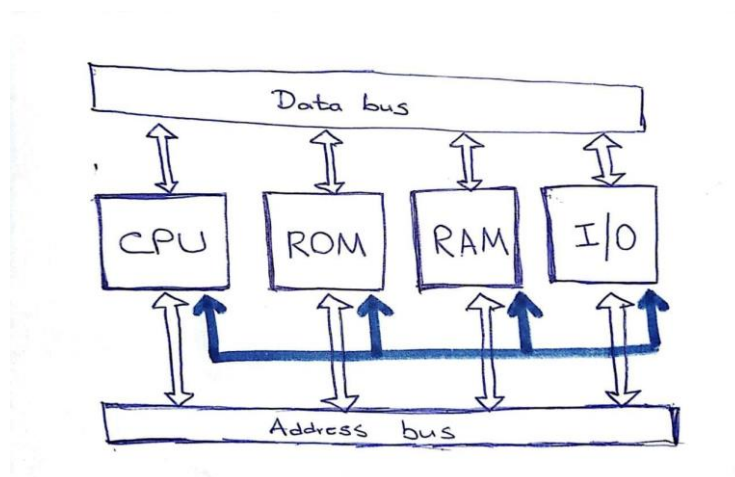
Question 1

1. A descriptive detailing of how software and hardware applications interact in order to build a computer program, or a platform is simply known as "Computer Architecture". It is a set of categories that define a computer program by the specification of its parts and the relations of them. Computer architecture is of 3 types. As system design, instruction set architecture & microarchitecture. But mainly we consider ISA & Microarchitecture.



- In System design architecture, it consists of all the hardware components inside a computer, such as GPU and direct memory access.
- In ISA- Instruction Set Architecture, it brings out all the functions and capabilities of the CPU according to the programming it can process or perform.
- In microarchitecture, it means that it consists of data paths, data processing and storage elements, and also how they should be executed in the Instruction Set Architecture.

2.



- **CPU**

Processing device is the computer's hardware component that helps in handling the storage and getting back data / retrieving data. These devices are responsible for processing information within the system. They carry out the instructions for programs to run and all the functions of the computer system. Some examples for processing devices are CPU, motherboard, chipset, network card and so on.

- **Memory Devices**

Memory devices act as a temporary memory area (in which data is stored or transferred) between the CPU (Central Processing Unit) and the main memory. It holds the most needed parts of data and the program which are most frequently used by the CPU. Encoding, storing, and retrieving information are the main functions of memory devices. Some examples for memory devices are USB flash drives, SSD, HDD and so on.

- **Input & Output Devices (I/O)**

Input & Output Devices are the branch for the user and the computer system for communication. They INPUT the information or data that are given to the computer system and OUTPUT the results. Some examples for I/O devices are touch pen, monitor, touchpad, keyboard, mouse and so on.

- **RAM (Random Access Memory)**

Random Access memory (RAM) is one of the most important factors in determining the performance of your system. RAM gives apps a place to store and access data in a short period of time. It stores the information your computer actively uses for quick access.

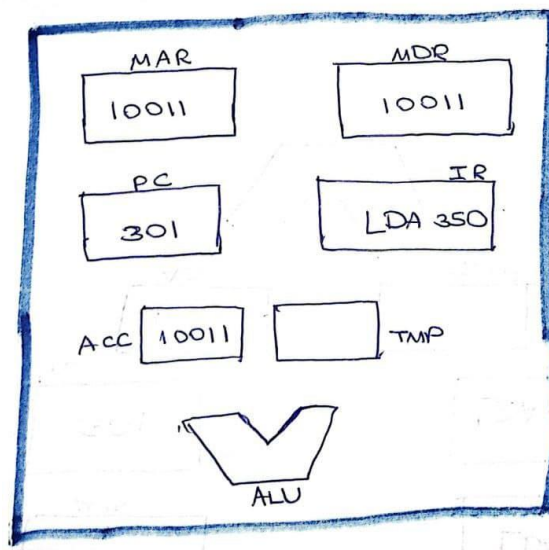
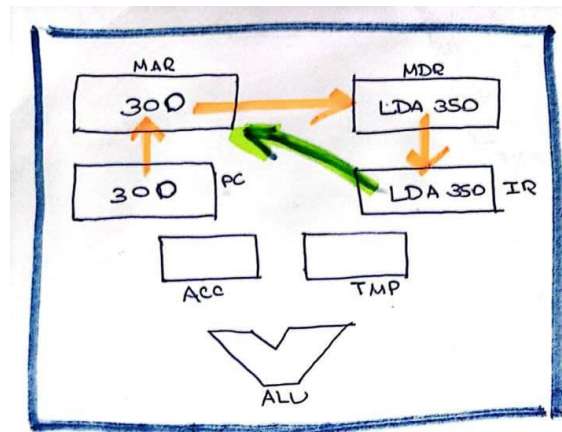
- **ROM (Read Only Memory)**

The ROM holds all the controls and commands needed for the operation of your computer system and its hardware. The ROM contains the BIOS (Basic Input / output System), also known as "Boot Loader".

3. Machine Cycle consists of 3 main steps as fetch, decode, execute. All these processes or so much important for the processor in order to execute the instructions.

- Fetch – All instruction is stored in a specific location in the memory that can be retrieved using a device called an instruction counter.
- Decode – the instructions that were fetched in the previous process are decoded in order to execute an instruction.
- Execute – Here, all the instructions that are decoded in the previous step are finally been executed by the computer processor.

4. i)



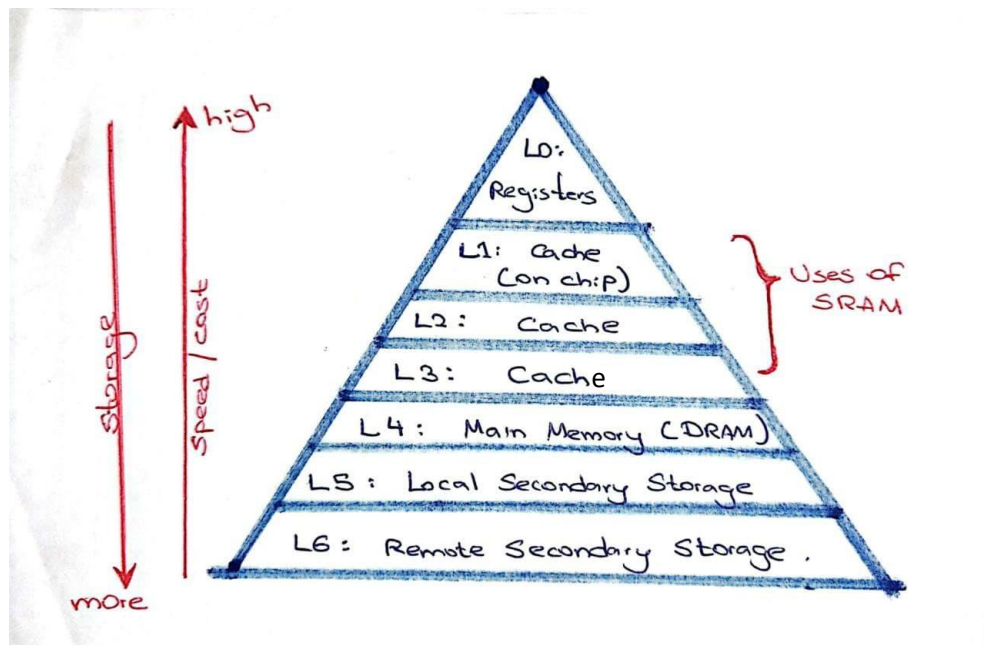
ii)

- When decoding the instruction is 301 PC = 302 and IR = SUB 351
- After Decoding 301 Instruction MAR = 351 while PC remains 302.
- The processor fetches the data and loads it to MDR and then MDR = 1011
- Since the Accumulator is already filled ACC=10011 and the MDR moves 1011 to Temp which makes TEMP=1011.

5. First John must consider his budget. As the prices of GPU are high due to the current situation of the world, he should be aware of how much he could spend for a laptop maximum. For video editing, he has to go for at least INTEL i5 – 8th gen processor. If he has the budget, he can go for AMD RYZEN 7 or RYZEN 9, or Intel i7 or Intel i9. He needs to have a RAM of at least 8GB and a VGA of at least NVIDIA G-Force GTX 1650 4GB. He needs to have an SSD, at least 500GB for perfect performance. If he has a higher budget, better VGA card like RTX 3060 and a 1TB of SSD can be recommended.

Question 2

1.



Register

A register is a Static Random-Access Memory or a SRAM in a processor of the computer that is used to store data word that's regularly 64 or 128 bits.

Register memory is one of the most important memories found in a processor. It is found almost in every processor. There are 2 types of registers as MAR and MDR. MAR stands for Memory Access Registers which holds the memory locations of the data that are needed to be accessed. MDR stands for Memory Data Register which's main purpose is to hold information.

Cache Memory

Cache memory, also called cache, is a memory system that automatically stores commands and data that are used for immediate processing by a central processing unit (CPU). The cache contains a copy of the most widely used information or program codes stored in large memory. Cache memory is also available in the processor. Rarely, however, could it be in another integrated circuit, divided into levels. Storage contains a chunk of data that is most needed in large memory.

RAM or Main Memory

RAM (Random Access) is the computer hardware on which the operating system (OS), operating system and data in the current application are stored for immediate access through the device processor. RAM is the main memory in a computer. It is much faster to read from and write than other types of storage, such as hard disk drive (HDD), solid-state drive (SSD) or optical drive.

SRAM – Static Random Access Memory

Static Random-Access Memory (Static RAM or SRAM) is a type of RAM that holds data in a stable way, that is, as long as the memory is strong. Unlike powerful RAM, it does not need to be upgraded. SRAM stores small data on four transistors using two integrated inverters. Two stable scenarios represent 0 and 1. During reading and writing, two additional transistors are used to control the availability of the memory cell. SRAM can operate at a higher speed than DRAM, which is more expensive due to its complex internal structure. SRAM is well-suited for second-generation applications such as faster CPU cache memory and registry storage. SRAM is often found on hard drives such as disc cache.

DRAM – Dynamic Access Memory

Dynamic access memory (DRAM) is a type of semiconductor memory commonly used for data or program code required by a computer processor to operate. RAM is closer to a computer processor and enables faster access to data than storage media such as hard disk drives and solid-state drives. Each DRAM memory cell is made up of a transistor and a capacitor within an integrated circuit, and a small amount of data is stored in the capacitor. DRAM

is widely used in digital electronics where low memory and high-power memory are required.

Secondary storage

Secondary storage is of 2 types as Local secondary storage and Remote secondary storage. Secondary storage is long-term and non-volatile storage.. Examples are Solid-state storage devices (SSD), hard disk drives (HDD), such as USB memory sticks, optical storage devices, such as CDs, DVDs and so on.

A Remote Data Storage service is a server and equipment space in a data center that can link directly to the Internet or a data connection for online safe data backup. Remote data storage solutions are used by businesses to provide dependable, secure, redundant connection and storage space for essential data.

2. Cache memory, also called cache, is a memory system that automatically stores commands and data that are used for immediate processing by a central processing unit (CPU). The archive contains a copy of the most widely used information or program codes stored in large memory. Cache memory is also available in the processor. Rarely, however, could it be in another integrated circuit, divided into levels. Storage contains a chunk of data that is most needed in large memory.

3.

- **Temporal Locality**

Data or information being used again within a small period of time is referred as Temporal Locality.

- **Spatial Locality**

Data or information being used within relatively close storage locations. There the CPU fetches the data and instruction of the next addresses and store data in the cache memory.

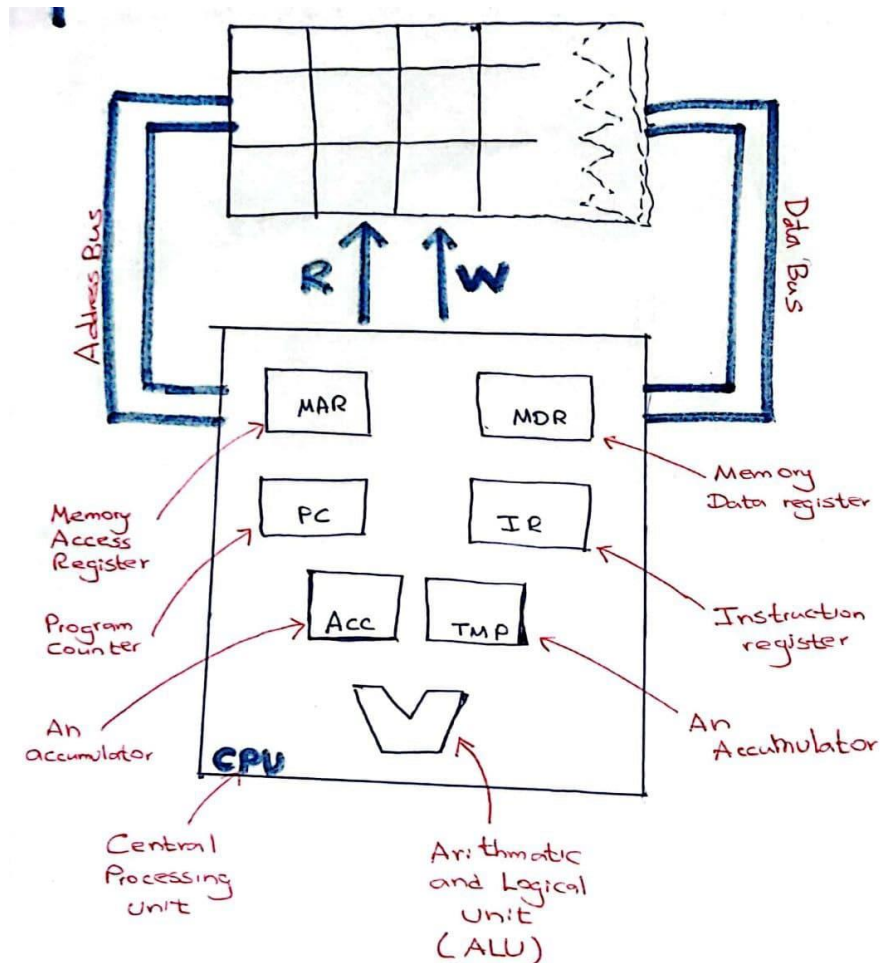
- **Harvard Architecture**

In Harvard architecture, there are separate memories and separate buses for fetching instructions and data. The main use of Harvard architecture other than von Neumann architecture is that CPU can access instruction and read and write data at the same time due to the usage of separate buses for data reading and writing.

- **Von Neuman Architecture**

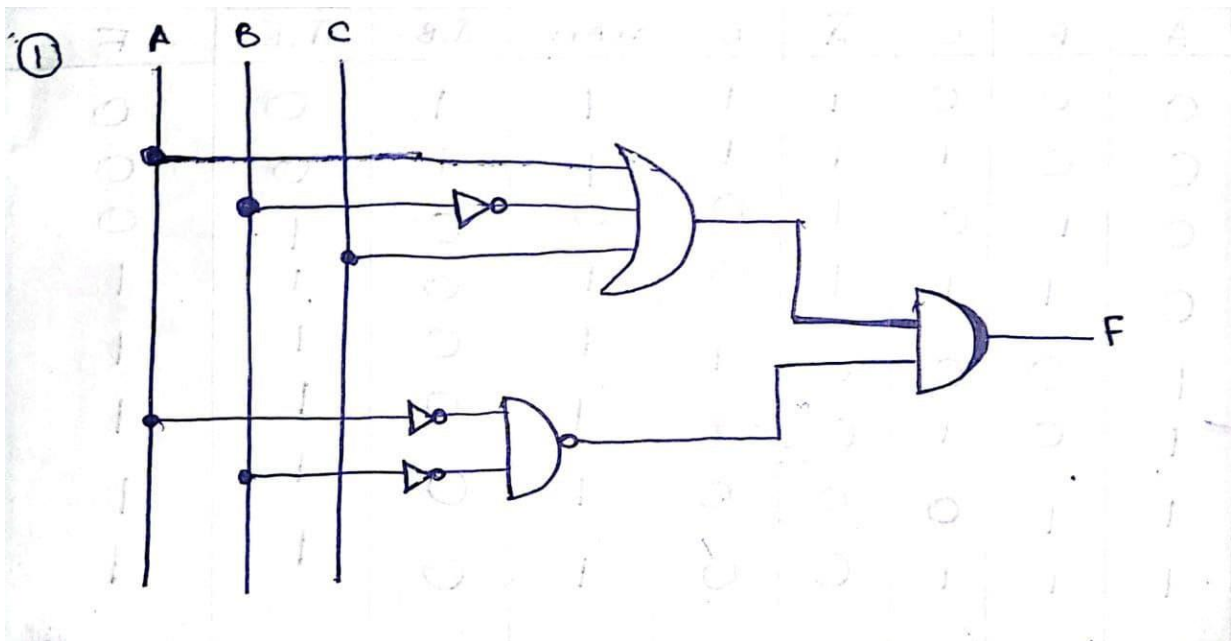
The Von Neuman Architecture consists of control unit, ALU (arithmetic logic unit), and registers. This architecture is based on stored programs where instruction and programs are stored in the same memory. This architecture is commonly used in modern day computers.

4.

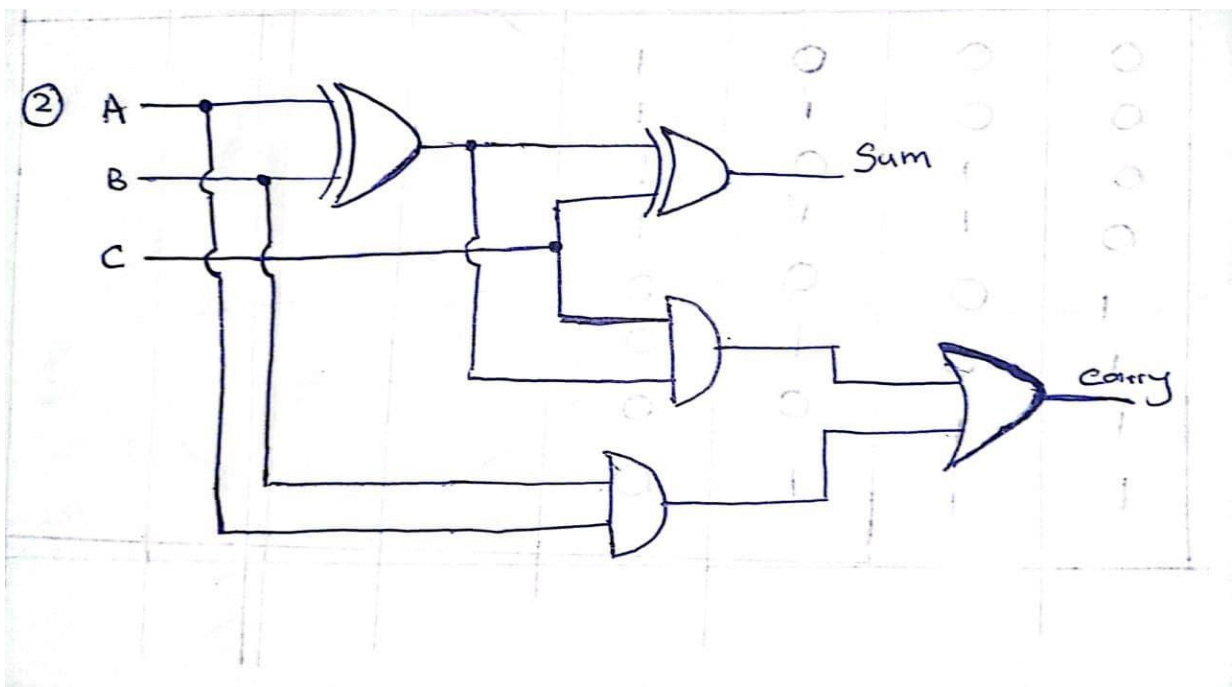


5. Secondary memory is Non-Volatile. But when it comes to external secondary memory, we store data on external hard drives or pen drives, which would help with sharing your data with other computers. External secondary storage devices are the devices which are connected externally to the computer system. And Internal secondary memory storage devices are the devices which has been directly connected to the motherboard.

Question 3



A	B	C	\bar{A}	\bar{B}	$A + \bar{B} + C$	$\bar{A} \cdot B$	$\bar{A} \cdot \bar{B}$	F
0	0	0	1	1	1	1	0	0
0	0	1	1	1	1	1	0	0
0	1	0	1	0	0	0	1	0
0	1	1	1	0	1	0	1	1
1	0	0	0	1	1	0	1	1
1	0	1	0	1	1	0	1	1
1	1	0	0	0	1	0	1	1
1	1	1	0	0	1	0	1	1



Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

③ (a) $F = A \cdot (\bar{A} + B)$

$\bar{A}A + AB \longrightarrow$ Distributive Law
 $0 + AB \longrightarrow$ Complement Law
 $\underline{AB} \longrightarrow$ Identity Law

(b) $F = (A+C) \cdot (AD + \bar{A}D) + AC + C$

$(A+C)A + AC + C \longrightarrow$ Redundancy Law
 $(A+C) \cdot A + C \longrightarrow$ Null Law
 $\underline{A+C} \longrightarrow$ Inverse Law

(c) $F = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C} + A\bar{B}C$

$\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}C$
 $\bar{B}\bar{C} + \bar{B}C(\bar{A} + A)$
 $\bar{B}\bar{C} + \bar{B}C$
 $\bar{B}(\bar{C} + C)$
 $\underline{\bar{B}}$

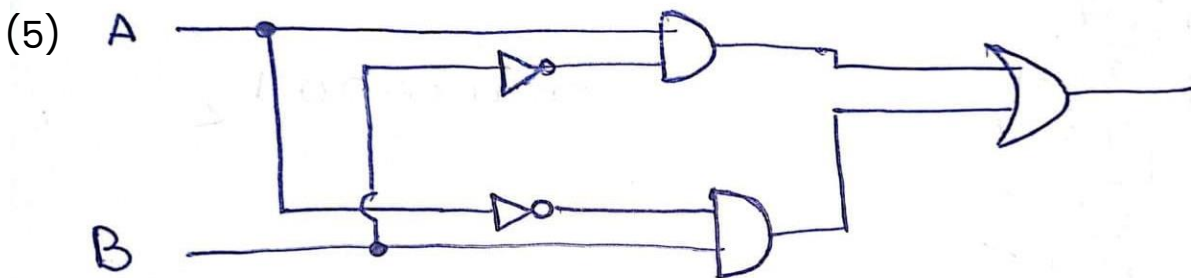
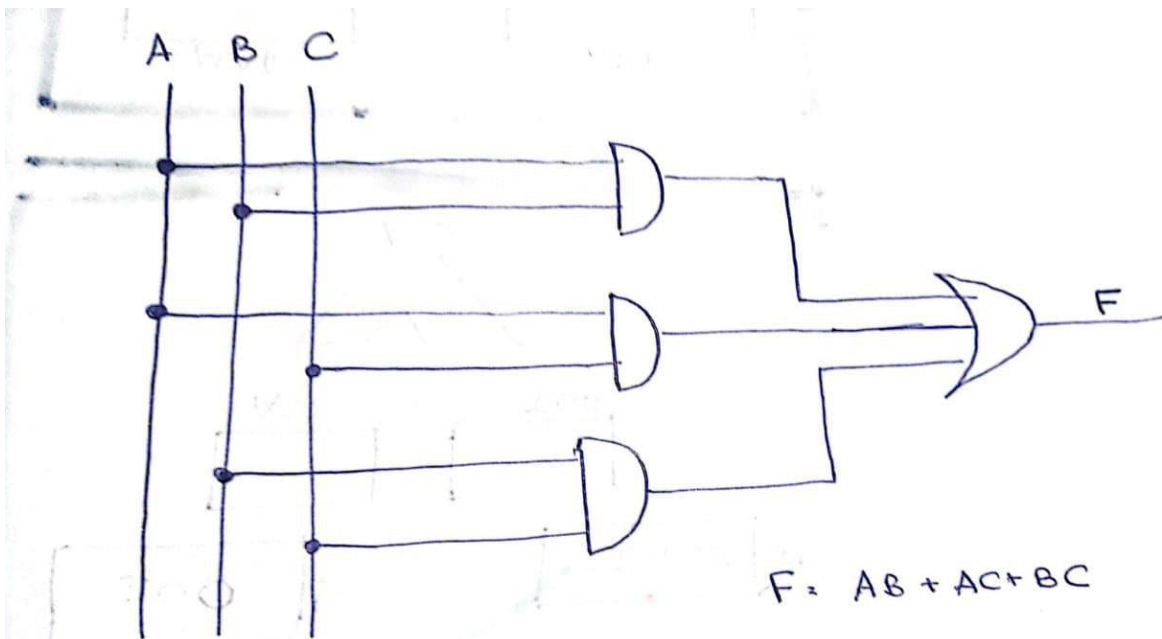
\longrightarrow Redundancy Law
 \longrightarrow Distributive Law
 \longrightarrow Inverse Law
 \longrightarrow Distributive Law
 \longrightarrow Inverse Law

④ $F = \bar{A}BC + A\bar{B}C + ABC\bar{C} + ABC$

Simplified using k-maps.

AB \ C	0	1
10		1
11	1	1
01		1
00		

Simplified expression $\Rightarrow AB + AC + BC$



Question 4

1. Primary memory is a volatile memory to store any information when the computer is turned on. It means it allows the processor to access services that are temporarily stored in a specific memory location. This memory is used to store real-time computer programs and data that the CPU needs. Primary memory is also known as main memory. It could be Random Access Memory (RAM), Cache, or data buses, but it's commonly RAM.

2.

address bus width = 32 bits

data bus width = 8 bits.

no. of addresses = $2^{\text{Address bus width}} = 2^{32}$

Capacity of memory = No. of addresses \times Data bus width

$$= 2^{32} \times 8$$

$$= 2^{32} \times 2^3 \text{ bits}$$

$$= 2^{35} \text{ bits}$$

$$= 2^5 \times 2^{30} \text{ bits}$$

$$= 32 \times G \text{ bits.}$$

$$= \underline{\underline{32 \text{ Giga bits.}}}$$

3.

③ no. of address = $2^{\text{address bus width}}$
 $16M = 2^{\text{address bus width}}$
 $2^4 \times 2^{20} = 2^{\text{address bus width}}$
 $2^{24} = 2^{\text{address bus width}}$
address bus width = 24 bits

4. Address Expansion } Memory Expansion
 Word Expansion }

5.

⑤ $4 \times 16k$ Memory
 Data bus $\rightarrow 4$ bits
 Address bus width = 16×2^{10}
 $= 2^4 \times 2^{10} (2^{14})$
 $= \underline{\underline{14 \text{ bits}}}$

Question 5

1. Combination Logic Circuits

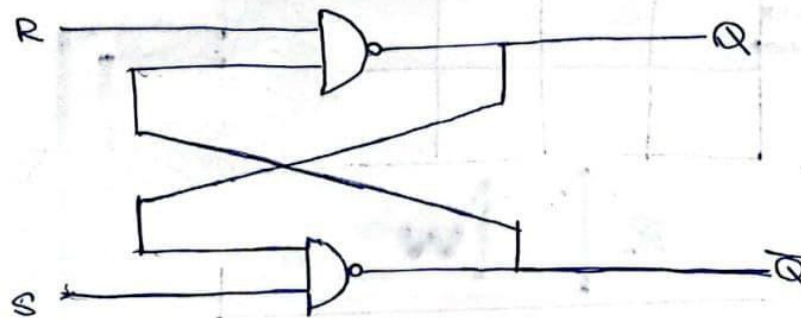
In a combinational circuit, the output is independent of time and merely depends on the input present at the time. As the output of a Combinational circuit is discrete of the time instant, no feedback is necessary for the next generation of output. Logic gates are the very important building blocks of combinational circuits. There is no memory element in these circuits. It's very simple to use and easy to manage.

Sequential Logic Circuits

In a sequential circuit the output is dependent not only on the current input but also on the prior output. The output of the Sequential circuit relies on its previous feedback; therefore, the output of previous input is being transferred as feedback. That feedback is using with input for following next output generation. Flip flops are the building blocks for successive circuits. Memory components are included in these circuits. this circuit is difficult to use and manage.

2.

(2) SR Latch using NAND Gates.



Case 1

Remove

S	R	Q	Q̄
0	1	0	1
1	1	0	1

Case 2

Remove

S	R	Q	Q̄
1	0	1	0
1	1	0	1

Case 3

Remove

S	R	Q	Q̄
0	0	0	0
1	1	0	0

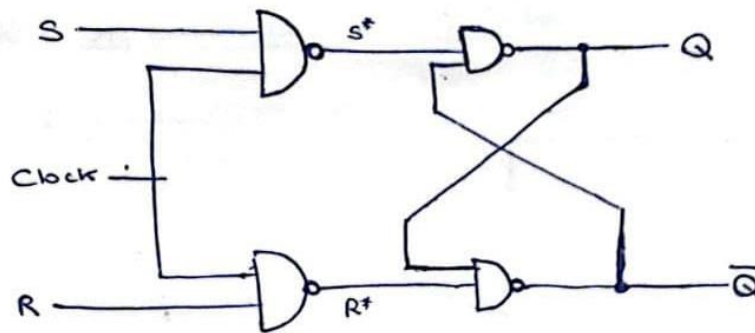
S	R	Q	Q̄
0	0	Not used	
0	1	0	1
1	0	1	0
1	1	Latch	

3. A type of signal that oscillates between a high and a low state and is utilized in order to coordinate actions of circuits is known as "a Clock Signal".

The CPU clock is the internal clock for the chip of CPU, having lower frequency data transfers.

CPU clock is used for measuring the speed of processor.

4.



$$S^* = \overline{(S \cdot C_{lk})} = \overline{S} + \overline{C_{lk}}$$

$$R^* = \overline{(R \cdot C_{lk})} = \overline{R} + \overline{C_{lk}}$$

Case 1 $\Rightarrow C_{lk} = 0 \quad S = x \quad R = x$

Case 2 $\Rightarrow C_{lk} = 1 \quad S = 0 \quad R = 0$

$C_{lk} = 1 \quad S = 0 \quad R = 1$

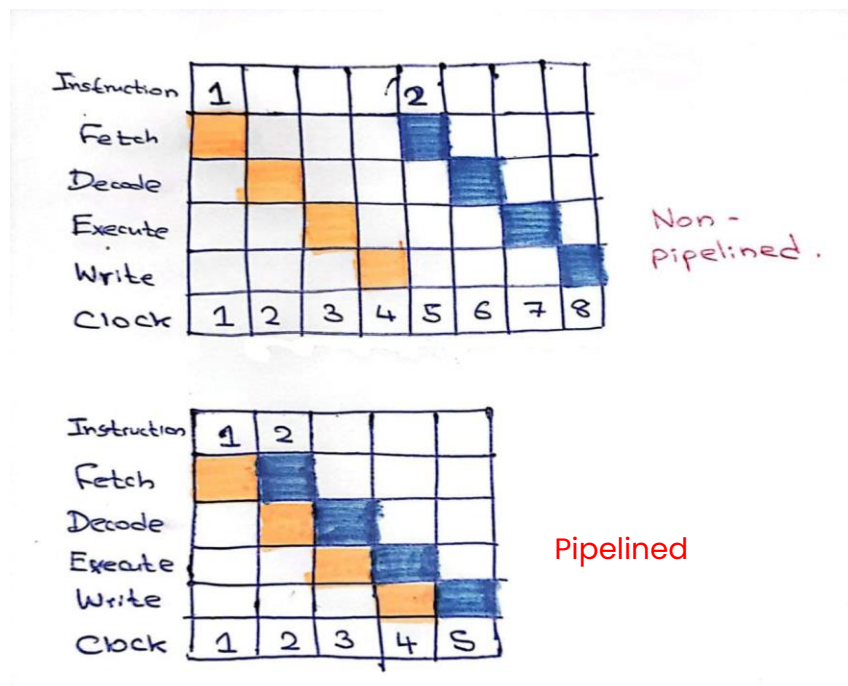
$C_{lk} = 1 \quad S = 1 \quad R = 0$

$C_{lk} = 1 \quad S = 0 \quad R = 0$

$C_{lk} = 1 \quad S = 1 \quad R = 1$

C_{lk}	S	R	Q	\overline{Q}
0	x	x	Latch	
1	0	1	1	0
1	1	0	0	1
1	0	0	Latch	
1	1	1	Not Used.	

5. CPU by using the processor resources in a more efficient manner. The number of instructions that can be executed in a unit of time at a given clock rate.



6. Pipeline Hazards

Pipelining hazards occur when one instruction cannot be flow on another immediately. There are 3 types of pipelining hazards.

- Structural Hazards – Attempting to use the same resource at the same time in two different ways.
- Data Hazards – Attempting to use an item before it is ready.
- Control hazards – Attempting to decide before a condition is evaluated.

Pipeline hazards can be prevented by using different methodologies. Such as,

- Hardware interlocks – In this moment, the second instruction is delayed stopping overlapping and causing a pipelining hazard.
- Operand forwarding – At this moment, it forwards the result one instruction to the next instruction.
- Delayed load – Here, compiler will input an empty function or a no operational function between the instruction which causes the hazard.