## LOGIC GATES (PRACTICE PROBLEMS)

**Key points and summary** – First set of problems from Q. Nos. 1 to 9 are based on the logic gates like AND, OR, NOT, NAND & NOR etc.

First four problems are basic in nature. Problems 3 & 4 are based on word statement.

Problems 5 to 9 are on Universal gates. How the logic circuits can be designed using these gates?

NAND gate implementation has been very common. The procedure is

- Write the Boolean expression in SOP form.
- Simplify the expression
- Double invert it

If Boolean function has only one term then implement by observation.

Problems 10 to 17 are on EX-OR, EX-NOR and other gates. Good number of problems are asked on EX-OR and EX-NOR gates. You have to be thorough with the SOP & POS expressions for these gates and how they have to be used in the problems. Practice these problems to get confidence.

- 1. Indicate which of the following logic gates can be used to realize all possible combinational Logic functions
  - (a) OR gates only

(c) EX OR gates only

(b) NAND gates only

(d) NOR gates only

[GATE 1989: 1 Mark]

**Ans.** (b) and (d)

NAND and NOR gates can be used to realize all possible combinational logic functions. That is why they are also called Universal gates.

- 2. The output of a logic gate is '1' when all its input are at logic 0. The gate is either
  - (a) NAND or an EX OR gate

(c) an OR or an EX NOR gate

(b) NOR or an EX-NOR gate

(d) an AND or an EX-OR gate

[GATE 1994: 1 Mark]

Ans. (b)

If we see first gate of the given options then options (c) and (d) are ruled out as OR and AND gates give 0 output for zero inputs. Now see option (a) where NAND gate satisfies the condition but EX-OR gates does not as it gives 0 output for the same inputs. Option (b) is the correct choice where both gates satisfy the given condition.

**3.** A locker has been rented in the bank. Express the process of opening the locker in terms of digital operation.

Ans.

The locker gate (F) can be opened by using one key (A) which is with the client and the other key which is with the bank (B). When both the keys are used the locker door opens. Locker door is opened i.e. F=1 when both keys are applied A=B=1.

So the process can be expressed as an AND operation.

F=A.B

- **4.** A bulb in a staircases has two switches, one switch being at the ground floor and the other one at the first floor. The bulb can be turned ON and also can be turned OFF by and one of the switches irrespective of the state of the other switch. The logic of switching of the bulb resembles.
  - (a) an AND gate

(c) an XOR gate

(b) an OR gate

(d) a NAND gate

[GATE 2013: 1 Mark]

Ans. (c)

If we look for the truth table of EX-OR gate for two inputs

A	В	F
0	0	0
0	1	1
1	0	1
1	1	0

We can see that the bulb can be put ON and OFF by any one of the switches.

Say, A ground floor switch A = 1, ON and A = 0 OFF

B first floor switch B = 1, ON and B = OFF

F is the bulb F = 1 is ON and 0 is OFF

Let both the switches are is off position (first row of truth table) the bulb is off (since F=0). If switch (A) is put on (A = 1) then bulb turn on (F = 1) OR of switch (B) is put on then also bulb turns.

Similarly you can verify for bulb to be off from either floor

**5.** A Boolean function f of two variables X and Y is defined as follows:

$$f(0, 0) = f(0, 1) = f(1, 1) = 1$$
;  $f(1, 0) = 0$ 

Assuming complements of X and Y are not available, a minimum cost solution for realizing using only 2-input NOR gates and 2-input OR gates (each having unit cost) would have a total cost of

(a) 1 unit

(c) 3 unit

(b) 4 unit

(d) 2 unit

[GATE 2004: 2 Marks]

Ans. (d)

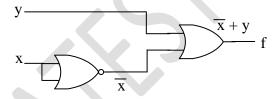
As per definition of Boolean function given in the problem a truth table can be formed

X	y	F
0	0	1
0	1	1
1	0	0
1	1	1

Since the realization is to be done using only NOR and OR gates so, POS equation is to be written i.e. write for 0 term at the output

$$F = \overline{x} + y$$

This function can be implemented as



Since only two gates are required so cost is 2 units.

- **6.** The Boolean function Y = AB + CD is to be realized using only 2 input NAND gates .The minimum number of gates required is
  - (a) 2

(c) 4

(b) 3

(d) 5

[GATE 2007: 1 Mark]

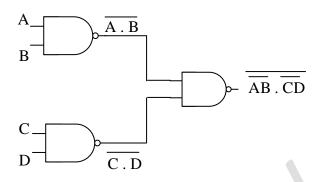
**(b)** 

$$Y = AB + CD$$

We double complement either side

i.e. 
$$\overline{\overline{Y}} = Y = \overline{\overline{AB} + \overline{CD}}$$
$$= \overline{\overline{AB} \cdot \overline{CD}}$$

Logic diagram for the expression is



So, requires three NAND gates

7. Minimum number of 2 input NAND gates required to implement the function,

$$F = (\bar{X} + \bar{Y})(Z + W)$$
 is

(a) 3

(c) 5

(b) 4

(d) 6

[GATE 1998: 1 Mark]

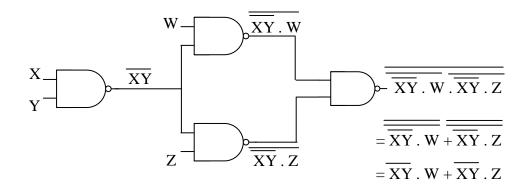
$$F = (\overline{X} + \overline{Y})(Z + W)$$

The Boolean expression is in POS form. It should be converted into SOP and simplified

$$F = (\overline{X} + \overline{Y})(Z + W)$$
$$= \overline{XY}(Z + W)$$

$$F = \overline{XY}Z + \overline{XY}W$$

Above expression cannot be simplified further.



- **8.** The minimum number of 2-input NAND gates required to implement the Boolean function  $Z = A\bar{B}C$ , assuming that A, B and C are available is
  - (a) Two

(c) Five

(b) Three

(d) Six

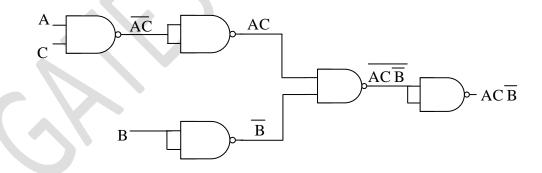
[GATE 1998: 1 Mark]

Ans. (c)

$$Z = A\overline{B}C$$

Since there is only one term so can be implemented directly.

$$Z = A\overline{B}C = AC\overline{B}$$



- **9.** The minimum number of NAND gates required to implement the Boolean function  $A + A\bar{B} + A\bar{B}C$  is equal to
  - (a) Zero

(c) 4

(b) 1

(d) 7

[GATE 1995: 1 Mark]

= A

Let 
$$F = A + A\overline{B} + A\overline{B}C$$
  
 $= A(1 + \overline{B}) + A\overline{B}C$   
 $= A + A\overline{B}C$   
 $= A(1 + \overline{B}C)$ 

So to implement above function no NAND gate is required.

**10.** The Boolean expression for the output of EX-NOR (equivalence) logic gate with inputs A and B is

(a) 
$$A\bar{B} + \bar{A}B$$

(c) 
$$(\bar{A} + B)(A + \bar{B})$$

(b) 
$$\bar{A}\bar{B} + AB$$

(d) 
$$(\bar{A} + \bar{B})(A + B)$$

[GATE 1993: 1 Mark]

Ans. The Boolean expression in SOP form for EX-NOR gate is

$$F = \overline{A}\overline{B} + AB$$

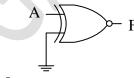
i.e. output is 1 when both inputs are same. The expression in POS form can be derived from SOP

$$A \odot B = \overline{A \oplus B} = \overline{A\overline{B} + \overline{A}B}$$
$$= \overline{A\overline{B}}.\overline{\overline{A}B}$$
$$= (\overline{A} + B).(A + \overline{B})$$

**Option** (c) is in **POS** form

Option (b) is in SOP form

11. The output of the logic gate in figure is



(a) 0

(c)  $\bar{A}$ 

(b) 1

(d) A

[GATE 1997: 1 Mark]

Ans. Given gate is EX-NOR gate

$$A \odot B = \overline{A \oplus B} = \overline{A}\overline{B} + AB$$

Here one input is grounded say B is grounded

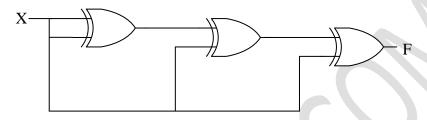
$$F = A \odot B = \overline{A}.\overline{0} + A.0$$

$$F = \overline{A}$$

So the output is  $F = \overline{A}$ 

Option (c)

12. For the circuit shown below the output F is given by



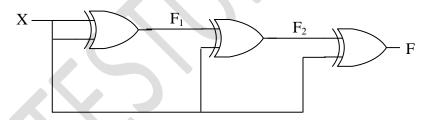
- (a) F = 1
- (b) F = 0

- (c) F = X(d)  $F = \overline{X}$

[GATE 1998: 1 Mark]

Output of first EX-OR gate is  $F_1 = X \oplus X = 0$ Ans.

Output 2nd EX=OR gate



$$F_2 = X \oplus 0 = X$$

Note if X = 1, then output is 1

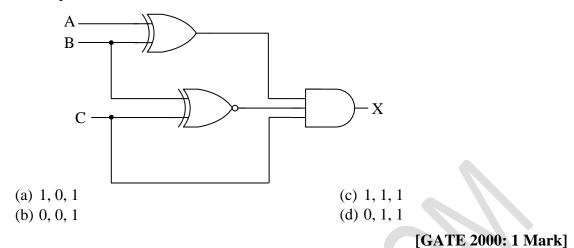
If X = 0, then output is 0

So whatever is the input the output is same so  $F_2 = X$ 

Output of 
$$3^{rd}$$
 EX-OR  $F = X \oplus X = 0$ 

Option (b)

13. For the logic circuit shown in the figure, the required input condition (A,B,C) to make the output X=1 is



Ans. (d)

As per the result the output X has to be 1, so all the inputs of AND gate should be 1.

i.e. C must be equal to 1.

One input to EX-NOR is 1(i.e. C)

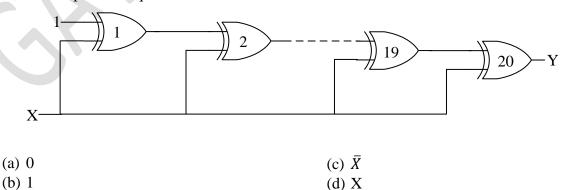
The other input should also be 1 to get the 1 output i.e. B=1

One of the input to EX-OR is 1(B=1) the other input has to be 0 to get 1 output at EX-OR Gate.

So, A=0, B=1 And C=1

Option (d)

**14.** If the input to the digital circuit (in the figure) consisting of cascaded 20 XOR gates is X, then output Y is equal to



[GATE 2002: 1 Mark]

**Ans.** (b)

**Output of first XOR** 

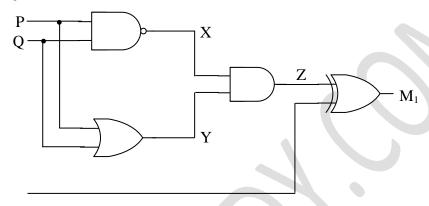
$$F_1 = \overline{A}B + A\overline{B} = 0.X + 1.\overline{X} = \overline{X}$$

Output of 2<sup>nd</sup> XOR

$$F_2 = \overline{X} \oplus X = 1$$

Now the  $3^{rd}$  XOR has the same input as first gate. So after 4, 6, 8, ..... $20^{th}$  XOR the output will be 1.

**15.** Which of the following Boolean expressions correctly represents the relation between P, Q, R and  $M_1$ .



- (a)  $M_1 = (P OR Q) XOR R$
- (b)  $M_1 = (P \text{ AND } Q) \text{ XOR } R$

- (c)  $M_1 = (P \text{ NOR } Q) \text{ XOR } R$
- (d)  $M_1 = (P XOR Q) XOR R$

[GATE 2008: 1 Mark]

Ans. (d)

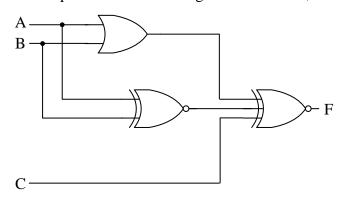
Boolean expression for the given circuit is

$$M_1 = [\overline{P \cdot Q} \cdot (P + Q)] \oplus R$$
$$= [(\overline{P} + \overline{Q}) \cdot (P + Q)] \oplus R$$

The expression in the bracket is POS form of XOR gate

So, 
$$M_1 = [P \oplus Q] \oplus R$$

16. For the output F to be 1 is the logic circuit shown, the input combination should be



(a) A = 1, B = 1, C = 1

(c) A = 0, B = 1, C = 0

(b) A = 1, B = 0, C = 0

(d) A = 0, B = 0, C = 1

[GATE 2010: 1 Mark]

Ans. (d)

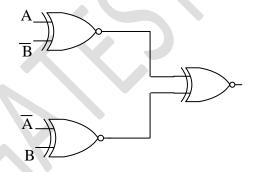
The same inputs A and B are connected to EX-OR and EX-NOR gates. So the Output of them will be complement of each other i.e. 0,1 or 1,0.

For F to be 1, the inputs to EX-NOR should be even (even number of 1's).

For the input 1's to be even numbers C has to be 1.

There is only one option with C=1 i.e. option (d).

17. The output of the circuit shown is equal to



- (a) 0
- (b) 1

- (c)  $\bar{A}B + A\bar{B}$
- (d)  $\overline{(A \oplus B)} \oplus (A \oplus B)$

[GATE 1995: 1 Mark]

Ans. (b)

**Boolean expression for output** 

$$F = (A \odot \overline{B}) \odot (\overline{A} \odot B)$$

Using associative property we can write

$$F = (A \odot \overline{A}) \odot (\overline{B} \odot B)$$

$$= 0 \odot 0$$

Note that  $A \odot \overline{A} = 0$ 

Since A and  $\overline{A}$  are complement of each other that

If 
$$A = 1$$
,  $\overline{A} = 0$ ,  $so$   $A \odot \overline{A} = 0$ 

Similarly the 2<sup>nd</sup> term.

$$(\overline{B} \odot B) = 0$$