NATIONAL SCHOOL OF BUSINESS MANAGEMENT

BSc in Management Information Systems (Special) (NSBM)– 22.2
BSc (Honours) in Software Engineering (NSBM)– 22.2
BSc (Honours) in Computer Networks (NSBM)– 22.2
BSc (Honours) in Computer Science (NSBM)– 22.2
BSc (Honours) Software Engineering (PU)– 22.2
BSc (Honours) Computer Networks (PU)– 22.2
BSc (Honours) Computer Science (PU)– 22.2
BSc (Honours) Computer Security (PU)– 22.2
Bachelor of Information Technology (NBIT): major in Web and Mobile Application Development (VU)– 22.2

Year 01 Semester 02 Examination
09 August 2023
CS 104.3 – Computer Architecture

Instructions to Candidates

1) **Answer All the Questions.**
2) Illustrate answers with sketches where required.
3) Time allocated for the examination is **three (03) hours.**
4) If a page or a part of this question paper is not printed, please inform the Supervisor immediately.
5) Write your index number in all pages of answer script.
6) Attach all answer sheets at the end of the examination.

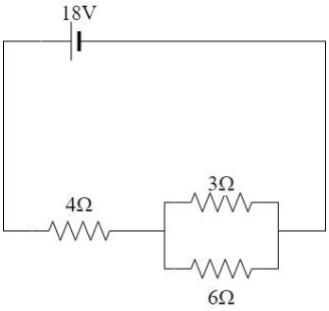
Question 1 (25 Marks)

1. Construct the truth table and the logical circuit for the following Boolean expressions.
   a. F = (A' + B) XOR (A.B')
   b. F = (A' NAND (B+C'))' NOR C

   (6 Marks)
2. Extract the SOP (Sum of Products) and POS (Product of Sums) expressions for the following truth table. (4 Marks)

A	B	C	Output
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

3. By using K-Maps simplify the above two expressions. (5 marks)
4. Construct the logic circuit for the simplified SOP expression. (5 marks)
5. Consider the following electrical circuit,



a) Calculate the total resistance of the system.
b) Calculate the current flow of the system.

(5 marks)

Question 2 (25 Marks)

1. "Central Processing Unit is considered as the brain of the computer system" explains the composition of the computer hardware components including ALU, control unit and memory devices. (Use a diagram to assist your answer) (5 marks)

2. Describe the sequence of events carried out during the machine cycle when executing the following instructions. (Use diagrams to assist your answer like you used to do in lecturers)

Adress	Content
722	LDA 1400
723	SUB 1401
724	STO 1403
1400	45
1401	26
1403	

(8 marks)

3. A system bus consists with 16 data lines and 8 address lines, (2 marks)
    a. How many addresses can be accessed with this bus ?
    b. How many data bits it can carry ?
4. Using the memory hierarchy pyramid explain why computer needs multiple memory units instead of one memory. (Use any diagram and examples) (6 marks)
5. Write brief descriptions for following topics. (4 marks)
    a. Multiplexed Bus
    b. Split cache vs Unified cache

Question 3 (25 Marks)

1. A typical machine uses an instruction set architecture that allocates 10 bits for the opcode and 26 bits for the operands. (5 marks)
    a. Briefly explain what is an Instruction Set.
    b. How many different instructions can it have ?
    c. What is the maximum memory size that it can address ?

2. Contrast the difference between following terms, (6 marks)
    a. Direct addressing vs Indirect addressing
    b. Fixed length Instruction vs Variable length Instruction

3. The following truth table represents the addition of two bits in computing, by extracting the simplified output expression from the table construct the logical circuit of the half adder.

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

(5 marks)

4. Explain the functionality of the 4-input multiplexer by using truth tables and logical circuits including the enabling signal. (Use diagrams and cases to assist your answer) (5 marks)

5. Briefly explain the difference between the multiplexer and the demultiplexer and mention a few applications of them. (4 marks)

Question 4 (25 marks)

1. “Clock signals are used to control the activation of sequential circuits”, briefly explain two triggering methods that are used with clock signals. (2 marks)

2. Demonstrate the functionality of the SR latch based on NAND gates including all the input cases and recheck each case with latching inputs. (Summary truth table and the logical circuit required) (6 marks)

3. Explain how SR latch formed the SR flip flop. (Use truth table with all the input cases and the logical circuit) (6 marks)

4. In a pipelined processor an instruction is executed through four stages as follows, and the times taken to each stage is mentioned as follows. (6 marks)

Stage	Time
Fetch	3
Decode	6
Execute	9
Store	3

   a) Draw a gnat chart to represent how this processor executes four similar instructions.
   b) Calculate the minimum time to execute four instructions.
   c) Calculate the Latency and the Throughput of this machine.

5. Mention three pipeline hazards and explain two solutions for any of them. (Can use diagrams for the explanation) (5 marks)