NATIONAL SCHOOL OF BUSINESS MANAGEMENT

BSc in Management Information Systems (Special) (NSBM)– 21.2
BSc (Honours) in Software Engineering (NSBM)– 21.2
BSc (Honours) in Computer Networks (NSBM)– 21.2
BSc (Honours) in Computer Science (NSBM)– 21.2
BSc (Honours) Software Engineering (PU)– 21.2
BSc (Honours) Computer Networks (PU)– 21.2
BSc (Honours) Computer Science (PU)– 21.2
BSc (Honours) Computer Security (PU)– 21.2
Bachelor of Information Technology (NBIT): major in Web and Mobile Application Development (VU)– 21.2

Year 01 Semester 02 Examination
15th August 2022
CS104.3 – Computer Architecture

Instructions to Candidates

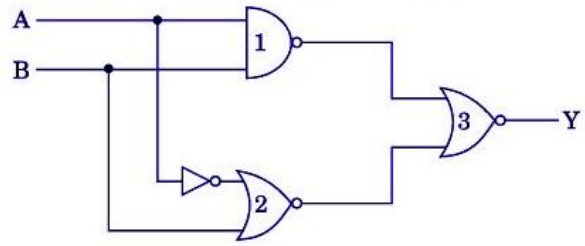
1) **Answer all questions.**
2) **Time allocated for the examination is five (05) hours (Including downloading and uploading time)** . (Note: **No email submissions are accepted under any condition.)**
3) Weightage of Examination: 60% out of final grade
4) Download the paper, provide answers to the selected questions in a word document.
5) Please upload the document with answers (Answer Script) to the submission link before the submission link expires
6) Answer script should be uploaded in PDF Format
7) Under any circumstances E-mail submissions would not be taken into consideration for marking. Incomplete attempt would be counted as a MISSED ATTEMPT.
8) The Naming convention of the answer script – Module Code_Subject name_Index No
9) You must adhere to the online examination guidelines when submitting the answer script to N-Learn.
10) Your answers will be subjected to Turnitin similarity check, hence, direct copying and pasting from internet sources, friend's answers etc. will be penalized.

Question 1. - 25 Marks

i. Explain the importance of Boolean expression simplification in Digital Circuit Designing. (03 Marks)

ii. Find the Boolean expression for the following circuit (02 Marks)

(1-NAND gate, 2-NOR gate, 3-NOR gate)



iii. Simplify the following expressions using De Morgan's Law. (04 Marks)

a. $\overline{(\overline{X}+Z)(\overline{XY})}$

b. $\overline{(\overline{X\cdot\overline{Y}})\cdot(\overline{Y}+Z)}$

iv. Z = f (A, B, C, D)

Z =1 for the minterms (0, 2, 5, 7)

Z= don't care for the minterms (8,10, 13,15)

Z = 0 for the remaining minterms.

a. Draw the truth table (04 marks)

b. Simplify Z using K- map method (06 Marks)

c. Draw the digital circuit diagram to get Z as output (06 Marks)

Question 2. - 25 Marks

i. Draw the truth table of Full Adder and implement the circuit using basic logic gates. (04 Marks)

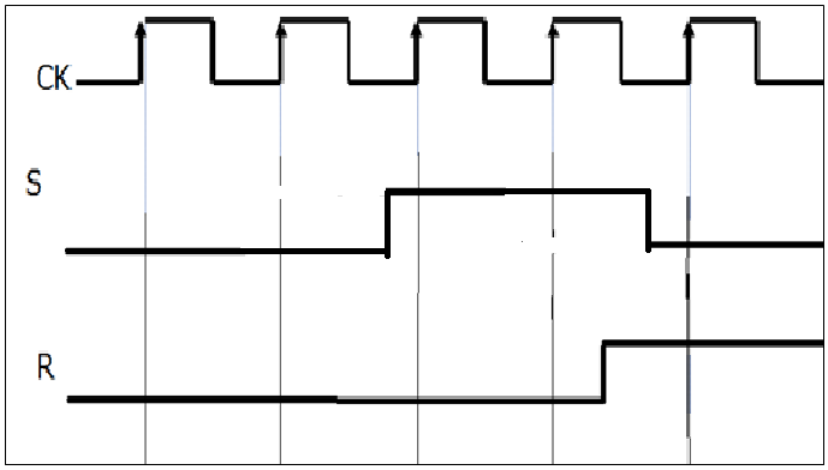
ii. An assembly line has 3 failsafe sensors and 1 emergency shutdown switch. The assembly line will be deactivated by switching off the emergency shutdown switch if anyone of the following conditions occur.

- If the emergency switch is pressed, the system shuts down.
- If sensor 1 and sensor 2 are activated at the same time, the system shuts down.
- If sensor 1 and sensor 3 are activated at the same time, the system shuts down.

- If all three sensors are activated at the same time, the system shuts down.
  a. Determine the truth table for the circuit. (02 Marks)
  b. Obtain the simplified
     i. SOP expression (02 Marks)
     ii. POS expression (02 Marks)
  c. Implement the circuit using logic gates for (i) and (ii) part(b). (08 Marks)

iii. Complete the truth table of J-K flip flop and derive its excitation table. (03 Marks)

iv. Draw the output waveform Q and $\overline{Q}$ of a **positive** edge triggered SR flip flop. Assume that the initial value of the flip flop is 0. (04 Marks)



Question 3. - 25 Marks

i. Describe the role of CPU in terms of computer architecture. (02 Marks)

ii. Including the assumption made, explain **Von Neumann Architecture** with suitable diagram. (3 Marks)

a. What is known as the Von Neumann bottleneck? (2 Marks)

b. Describe two reasons which led to increase Von Neumann bottleneck in recent years (4 Marks)

c. Describe two Approaches to overcoming the von Neumann Bottleneck. (4 Marks)

iii. Explain the functionality of the ALU with an example. Use a diagram to assist your answer. (02 Marks)

iv. Describe the sequence of events carried out during the machine cycle when executing the following instructions with suitable diagram. (08 Marks)

Address	Contents	
499	LDA 1000	
500	SUB 1001	Subtract the contents of the Accumulator with the contents of the memory location 1001 and store the result back in the Accumulator.
501	STO 1002	
502	JMP 600	
1000	6	
1001	2	
1003		

Question 4. - 25 Marks

i. Explain the arrangement of 256-bit memory with suitable diagram. With reasoning the number of address lines and control lines of it. (4 Marks)

ii. There is a 3 x 512 bits memory chip. Calculate the capacity of the memory chip in Bytes. (02 Marks)

iii. Calculate the capacity of a memory. If, Address bus width= 16 bits Data bus width= 8 bits (02 Marks)

iv. What are the memory expansion techniques (03 Marks)

v. In a memory there are 16M addresses. What is the width of the address bus? (03 Marks)

vi. Build an 8X64 bits memory chip using 8X16 bits memory chip. (04 Marks)

vii. Construct an 4x16K memory using 1x4k memories (07 Marks)

*******END*******