AMERICAN INTERNATIONAL UNIVERSITY BANGLADESH

Faculty of Engineering

Laboratory Report Cover Sheet

Students must complete all details except the faculty use part.

Please submit all reports to your subject supervisor or the office of the concerned faculty.

Laboratory Title: _____

Experiment Number: __7___ Due Date: _____ Semester: _____

Subject Code: _____ Subject Name: _____ Section: ____

Course Instructor: Degree Program: _____

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Group Number (if applicable): Individual Submission Group Submission

No.	Student Name	Student Number	Student Signature	Date
Submitted by:				
1				
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2				
3				
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5				

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Total Marks: _____ Marks Obtained: _____

Faculty comments_____

ABSTRACT:

This experiment is mainly focused on implementing a synchronous and an asynchronous using flipflop. The objective is to construct the circuit on breadboard by using synchronous and an asynchronous counter, noted down the outputs from given combinational inputs and verify them with their respected truth table. Along with trainer board counters, LED's and wires are required and multisim software used for simulated verification. It is proven that the experimental output for these counters match with their truth table values. The result signifies that the conventional circuit can be constructed using counter, flipflop and they are applicable is arithmetic unit Design.

INTRODUCTION:

The implementing is basically a digital circuit design which the output depends on the given input of clock pulse at a certain point of time. This experiment is illustration of implementing an asynchronous and synchronous counter using flipflop counter is a sequential circuit. A digital circuit which is used for a counting pulses is known counter. Counter is widest application of flipflop. A flipflop is electronic circuit with two stable that can be used to store binary data. The store data can be change by applying varying inputs. A group of flipflop with a clock signal applied.

There are two types of counters-

- Asynchronous counter
- Synchronous counter

THEORY AND METHODOLOGY:

Asynchronous counter

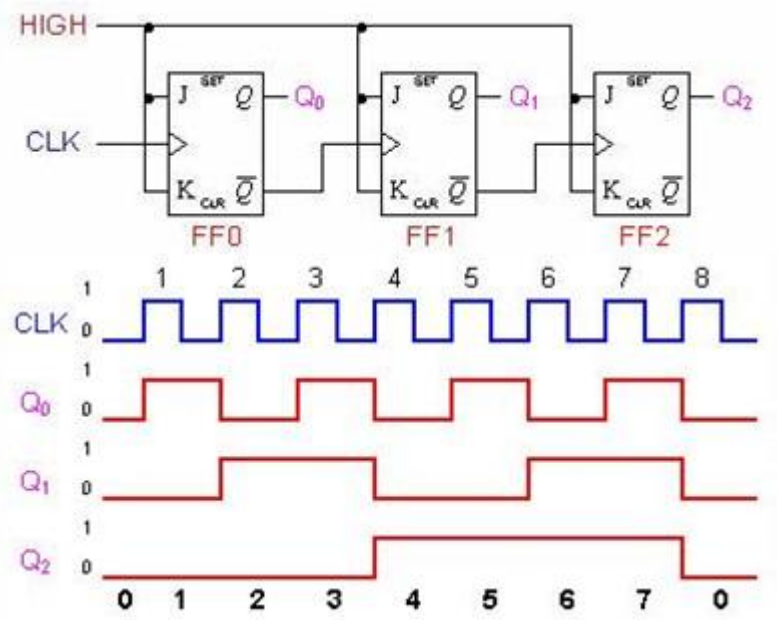


Figure 9.1: 3 bit Asynchronous counter and its timing diagram

In figure 9.1, a three-bit asynchronous counter is displayed. Only the clock input of the first flip-flop (FF0) is connected to the external clock. As a result, FF0 switches states at the falling edge of every clock pulse, whereas FF1 only does so when the Q output of FF0 triggers it. The transition of the input clock pulse and a transition of the Q output of FF0 can never happen at precisely the same moment due to the intrinsic propagation delay through a flip-flop. Therefore, an asynchronous operation results from the flip-flops being unable to be triggered simultaneously.

A three-bit counter that can count from 0 to 7 is shown in Figure 9.1. The three flip-flops' clock inputs are connected to one another in a cascade. Each flip-flop has a T input that is connected to a constant of 1, which means that on each positive edge of its clock, the flip-flop's state will be reversed (toggled). We're assuming that the circuit's main goal is to count the number of pulses that come in on the Clock input's main input. As a result, the Clock line is connected to the clock input of the first flip-flop. The Q output of the flip-flop before it drives the clock inputs of the other two flip-flops. Therefore, they toggle their state whenever the preceding flip-flop changes its state from Q = 1toQ = 0, which results in a positive edge of the Q signal.

A timing diagram for the counter is shown in Figure 9.1. Every clock cycle, Q0's value changes once. Shortly after the clock signal's positive leading edge, the transition occurs. The propagation delay through the flip-flop is what causes the delay. The value of Q1 changes immediately after the negative edge of the Q0 signal because Q0 clocks the second flip-flop. Similar to Q1, Q2 also experiences a change in value immediately following Q1's negative edge. The timing diagram shows that the counting sequence is 0, 1, 2, 3, 4, 5, 6, 7, 0, 1, and so on if we use the values Q2Q1Q0 as the count. This circuit is a modulo-8 counter. Because it counts in the upward direction, we call it an up-counter.

Synchronous counter

In synchronous counters, all of the flip-flops' clock inputs are linked together and are activated by the input pulses. As a result, all flip-flops change state at once. Since all flip-flops are triggered simultaneously, the main benefit of synchronous counters is that there is no cumulative time delay. As a result, this counter's maximum operating frequency will be far higher than that of the analogous ripple counter.

Table 9.1 displays a four-bit up-counter's contents over the course of eight clock cycles, assuming that the count starts out at 0. Each clock cycle causes bit Q0 to change, as can be seen by looking at the arrangement of bits in each row of the table. Only when Q0 is 1, bit Q1 changes. When Q1 and Q0 are both equal to 1, only bit Q2 changes. A given flip-flop generally changes its state for an n-bit up-counter only when all of the flip-flops before it are in the state Q = 1.

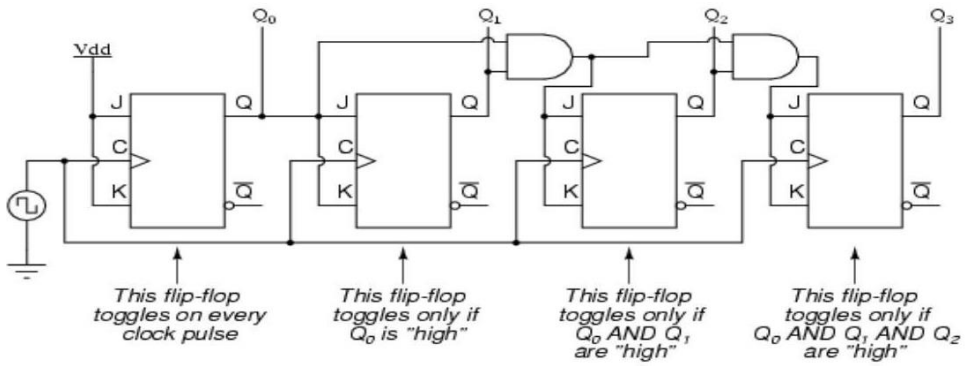


Figure 9.2a: A four-bit Synchronous Up Counter

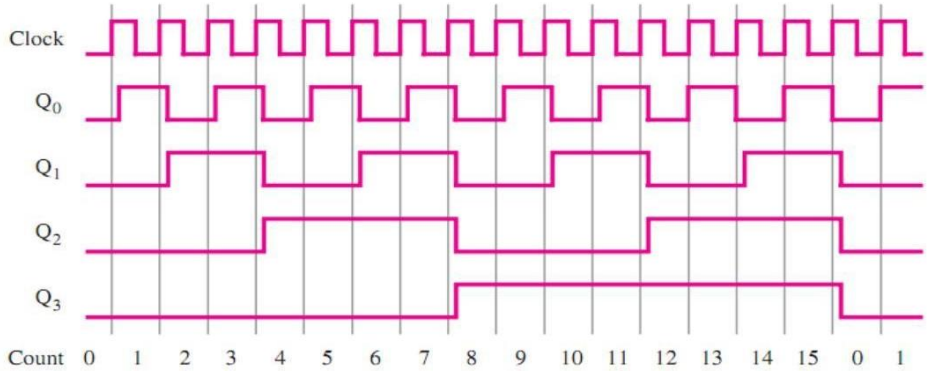
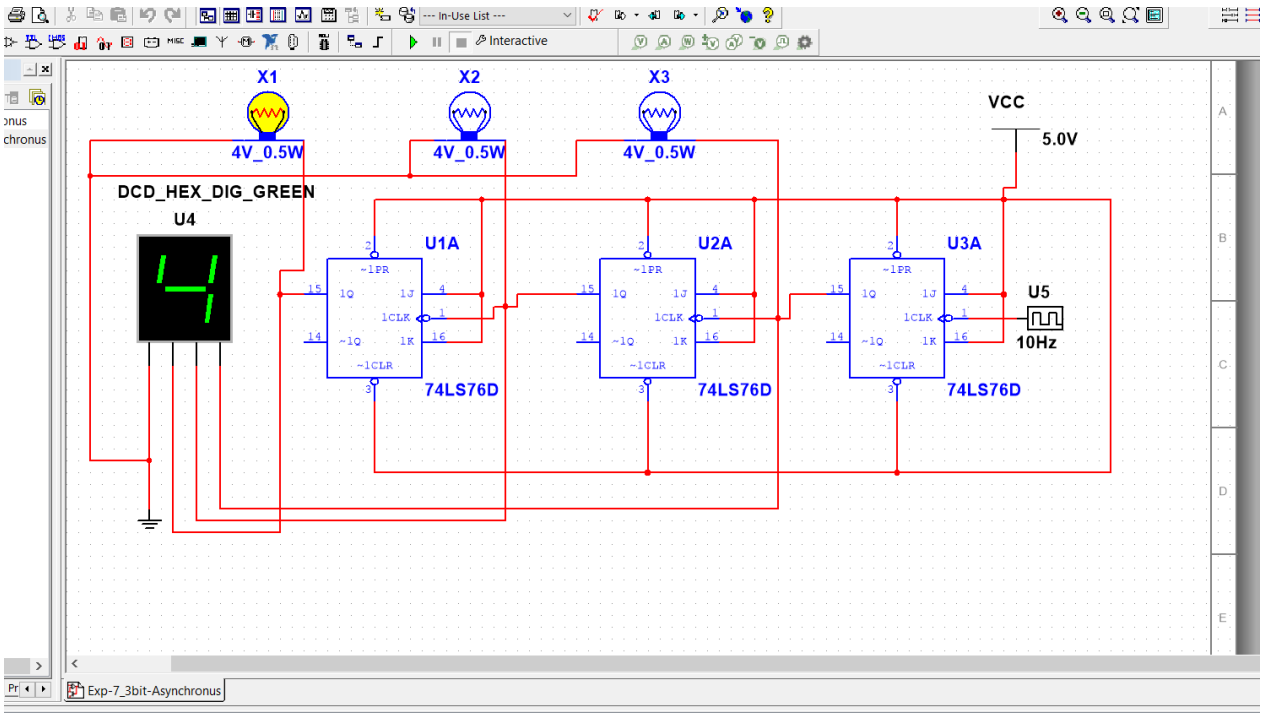


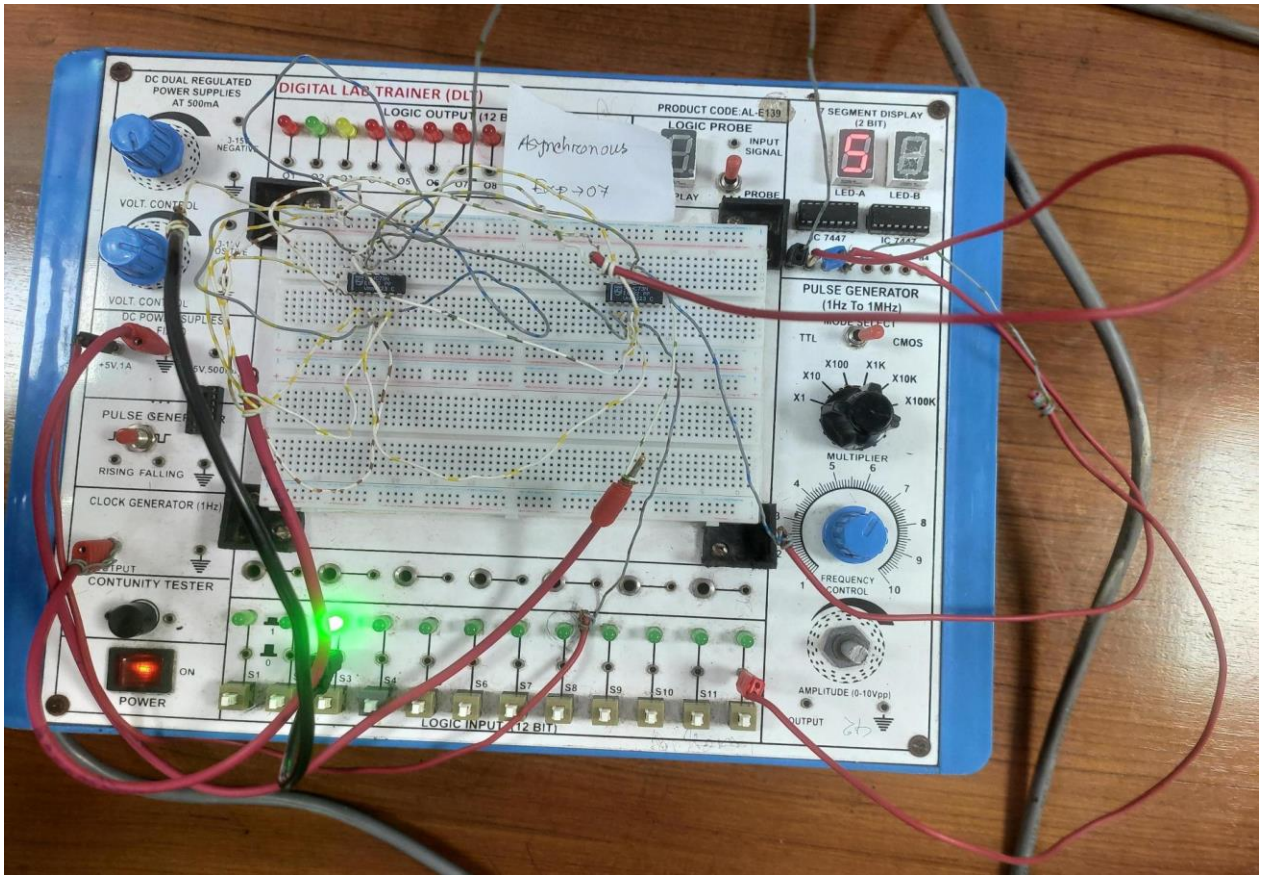
Figure 9.2b: The timing diagram of a four-bit Synchronous Up Counter

SIMULATION:

Asynchronous:

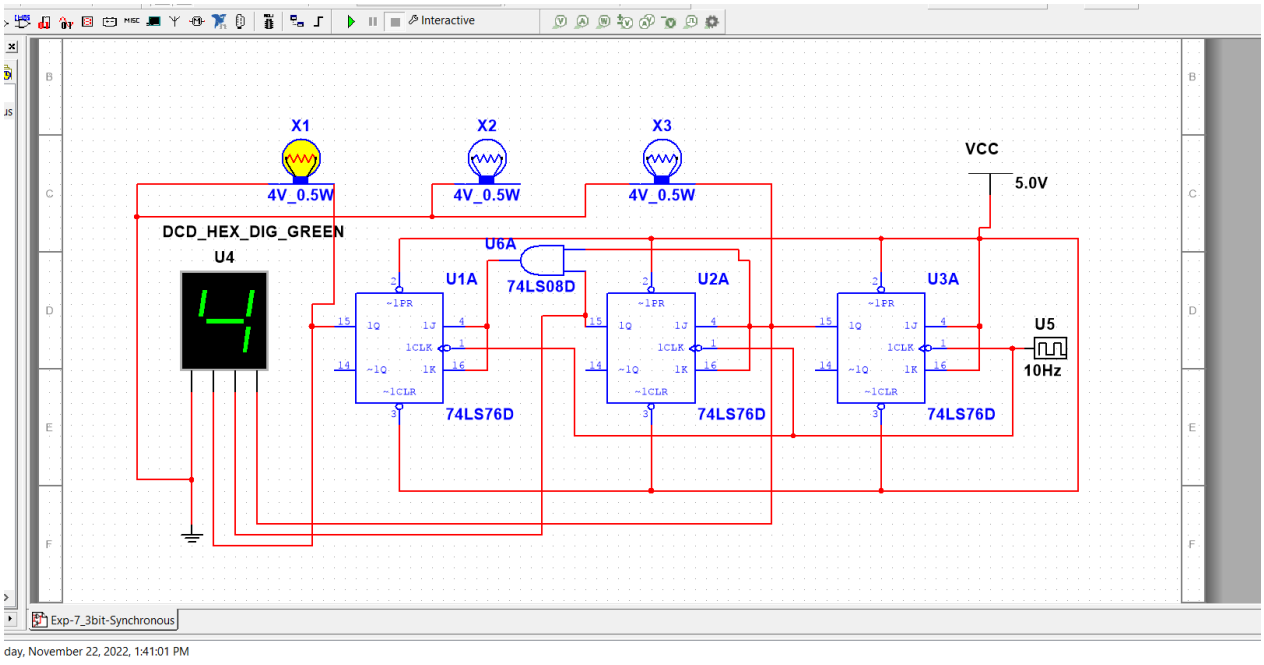


Multisim Simulation

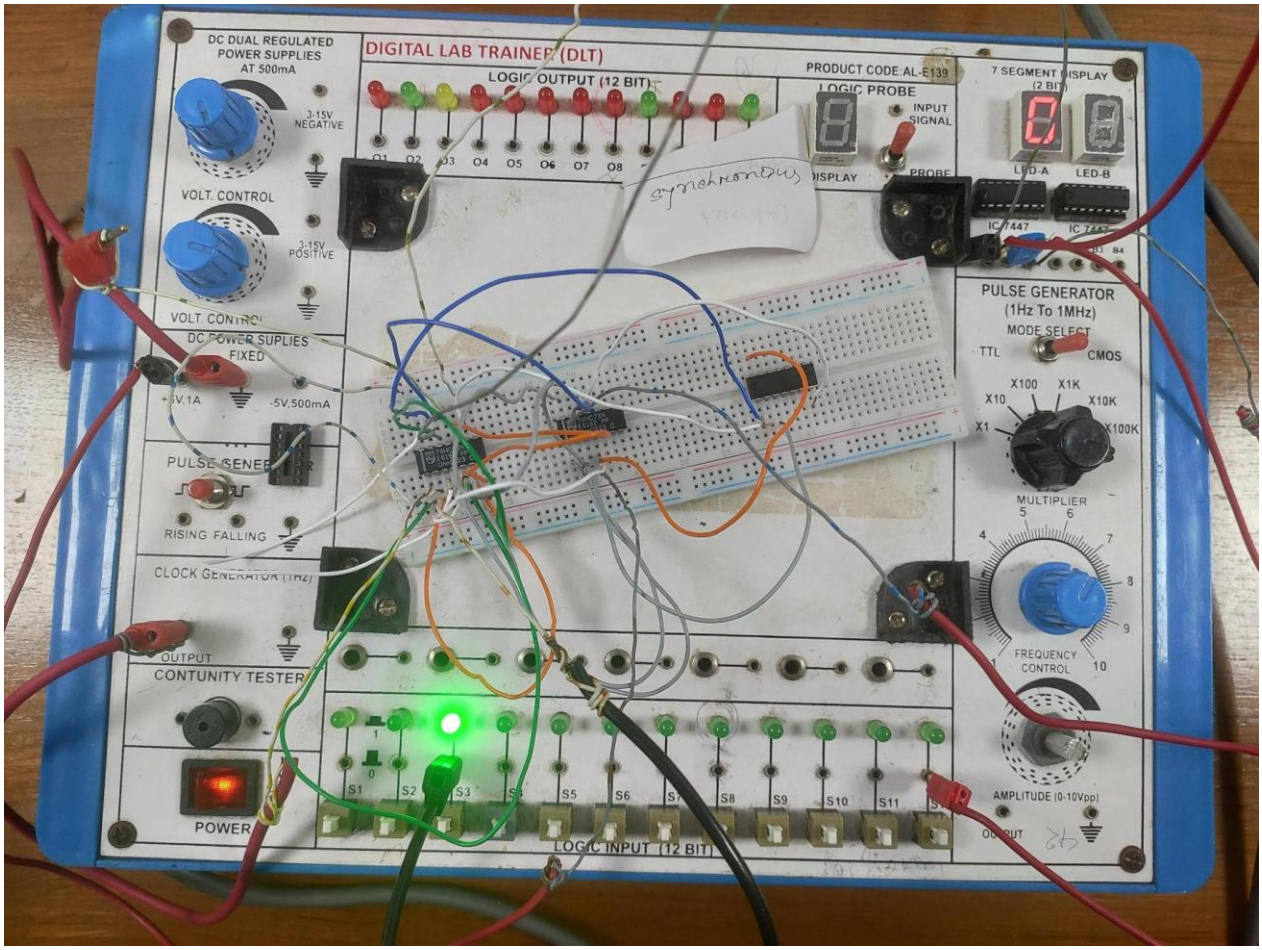


Lab Simulation

Synchronous:



Multisim Simulation



Lab Simulation

RESULT:

Truth table of Flip Flop-

Clock	J	K	Q_{n+1}	State
0	x	x	Q_n	
1	0	0	Q_n	Hold
1	0	1	0	Reset
1	1	1	1	Set
1	1	1	$\overline{Q}_n$	Toggle

DISCUSSION:

In the beginning of the experiment the concept of counters was discussed. There are many counters such as Asynchronous and synchronous. We have learned about these two counters. In this lab we implemented total 2 circuit, first one was 3-bit Asynchronous counter Logic circuit. And Last one was 4-bit Synchronous Up Counter.

At first our respected faculty give us the theory concept. Then we implemented these counter in circuit board. After doing the implementation our circuit was matched with the accepted result. That's why the counter was showed the result properly. After doing the lab physically we implemented in simulation software also. We implemented using Multisim software.

Although we got theory clearly but in our circuit board asynchronous circuit was matched properly but the synchronous didn't match accurately. Our instructor helps us with the problem. But we got all the results in our simulation and simulation results matched with the counter sequence properly.

To conclude, we just want to say that our simulation results perfectly matched with theory concept. For the physical implementation we have faced some problems which we eventually overcome with the help of our instructor. As the criteria was full filled according to the instruction so we can say that our experiment was successful.

CONCLUSION:

To sum up, synchronous and an asynchronous circuit designing can do operation with binary digit asynchronous input or a flipflop have control over the outputs regardless of clock input status. These inputs are called preset and clear. Using these on a synchronous and asynchronous counter digit circuit can be implemented easily. For conclusion the theoretical idea data can't be verified by comparing expiring experimental data with it.

REFERENCES:

1. GyaaniBuddy. (n.d.). *3-bit Asynchronous Counter*. [online] Available at: https://www.gyaanibuddy.com/assignments/assignment-detail/3-bit-asynchronous-counter/ [Accessed 22 Nov. 2022].
2. Basic Electronics Tutorials. (2013). *Synchronous Counter and Decade Counter Tutorial*. [online] Available at: https://www.electronics-tutorials.ws/counter/count_3.html.