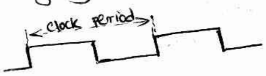
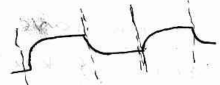
L-5

Defect Avoidance

Analgoy: Ideal vs Real clock signals of defect in real cases

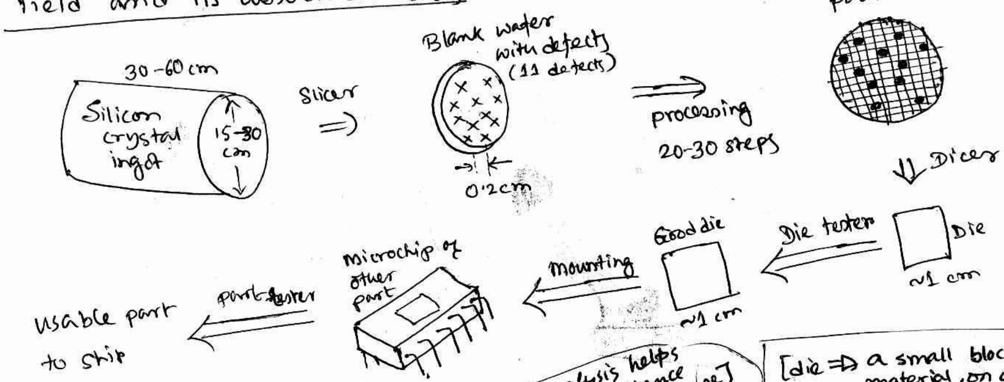


Ideal clok signal
① Shaprp edges
② exact constant periods



Real clock
Quiet different!

Yield (produce?) and its associated costs



yield → 50%
mean 1 million detective out of 2M
⇒ To achieve 100 defects per million (DPM), we must catch 999,900 defects out of 1M defects.
We need a coverage of 99.99%.
Gaining 99.9% cost significantly less than achieving 99.99%. So, consider discarding 1~2% false positive.

[die ⇒ a small block of semiconductor material, on which a given functional ckt is fabricated
wafer/slice/substrate ⇒ a thin slice of semiconductor marterial, which can contain a # of dies]

Effect of die size on Yield [This analysis helps in defect avoidance in decision phase]

⇒ Small size : 120 dies, 109 good 
⇒ large " : 26 " , 15 good 

} dramatic decrease in yield with larger dies

* Die yield = (# of good dies) / (Total # of dies)

* Die yield = wafer yield * [1 + (Defect density × Die area) / a] $^{-a}$

⇒ a → 3~4 for modern CMOS processes

So, area ↑ yield ↓

* Die cost = (Cost of wafer) / (total # of dies * die yield)

= (cost of wafer) * $\underbrace{\text{(Die area / wafer area)}}_{\text{(1/ total \# of dies)}}$ / (Die yield)

Defect modeling: [This analysis helps in defect avoidance in testing phase]

Defects (Two main types)

- → Global or gross-area defects: Due to scratches, over- and under-etching
- → local or spot defects: Due to process imperfection (extra or missing materials), effect of airborne particles.

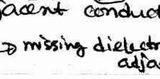
[Not every ~~spot~~ spot defect leads to structural or parametric damage. Actual damage depends on location and size]

Two examples:

Extra-material ... connect pr... roximate ~~connectors~~ conductors

} Extra material connecting proximate cond...

... may connect adjacent conductors

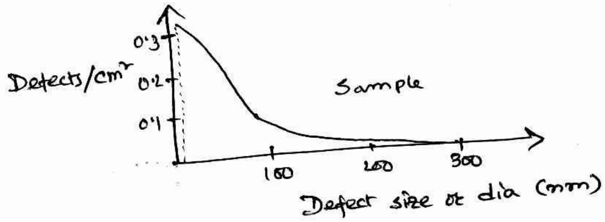
...ig →  → missing dielectric connects adjacent conductr...

Empirical defect-size distribution model

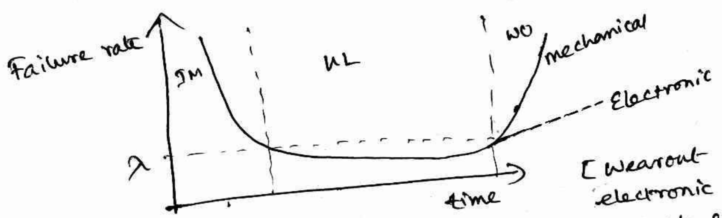
⇒ Defects typically ranges from a min size (x_{min}) to a max size (x_{max}). Defects outside this range have a negligible effect.

⇒ Defect density, $f(x) = \begin{cases} k x^{-p} & \text{for } x_{min} < x < x_{max} \\ 0 & \text{otherwise} \end{cases}$

$x \rightarrow$ defect dia
$k \rightarrow$ normalizing constant
$p \rightarrow$ exponent param ranging [2, 3.5]

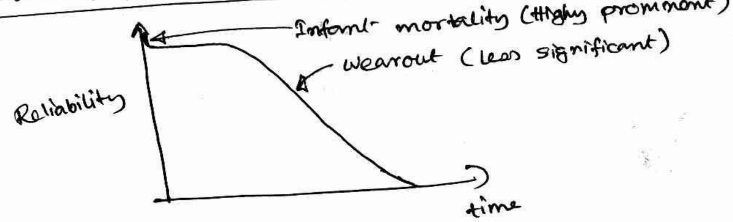


⇒ Component's life : Follows bathtub curve (Infant mortality, useful life, and end-of-Life wearout)



[Wearout is less prominent for electronic components compared to that for mechanical components]

Survival probability for electronic components



⇒ So, we need to expose existing and latent defects that lead to infant mortality ⟶ Process of doing this is burn-in ~~or~~ and stress testing

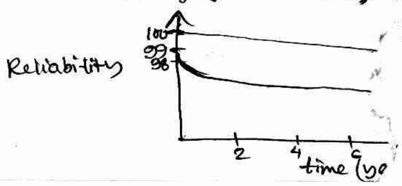
Burn-in and stress testing

→ For revealing defects causing infant mortality, one needs to test a component under various environmental and usage scenarios

→ An alternative to such extented testing is to expose the component to abnormally harsh conditions for acceleraing exposure of defects.

⇒ Normally done under high temperature (in ovens), and thus it is named as "Burn-in". ↳ highly-precise and costly

⇒ Burn-in : Refers to harsher-than-normal treatment, including using greated loads, higher clock freq, excessive shock and vibrat^n, e



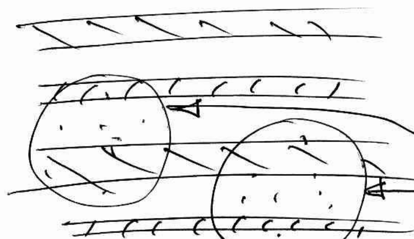
components burn-in for 3 years

1 =>

[Not every spot defect leads to structural or parametric damage.
-Actual damage depends on locaⁿ & size]

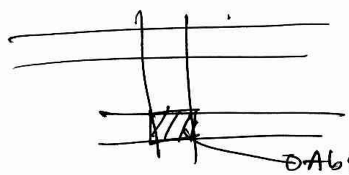
Two example

1. Extra material : can connect physically proximate conductors



connects proximate conductors

2. Pinhole defect : Absence of dielectric material can connect conducting layers



3D fig

Absence of dielectric material connects adjacent conductors

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[2]

=> Burn in : Refers to harsher-than-normal treatment, including using greater loads, higher clock freq, excessive shock & vibraⁿ, etc