Heaven's Light is Our Guide

Rajshahi University of Engineering & Technology

B.Sc. Engineering 3rd Year Odd Examination, 2020

Department of Electrical & Computer Engineering

Course No: **ECE 3117** Course Title: **Software Engineering & Information System Design**

Full Marks: **72** Time: **3** Hours

N.B. (i) Answer **SIX** questions taking any **THREE** from each section.
(ii) Figures in the margin indicate full marks.
(iii) Use separate answer script for each section.

SECTION-A

Q.1(a) What are the elements of a system? Can you have a viable system without feedback? Explain. 04

(b) Distinguish between: 04
(i) Interaction and independence
(ii) Open and closed systems

(c) How would an analysis determine the user's needs for a system? Explain briefly. 04

Q.2(a) Suppose you were assigned to make a website for ECE-RUET. The project was small and you were provided 2 team members. Watching your progress RUET administration has decided to give you a project of result publishing system of RUET. Here, the budget is limited and result system is too complex. Now, answer the following questions. 3x4 =12

(i) What is SDLC? Will you follow any SDLC model for ECE-RUET website project? If so, which one and why?

(ii) For developing online result publishing system, which SDLC model will you choose and why?

(iii) If you are provided a team of 10 members, which framework will you use for team management? Also explain the roles of different people involved with the result publishing project.

Q.3(a) Explain coupling and cohesion. 02

(b) What is software testing? Differentiate between black-box and white-box testing. 04

(c) Why quality control is important in software engineering? How it is different from quality assurance. 04

(d) What is software re-engineering? 02

Q.4 (a) Describe the steps of ~~recruitment~~ requirement analysis. 04

(b) What are the differences between functional and non-functional requirements? 03

(c) What is architectural design? Describe the issues involved in architectural design. 05

SECTION-B

Q.5 (a) Suppose, you want to develop an automated system for the fiance section of RUET. Salaries, bonuses, TA-DA etc. will be processed digitally in the new system. Now answer the following questions- 4x3 =12

(i) How will you determine the users' actual need?

(ii) Which difficulties you may face in the process of information gathering why?

(iii) Which tools will you use for information gathering and why?

(iv) If you need to take the interview of the Vice-chancellor of RUET in the process, which strategy will you follow to have a successful interview?

Q.6 (a) Give a real-world example where you can implement the spiral model. 06

(b) What are the roles of scrum? 06

Q.7(a) What are the key considerations involved in feasibility analysis? 03

(b) What is DFD? Explain each symbol used in a DFD. 03

(c) Explain logical data description hierarchy. 02

(d) Suppose, a publisher company provides 25% discount for the bookstores. If the number of books ordered by a bookstore is less than 30, then no discount is allowed. The publisher also provides 20% and 5% discounts for libraries and individuals respectively. For individuals discount is allowed only if at least 5 books are purchased at a time. Now draw a decision tree for the given information. 04

Q.8(a) Differentiate between verification and validation. 04

(b) What is software quality assurance? Explain briefly. 04

(c) What is the quality attribute of a software? 04

Heaven's Light is Our Guide

Rajshahi University of Engineering & Technology

B.Sc. Engineering 3rd Year Odd Examination, 2020

Department of Electrical & Computer Engineering

Course No: **ECE 3109** Course Title: **Power System**

Full Marks: 72 Time: 3 Hours

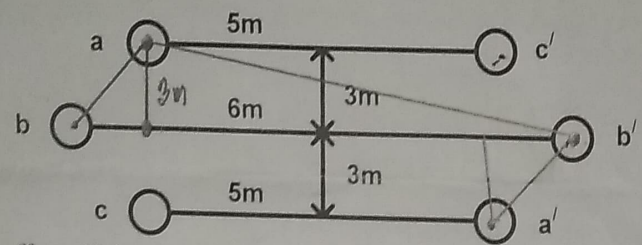
N.B. (i) Answer **SIX** questions taking any **THREE** from each section.
(ii) Figures in the margin indicate full marks.
(iii) Use separate answer script for each section.

SECTION-A

Q.1(a) How inductance is formed in a transmission line? 03

(b) Prove that the capacitance to neutral for the two wire line is twice the line-to-line capacitance. 04

(c) Find the inductance per phase per km of double circuit 3-phase line shown in the following figure. The conductors are transposed and are of radius 0.75 cm each. The phase sequence is ABC. 05



Q.2(a) Define (i) skin effect, (ii) bundled conductor, & (iii) long transmission line. 03

(b) Prove that, $\bar{A}\bar{D} - \bar{B}\bar{C} = 1$ for medium transmission lines by using nominal π method. 04

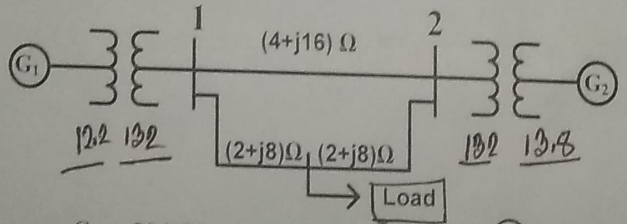
(c) A 3-phase, 50 Hz, overhead transmission line delivers 10 MW at 0.8 p.f. lagging and at 66 KV. The resistance and inductive reactance of the line per phases are 10 Ω and 20 Ω respectively while capacitance admittance is 4×10^{-4} siemen. Calculate the sending end voltage and power factor. 05

Q.3(a) Derive the relationship between the old and new per unit impedances considering the change in base values. 04

(b) Prove that, the admittance of a power system network is, 03

$$Y_{ij}^{k+1} = Y_{ij}^{k} - \frac{Y_{im}^{k} Y_{mj}^{k}}{Y_{mm}^{k}}$$, where the symbols have their usual meaning.

(c) Draw the per-unit impedance diagram of the system shown in the following figure, 05



where,

G_1:	50 MVA,	12.2 KV,	X_{g1}=0.10 pu
G_2:	20 MVA,	13.8 KV,	X_{g2}=0.10 pu
T_1:	80 MVA,	12.2/132 KV,	X_{T1}=0.10 pu
T_2:	40 MVA,	13.8/132 KV,	X_{T2}=0.10 pu
Load:	50 MVA,	0.85 p.f. lagging operation at 130 KV	

Q.4 (a) Explain the effects on a system when a large load is suddenly removed from it. 04

(b) Describe the synchronous condenser method of voltage control for a transmission line. 03

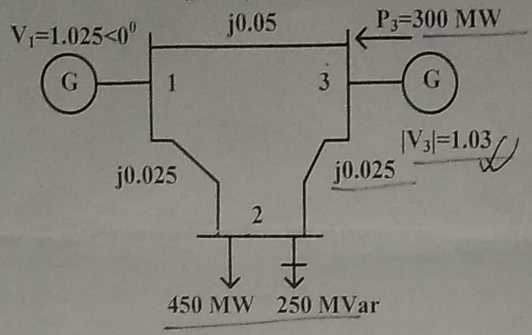
(c) A 3-phase, 50 Hz, 400 V motor develops 100 H.P., the power factor being 0.75 lagging and efficiency 93%. A bank of capacitors is connected in delta across the supply terminals and power factor raised to 0.95 lagging. Each of the capacitance units is built of 4 similar 100 V capacitors. Determine the capacitance of each capacitor. 05

SECTION-B

Q.5 (a) What are the differences between Gauss-Seidel method and Newton Raphson method? 03

(b) What is the Jacobian matrix? How the elements of Jacobian matrix are computed? 04

(c) Determine the phasor values of voltage at bus 2 and 3 by using the Gauss-Seidel method. The following figure shows the single line diagram of a simple three-bus system where line impedances are marked in per unit on a 100-MVA base. Perform 2 iterations. 05

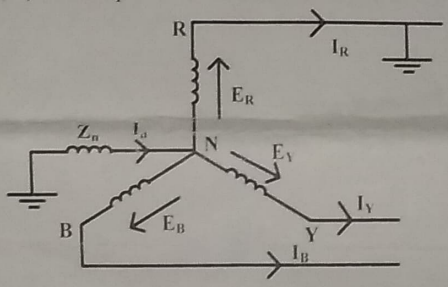


Q.6 (a) Define faults in power system. Classify various types of faults on power system. 04

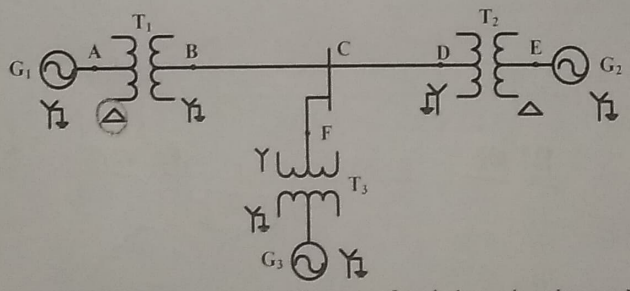
(b) Which unsymmetrical fault is most severe for power system? Why? 03

(c) The currents in a 3-phase unbalanced system are: 05
$\overline{I_R} = (12 + j6)A$, $\overline{I_Y} = (12 - j12)A$, $\overline{I_B} = (-15 + j10)A$. The phase sequence is in RYB. Calculate the zero, positive and negative sequence components of the currents.

Q.7(a) An unloaded generator is grounded through a reactance Z_n as shown in the following figure. If a single line to the ground fault occurs, draw (i) positive sequence network, (ii) negative sequence network, and (iii) zero sequence network. 04



(b) Draw the negative and zero sequence network for the following system. 04



(c) Obtain the symmetrical components for the set of unbalanced voltages $V_a = 200\angle -140^0$, $V_b = 150\angle 100^0$ and, $V_c = 120\angle -20^0$. 04

Q.8(a) Compare among dynamic stability, transient stability, steady-state stability. 03

(b) Determine the solution of the swing equation. 05

(c) how does equal area criterion determine the stability of a system? 04

Heaven's Light is Our Guide

Rajshahi University of Engineering & Technology

B.Sc. Engineering 3rd Year Odd Examination, 2020

Department of Electrical & Computer Engineering

Course No: **ECE 3119** Course Title: **Computer Architecture & Design**

Full Marks: **72** Time: **3** Hours

N.B. (i) Answer **SIX** questions taking any **THREE** from each section.
(ii) Figures in the margin indicate full marks.
(iii) Use separate answer script for each section.

SECTION-A

Q.1(a) What are the relationship between computer architecture and organization? Explain briefly. 04

(b) Define the following terms: (i) PC, (ii) IR, (iii) MAR, (iv) MBR 02

(c) Perform the following operations by showing program execution: 06
A program fragment that adds the contents of the memory word at address 940 to the contents of the memory word at address 941 and stores the result in the later section. Also shows the contents of AC, PC, IR for each step.

Q.2(a) A benchmark program is run on an 80 MHz processor. The executed program consists of 10,0000 instruction executions, with the following instruction mix and clock cycle count: 06

Instruction Type	Instruction Count	Cycles per Instruction
Integer arithmetic	45,000	1
Data transfer	32,000	2
Floating point	15,000	2
Control transfer	8,000	2

Determine the effective CPI, MIPS rate, and execution time for this program.

(b) List and briefly explain two approaches to dealing with multiple interrupts. 04

(c) Consider a μp generating a 16-bit address and having a 16-bit data bus. What is the maximum memory address space that the processor can access directly if it is connected to a 16-bit memory? 02

Q.3(a) Draw the flowchart for unsigned binary division and solve the problem where 7 divided by 3. 05

(b) Represent 263.3 in IEEE 754 32-Bit floating point notation. 04

(c) Consider a 32 bit hexadecimal value 12345678 and that it is stored in a 32 bit word in byte addressable memory at byte location 184. Store this value using both big ending and little endian techniques. 03

Q.4 (a) Briefly define the seven RAID levels. 05

(b) Write down the hardware events occur when an I/O device completes an I/O operation in the case of interrupt-driven I/O. 04

(c) What are the drawbacks of programmed and Interrupt-driven I/O? What is the function of DMA? 03

SECTION-B

Q.5 (a) What is the purpose of translation lookaside buffers? 02

(b) What are the differences between big ending and little ending? 03

(c) Compare zero, one, two and three- addresses machines by writing programs to compute X=(A+B x C)/(D-E x F) for each of the four machines. 07

Q.6 (a) Show the instruction formats of R-type, I-type, and J-type. 03

(b) Writing MIPS code for the following C code: 09

(i) while (save[i]==k)i+=1 where i is in $S3, base address of save is in $S6, k is in $S5

(ii)
```
if (A[6]==c[6])
f[8]=g[8]+c[5]+A[A[2]]
else
   f[9]=g[5]+c[3]
```
where base address of A is $S0, c is $S2, f is $S3 and g is $S1.

(iii) A[12]=h+A[8] where h is in $S2, base address of A is in $S3.

Q.7(a) Identify the write-read, write-write and read-write dependencies in the following sequence: 04

I_1: R1=50
I_2: R1=R3+R4
I_3: R2=R4-10
I_4: R4=R1+R2
I_5: R2=R1+45

(b) Differentiate between multiprogramming and multiprocessing. 03

(c) Explain the taxonomy of parallel processor architecture. 05

Q.8(a) Define FPGA. Draw and explain the basic architecture of FPGA. 05

(b) Explain some real-world applications of FPGA. 04

(c) Distinguish between ASCI and FPGA. 03

Heaven's Light is Our Guide

Rajshahi University of Engineering & Technology

B.Sc. Engineering 3rd Year Odd Examination, 2020

Department of Electrical & Computer Engineering

Course No: **ECE 3111** Course Title: **Microprocessor & Assembly Languages**

Full Marks: **72** Time: **3** Hours

N.B. (i) Answer **SIX** questions taking any **THREE** from each section.
(ii) Figures in the margin indicate full marks.
(iii) Use separate answer script for each section.

SECTION-A

Q.1(a) Suppose we look at an instruction that adds the contents of register AX to the contents of the memory word at address 0. Write down the necessary steps happen inside a computer to accomplish this task. 04

(b) Differentiate between the high-level programming language and assembly programming language. 03

(c) Describe the two modes of operation of the 80286 microprocessor. 02

(d) Explain the operation of different general-purpose registers of 8086 microprocessor. 03

Q.2(a) For each of the following instructions, give the new destination contents and the new settings of CF, SF, ZF, PF, and OF. 04

(i) NEG AL; where AL contains 7Fh

(ii) SUB AX, BX; where AX contains 0000h and BX contains 8000h.

(b) Write down four main functions of operating systems. 04

(c) Write a full assembly code for the following decision structures: 04

```
IF AX<BX
 THEN
  IF BX<CX
   THEN
    Put 0 in AX
     ELSE
      Put 0 in BX
       END_IF
 END_IF
```

Q.3(a) Write assembly code to read one of the hex digits A-F and display it on the next line in decimal. 03

Sample execution: C
In decimal it is 12

(b) SUB AX, BX, where AX contains 8000h and BX contains 0001h. Now show the results of the status flag registers. 03

(c) Suppose that AX and BX both contain positive numbers, and ADD AX, BX is executed. Show that, there is a carry into the msb but no carry out of the msb if and only if signed overflow occurs. 03

(d) Write the appropriate assembly code for the following: 03
If AX contains a negative number, put-1 in BX;
If AX contains 0, put 0 in BX;
If AX contains a positive number, put 1 in BX.

Q.4 (a) Write an assembly program to display the multiplication table of a given integer. 04

Sample execution:
Input the number: 5
Expected output:
5x1=5
5x2=10

5x10=50

(b) Suppose that AX=1234h, BX=5678h, CX=9ABCh, and SP=100h. Evaluate the contents of AX, BX, CX, and SP after executing the following instructions: 04

```
PUSH AX
PUSH BX
XCHG AX, CX
POP CX
PUSH AX
POP BX
```

(c) Suppose SP=0200h, top of stock=012Ah. Evaluate the contents of IP and SP: "After RET is executed, where RET appears in a NEAR procedure." 04

SECTION-B

Q.5 (a) Write an assembly program to read a sequence of characters and display them in reverse order on the next line using stack. 04

(b) What happens when CALL and RET executed? 03

(c) Write a procedure in assembly language named FACTORIAL that will compute N! for a positive number N. The procedure should receive N in CX and return N! in AX. Suppose the overflow does not occur. 03

(d) How can you check the resultant value of an operation is zero or not in assembly language? 02

Q.6 (a) Consider "A" is an MxN word array stored in row-major order. 06

(i) Where does row I begin?

(ii) Where does column j begin?

(iii) How many bytes are there between elements in a column?

(b) Write a procedure REVERSE that will reverse an array of N words. The procedure is entered with SI pointing to the array, and BX has the number of words N. 04

(c) Suppose A is a 5x7- word array stored in row-major order. Write some code to (i) clear row 3, and (ii) clear column 4. Use based indexed mode. 02

Q.7(a) Suppose the following declarations have been made: 04

```
STRING1 DB "FGHIJ"
STRING2 DB "ABCDE"
        DB 5 DUP (?)
```

Write instructions to move STRING1 to the end of STRING2, producing the string "ABCDEFGHIJ".

(b) Suppose the following string has been declared: 04

STRING DB "TH*S* G*S* AR* B*ASTS"

Write instructions that will cause each "*" to be replaced by "E".

(c) Write short note on the followings: 04

(i) CLD (ii) STD

(iii) XLAT (iv) PTR

Q.8(a) Why do we need to use the following instructions? 04

```
MOV AX, @DATA
MOV ES,AX
```

(b) Consider the array declaration given below: 03

W DB 10, 20, 30, 50, 60

Write instructions to insert 40 between 30 and 50. Assume DS and ES are initialized to the data segment.

(c) Discuss the steps involved in creating and running an assemble program. 03

(d) What do you mean by interruption? 02

Heaven's Light is Our Guide

Rajshahi University of Engineering & Technology

B.Sc. Engineering 3rd Year Odd Examination, 2020

Department of Electrical & Computer Engineering

Course No: **ECE 3107** Course Title: **Electrical Machines II**

Full Marks: **72** Time: **3** Hours

N.B. (i) Answer **SIX** questions taking any **THREE** from each section.
(ii) Figures in the margin indicate full marks.
(iii) Use separate answer script for each section.

SECTION-A

Q.1(a) Explain the necessity and working arrangement of commutator and brush in a DC generator. 05

(b) A conductor 0.254m in length is moving in a magnetic field of 0.465 Wb per square meter. Determine the voltage induced in the conductor if the speed of the conductor is 15.24 m/s. 03

(c) Derive the generalized e.m.f. equation of a DC generator. 04

Q.2(a) Briefly describe the reasons of failure of the voltage build-up process in a self excited shunt generator and also explain how these problems can be solved. 05

(b) Assume that, you need to deliver some power to a place which is very near from the generating station. What type of compounding will you prefer in this scenario so that the terminal voltage of the generator remain fixed. 04

(c) "Shifting the brush position can not reduce armature reaction for varying load. If the load is constant then the position of magnetic neutral would be stationary to some extent". Justify the statement. 03

Q.3(a) A DC motor is running with a certain load. If we suddenly reduce the load of the motor, what changes will take place? 03

(b) Explain any three methods used for the speed control of DC shunt motor. 04

(c) In our machine lab, we have a DC shunt motor with following ratings: 5 hp, 240 V, 20.4 A full load current, 202 Ω field resistance and 0.71 Ω armature resistance. Determine, 05

(i) Power delivered to motor
(ii) Power dissipated in shunt field
(iii) Power dissipated in the armature
(iv) Electrical power converted into mechanical power

Q.4 (a) Dept. of ECE has a 3-point starter in their lab. But they are planning to buy a 4-point starter and use it in the lab instead of the 3-point starter. What could be the reason behind this? 03

(b) Determine the resistance of each step of a starter for the following motor; 10 hp, 240 V, 0.5 Ω armature circuit resistance, 45 A full load current. Starting current to be 150% of the full load current. 05

(c) What is the difference between speed control and braking? Explain the rheostatic braking with necessary diagram. 04

SECTION-B

Q.5 (a) Describe with necessary diagram the brushless systems of excitation for synchronous generator. 04

(b) Explain why the terminal voltage of a synchronous generator is different from the internally generated voltage at loaded condition. 04

(c) A 200-KVA, 480-V, 50-Hz, Y-connected alternator with a rated field current of 5A was tested, and the following data were taken: 04

(i) $V_{T,OC}$ at the rated I_F was measured to be 540V.
(ii) $I_{L,SC}$ at the rated I_F was measured to be 300A.
(iii) When a DC voltage of 10V was applied to two of the terminals, a current of 25A was measured.

Find the values of the armature resistance and the approximate synchronouss reactance in ohms.

Q.6 (a) Why the frequency of the incoming generator is kept a bit higher than that of the running system? What will happen if the frequency of the incoming generator is lower? 04

(b) Two generators (Gen-1 and Gen-2) are supplying a real load totaling 2.5 MW at 0.8 p.f. lagging. Gen-1 has no-load frequency of 51.5 Hz and a slope S_{P1} of 1 MW/Hz. Gen-2 has a no-load frequency of 51.0 Hz and a slope S_{P2} of 1MW/Hz. At what frequency is this system operating, and how much power is supplied by each of the two generators? 04

(c) Why synchronous motors are not self-starting? How can we make it self-starting? 04

Q.7(a) What will happen if we change the load on a synchronous motor with constant excitation? Explain with necessary phasor diagrams. 04

(b) Derive the expression, $(P_m)_{max} = \frac{E_b V}{X_s}$ for synchronous motor, where the symbols have their usual meaning. 04

(c) A steeper motor has a step angle of 2.5^0. Determine (i) resolution, (ii) number of steps required for the shaft to make 25 revolutions and (iii) shaft speed, if the steeping frequency is 3600 pps. rps. 04

Q.8(a) Explain the half steeping of a VR stepper motor. 04

(b) How PMDC is better than a DC motor? 03

(c) How does a servo motor operate? 05