Heaven's Light is Our Guide

Rajshahi University of Engineering & Technology

B.Sc. Engineering 3rd Year Odd Semester Examination, 2019

Department of Electrical & Computer Engineering

Course No: **ECE 3119** Course Title: **Computer Architecture & Design**

Full Marks: **72** Time: **3** Hours

N.B. (i) Answer **SIX** questions taking any **THREE** from each section.
(ii) Figures in the margin indicate full marks.
(iii) Use separate answer script for each section.

SECTION-A

Q.1(a) What do you mean by computer organization and computer architecture? 03

(b) List and briefly define some of the techniques used in contemporary processors to increase speed. 04

(c) Explain the differences between multicore systems and MICs. 03

(d) What are the basis measures used to express the computer performance? 02

Q.2(a) What is Moore's law? What is the importance of performance balancement? 05

(b) A benchmark program is run on an 80 MHz processor. The executed program consists of 1,00,000 instructions with the following: 07

Instruction Type	Instruction Count	CPI
Integer arithmetic	45000	1
Data transfer	32000	2
Floating point	15000	2
Control transfer	8000	2

Determine the effective CPI, MIPS rate and execution time for this program.

Q.3(a) Describe the Instruction cycle state diagram. 04

(b) What is an interrupt? Draw the program flow diagram for the both case of short *I/O* wait and long *I/O* wait with interrupt system. 04

(c) Give an example of for the approach of priority interrupt technique to handle multiple interrupts and explain it. 04

Q.4(a) What is the general relationship among access time, memory cost and capacity? 03

(b) Briefly explain direct mapping, associative mapping and set-associative mapping. 05

(c) What are the differences between DRAM and SRAM in terms of characteristics such as speed size and cost? 04

SECTION-B

Q.5(a) List and briefly explain five important instruction set,design issues. 04

(b) Draw the instruction cycle state diagram with proper labeling. 04

(c) Briefly explain with necessary drawings direct addressing and relative addressing. 04

Q.6(a) Consider that five instructions to execute I_1, I_2, I_3, I_4 and I_5. Each has 4 steps (F,D,E,W). Each part has 1.5 clock cycles to execute. Compare the performance of 06

(i) Pipelining
(ii) Super pipelining
(iii) Scalar pipelining

(b) Briefly describe MAR, MBR, PC and IR with figure. 04

(c) What do you mean by RAID? 02

Q.7(a) What are some typical distinguishing characteristics of RISC organization and CISC organization? 04

(b) Consider the following high level instruction: 06

Result=2A+3B-C.

Now write dowh the assembly instructions for above expression considering both RISC and CISC organization.

(c) Write short note on operating system call. 02

Q.8(a) What is instruction-level parallelism? 02

(b) What is FPGA? Draw a simple FPGA logic block. 04

(c) What is virtual memory? Discuss paging. 02

(d) Discuss the working procedure of cash memory to speed up the µp operation. 04

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B.Sc. Engineering 3rd Year Odd Semester Examination, 2019

Department of Electrical & Computer Engineering

Course No: **ECE 3109** Course Title: **Power System**

Full Marks: **72** Time: **3** Hours

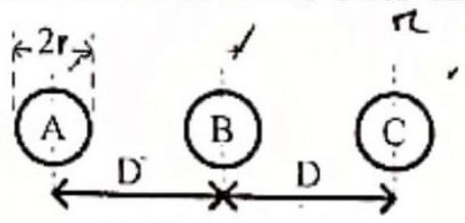
N.B. *(i) Answer any **SIX** questions taking **THREE** from each section.*
(ii) Figures in the margin Indicate full marks.
(iii) The questions are of equal value
(iv) Use separate answer script for each section

Section - A

Q1 (a) Derive an expression for determining inductance per phase of a 3-Φ overhead transmission line when conductors are asymmetrically placed but transposed completely. 04

(b) What is proximity effect? Derive an expression for determining capacitance between the conductors of a two wire transmission line. Also show that the capacitance to neutral for two wire line is twice the line-to-line capacitance. 04

(c) A 3-Φ 50 Hz transmission line consists of three equal conductors of radius r, placed in a horizontal plane, with a spacing of 6m between the middle and each outer conductor as shown in the figure below. Determine the inductive reactance per phase per km of transposed line if the radius of each conductor is 12.5 mm. 04



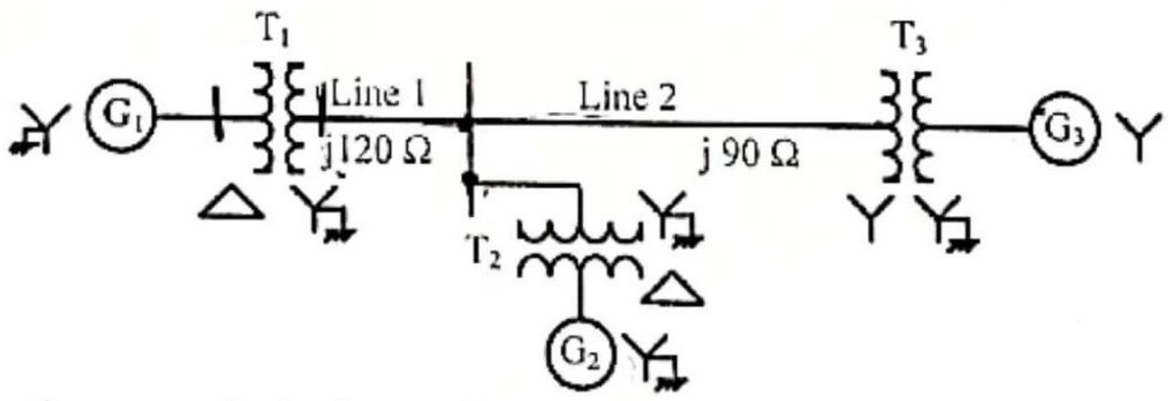
Q2 (a) What is skin effect? Why is it absent in the d.c. system? 03

(b) Define per unit system. Why does per unit computation be convenient for power system analysis? 04

(c) Draw the impedance diagram of the power system network shown in the following figure. The ratings of the generators and transformers are given below: 05

G_1 :	25 MVA	6.6 KV	X_1=0.20 p.u.
G_2 :	15 MVA	6.6 KV	X_2=0.15 p.u.
G_3 :	30 MVA	13.2 KV	X_3=0.15 p.u.
T_1 :	30 MVA	6.6/115 KV(Δ-Y)	X_{T1}=0.10 p.u.
T_2 :	15 MVA	6.6/115 KV(Δ-Y)	X_{T2}=0.10 p.u.
T_3 :	Single phase unit each rated 10 MVA, 6.9/69 KV, X_{T3}=0.10 pu.		

Select base values of 30 MVA and 6.6 KV at the terminal of Generator-1.



Q3 (a) How admittance bus matrix is formed? 03

(b) Define swing bus, PQ bus and PV bus. 03

(c) The following figure shows the one-line diagram of a simple 3-bus power system. The magnitude of voltage at bus 1 is adjusted to 1.05 per unit. The scheduled loads at buses 2 and 3 are as marked on the diagram. Line impedances are marked in per unit on a 100-MVA base and the line charging susceptances are neglected. Determine, 06

(i) Voltage at bus 2 and 3 using Gauss-Seidel method (accurate to three decimal places)

(ii) Find slack bus real and reactive power.

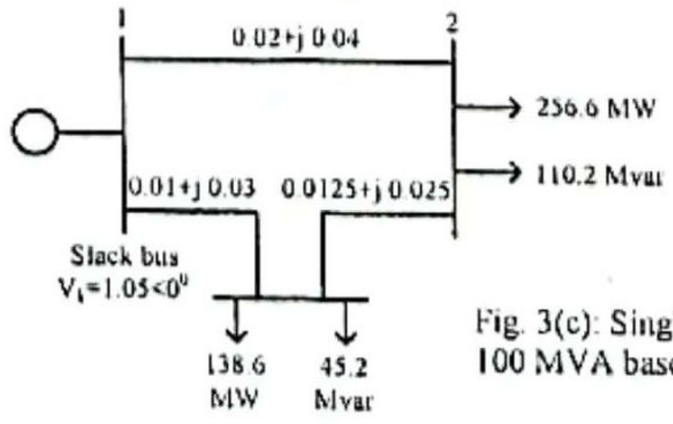


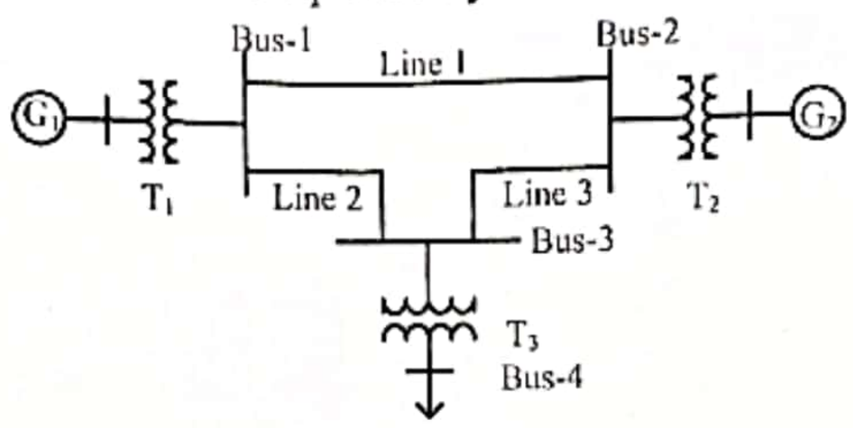
Fig. 3(c): Single line diagram (impedances in pu on 100 MVA base)

Q4 (a) Define Ferranti effect. How can it be reduced? 03

(b) The single line diagram of a 3-Φ system is shown in the following figure. Using a common base S_b=50 MVA, draw the impedance diagram in per unit including the load impedance. The manufacturer's nominal ratings are given as follows. 06

G_1 :	48 MVA	20 KV	X=20%
G_2 :	25 MVA	13.8 KV	X=15%
T_1 :	50 MVA	20/110 KV	X=08%
T_2 :	30 MVA	13.8/110 KV	X=06%
T_3 :	50 MVA	110/11 KV	X=10%

The 3-Φ load at bus-4 absorbs 60 MVA at 0.8 pf lagging and lines 1, 2 and 3 have the reactance of 40 Ω, 32 Ω and 30 Ω respectively.



(c) How can we find new per unit impedance from old per unit impedance? 03

Section -B

Q5 (a) Which fault is most severe in power system and why? 02

(b) How short circuit currents can be limited in symmetrical fault? 03

(c) If we connect a feeder reactor, what advantages and disadvantages we will find? 03

(d) A 3-Φ, 20 MVA, 10 KV alternator has internal reactance of 5% and negligible resistance. Find external reactance per phase to be connected in series with the alternator so that steady current of short circuit does not exceed 8 times the full load current. 04

Q6 (a) What are the symmetrical components of an unbalanced system? 02

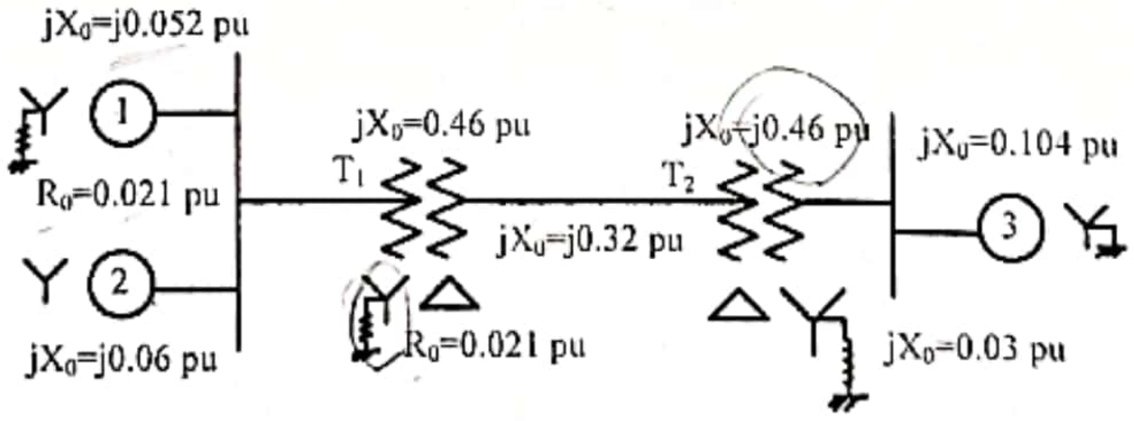
(b) Determine the fault current for a line to line fault in a 3-Φ system. 05

(c) The currents in a 3-Φ unbalanced system are: $\vec{I}_R = (12 + j6)A$, $\vec{I}_Y = (12 - j12)A$, and $\vec{I}_B = (-15 + j10)A$. The phase sequence is in RYB. Calculate zero, positive and negative sequence components of currents. 05

Q7 (a) Derive the second order differential equation (swing equation) which governs the rotor dynamics of a synchronous machine instability study. 04

(b) Define sequence impedance. Draw and explain the sequence networks for an unloaded generator grounded through a reactance. 04

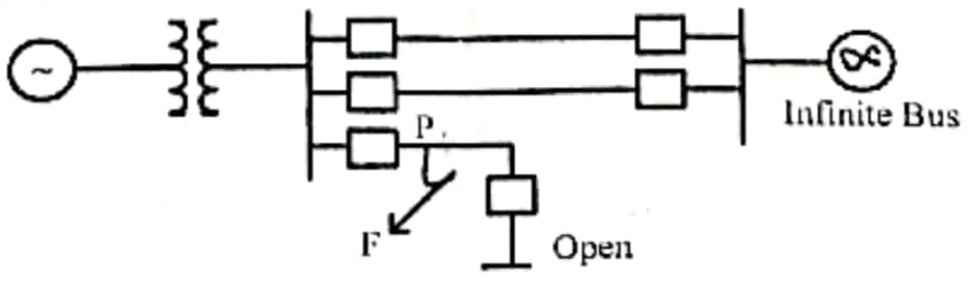
(c) Draw the zero-sequence network for the system shown in the following figure. 04



Q8 (a) Derive an expression for critical clearing angle for an OMIB (one machine to infinite bus) system when power transfer during fault is zero. 04

(b) Describe equal area criterion for power system stability analysis. 04

(c) The one line diagram of the following figure shows a generator transmitting power to an infinite bus through parallel line. The machine is delivering 1.0 pu power and both the terminal voltage and infinite-bus voltages are 1.0 pu. Numbers on the diagram indicate the values of the reactances on a common system base. Calculate the critical clearing angle and critical clearing time for the system when a three phase fault occurs at point P. Consider H is 5 MJ/MVA. 04



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B.Sc. Engineering 3rd Year Odd Semester Examination, 2019

Department of Electrical & Computer Engineering

Course No: **ECE 3111** Course Title: **Microprocessor & Assembly Languages**

Full Marks: **72** Time: **3**

Hours

N.B. *(i) Answer any **SIX** questions taking **THREE** from each section.*
(ii) Figures in the margin Indicate full marks.
(iii) The questions are of equal value
(iv) Use separate answer script for each section

Section - A

Q1	(a)	What do you mean by 16 bit computer system? If 16 bit OS is installed in 32 bit hardware architecture what will be the changes of efficiency?	04
	(b)	If a memory location has physical address 80FD2h, in what segment does it have offset BFD2h?	03
	(c)	Write down an assembly code which will take two single digits as input and show the largest one as output.	05
Q2	(a)	What is the importance of flag register for microprocessor? Discuss the features of the flag register of 8086 µp.	04
	(b)	How can a signal overflow be occurred? If AX contains 19BCh and BX contains 81FEh, what will be the effects on flag register for the operation SUB AX,BX.	05
	(c)	Draw with proper labeling a general architecture of a µp.	03
Q3	(a)	What do you mean by interrupt? How are different kinds of interrupts managed in computer? Discuss.	04
	(b)	Write down an assembly program using a CASE structure to do the followings. Read a character, If its 'E' the display "Electrical" If its 'C' the display "Computer" Otherwise display "Unknown"	05
	(c)	*How can you check the* resultant value of an operation is zero or not in assembly language?	03
Q4	(a)	What do you know about addressing modes? Discuss briefly.	04
	(b)	Write down some examples of conditional jump and unconditional jump. Is there any limitation of jumping in assembly code?	04
	(c)	Write a program that reads a string of capital letters ending with a carriage return, and display the longest word. Sample Input: "Attentive Student can do well in Examination" Sample Output: Attentive	04

Section -B

Q5	(a)	How many types of microprocessor are available? Draw and discuss the architecture of RISC and CISC microprocessor.	05
	(b)	What is read and write operation in 8086 µp? Draw the clock diagram of write operation in minimum mode of 8086 µp.	04
	(c)	Differentiate between the following two instructions : MOV AX,2437H and MOV AX,[2437H]	03
Q6	(a)	What are the restrictions of using MOV and XCHG instructions? How to overcome the restrictions?	04
	(b)	What is VRAM? Write down the importance of using VRAM to improve system performance.	04
	(c)	Write instruction to generate the following output. (i) Count the number of 1 bit in an ASCII Character. (ii) If AL contains 1 or 3 print 'zero' otherwise print 'One'	04
Q7	(a)	What is DMA controller? Discuss the architecture of 8257 DMA controller.	06
	(b)	Mention some application of DMA controller.	03
	(c)	Consider the array declaration given below. W DB 10,20,30,50,60 Write your instructions to insert 40 between 30 and 50. Assume DS and ES are initialized to the data segment.	03

Q8 (a) Why AX is called accumulator register? 02

(b) What is peripheral interfacing? Draw the block diagram of memory and I/O interfacing. 04

(c) What is SHL and SHR instruction? Suppose AX and BX both contains negative numbers and MOV AX, BX instruction is executed. Show that there is a carry out of the msb, but no carry into the msb if and only if signed overflow occurs. 03

(d) Write instruction to take input from user and check the number is an odd number or an even number. 03

AH AL

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Rajshahi University of Engineering & Technology

B.Sc. Engineering 3rd Year Odd Semester Examination, 2019

Department of Electrical & Computer Engineering

Course No: **ECE 3107** Course Title: **Electrical Machines II**

Full Marks: **72** Time: 3 Hours

N.B. (i) Answer **SIX** questions taking any **THREE** from each section.
(ii) Figures in the margin indicate full marks.
(iii) Use separate answer script for each section.

SECTION-A

Q.1	(a)	Describe Fleming's right hand rule. What factors determine the voltage induced in a wire?	04
	(b)	In a single-coil dynamo, describe the difference between the voltage induced in the coil and the voltage from the brushes.	04
	(c)	A generator is to be having four poles and 60,000 lines per pole. The coils are to have 60 turns with an average induced voltage of 15V per coil. The speed of rotation is to be 3600 rpm. Is this design satisfactory? If not, what can be done in order not to exceed voltage rating?	03
	(d)	Where should the brushes be located in a dynamo?	01
Q.2	(a)	When obtaining a magnetization curve in the laboratory, why it is essential that the current must increase until saturation is obtained?	02
	(b)	List the reasons why a generator may fail to build up. How can each failure be corrected?	04
	(c)	A long shunt compound generator has a shunt field winding of 1000 turns per pole and series field winding of 4 turns per pole. In order to obtain the same rated voltage at full load to no load for operation as a shunt generator, it is necessary to increase the field current by 0.2A. The armature current of the compound generator is 80A and series field resistance is 0.05Ω. Calculate (i) the number of series field ampere turns required for flat compound generator action. (ii) Diverter resistance for flat compound operation.	04
	(d)	Draw the external characteristics curves of self-excited DC generators.	02
Q.3	(a)	Let us consider a 10MW and a 15MW generators are connected in parallel and supplying a load of 18MW. Suddenly, load demand increases to 22MW. How this extra load will be shared by these two generators?	03
	(b)	Define counter EMF. How counter EMF is produced in DC motor? What is its significance?	05
	(c)	A 5hp, 240V DC motor with full load current 20.4A, field resistance 202Ω has the armature resistance 0.71Ω. Determine (i) power dissipated in the shunt field. (ii) electrical power converted to mechanical power	04
Q.4	(a)	What is the main disadvantage of a 3-point starter? How a 4-point starter can remove this disadvantage? Explain with necessary diagrams.	04
	(b)	What are the methods of braking of the DC motors? What is regenerative braking?	04
	(c)	Determine the resistance of each step of a starter for 10hp, 240V DC motor with 0.5Ω armature resistance and 45A full load current. Starting current to be 125% of full load current.	04

SECTION-B

Q.5	(a)	How can we use a DC generator to supply AC power?	02
	(b)	What are the advantages of stationary armature over rotating armature?	02
	(c)	Define synchronous impedance. How can we measure the synchronous impedance of an alternator?	04
	(d)	A 100kVA, 3000V, 50Hz 3-Φ star connected alternator has effective armature resistance of 0.2Ω. The field current of 40A produces short circuit current of 200A and open circuit EMF of 1040V(line). Calculate the full load voltage regulations at 0.8pf lagging and 0.8pf leading. Draw phasor diagrams.	04
Q.6	(a)	Explain the effect of change of load on an alternator with phasor diagrams for (i) lagging pf. (ii) leading pf and (iii) unity pf.	04
	(b)	How does a synchronous motor operate? How can we make it self-starting?	05
	(c)	A 75kW, 3-Φ, Y-connected, 50Hz, 440V cylindrical rotor synchronous motor oprates at rated condition with 0.8 pf lagging. The motor efficiency excluding field and stator losses is 95% and $X_s = 2.5\Omega$. Calculate (i) back EMF and (ii) pull-out torque of the motor.	03
Q.7	(a)	Define (i) synchronous condenser, (ii) slipping a pole, (iii) speed regulation and (iv) slip	04
	(b)	List and briefly explain any method of starting polyphase synchronous motors	04
	(c)	It is desired to operate a synchronous motor at a speed of 5000 r/min. If only a 60Hz supply is available, what motor-generator set will provide the proper AC source for the synchronous motor?	04
Q.8	(a)	What is servo-motor? Write few application of servomotors.	04
	(b)	Explain the operation of a stepper motor.	04
	(c)	Give two disadvantages of using a variable resistor in series with the line to control the speed of a universal motor.	04