Chapter 6:
Digital Arithmetic: Operations & Circuits

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Chapter 6 Objectives

- *Selected areas covered in this chapter*:
  - Binary addition, subtraction, multiplication, division.
  - Differences between binary addition and OR addition.
  - Basic operation of a half adder circuit.
  - Basic operation of a full adder circuit.
  - Operation of a parallel adder circuit.
  - Operation of a parallel subtractor circuit.
  - Operation of a parallel adder/subtractor circuit.
  - Operation of a BCD adder circuit.
  - ALU integrated circuits for various logic and arithmetic operations on input data.

6-1 Binary Addition

- Binary numbers are added like decimal numbers.
  - In decimal, when numbers sum more than 9, a carry results.
  - In binary when numbers sum more than 1, a carry takes place.
- Addition is the basic arithmetic operation used by digital devices for subtraction, multiplication & division.

6-1 Binary Addition

Four possible situations when addition one bit to another in any position of a binary number.

$$0 + 0 = 0$$

$$0 + 1 = 1$$

$$1 + 0 = 1$$

$$1 + 1 = 10$$

For uniformity

$$0 + 0 = 00$$

$$0 + 1 = 01$$

$$1 + 0 = 01$$

$$1 + 1 = 10$$

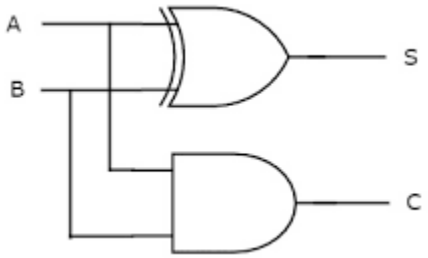
6-2 Design of a Half Adder

- Construct a truth table…
  - 2 inputs (2 numbers to be added).
  - 2 outputs (sum and carry).

Augend Bit Input A	Added Bit Input B		Sum Bit Output S	Carry Bit Output C
0	0		0	0
0	1		1	0
1	0		1	0
1	1		0	1

6-2 Design of a Half Adder

- S=A`B+AB`=A $\oplus$ B
- C=AB
- Now Draw the Circuit.



6-3 Design of a Full Adder

- Construct a truth table…
  - 3 inputs (2 numbers to be added and carry in).
  - 2 outputs (sum and carry out).

Augend bit input	Addend bit input	Carry bit input		Sum bit output	Carry bit output
A	B	C_{IN}		S	C_{OUT}
0	0	0		0	0
0	0	1		1	0
0	1	0		1	0
0	1	1		0	1
1	0	0		1	0
1	0	1		0	1
1	1	0		0	1
1	1	1		1	1

6-3 Design of a Full Adder

- Use algebraic methods or K-maps to simplify the resulting SOP form.
  - The result is the logic circuit shown here.

K-map for Cout:

	A`B`	AB`	AB	A`B
C`in	0	0	1	0
Cin	0	1	1	1

There are 3 pairs. So the result is

Cout = AB + ACin + BCin

6-3 Design of a Full Adder

- K-map for Sum:

	A`B`	AB`	AB	A`B
C`in		1		1
Cin	1		1	

- All are isolated 1.
- Sum=AB`C`+A`BC`+A`B`C+ABC

  =C`(AB`+A`B)+C(A`B`+AB)

  =C`(A $\oplus$ B)+C(A $\oplus$ B)`

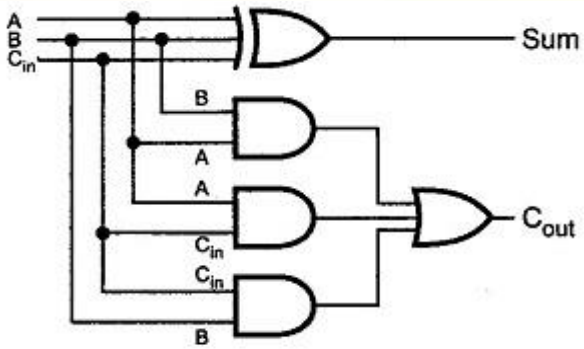
  =C`X+CX`; Let X= A $\oplus$ B

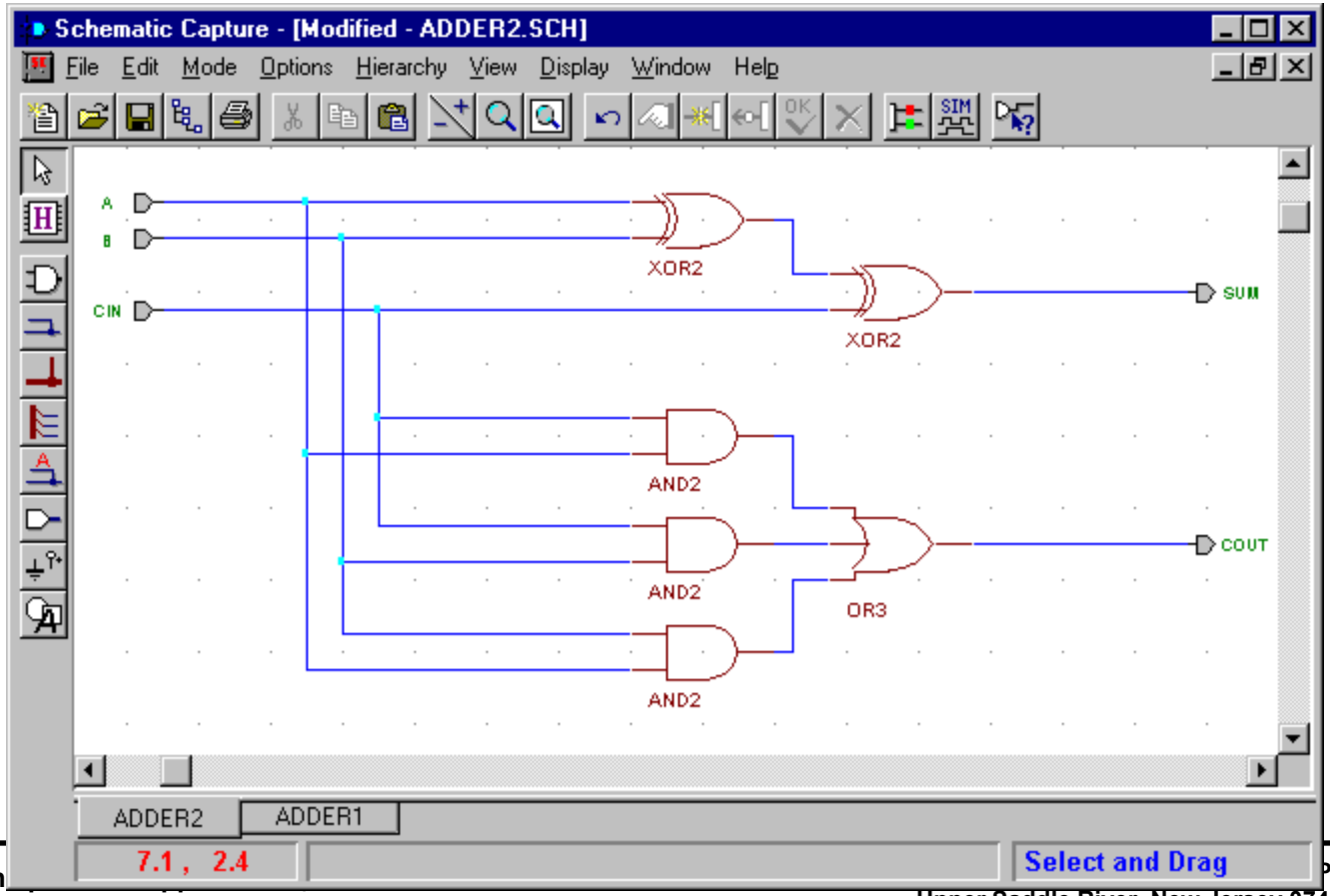
  =C $\oplus$X

  =C $\oplus$ A $\oplus$ B

  = A $\oplus$ B $\oplus$ Cin

6-3 Design of a Full Adder

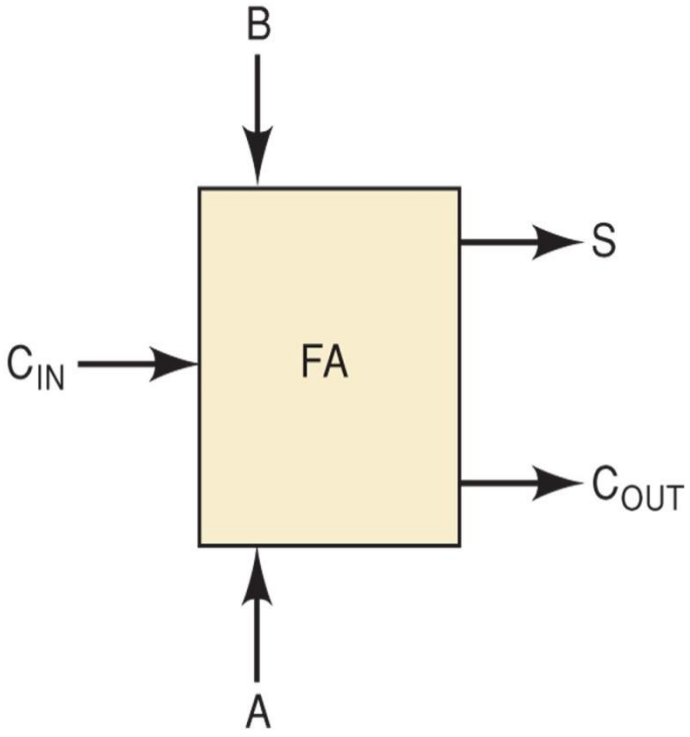




6-3 Design of a Full Adder

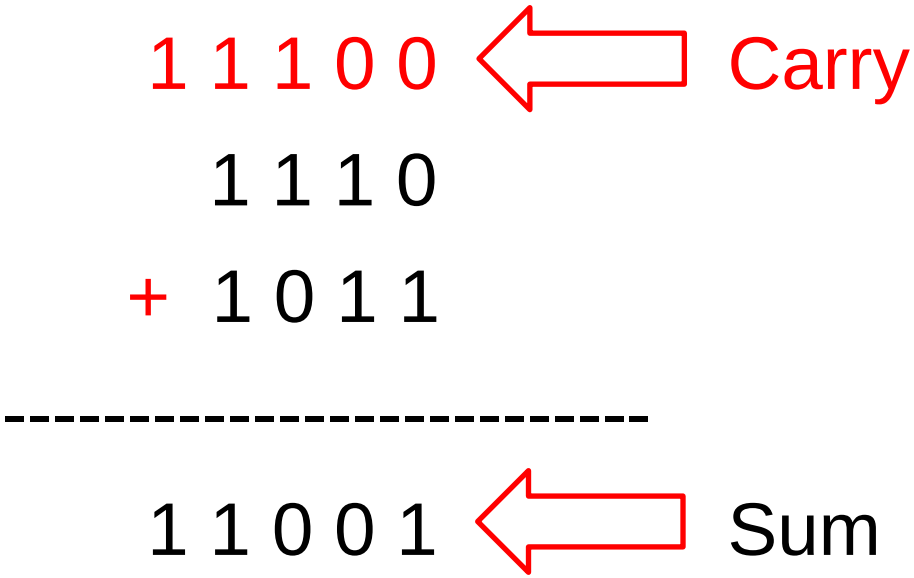
- Block diagram of a Full Adder

Augend bit input	Addend bit input	Carry bit input		Sum bit output	Carry bit output
A	B	C_{IN}		S	C_{OUT}
0	0	0		0	0
0	0	1		1	0
0	1	0		1	0
0	1	1		0	1
1	0	0		1	0
1	0	1		0	1
1	1	0		0	1
1	1	1		1	1



6-4 4-bit Parallel Adder

- Suppose we want to add 2 four bit number like 1110+1011
- So we can follow the following procedure



6-4 4-bit Parallel Adder

C4 C3 C2 C1 C0 Carry

AUGEND A3 A2 A1 A0 A

ADDEND B3 B2 B1 B0 B

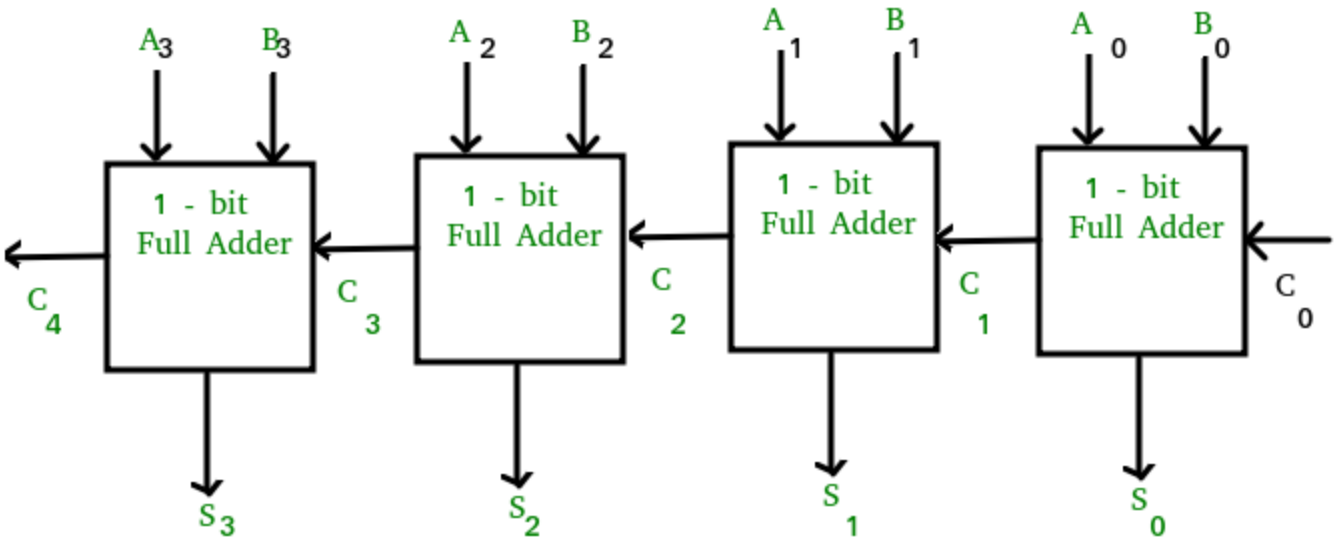
SUM S4 S3 S2 S1 S0 S

AUGEND A3 A2 A1 A0 ADDEND B3 B2 B1 B0

Generate sum bits, $S = A \oplus [B \oplus Cin]$

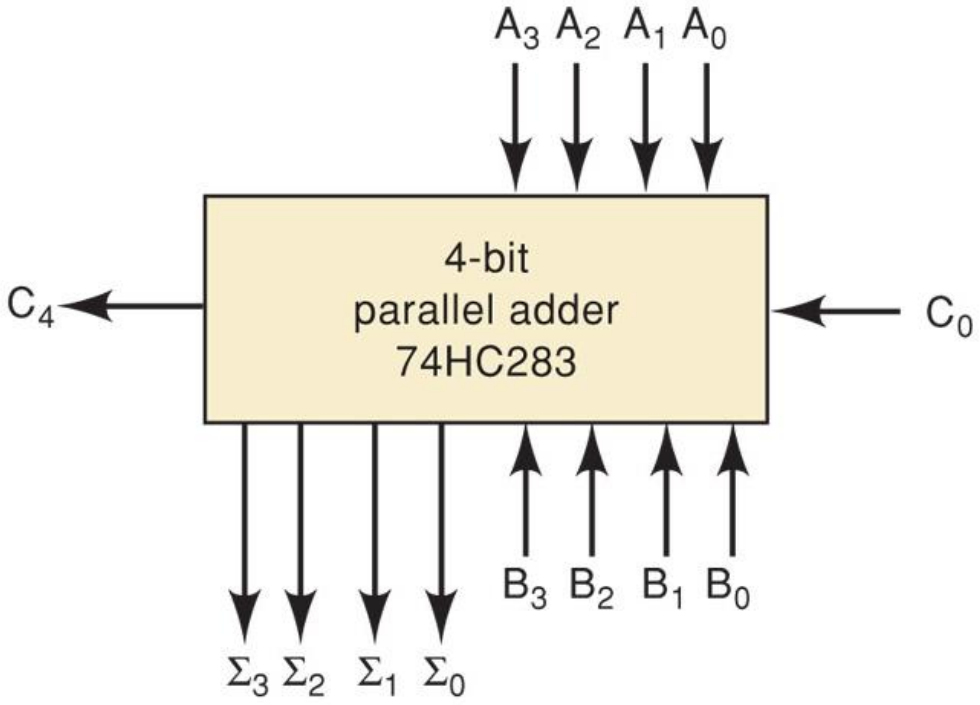
Generate carry bits, $Cout = A \cdot B + A \cdot Cin + B \cdot Cin$

Block diagram of a 4-bit parallel adder circuit using full adders.



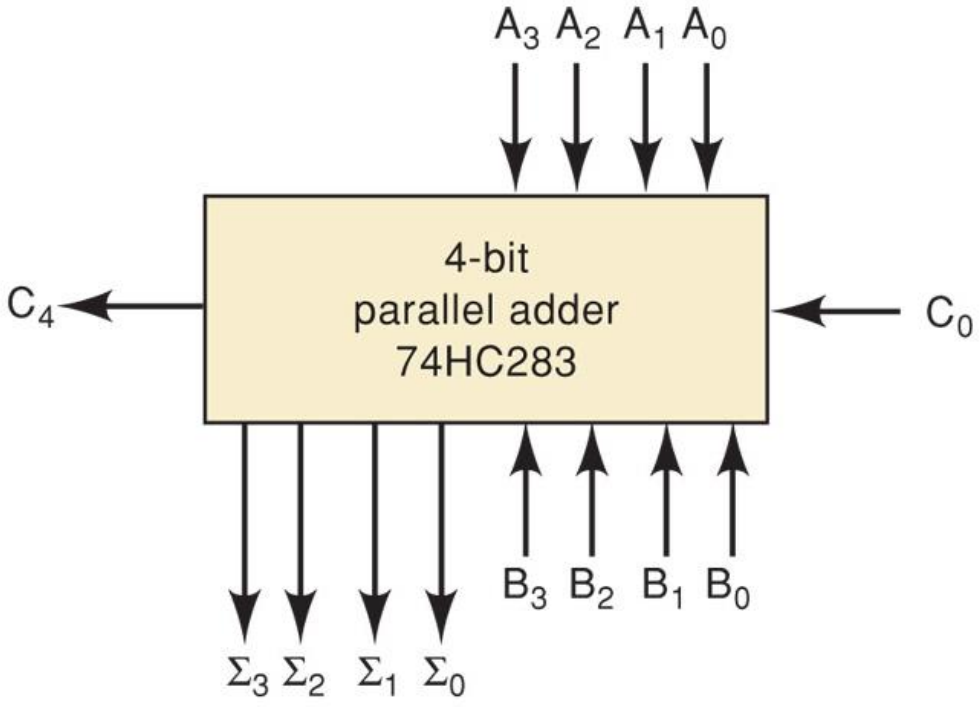
6-4 4-bit Parallel Adder

- The most common parallel adder is a 4 bit device.
  - 4 interconnected FAs, and look-ahead carry circuits.
    - 7483A, 74LS83A, 74LS283, and 74HC283 are all four-bit parallel-adder chips.



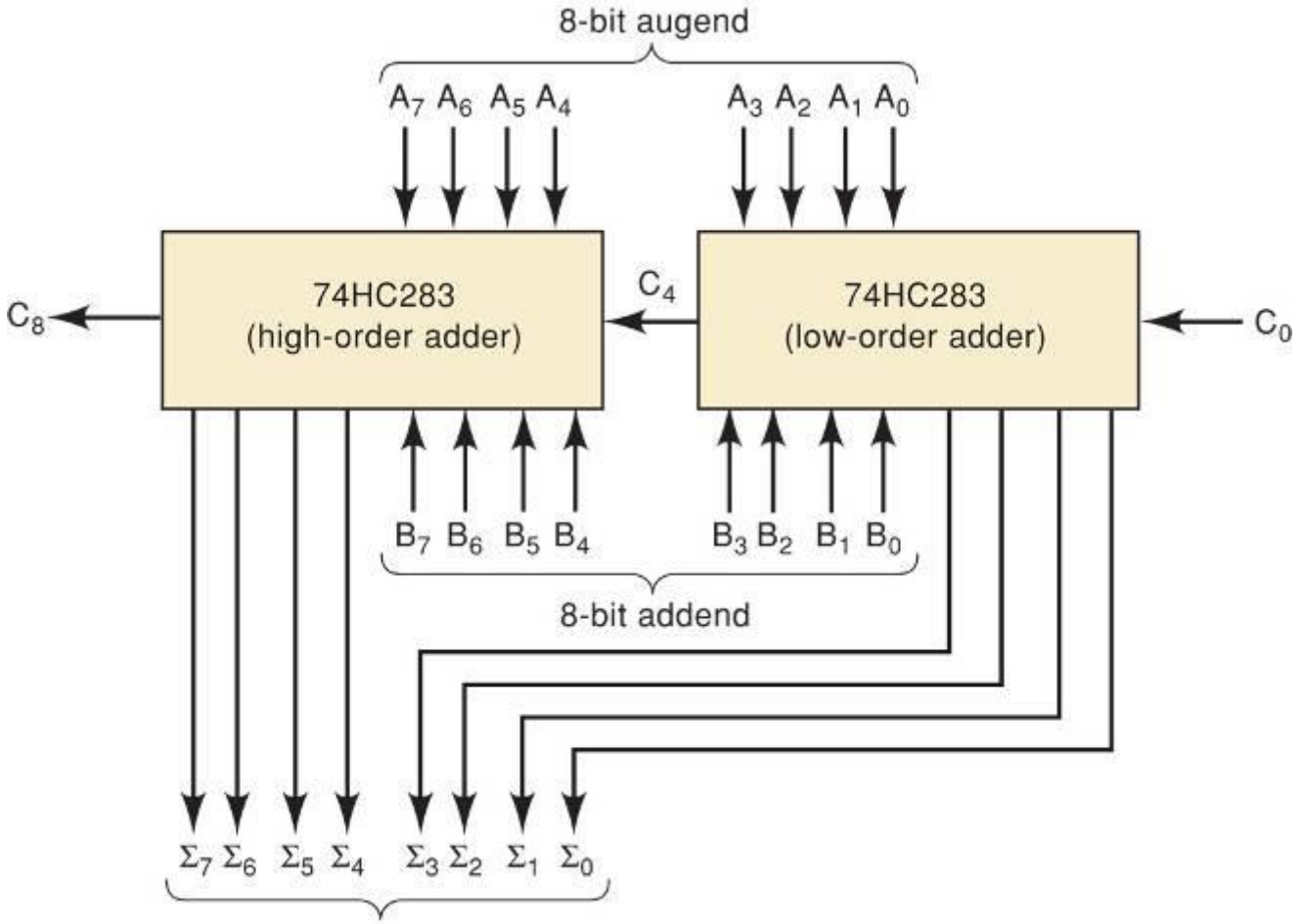
6-4 4-bit Parallel Adder

- The A and B lines each represent 4 bit numbers to be added.
  - C_0 is the carry-in, C_4 is the carry-out, Σ is the sum.



6-5 Cascading 4-bit Parallel Adder

Parallel adders may be cascaded together to add larger numbers, in this case two 8 bit numbers.



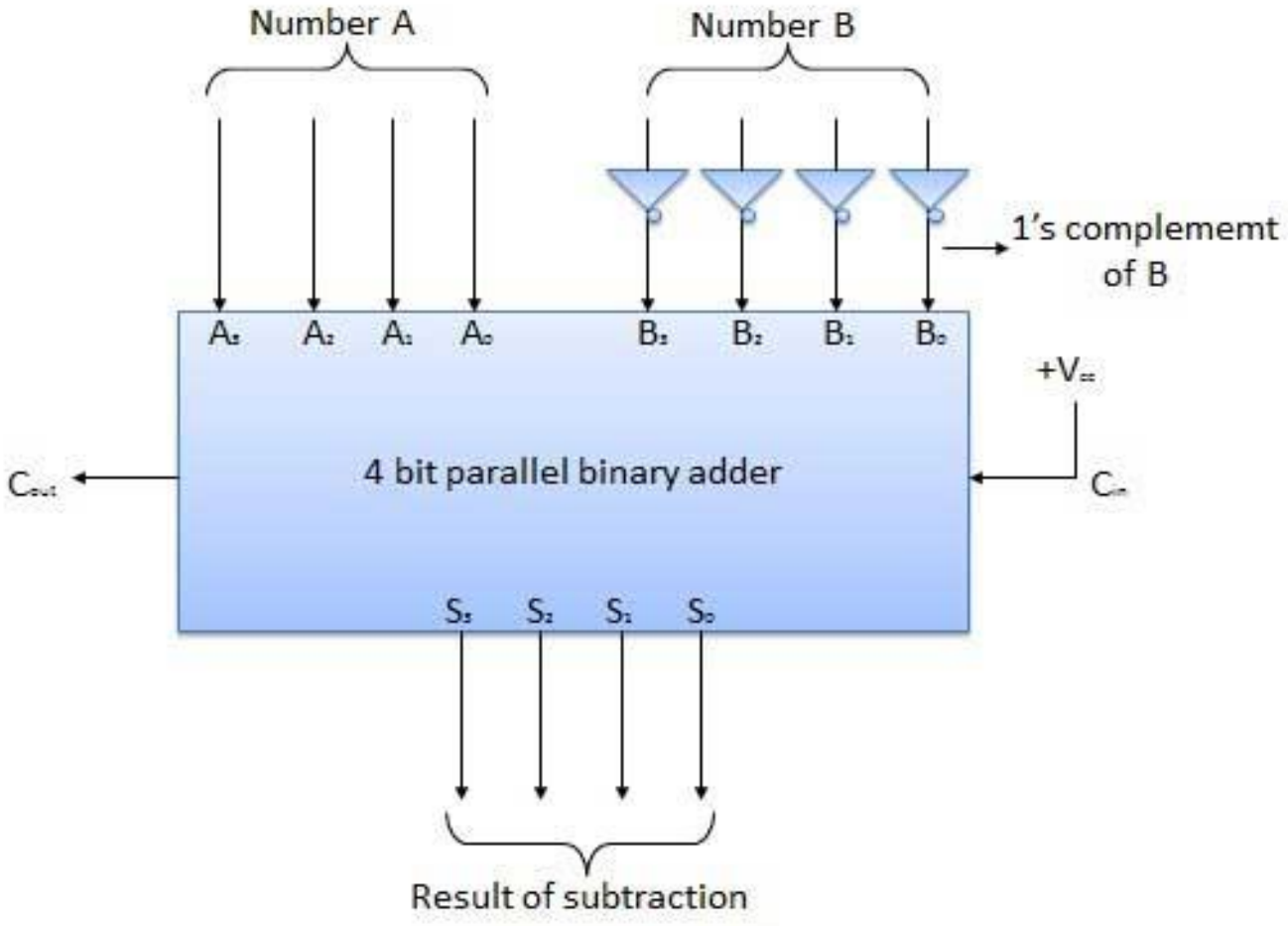
6-6 4-bit Parallel Subtractor

- **Subtraction in the 2's Complement System:**
- Subtraction using the 2's-complement system actually involves the operation of addition.
  - The number subtracted (subtrahend) is negated.
  - The result is added to the minuend.
  - The answer represents the difference.

  - That is A – B =A + (-B)

6-6 4-bit Parallel Subtractor

An adder can be used to perform subtraction by designing a way to take the 2's complement for subtraction—as shown.



6-7 4-bit Parallel Adder/Subtractor

4-bit Parallel adder/subtractor:

If Switch=0 then Adder

If Switch=1 then Subtractor

If S=0 then

First inputs are A3A2A1A0

Second inputs are B3B2B1B0 and C0=0

So this is addition

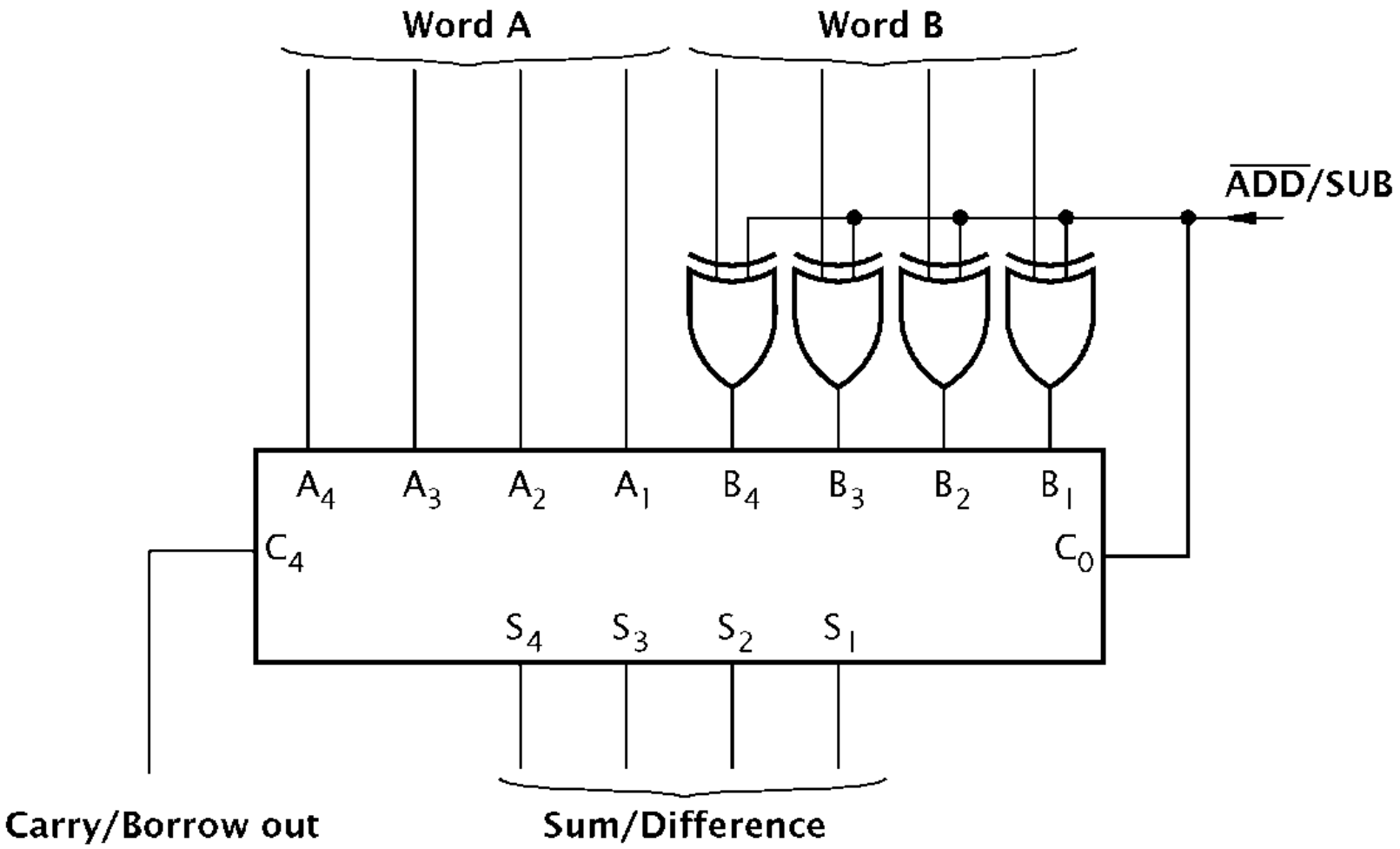
If S= then

First inputs are A3A2A1A0

Second inputs are B`3B`2B`1B`0 and C0=1

So this is Subtraction

6-7 4-bit Parallel Adder/Subtractor



6-8 BCD Adder

- What is BCD? Binary Coded Decimal

Decimal Number	BCD Code
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001

6-8 BCD Adder

BCD Addition:

- Example 1: 24+32=?
- 24=0010 0100+
- 32=0011 0010
- 56=0101 0110
- Example 2: 78+45=?
- 78=0111 1000+
- 45=0100 0101

? =1011 1101

\+ +

0110 0110

1 0010 0011=123

BCD Addition:

- When the sum of each decimal digit is less than 9, the operation is the same as normal binary addition.
- When the sum of each decimal digit is greater than 9, a binary 6 is added.
  - This will always cause a carry.

6-8 BCD Adder

A3A2A1A0

+

B3B2B1B0

S4S3S2S1S0

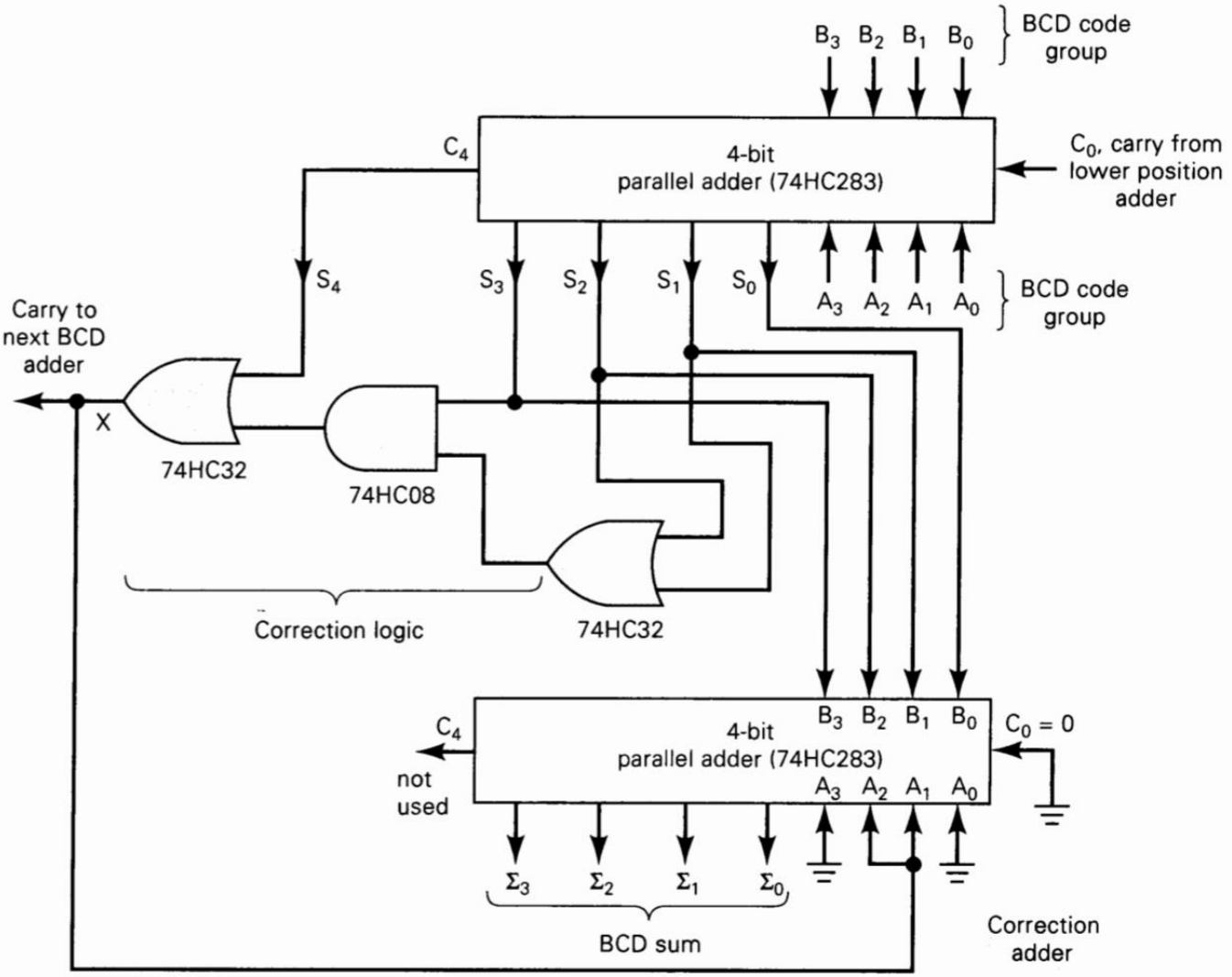
S4	S3	S2	S1	S0
0	0	1	1	1
0	1	0	0	0
0	1	0	0	1
0	1	0	1	0
0	1	0	1	1
0	1	1	0	0
0	1	1	0	1
0	1	1	1	0
0	1	1	1	1
1	0	0	0	0
1	0	0	0	1
1	0	0	1	0

- **Error Correction:**
- **Let us define X as a logic output that will be HIGH only when sum is greater than 9.**
- **If we examine the above table, we can see that X will be HIGH for following conditions:**
- **1. When S4=1 OR**
- **2. When S3=1 and (either S2 OR S1 OR both are 1)**
- **So,** $X = S4 + S3.(S2 + S1)$

6-8 BCD Adder

- A3A2A1A0
- 0 0 0 0 if X=0
- 0 1 1 0 if X=1
- A3=A0=0
- A2=A1=X

6-8 BCD Adder

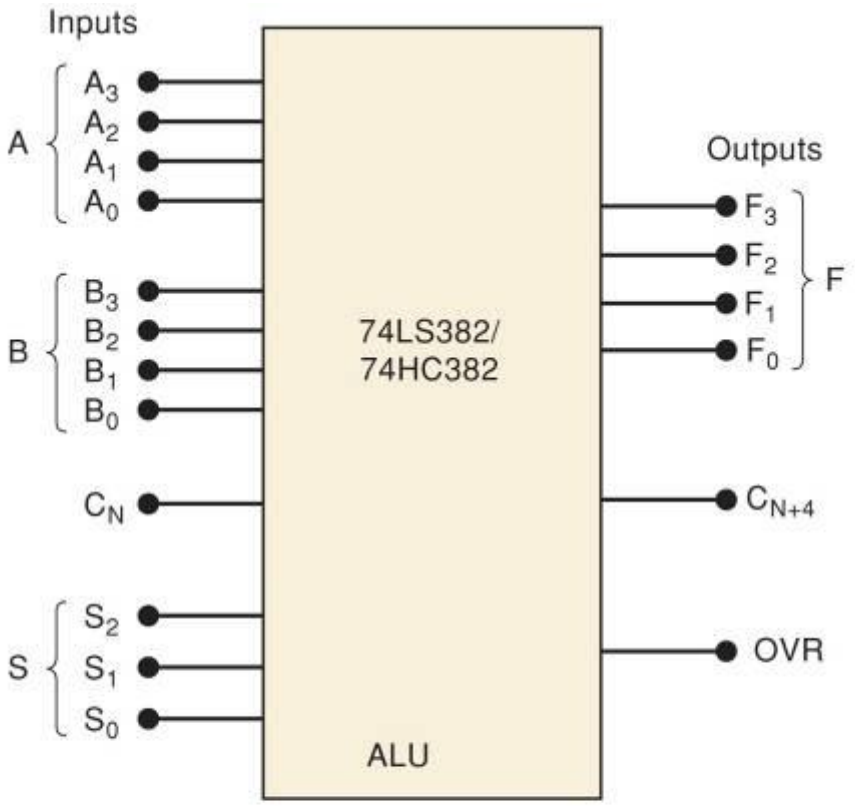


6-9 ALU Integrated Circuits

- ALUs can perform different arithmetic and logic functions as determined by a binary code on the function select inputs.

6-9 ALU Integrated Circuits

The 74LS382 (TTL) and HC382 (CMOS) is a typical device with 8 functions.



Function Table

S_2	S_1	S_0	Operation	Comments
0	0	0	CLEAR	$F_3F_2F_1F_0 = 0000$
0	0	1	B minus A	Needs $C_N = 1$
0	1	0	A minus B	
0	1	1	A plus B	Needs $C_N = 0$
1	0	0	A ⊕ B	Exclusive-OR
1	0	1	A + B	OR
1	1	0	AB	AND
1	1	1	PRESET	$F_3F_2F_1F_0 = 1111$

Notes: S inputs select operation.
OVR = 1 for signed-number overflow.

A = 4-bit input number
B = 4-bit input number
C_N = carry into LSB position
S = 3-bit operation select inputs

F = 4-bit output number
C_{N+4} = carry out of MSB position
OVR = overflow indicator

6-10 Expanding the ALU

- A single 74LS382 or 74HC382 operates on four-bit numbers. Two or more of these chips can be connected together to operate on larger numbers.

6-11 Model Question about this chapter

1. Draw the block diagram of 4 bit ALU chip (IC # 74382) and label the all inputs & outputs.
2. Describe 8(Eight) operations of the 4 bit ALU chip (IC # 74382) that perform by select inputs.
3. Design a BCD adder using IC # 7483 and basic gates if necessary. Briefly describe its operation.
4. What is BCD code? What is the problem in BCD addition? How can you overcome that?

6-11 Model Question about this chapter

5. Write down the truth tables of half adder and full adder. Design half adder and full adder using K-map or otherwise.
6. Briefly describe the operation of IC# 7483(4-bit parallel adder).
7. Design 4-bit Subtractor using IC # 7483(4-bit parallel adder).
8. Design a 4-bit parallel Adder/Subtractor using IC # 7483 and other logic gates if necessary. Briefly describe its operation.

6-11 Model Question about this chapter

9. Design 8-bit parallel Adder using IC # 7483(4-bit parallel adder).
10. Design 8-bit parallel Subtractor using IC # 7483(4-bit parallel adder).
11. Design 8 bit ALU chip using 4 bit ALU chips (IC # 74382) and label the all inputs & outputs.
12. Describe 8(Eight) operations of the 8 bit ALU chip that perform by select inputs.