Chapter 5:
Flip-Flops and Related Devices

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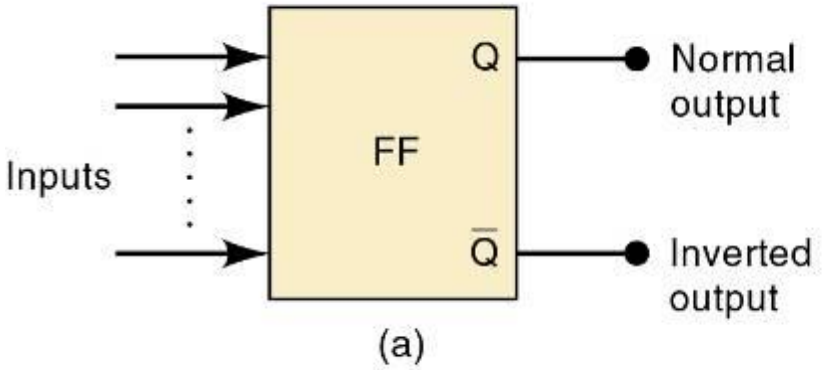
Chapter 5 Objectives

- *Selected areas covered in this chapter*:
  - Basic structures of flip-flops.
  - Constructing/analyzing operation of latch made from NAND or NOR gates.
  - Differences of synchronous/asynchronous systems.
  - Operation of edge-triggered flip-flops.
  - Constructing/analyzing operation of clocked S-R flip-flop.
  - Constructing/analyzing operation of clocked J-K flip-flop.
  - Constructing/analyzing operation of clocked D flip-flop.
  - Basic operation of asynchronous inputs J-K flip-flop.
  - Counter and frequency division.
  - MOD 8 Up Counter, Down Counter, Up/Down Counter
  - MOD 16 Up Counter, Down Counter, Up/Down Counter

- The most important memory element is the **flip-flop** (FF)—made up of an assembly of logic gates.



(a)

Output states

$Q = 1, \overline{Q} = 0$: called HIGH or 1 state; also called SET state

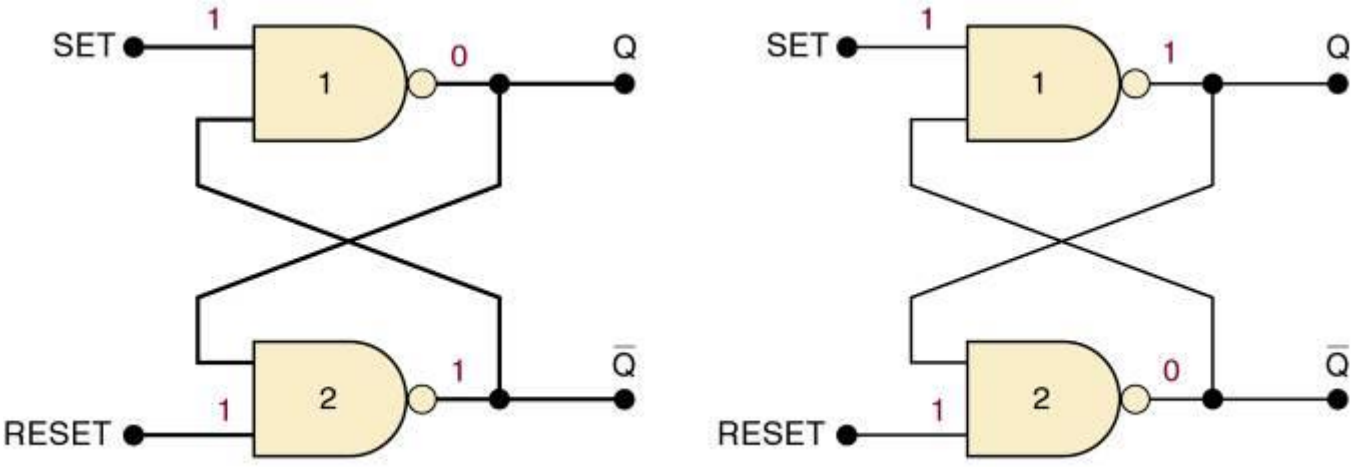
$Q = 0, \overline{Q} = 1$: called LOW or 0 state; also called CLEAR or RESET state

(b)

The flip-flop is known by other names, including *latch* and *bistable multivibrator.*

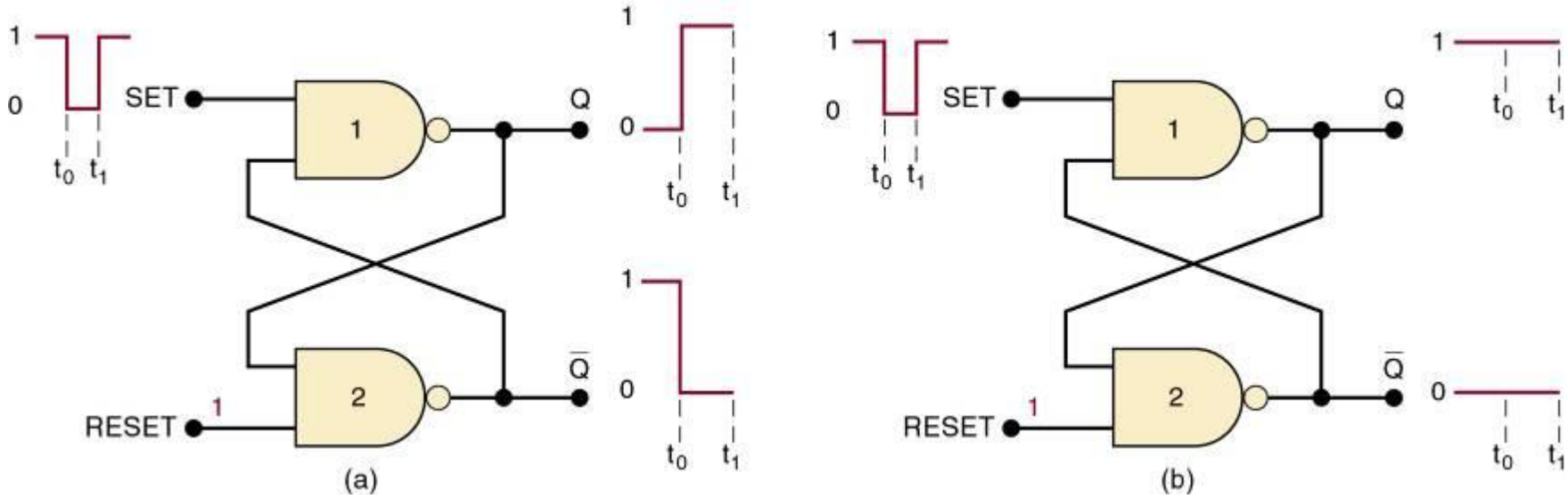
5-1 NAND Gate Latch

- The **NAND** gate latch or simply latch is a basic FF.
  - Inputs are *SET* and *CLEAR* (*RESET*).
- Inputs are active-LOW—output will change when the input is pulsed LOW.
  - When the latch is set: **Q** = 1 and $\overline{\mathbf{Q}}$ = 0
  - When the latch is clear or reset: **Q** = 0 and $\overline{\mathbf{Q}}$ = 1



5-1 NAND Gate Latch – Setting the Latch (FF)

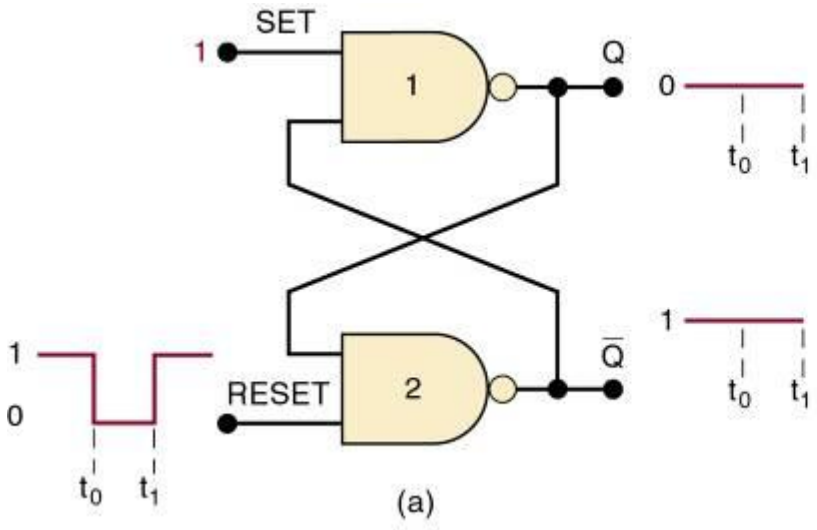
- Pulsing the SET input to the 0 state...
  - (a) *Q* = 0 prior to SET pulse.
  - (b) *Q* = 1 prior to SET pulse.

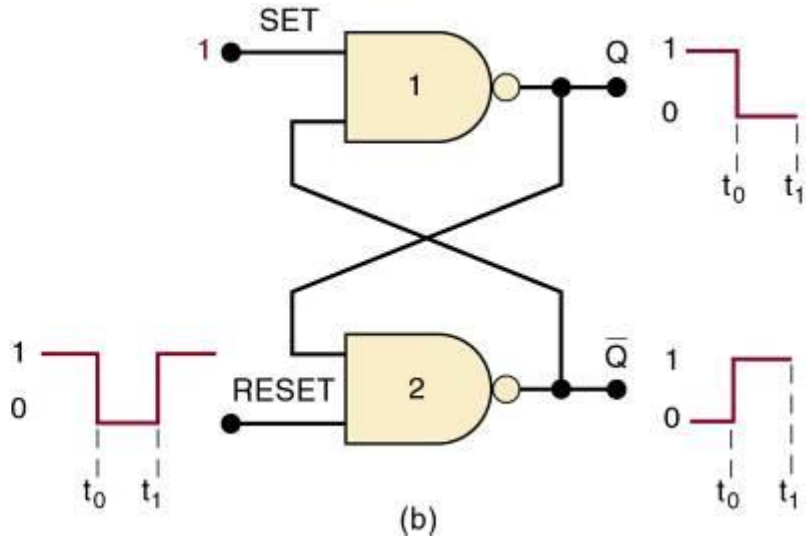


In both cases, *Q* ends up HIGH.

5-1 NAND Gate Latch – Resetting the Latch (FF)

- Pulsing RESET LOW when...
  - (a) $Q = 0$ prior to the RESET pulse.
  - (b) $Q = 1$ prior to the RESET pulse.

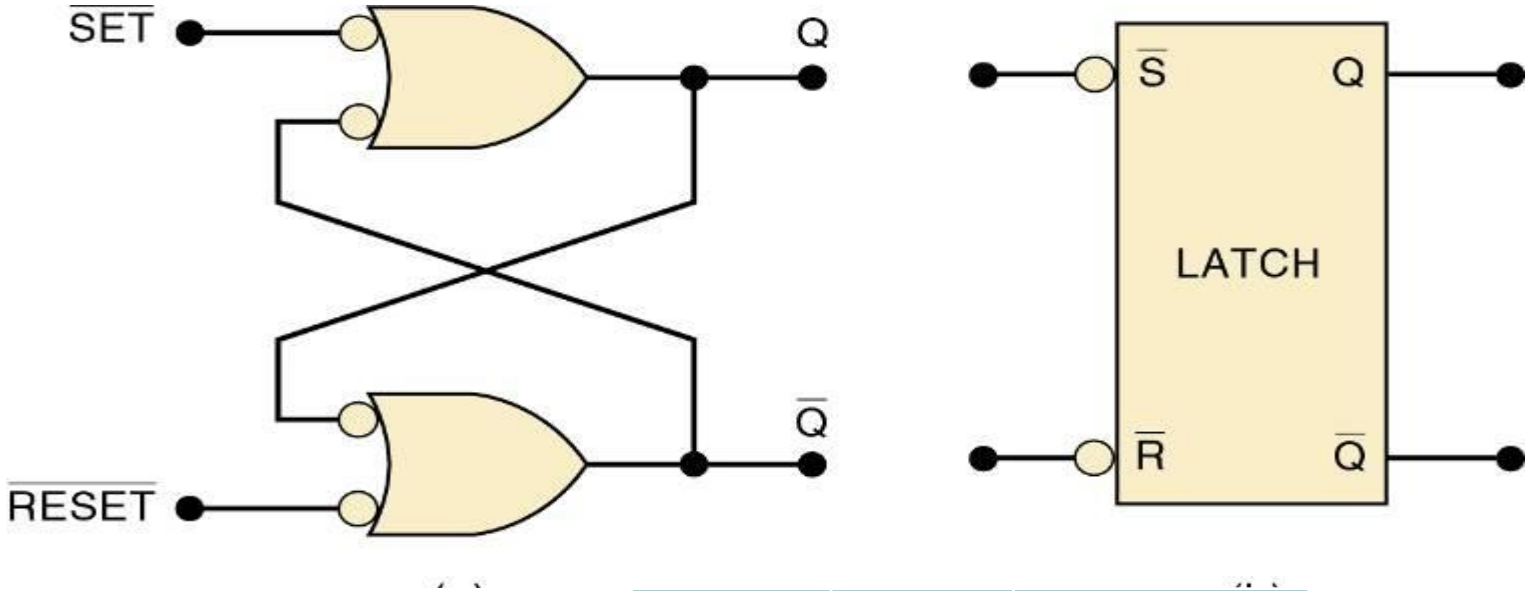




In each case, *Q* ends up LOW.

5-1 NAND Gate Latch – Alternate Representations

NAND latch equivalent representations and simplified block diagram.

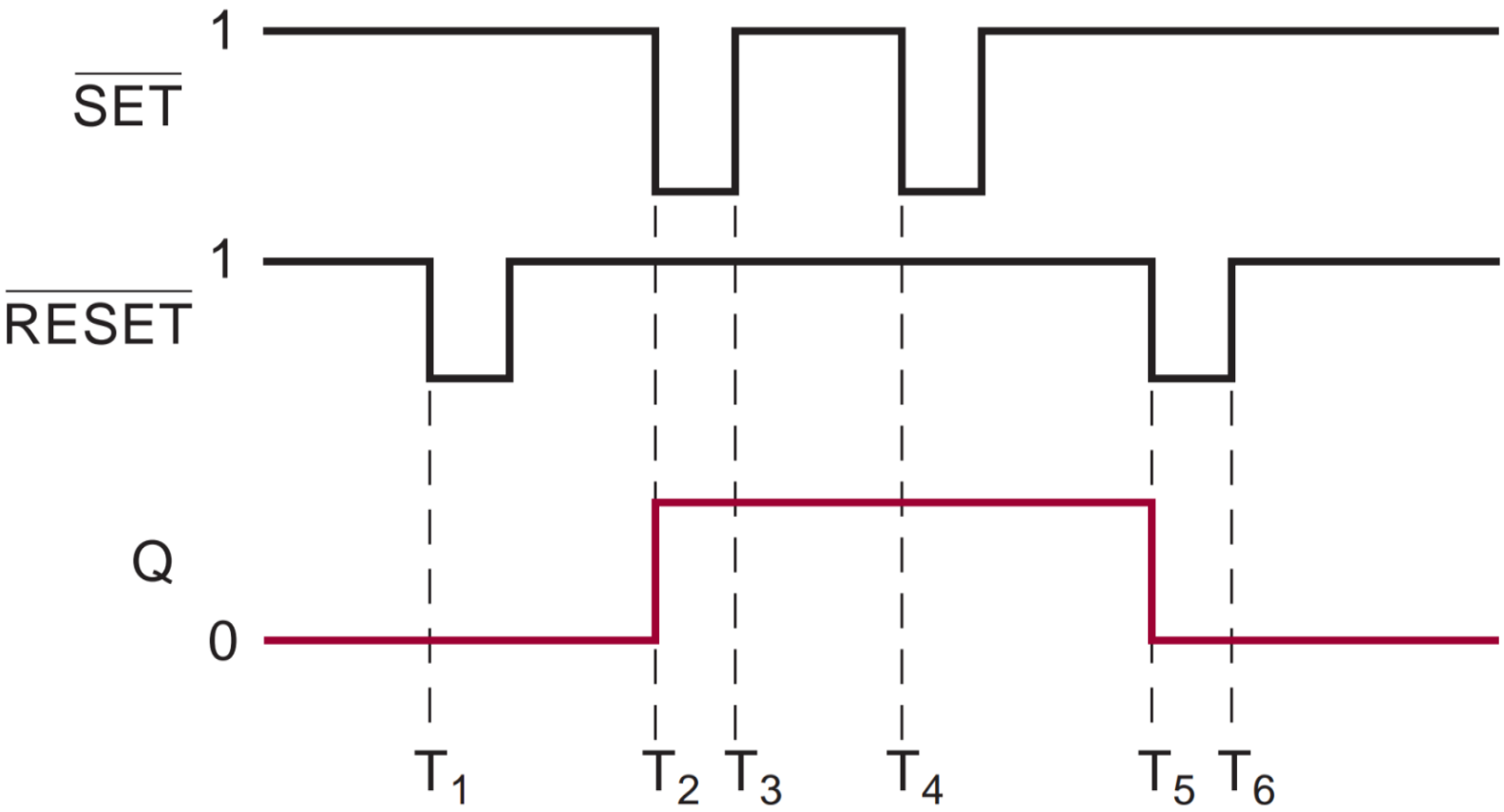


Set	Reset	Output(Q)
0	0	Invalid
0	1	1
1	0	0
1	1	No Change

5-1 NAND Gate Latch - Summary

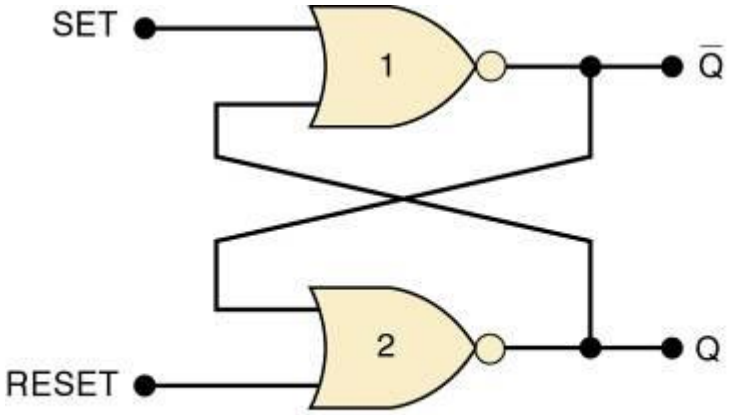
- Summary of the **NAND** latch:
  - **SET = 1, RESET = 1**—Normal resting state, outputs remain in state they were in prior to input.
  - **SET = 0, RESET = 1**—Output will go to $Q = 1$ and remains there, even after SET returns HIGH.
    - Called *setting* the latch.
  - **SET = 1, RESET = 0**—Will produce $Q = 0$ LOW and remains there, even after RESET returns HIGH.
    - Called *clearing* or *resetting* the latch.
  - **SET = 0, RESET = 0**—Tries to set and clear the latch at the same time, and produces $Q = \overline{Q} = 1$.
    - Output is unpredictable, and this input condition should not be used.

- Waveform diagram of NAND Latch



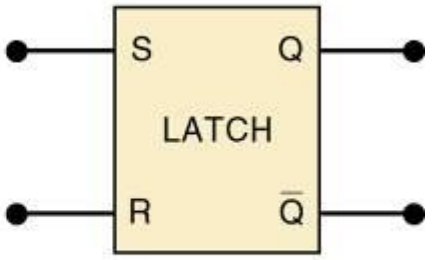
5-2 NOR Gate Latch

- Two cross-coupled **NOR** gates can be used as a **NOR** gate latch—similar to the **NAND** latch.
  - The **Q** and $\overline{\mathbf{Q}}$ outputs are reversed.



Set	Reset	Output
0	0	No change
1	0	Q = 1
0	1	Q = 0
1	1	Invalid*

*Produces $Q = \overline{Q} = 0$.

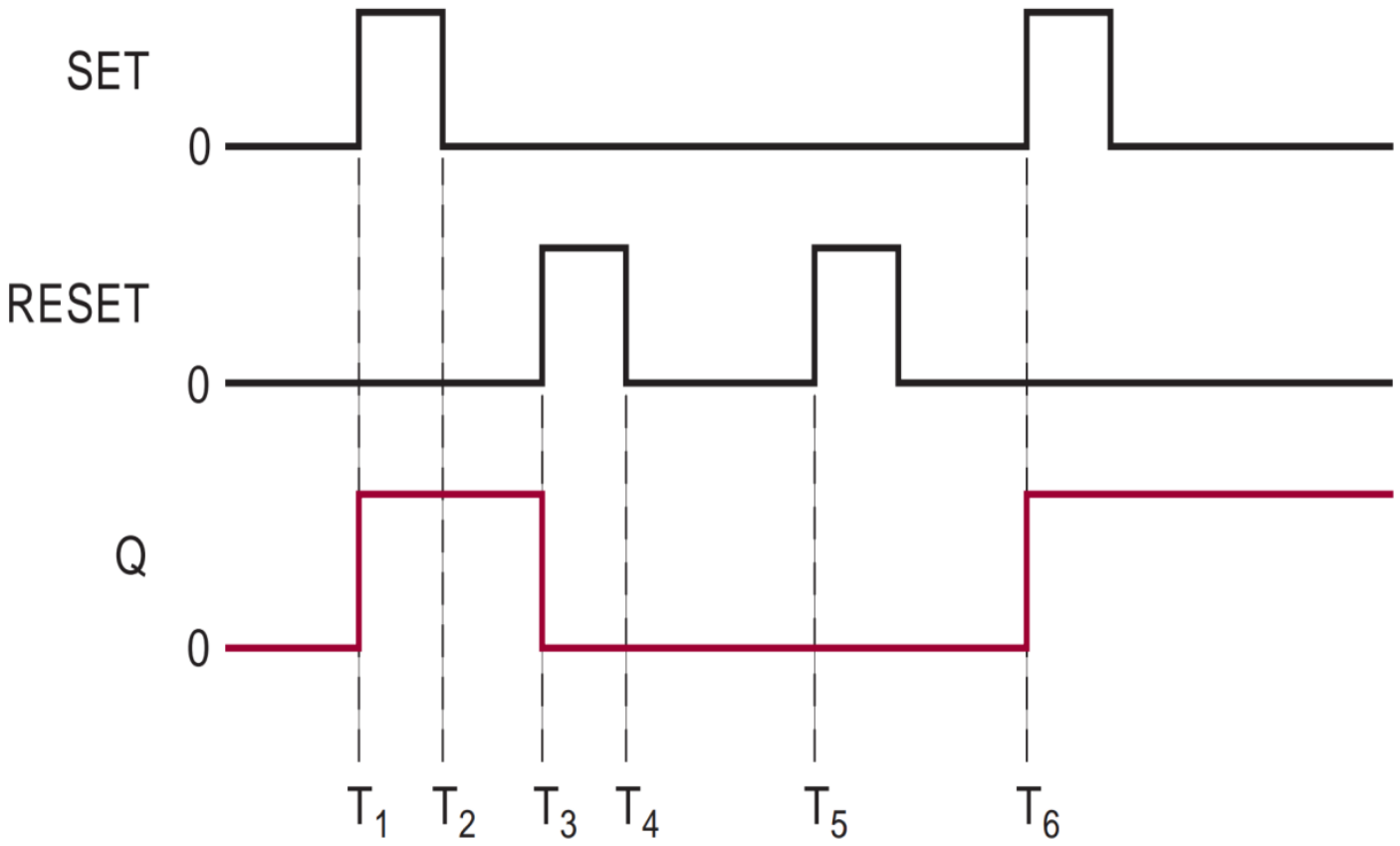


The SET and RESET inputs are active-HIGH.
Output will change when the input is pulsed HIGH.

5-2 NOR Gate Latch - Summary

- Summary of the **NOR** latch:
  - **SET = 0, RESET = 0**—Normal resting state, No effect on output state.
  - **SET = 1, RESET = 0**—will always set $Q = 1$, where it remains even after SET returns to 0.
  - **SET = 0, RESET = 1**—will always clear $Q = 0$, where it remains even after RESET returns to 0.
  - **SET = 1, RESET = 1**—Tries to set and reset the latch at the same time, and produces $Q = \overline{Q} = 0$.
    - Output is unpredictable, and this input condition should not be used.

- Waveform diagram of NOR Latch



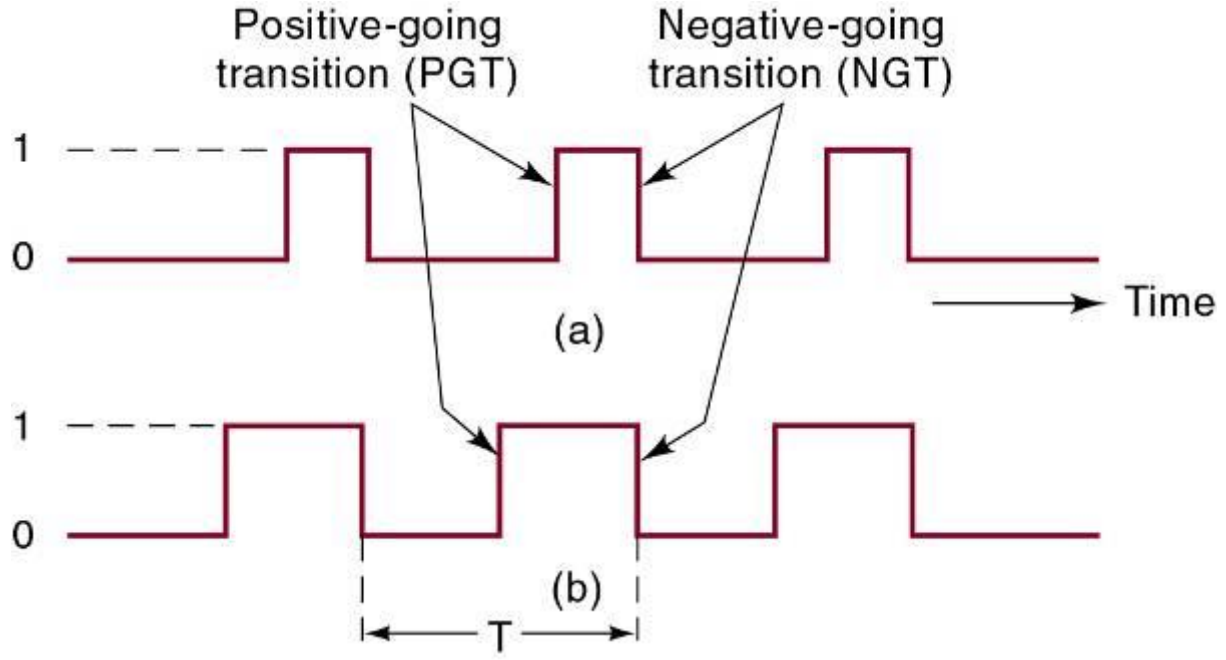
5-3 Clock Signals and Clocked Flip-Flops

- Digital systems can operate either *asynchronously* or *synchronously.*
  - **Asynchronous system**—outputs can change state at any time the input(s) change.
  - **Synchronous system**—output can change state only at a specific time in the clock cycle.

5-3 Clock Signals and Clocked Flip-Flops

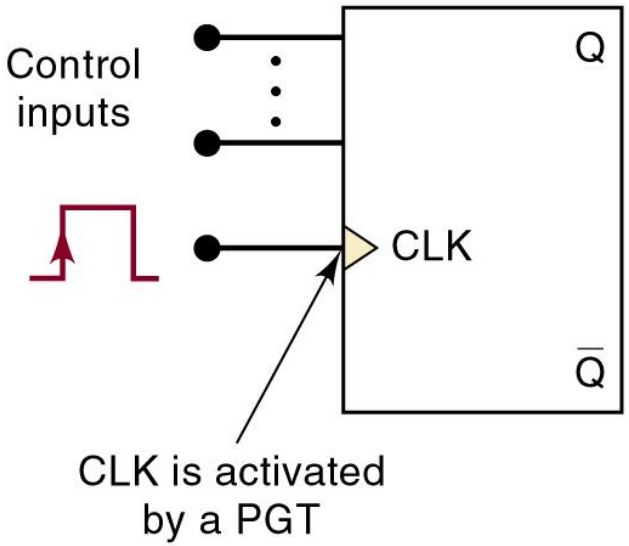
- The clock signal is a rectangular pulse train or square wave.
  - Positive going transition (PGT)—clock pulse goes from 0 to 1.
  - Negative going transition (NGT)—clock pulse goes from 1 to 0.

Transitions are also called *edges*.

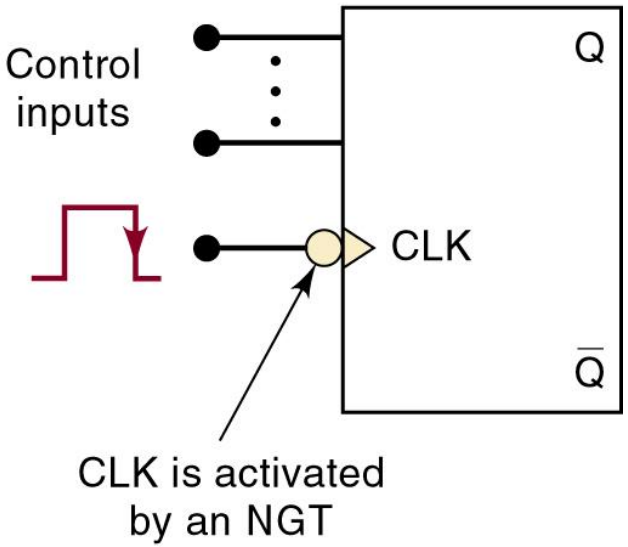


- Clocked FFs change state on one or the other clock transitions.
  - Clock inputs are labeled CLK, CK, or CP.

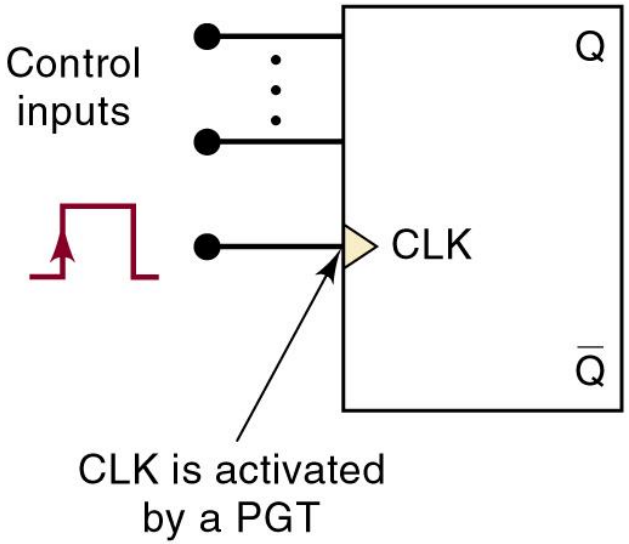
A small triangle at the CLK input indicates that the input is activated with a PGT.

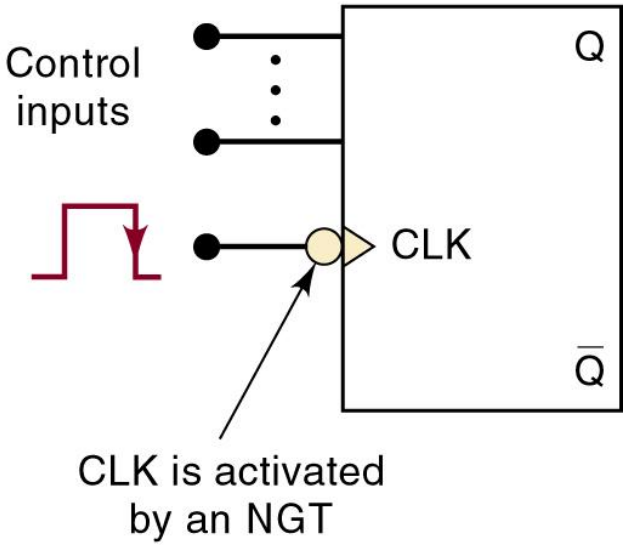


A bubble and a triangle indicates that the CLK input is activated with a NGT.



- Control inputs have an effect on the output only at the active clock transition (NGT or PGT)—also called synchronous control inputs.
  - The control inputs get the outputs ready to change, but the change is not triggered until the CLK edge.



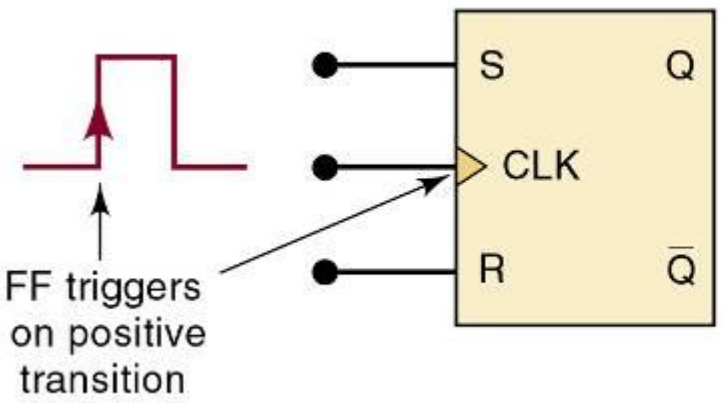


5-4 Clocked S-R Flip-Flop

- The *S* and *R* inputs are synchronous *control* inputs, which control the state the FF will go to when the clock pulse occurs.
  - The *CLK* input is the **trigger** input that causes the FF to change states according to the *S* and *R* inputs.
- SET-RESET (or SET-CLEAR) FF will change states at positive- or negative-going clock edges.

5-4 Clocked S-R Flip-Flop

A clocked S-R flip-flop triggered by the positive-going edge of the clock signal.



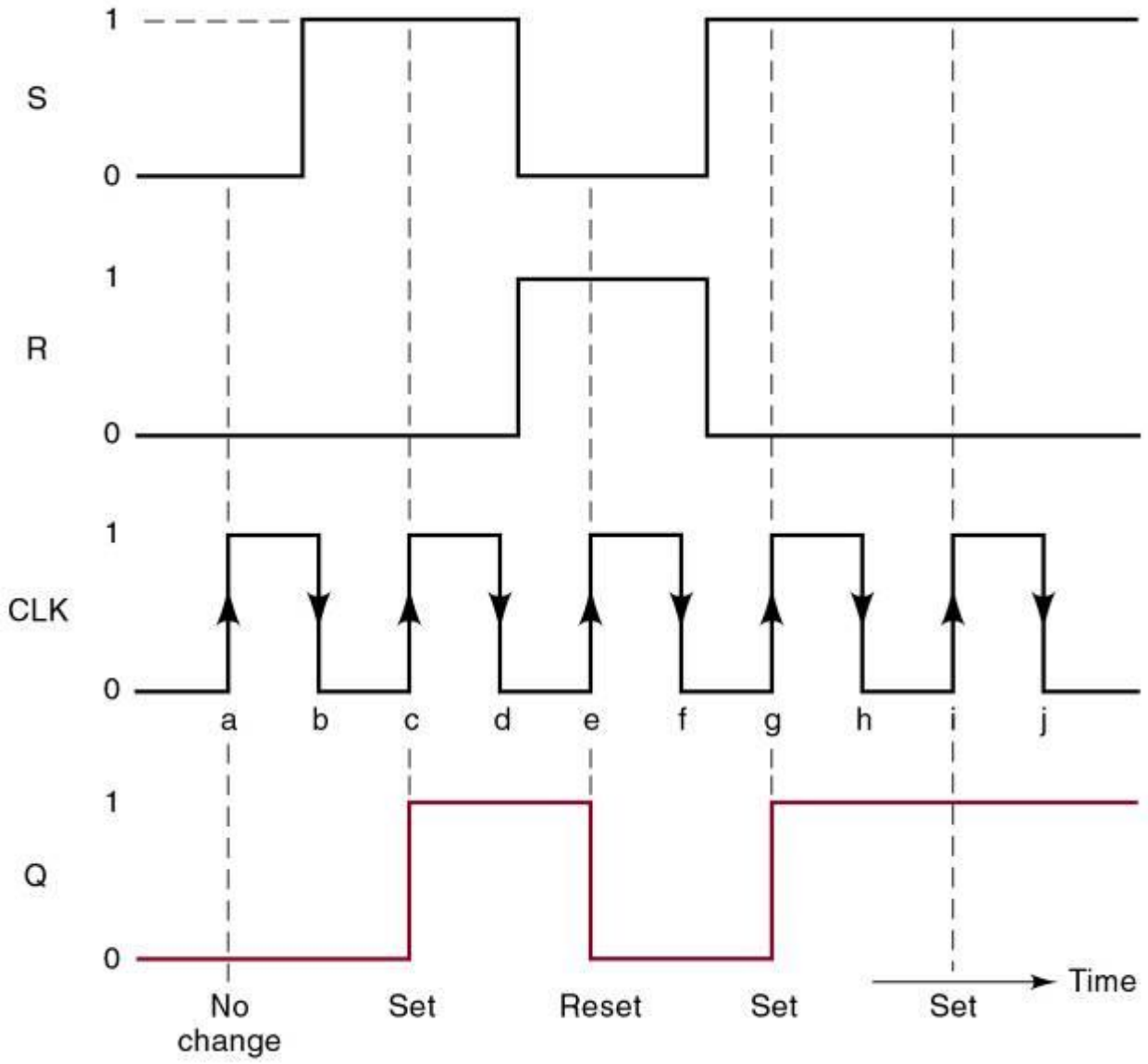
Inputs			Output
S	R	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	Ambiguous

Q_0 is output level prior to ↑ of CLK.
↓ of CLK produces no change in Q.

The *S* and *R* inputs control the state of the FF in the same manner as described earlier for the NOR gate latch, but the FF does *not* respond to these inputs *until* the occurrence of the PGT of the clock signal.

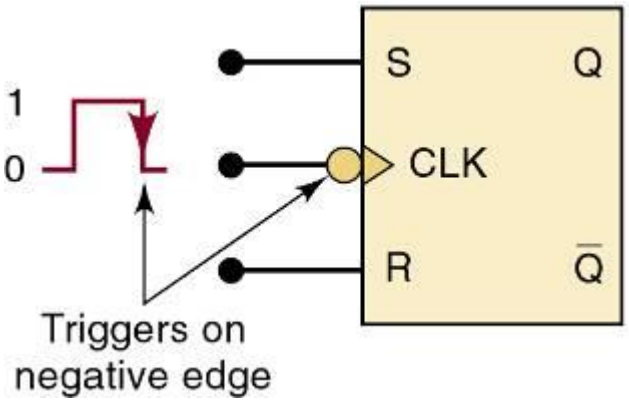
5-4 Clocked S-R Flip-Flop

Waveforms of the operation of a clocked S-R flip-flop triggered by the positive-going edge of a clock pulse.



5-4 Clocked S-R Flip-Flop

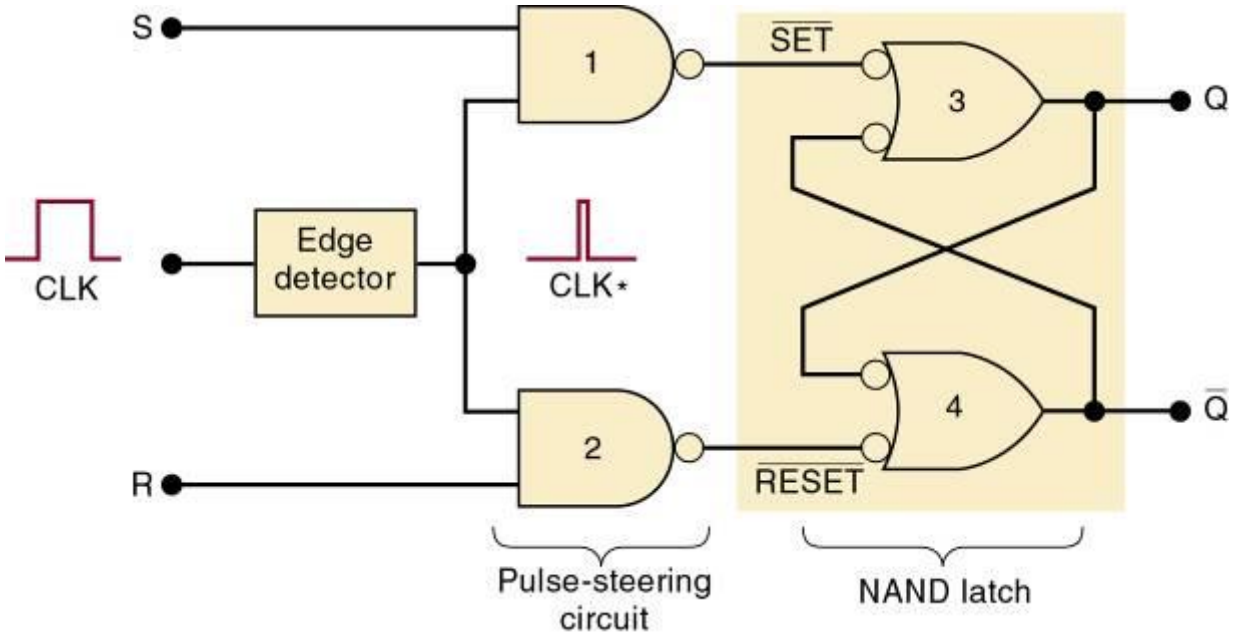
A clocked S-R flip-flop triggered by the negative-going edge of the clock signal.



Inputs			Output
S	R	CLK	Q
0	0	↓	Q_0 (no change)
1	0	↓	1
0	1	↓	0
1	1	↓	Ambiguous

Both positive-edge and negative-edge triggering FFs are used in digital systems.

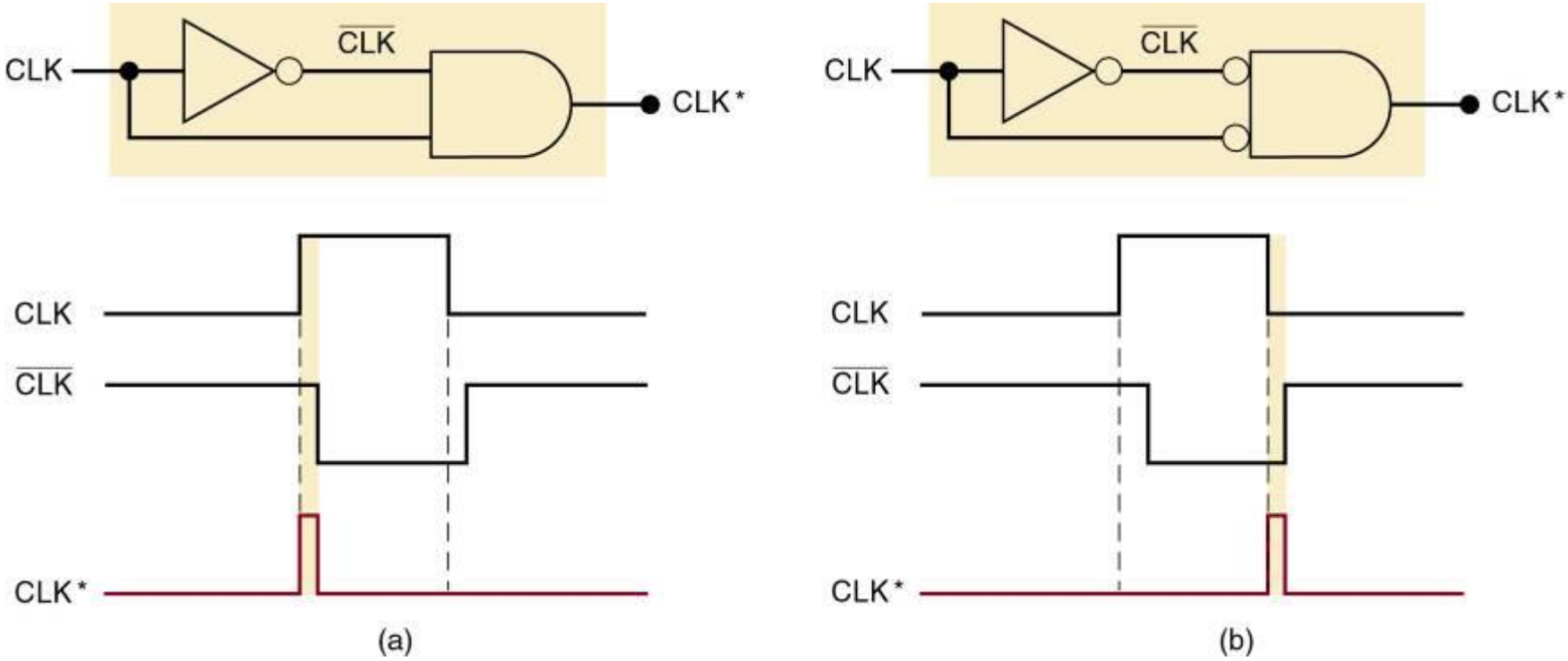
5-4 Clocked S-R Flip-Flop – Internal Circuitry



- An edge-triggered S-R flip-flop circuit features:
  - A basic **NAND** gate latch formed by **NAND**-3 and **NAND**-4.
  - A **pulse-steering circuit** formed by **NAND**-1 and **NAND**-2.
  - An **edge-detector circuit.**

5-4 Clocked S-R Flip-Flop – Internal Circuitry

- Implementation of edge-detector circuits used in edge-triggered flip-flops:
  - (a) PGT; (b) NGT.



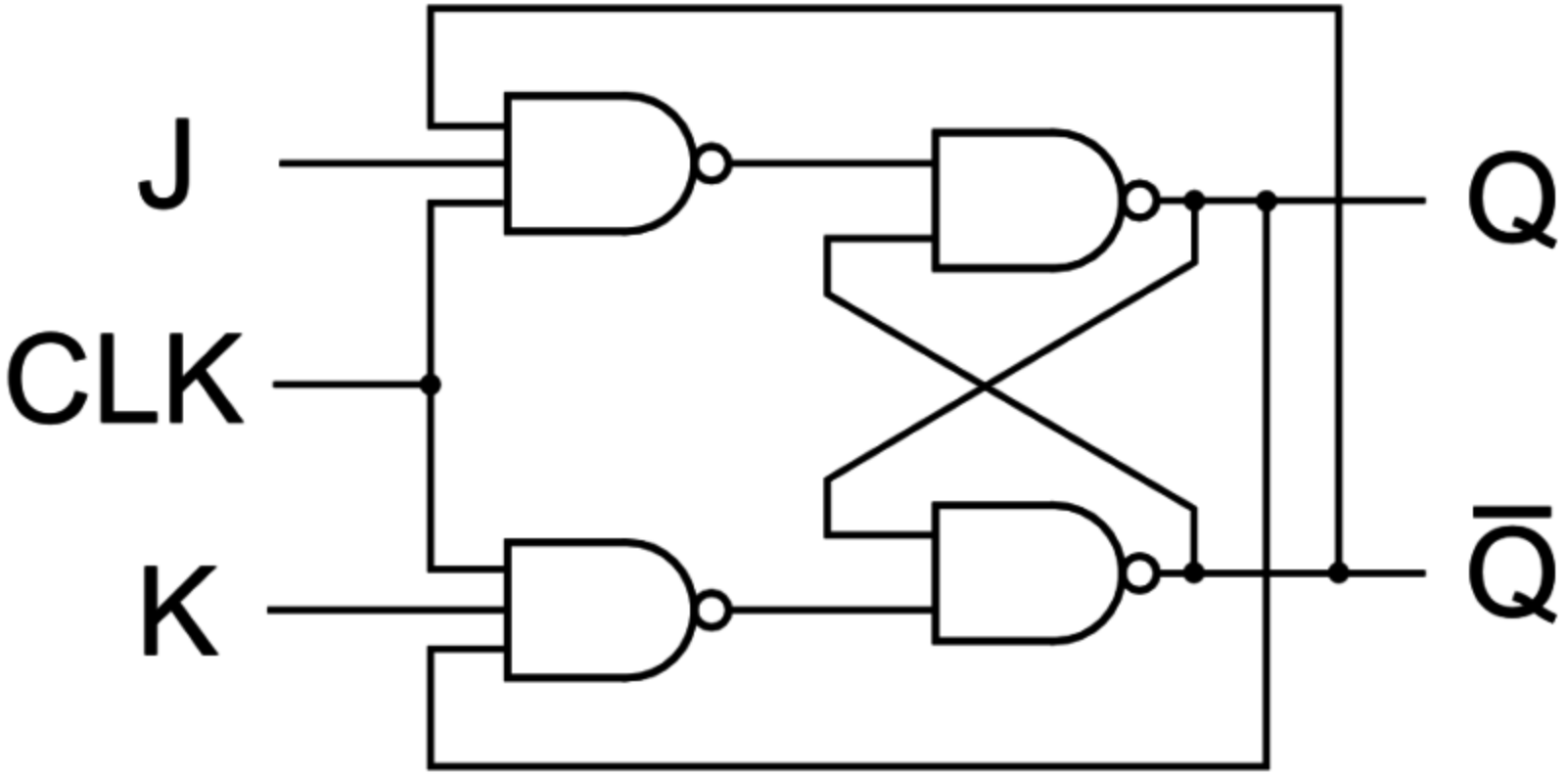
The duration of the *CLK** pulses is typically 2–5 ns.

5-5 Clocked J-K Flip-Flop

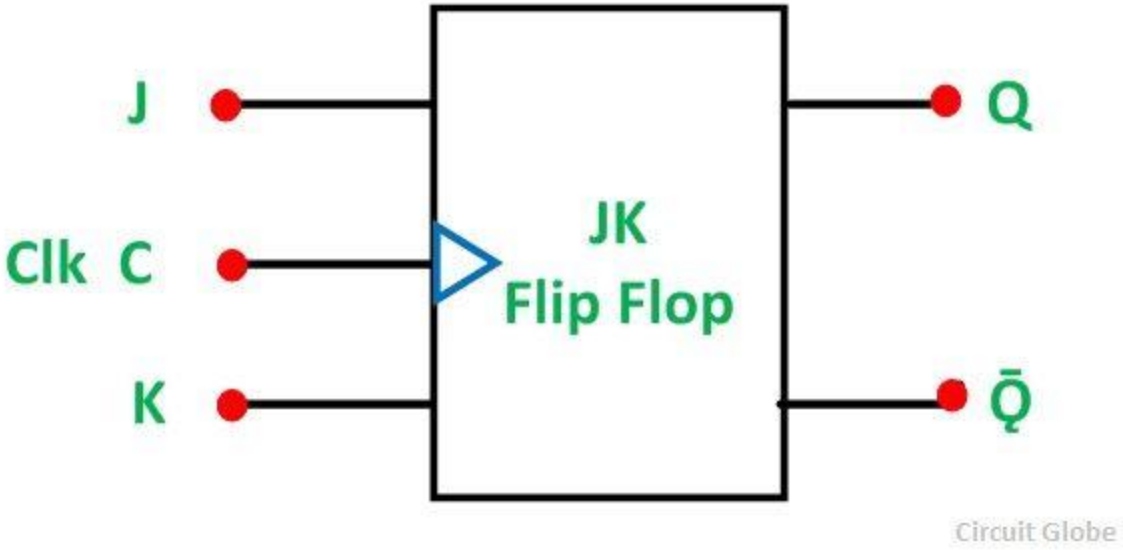
- Operates like the S-R FF.
  - J is SET, K is CLEAR.
- When J and K are both HIGH, output is toggled to the opposite state.
  - May be positive going or negative going clock trigger.
- Much more versatile than the S-R flip-flop, as it has no ambiguous states.
  - Has the ability to do everything the S-R FF does, plus operates in toggle mode.

5-5 Clocked J-K Flip-Flop – Internal Circuitry

- Internal Circuit of Clocked J-K Flip-Flop

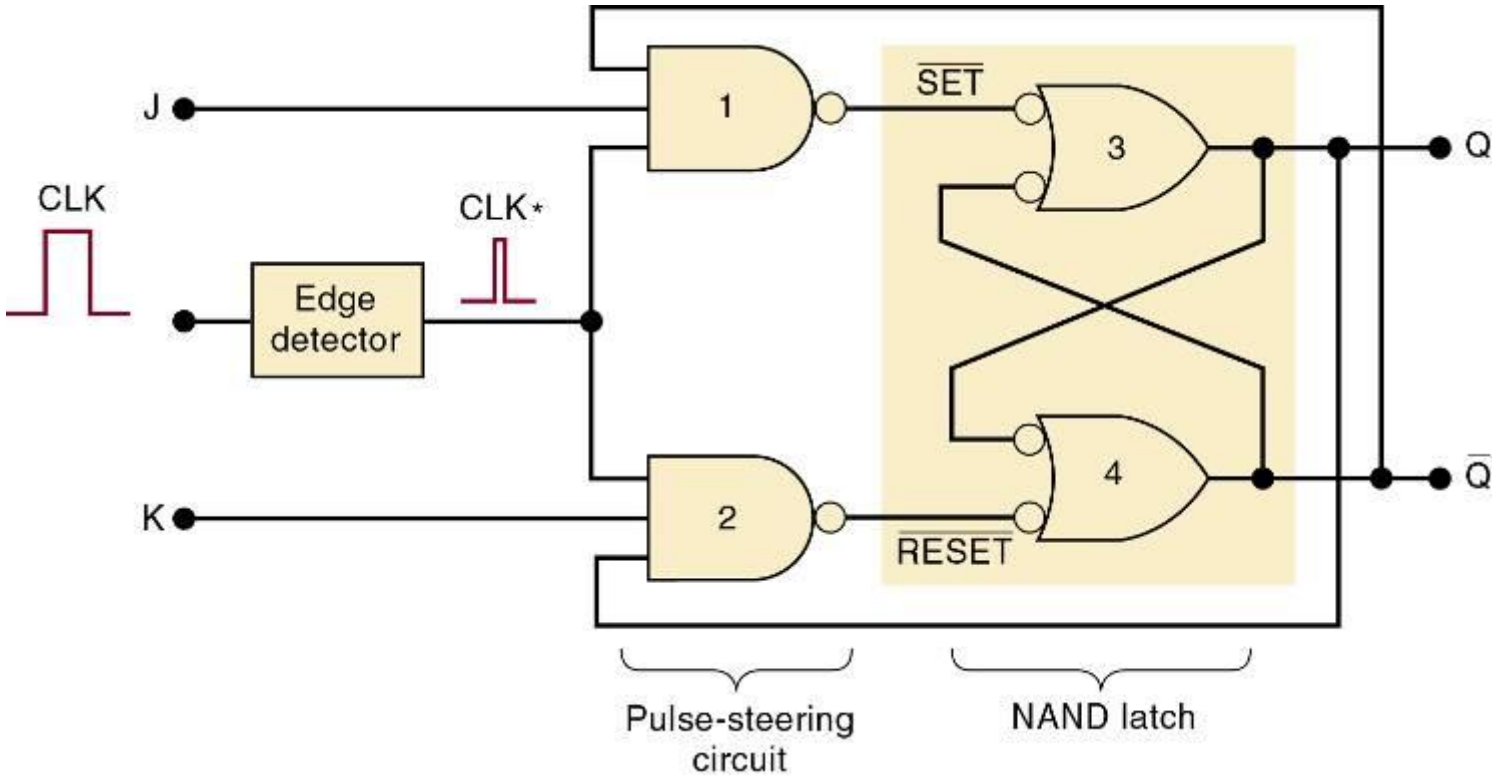


- Block Diagram Clocked J-K Flip-Flop

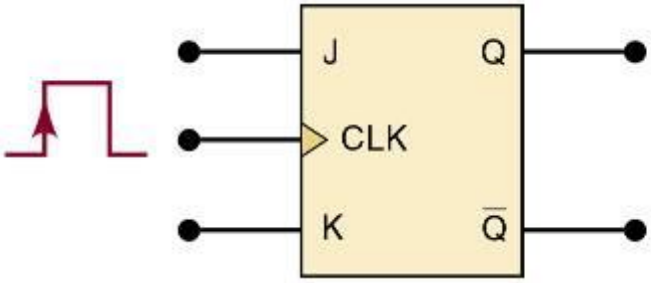


5-5 Clocked J-K Flip-Flop – Internal Circuitry

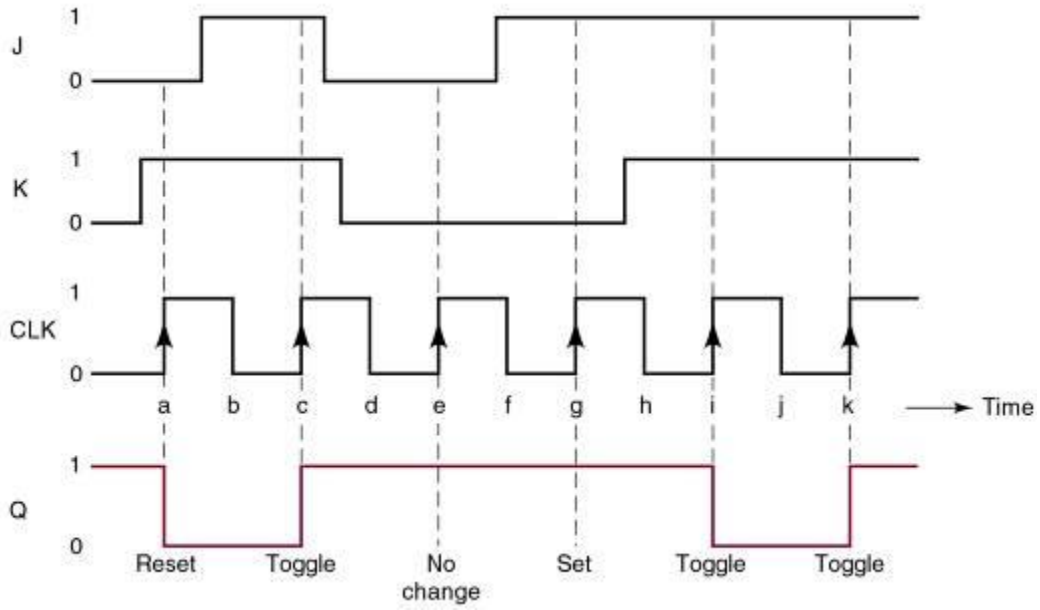
- The internal circuitry of an edge-triggered J-K flip-flop contains the same three sections as the edge-triggered S-R flip-flop.



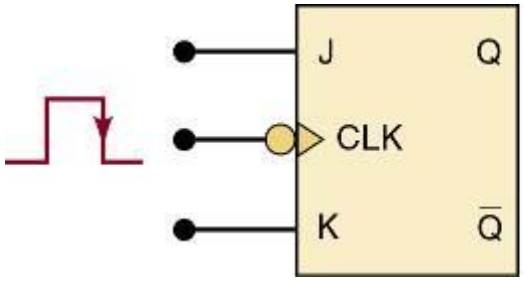
Clocked J-K flip-flop that responds only to the positive edge of the clock.



J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\overline{Q}_0$ (toggles)



Clocked J-K flip-flop that responds only to the negative edge of the clock.

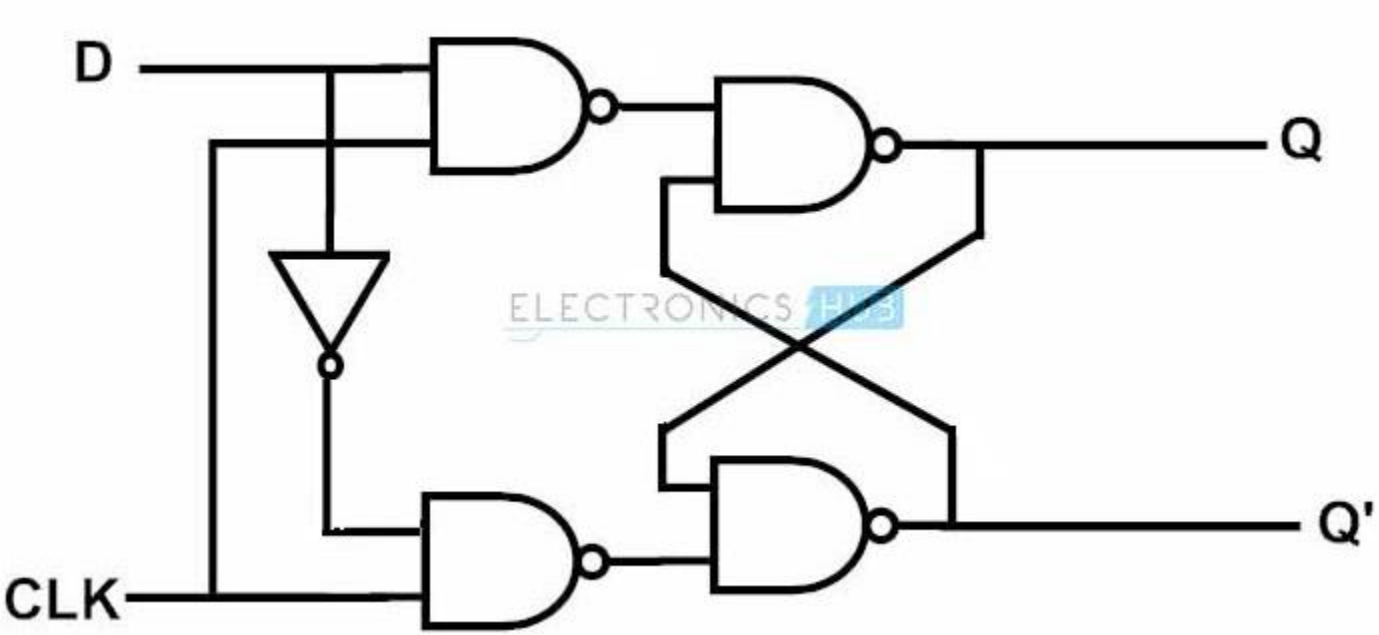


J	K	CLK	Q
0	0	↓	Q_0 (no change)
1	0	↓	1
0	1	↓	0
1	1	↓	$\overline{Q_0}$ (toggles)

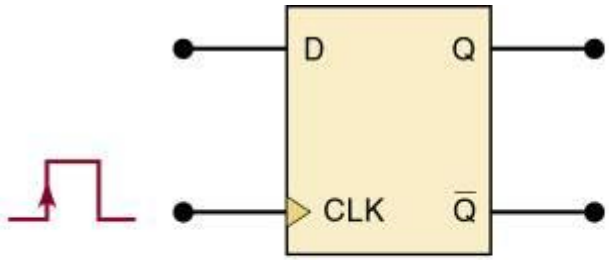
5-6 Clocked D Flip-Flop

- One data input—output changes to the value of the input at either the positive- or negative-going clock trigger.
- May be implemented with a J-K FF by tying the J input to the K input through an inverter.
- Useful for parallel data transfer.

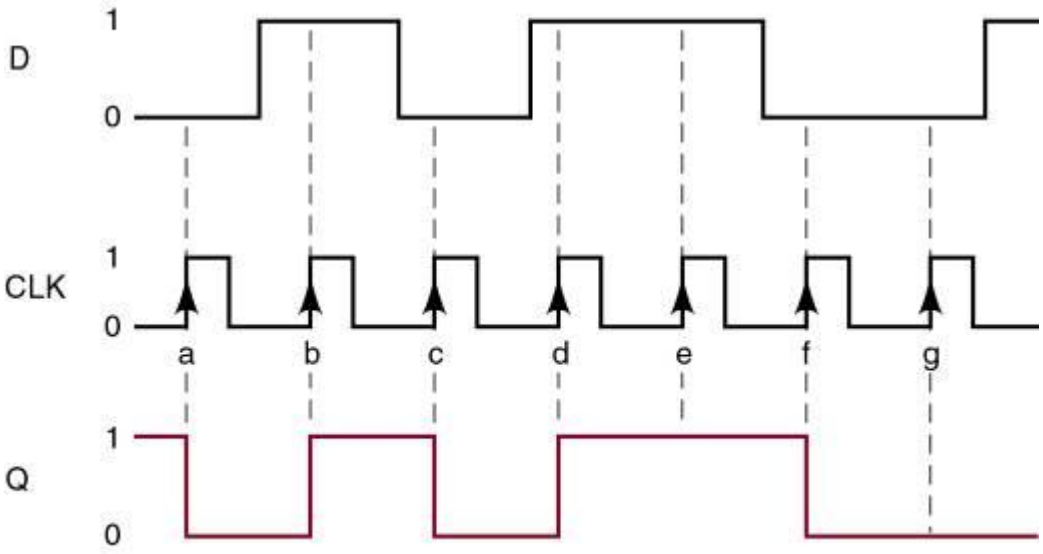
- Internal Circuit of Clocked D Flip-Flop



D flip-flop that triggers only on positive-going transitions.



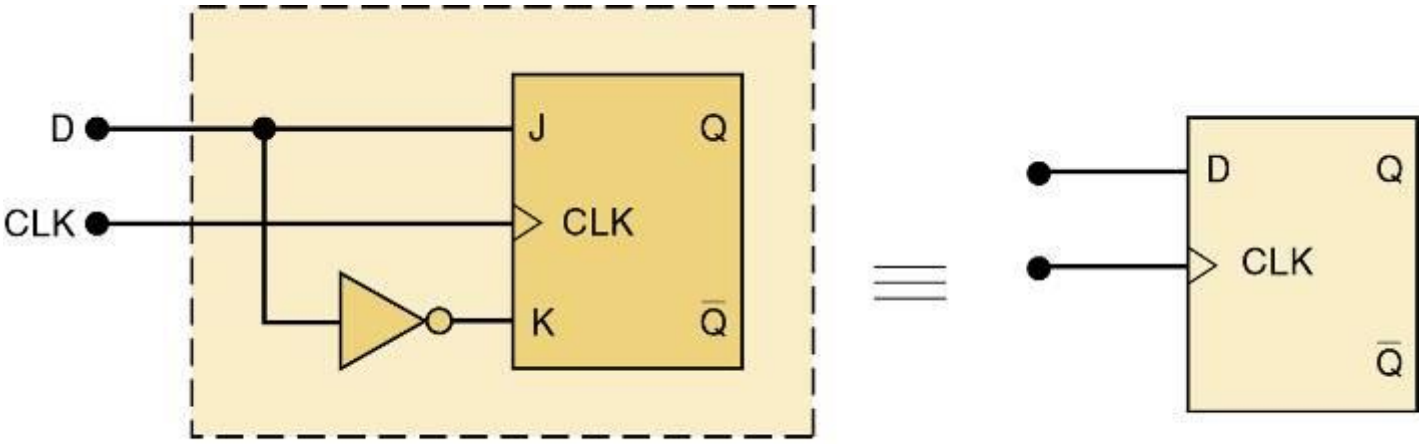
D	CLK	Q
0	↑	0
1	↑	1



5-7 Clocked J-K to D Flip-Flop - Implementation

- A clocked D flip-flop is implemented by adding a single INVERTER to the clocked J-K flip-flop.
  - The same can be done to convert a S-R flip-flop to a D flip-flop.

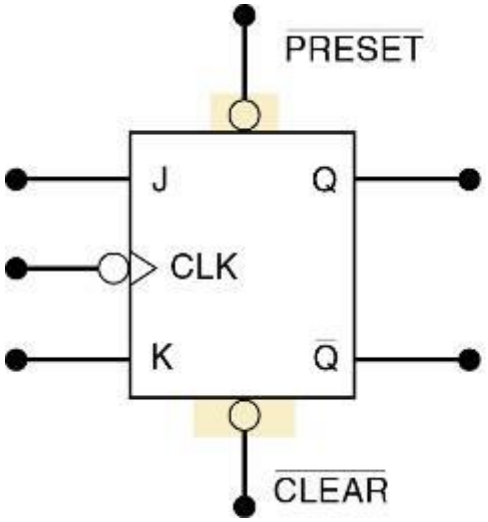
Edge-triggered D flip-flop implementation from a J-K flip-flop.



5-8 Asynchronous Inputs

- Inputs that depend on the clock are synchronous.
- Most clocked FFs have asynchronous inputs that do not depend on the clock.
  - Labels PRE & CLR are used for asynchronous inputs.
- Active-LOW asynchronous inputs will have a bar over the labels and inversion bubbles.
- If the asynchronous inputs are not used they will be tied to their inactive state.

Clocked J-K flip-flop with asynchronous inputs.

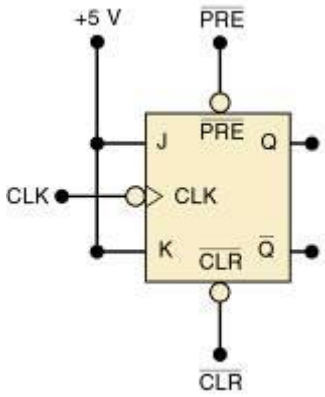


J	K	Clk	$\overline{PRE}$	$\overline{CLR}$	Q
0	0	↓	1	1	Q (no change)
0	1	↓	1	1	0 (Synch reset)
1	0	↓	1	1	1 (Synch set)
1	1	↓	1	1	$\overline{Q}$ (Synch toggle)
x	x	x	1	1	Q (no change)
x	x	x	1	0	0 (asynch clear)
x	x	x	0	1	1 (asynch preset)
x	x	x	0	0	(Invalid)

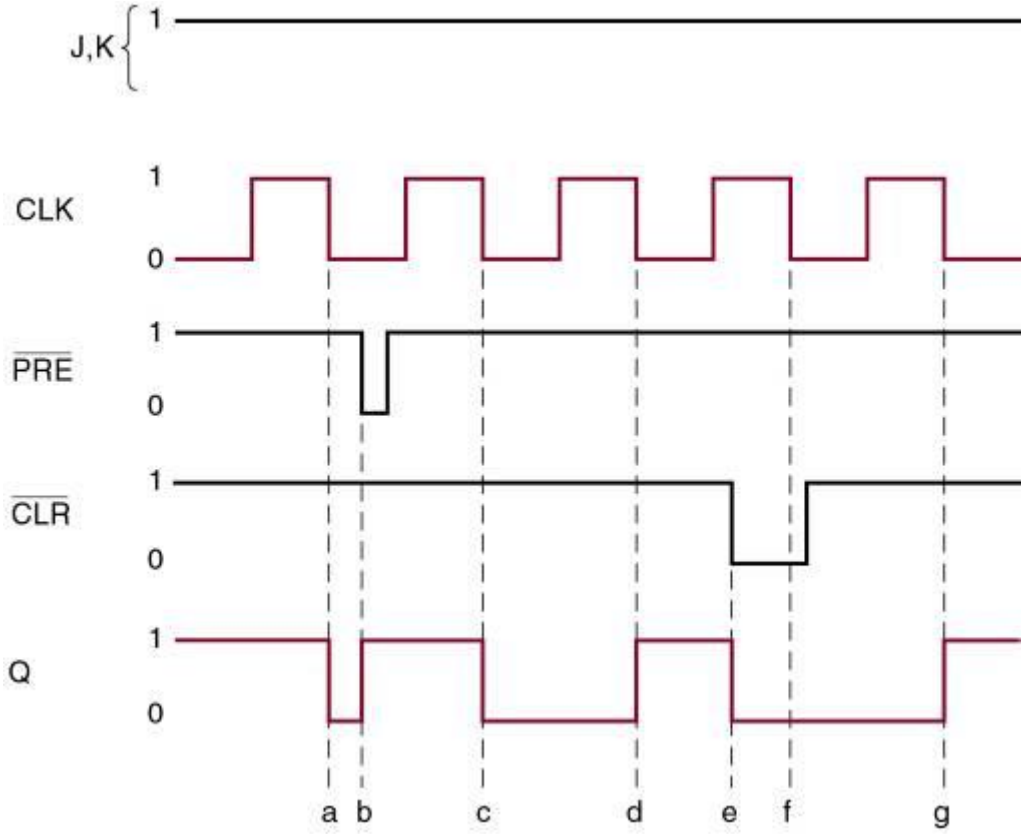
5-8 Asynchronous Inputs - Designations

- IC manufacturers do not agree on nomenclature for asynchronous inputs.
  - The most common designations are *PRE* (PRESET) and *CLR* (CLEAR).
    - Clearly distinguished from synchronous SET & RESET.
  - Labels such as *S-D* (direct SET) and *R-D* (direct RESET) are also used.

A J-K FF that responds to a NGT on its clock input and has active-LOW asynchronous inputs.



Point	Operation
a	Synchronous toggle on NGT of CLK
b	Asynchronous set on $\overline{PRE}$ = 0
c	Synchronous toggle
d	Synchronous toggle
e	Asynchronous clear on $\overline{CLR}$ = 0
f	$\overline{CLR}$ overrides the NGT of CLK
g	Synchronous toggle



5-9 Flip-Flop Timing Considerations - Parameters

- Important timing parameters:
  - Setup and hold times
  - **Propagation delay**—time for a signal at the input to be shown at the output. (t_{PLH} and t_{PHL})
  - **Maximum clocking frequency**—Highest clock frequency that will give a reliable output. (f_{MAX})
  - **Clock pulse HIGH and LOW times**—minimum clock-time between HIGH/LOW changes.($t_W(L)$; $t_W(H)$)
  - **Asynchronous Active Pulse Width**—time the clock must HIGH before going LOW, and LOW before going HIGH.
  - **Clock transition times**—maximum time for clock transitions,
    - Less than 50 ns for TTL ; 200 ns for CMOS

5-10 Flip-Flop Applications

- Frequency Division
- Counting

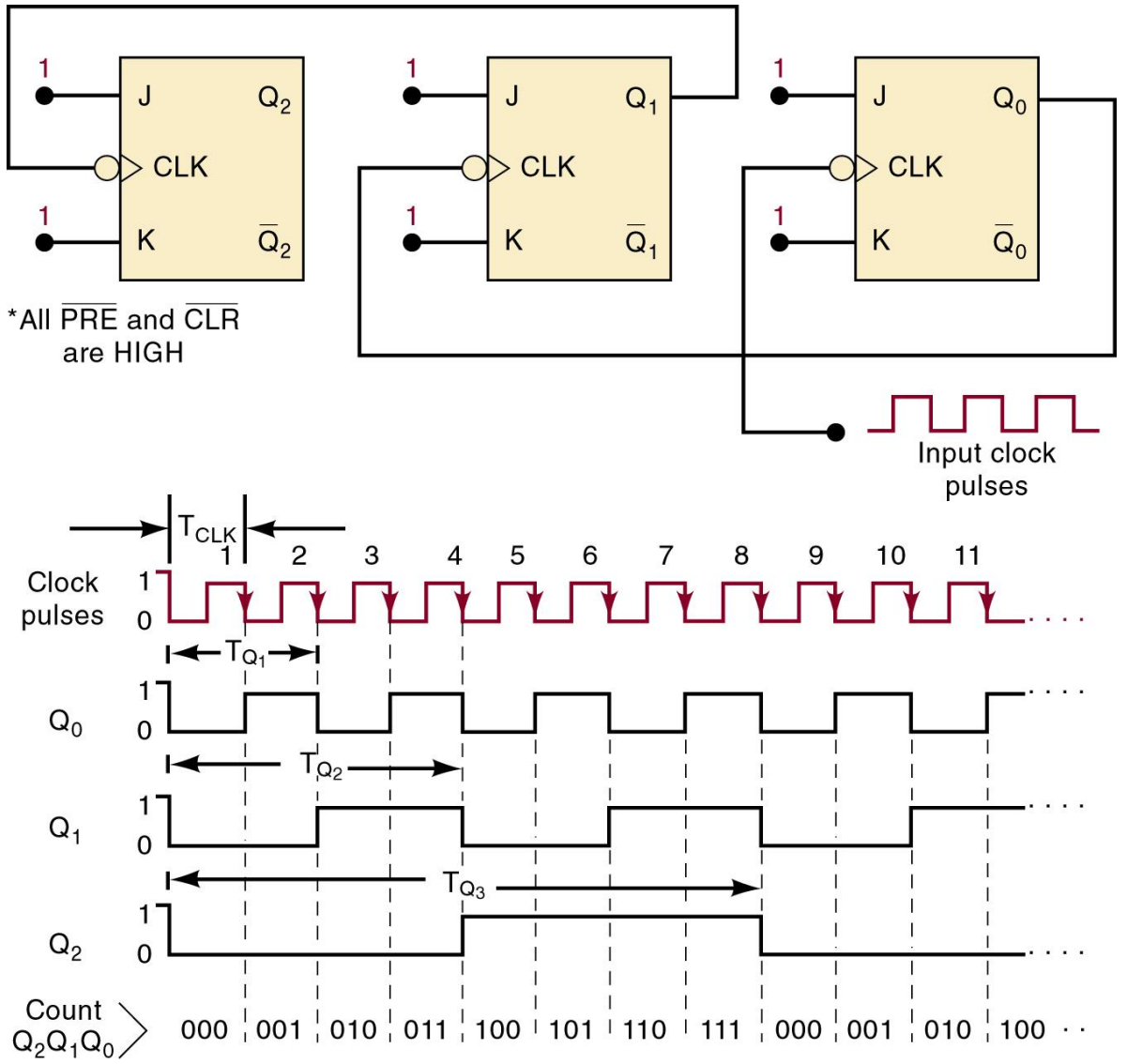
5-11 Frequency Division and Counting

J-K flip-flops wired as a three-bit binary counter (MOD-8).

Each FF divides the input frequency by 2.

Output frequency is 1/8 of the input (clock) frequency.

A fourth FF would make the frequency 1/16 of the clock.



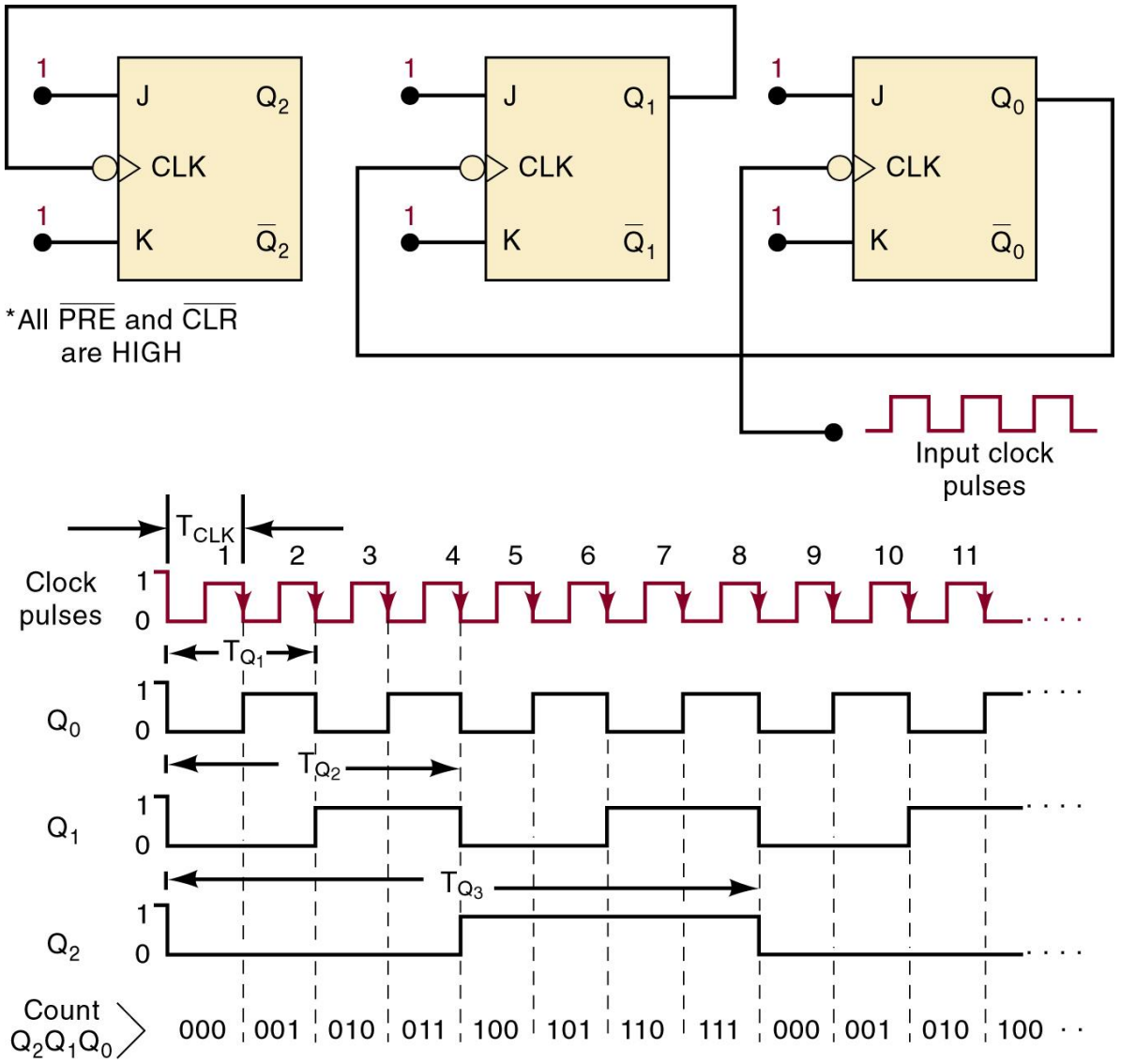
5-11 Frequency Division and Counting

J-K flip-flops wired as a three-bit binary counter (MOD-8).

This circuit also acts as a binary counter.

Outputs will count from 000 to 111 or 0 to 7.

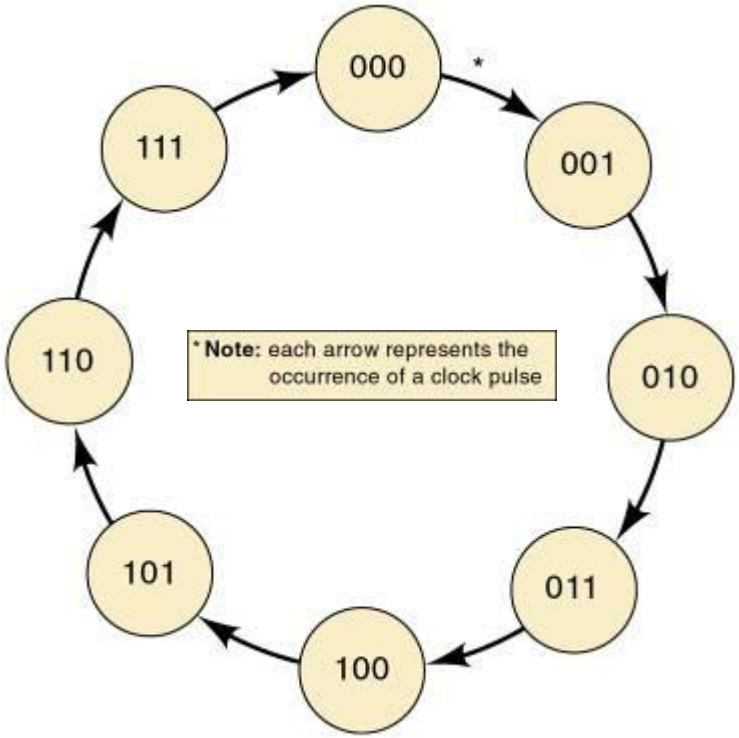
The number of states possible in a counter is the modulus or MOD number.



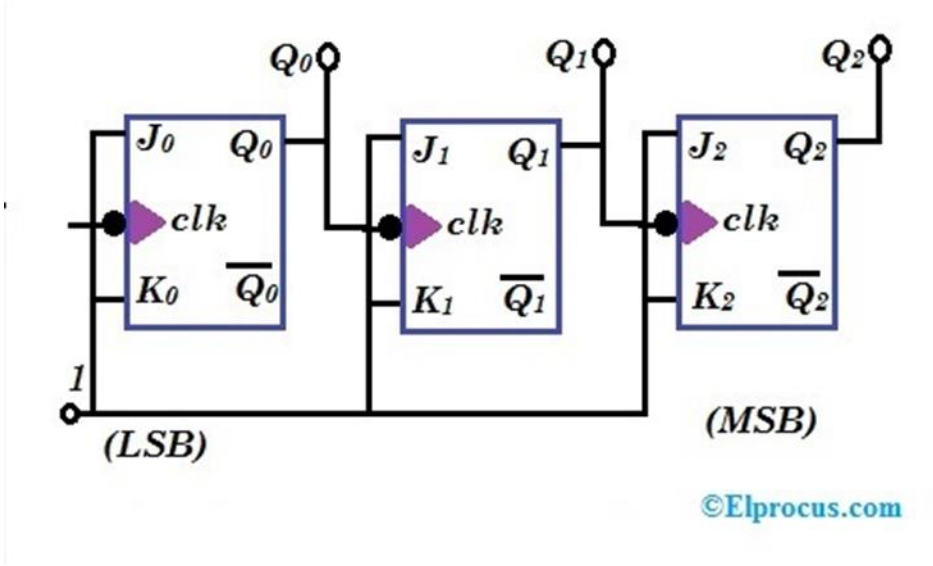
A MOD-8 (2^3) counter.

If another FF is added it would become a MOD-16 (2^4) counter.

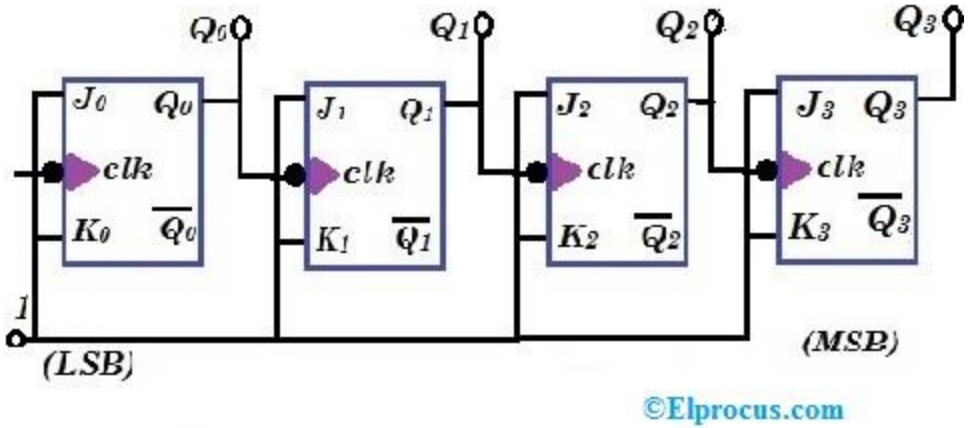
2^2	2^1	2^0	
Q_2	Q_1	Q_0	
0	0	0	Before applying clock pulses
0	0	1	After pulse #1
0	1	0	After pulse #2
0	1	1	After pulse #3
1	0	0	After pulse #4
1	0	1	After pulse #5
1	1	0	After pulse #6
1	1	1	After pulse #7
0	0	0	After pulse #8 recycles to 000
0	0	1	After pulse #9
0	1	0	After pulse #10
0	1	1	After pulse #11
.	.	.	. . .
.	.	.	. . .
.	.	.	. . .



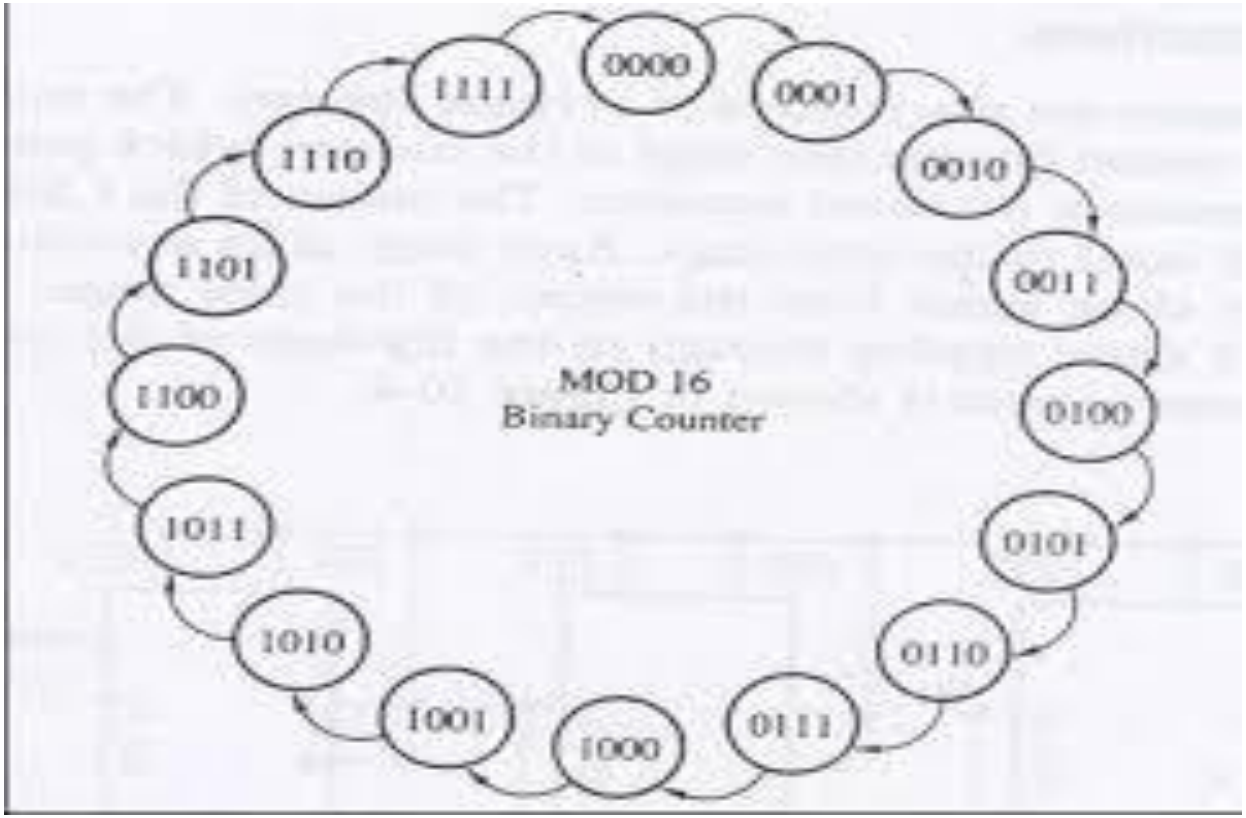
- Internal Circuit of MOD 8 Up Counter



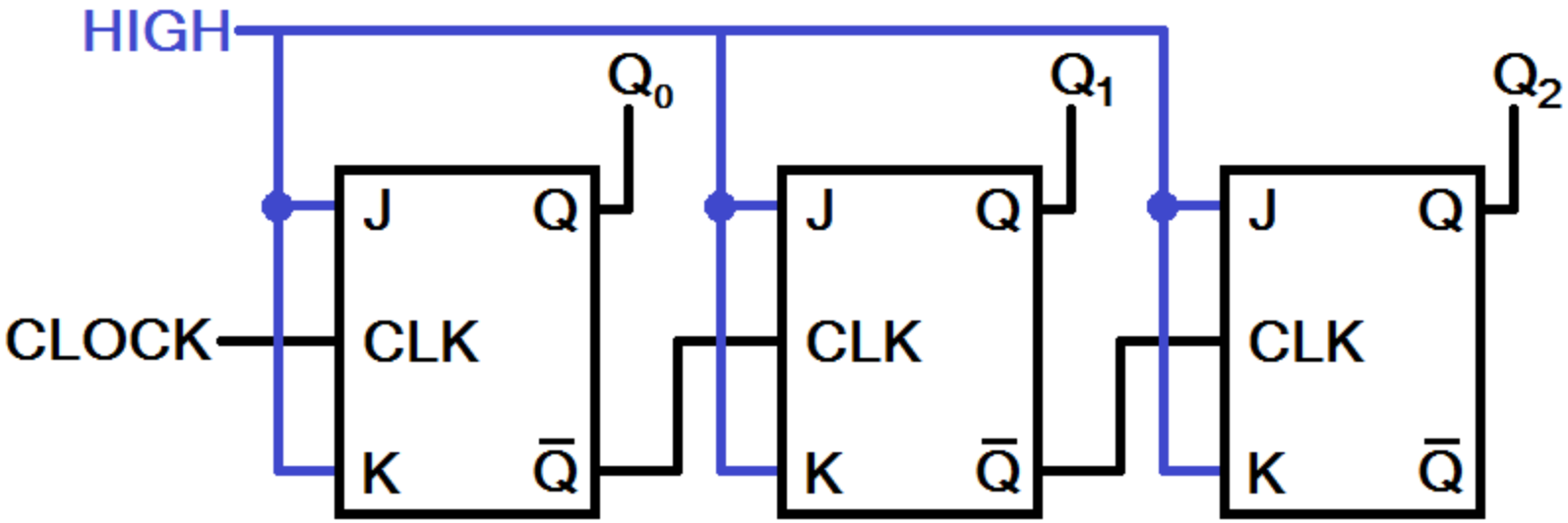
- Internal Circuit of MOD 16 Up Counter



- State Transition diagram of MOD 16 Up Counter

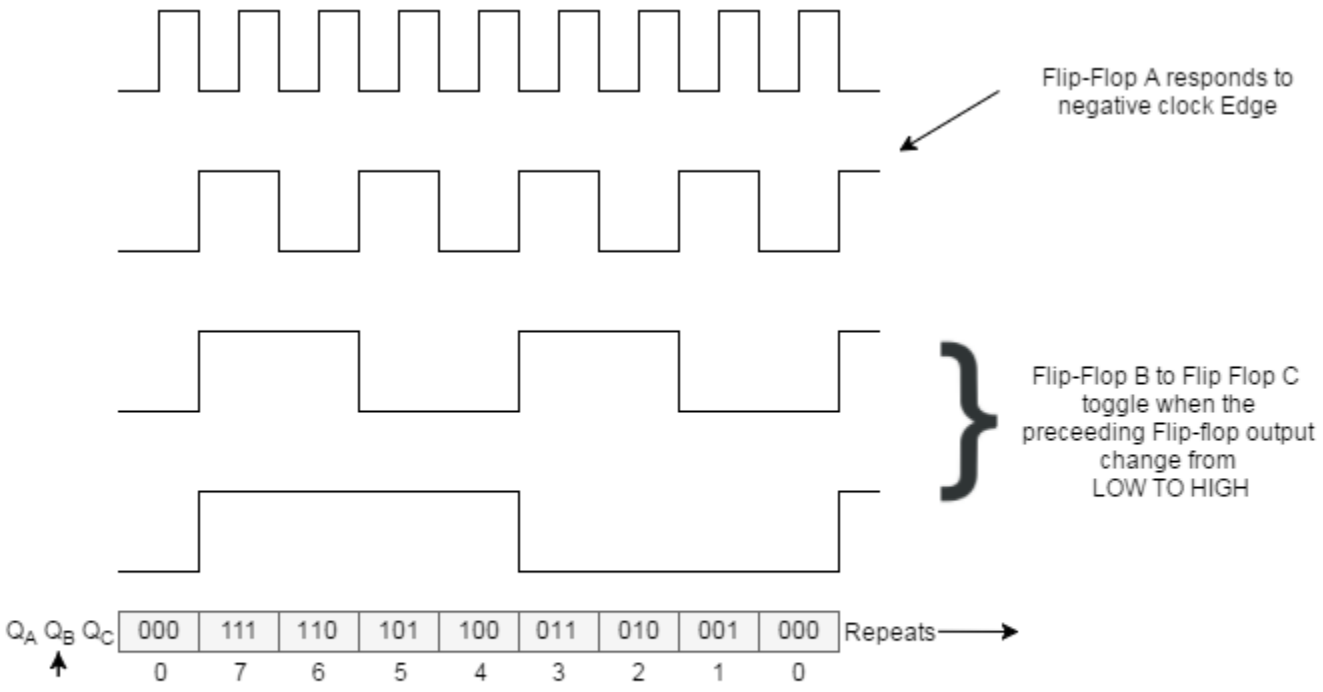


- Internal Circuit of MOD 8 Down Counter



5-11 Frequency Division and Counting

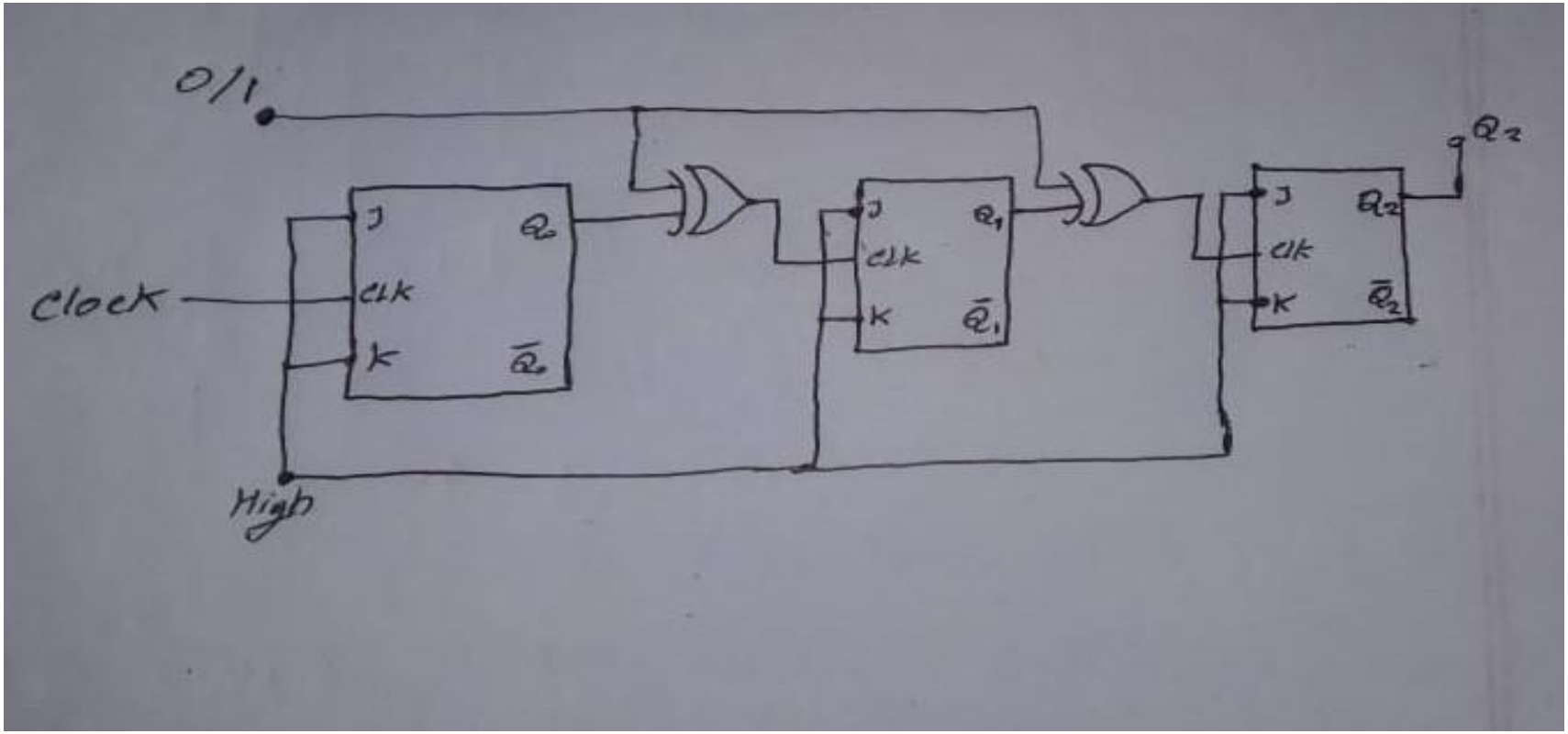
- Outputs will count from 111 to 000 or 7 to 0.



Timing Diagram of a 3bit Down Counter

5-11 Frequency Division and Counting

- Internal Circuit of MOD 8 Up/Down Counter



- If S=0 then clock of 2nd FF is Q0 and clock of 3rd FF is Q1, So it is Mod 8 Up counter.
- If S=1 then clock of 2nd FF is Q`0 and clock of 3rd FF is Q`1, So it is Mod 8 Down counter.

Question 1

Consider a counter circuit that contains six FFs wired in the arrangement Q5Q4Q3Q2Q1Q0

(a) Determine the counter's MOD number.

(b) Determine the output frequency in KHz when the input clock frequency is 1 MHz.

(c) What is the range of counting states for this counter?

(d) Assume a starting state (count) of 001001. What will be the counter's state after 129 pulses?

5-12 Model Question about this chapter

Question 2

A 20-kHz clock signal is applied to a J-K flip-flop with J=K=1. What is the frequency of the FF output waveform?

Question 3

a) How many FFs are required for a counter that will count 0 to 255?

b) What is the MOD number of the counter?

Question 4

a) What is the frequency of the output of the eighth FF when the input clock frequency is 512 kHz?

b) If this counter starts at 00011001, what will be its state after 520 pulses?

Question 5

A binary counter is being pulsed by a 256-kHz clock signal. The output frequency is 2 kHz.

(a) Determine the MOD number.

(b) Determine the counting range.

Question 6

(a) How many FFs are required to build a binary counter that counts from 0 to 1023?

(b) Determine the output frequency in Hz of this counter for an input clock frequency of 2 MHz.

(c) What is the counter's MOD number?

(d) If the counter is initially at zero, what count will it hold after 2060 pulses?

Question 7

Consider a MOD 16 up counter for the following questions:

- If the counter is initially at 1011 state, determine the output state after 83 pulses.
- If the input frequency of the clock signal is 10 MHz, what is the output frequency in KHz.
- Draw the state transition diagram of the counter.

Question 8

A photo detector circuit is being used to generate a pulse each time a customer walks into a certain establishment. The pulses are fed to an eight-bit counter. The counter is used to count these pulses as a means for determining how many customers have entered the store. After closing the store, the proprietor checks the counter and finds that it shows a count of 00001001=9. He knows that this is incorrect because there were many more than nine people in his store. Assuming that the counter circuit is working properly.

a) What could be the reason for the discrepancy?

b) How can you overcome from the discrepancy?

5-12 Model Question about this chapter

Question 9: Draw the internal circuit of clocked JK flip-flop. Briefly describe the operation of the flip-flop.

Question 10: Draw the internal circuit of clocked D flip-flop. Briefly describe the operation of the flip-flop.

Question 11: Convert JK to D flip-flop. Briefly explain.

Question 12: Define Mod number of counter.

Question 13: What are PGT and NGT?

Question 14: What are up and down counter?

5-12 Model Question about this chapter

Question 15: Draw the internal circuit of clocked S-C flip-flop. Briefly describe the operation of the flip-flop.

Question 16: Draw the internal circuit of NAND Latch. Briefly describe the operation of the Latch.

Question 17: Draw the internal circuit of NOR Latch. Briefly describe the operation of the Latch.

Question 18: Draw the internal circuit of MOD 8 up counter using J-K flip-flops. Briefly describe the operation of the counter.

5-12 Model Question about this chapter

- Question 19: Draw the internal circuit of MOD 16 up counter using J-K flip-flops. Briefly describe the operation of the counter.
- Question 20: Draw the internal circuit of MOD 8 down counter using J-K flip-flops. Briefly describe the operation of the counter.
- Question 21: Draw the internal circuit of MOD 16 down counter using J-K flip-flops. Briefly describe the operation of the counter.
- Question 22: Draw the internal circuit of MOD 8 up/down counter using J-K flip-flops & logic gates. Briefly describe the operation of the counter.