



UNIVERSITY OF ASIA PACIFIC

Department of Computer Science & Engineering

Course Title : Digital Logic & System Design Lab

Course Code : CSE 210

Experiment No. : 01

Experiment Name : Test and verify the truth table of following gates: AND gate, OR gate, NOT gate, NAND gate, NOR gate, Exclusive-OR gate.

Date of Performance : 18-01-2022

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Department of CSE

University of Asia Pacific

Problem Statement : Test and verify the truth table of following gates: AND gate, OR gate, NOT gate, NAND gate, NOR gate, Exclusive-OR gate.

Input & Output Variables Specification: We are using **A,B** as input and **Y** as output variable.

Truth Table:

AND Gate

Input		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

OR Gate

Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

NOT Gate

Input		Output
0		1
1		0

NAND Gate

Input		Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

NOR Gate

Input		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

XOR Gate

Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Logic Expression:

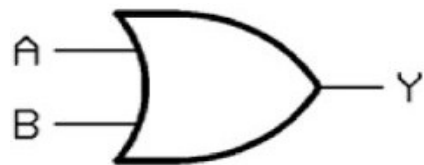
Logic Gate	Logic Expression
AND	$Y = A \cdot B$
OR	$Y = A + B$
NOT	$Y = \overline{A}$
NAND	$Y = \overline{A \cdot B}$
NOR	$Y = \overline{A + B}$
XOR	$Y = A \oplus B$

Logic Diagram:

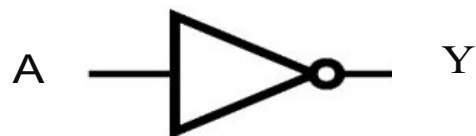
AND Gate:



OR Gate:



NOT Gate:



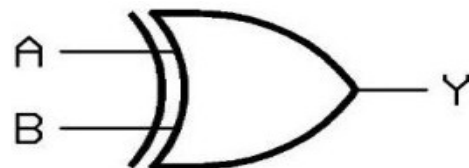
NAND Gate:



NOR Gate:

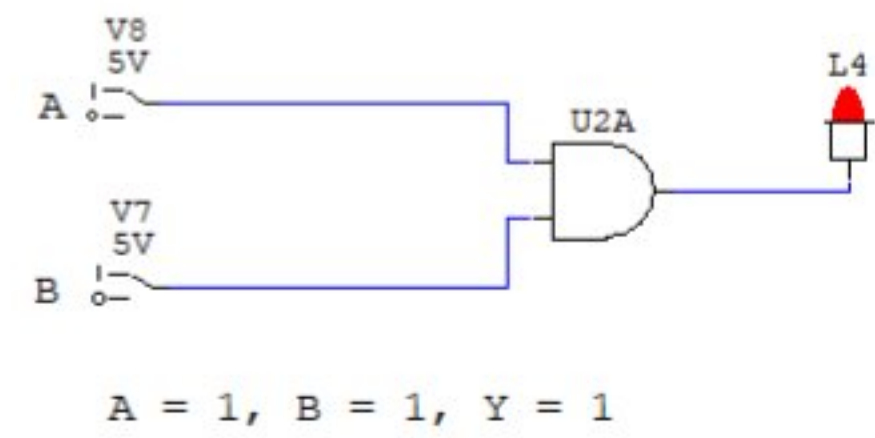
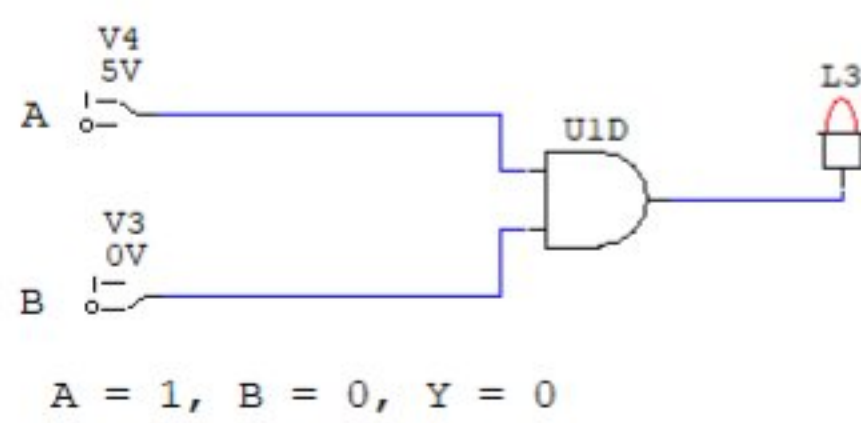
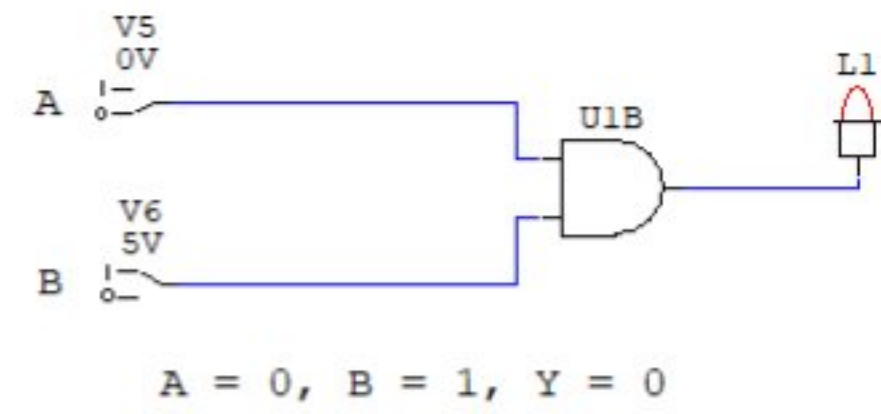
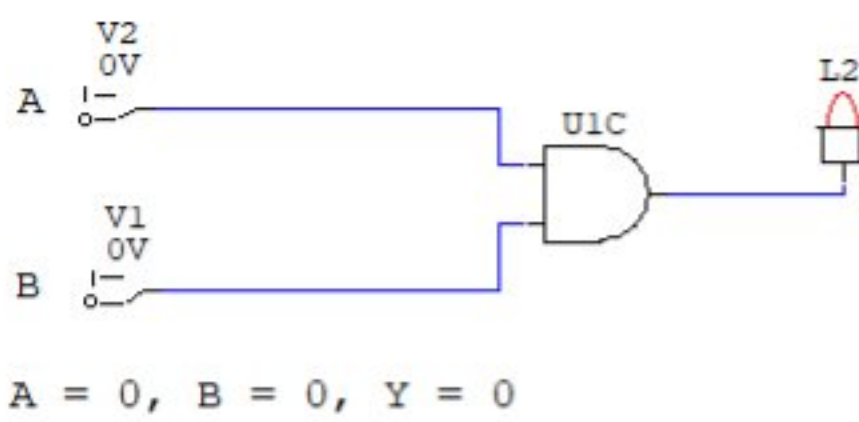


XOR Gate:

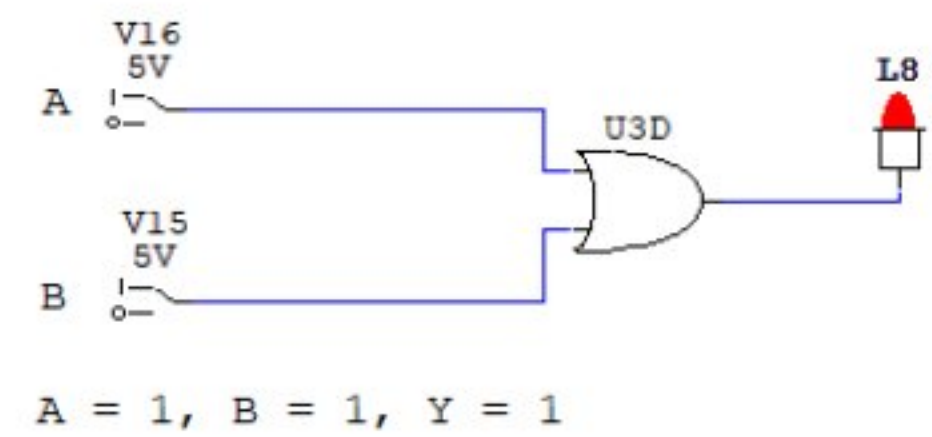
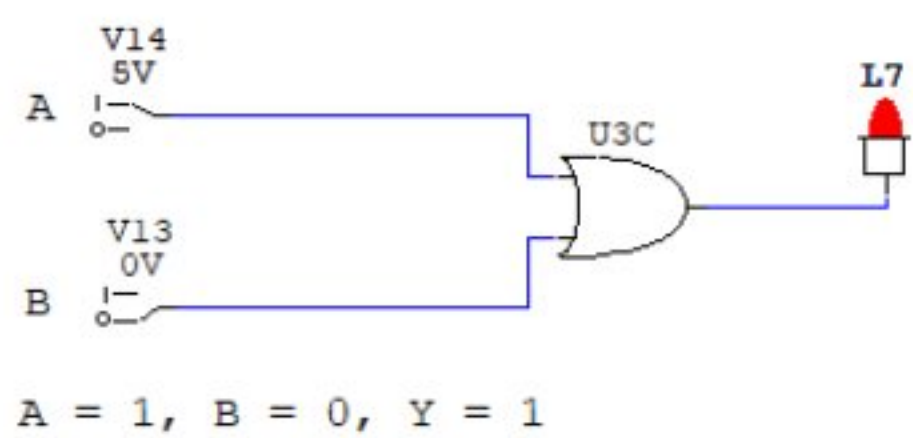
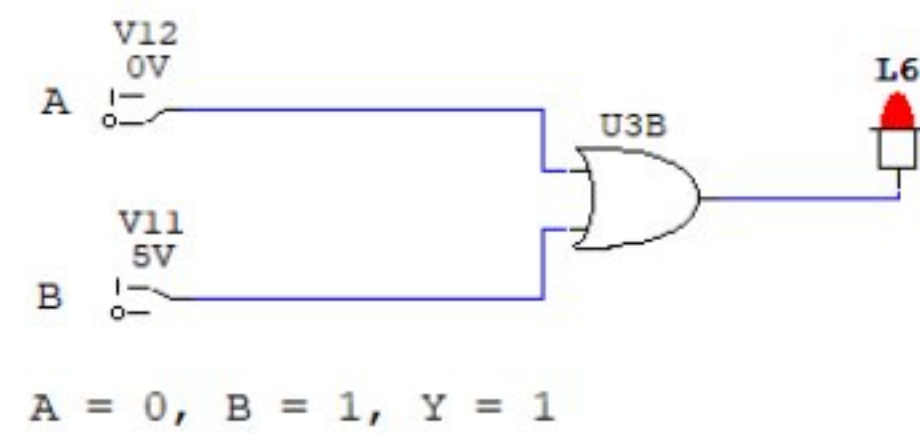
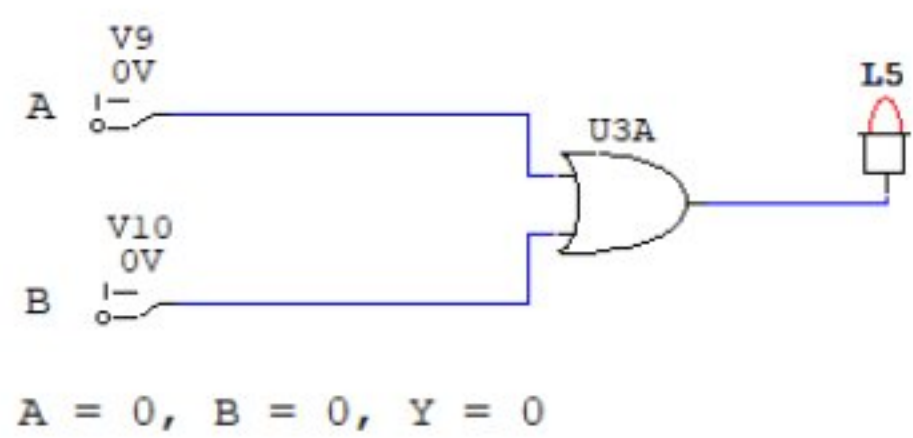


Circuit Diagram:

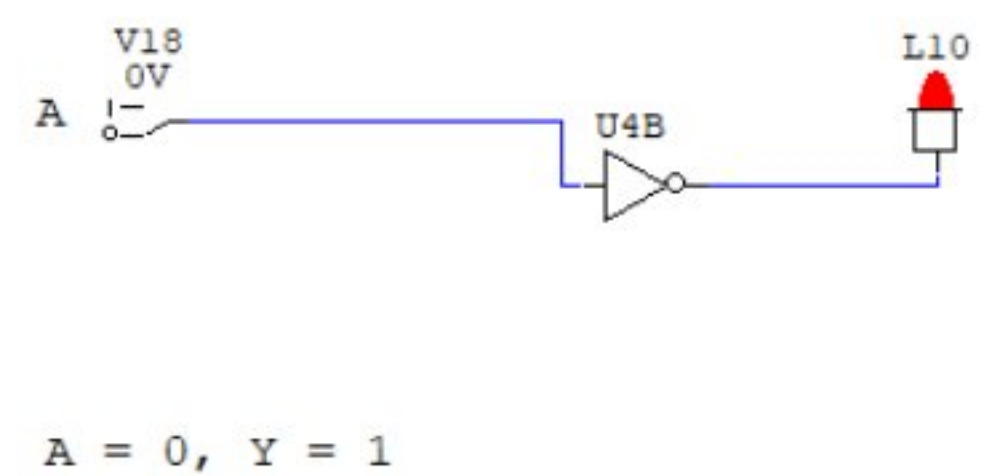
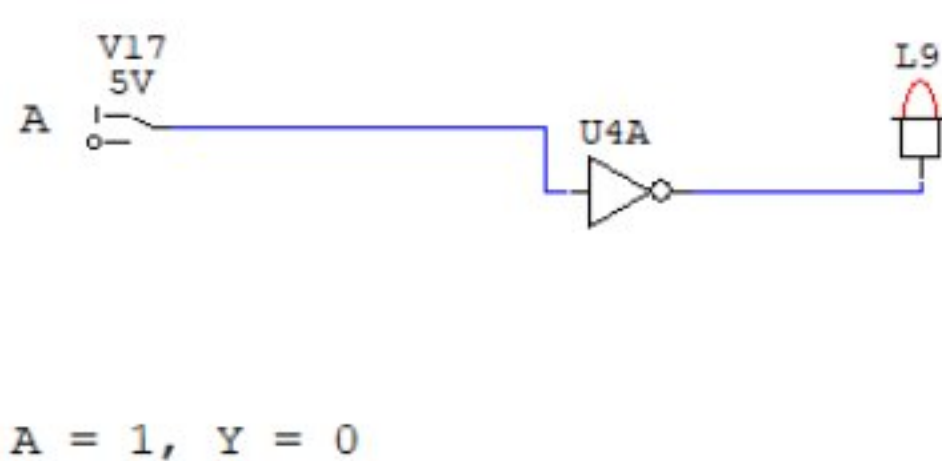
AND Gate:



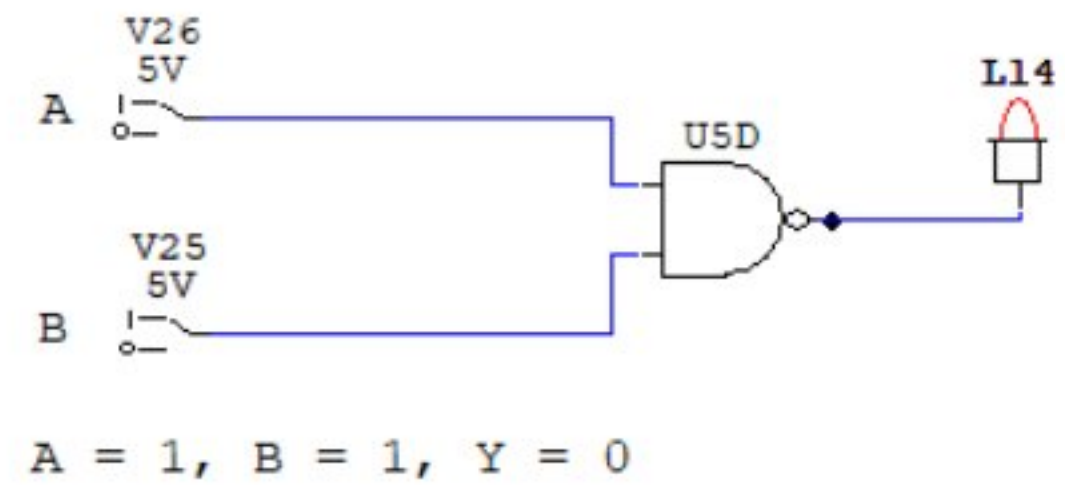
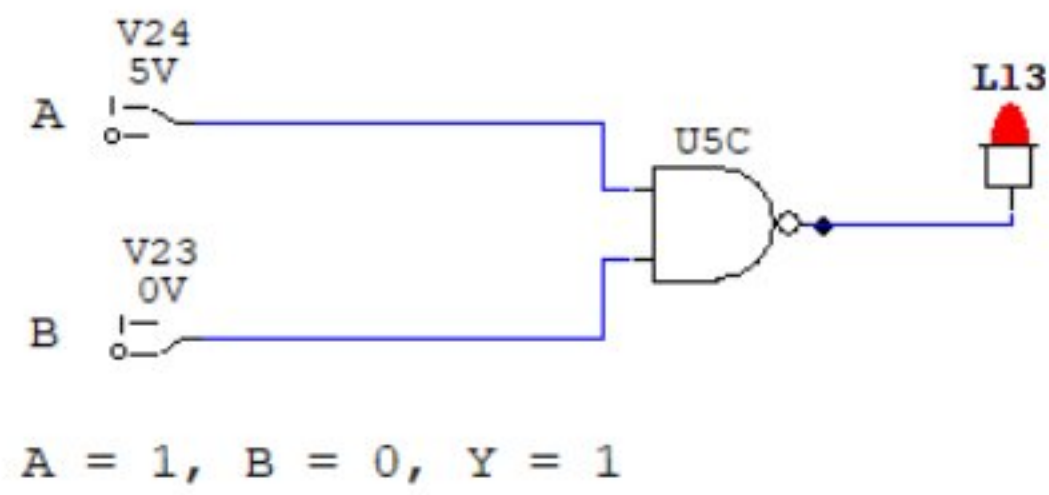
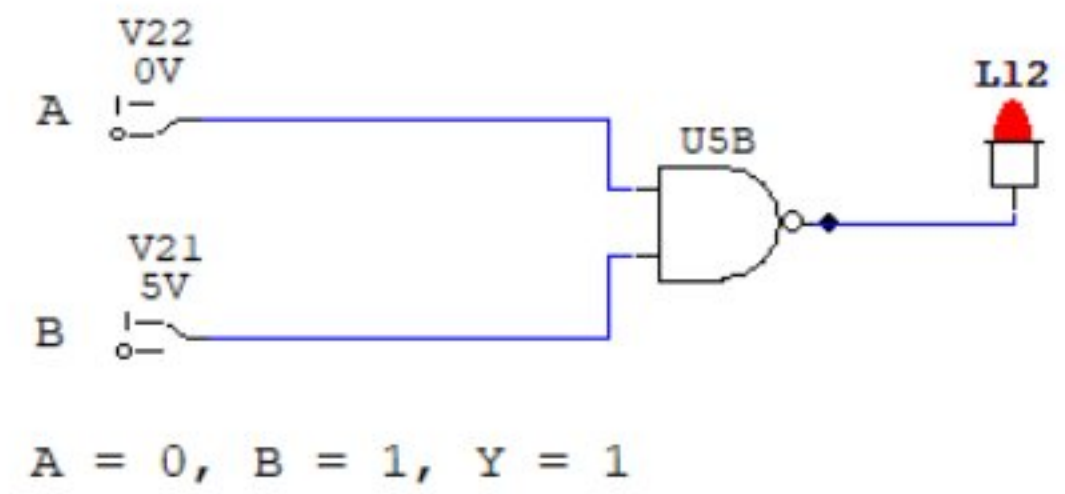
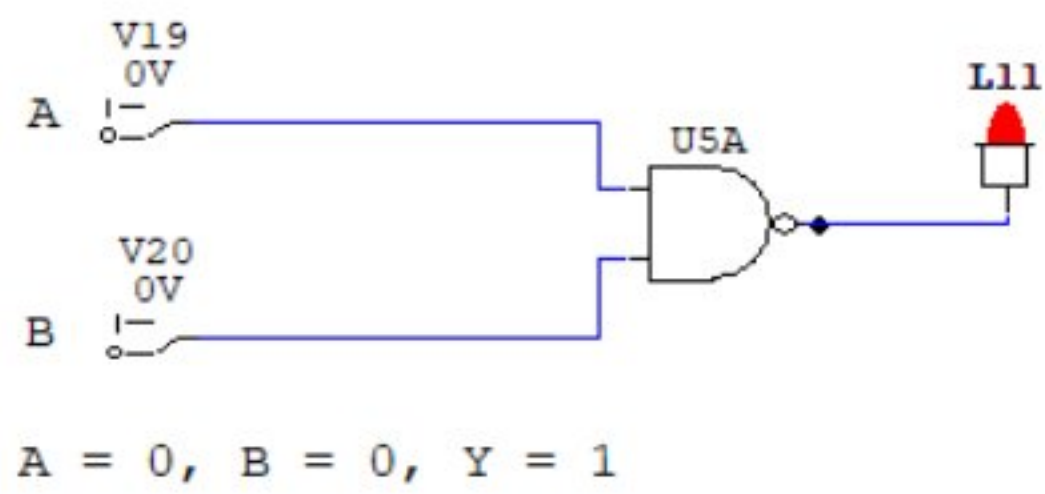
OR Gate:



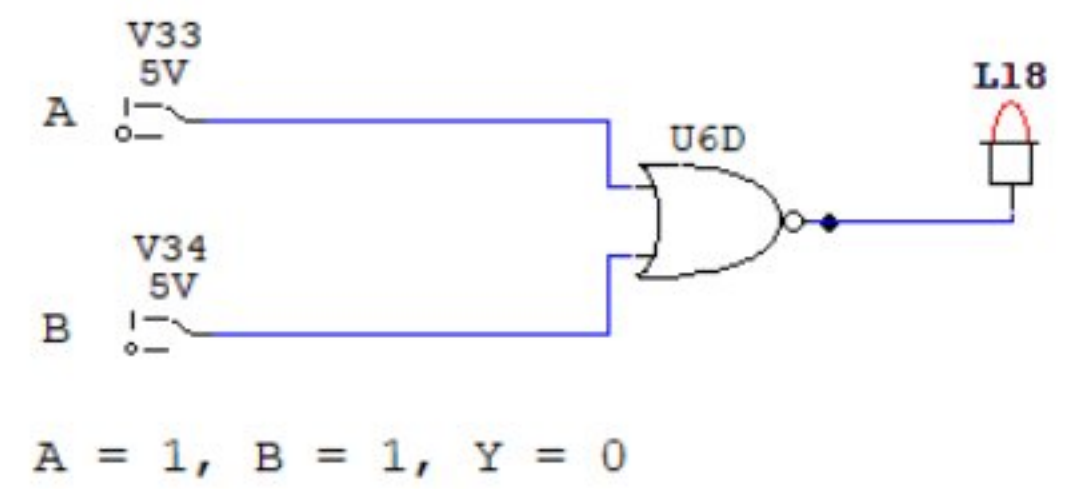
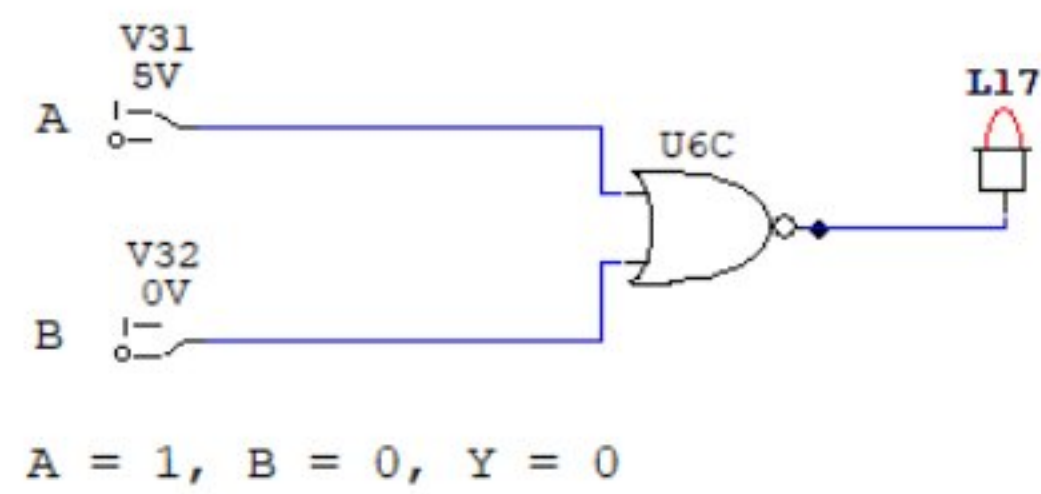
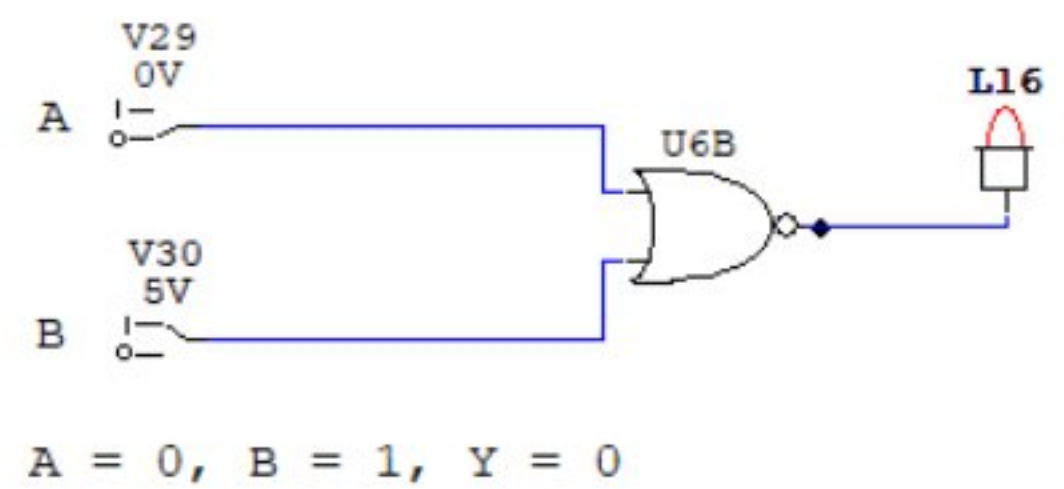
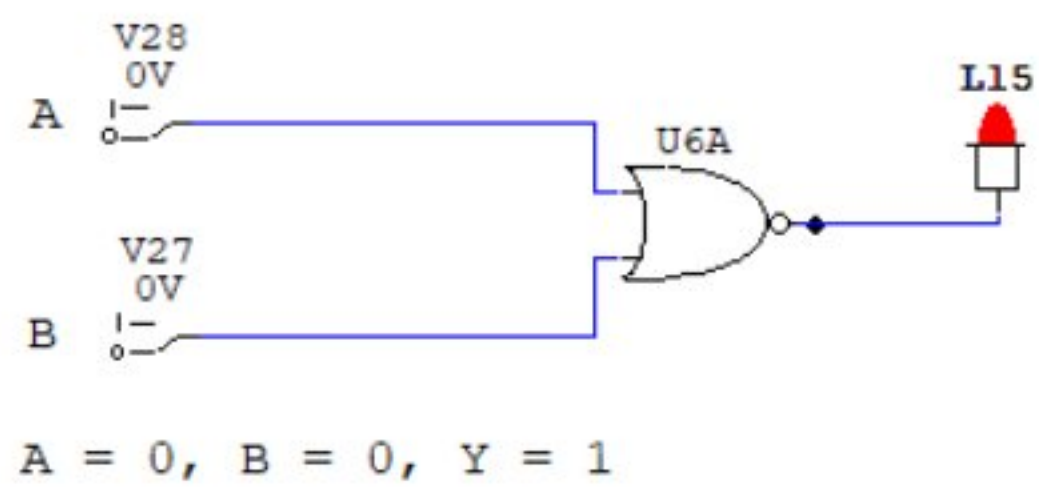
NOT Gate:



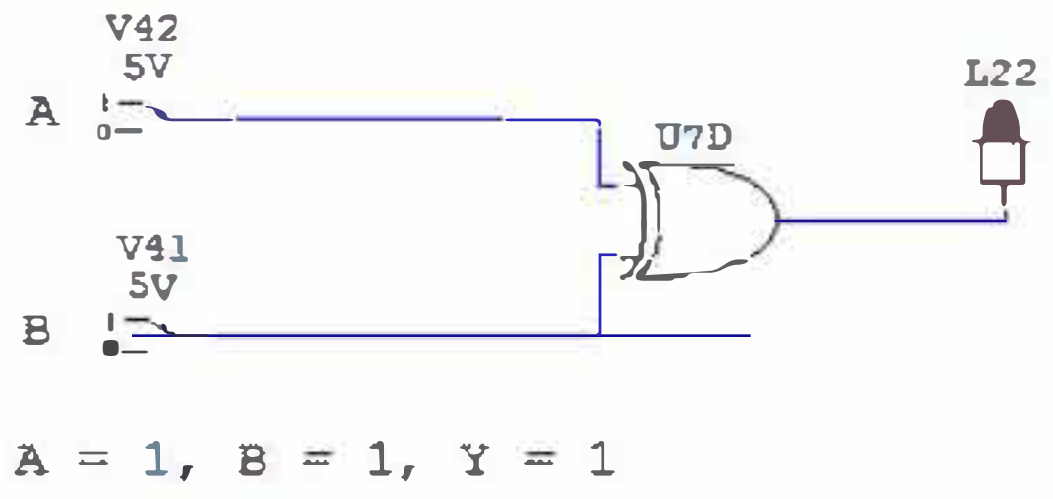
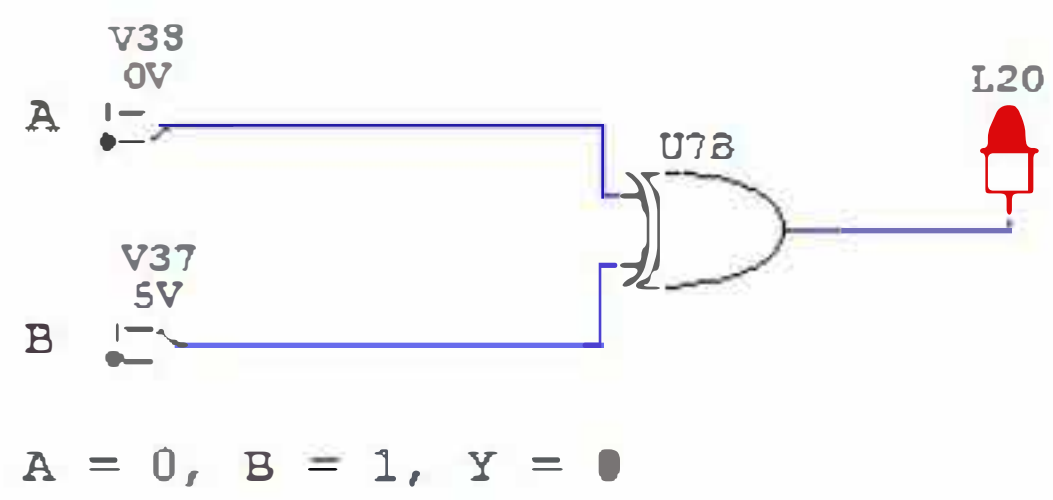
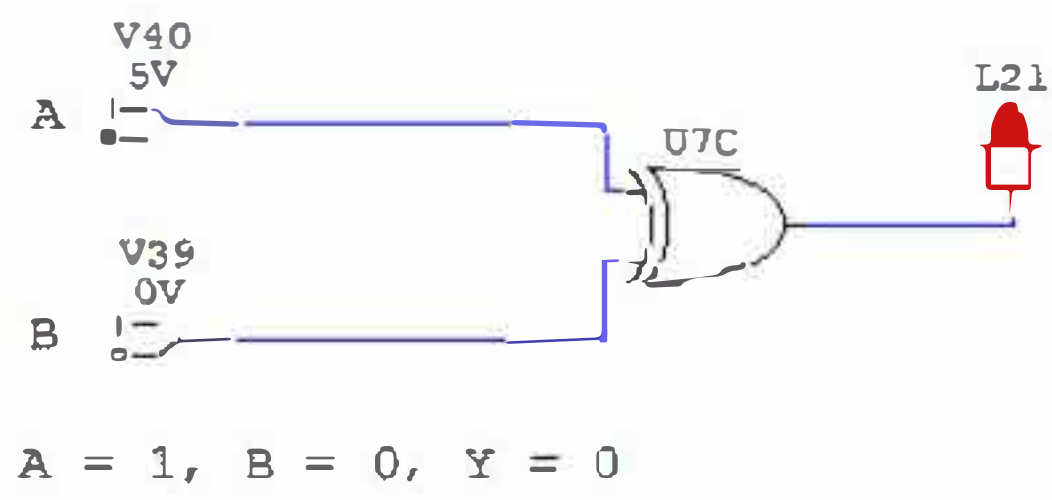
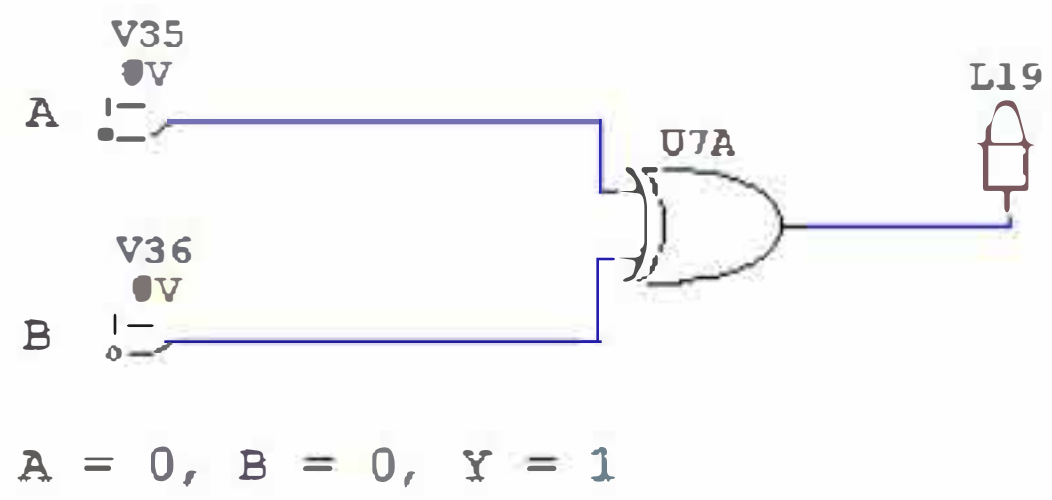
NAND Gate:



NOR Gate:



XOR Gate:



Pin Configurations-

AND GATE IC-7408

OR GATE IC-7432

NOT GATE IC-7404

NAND GATE IC-7400

NOR GATE IC-7402

XOR GATE IC-7486

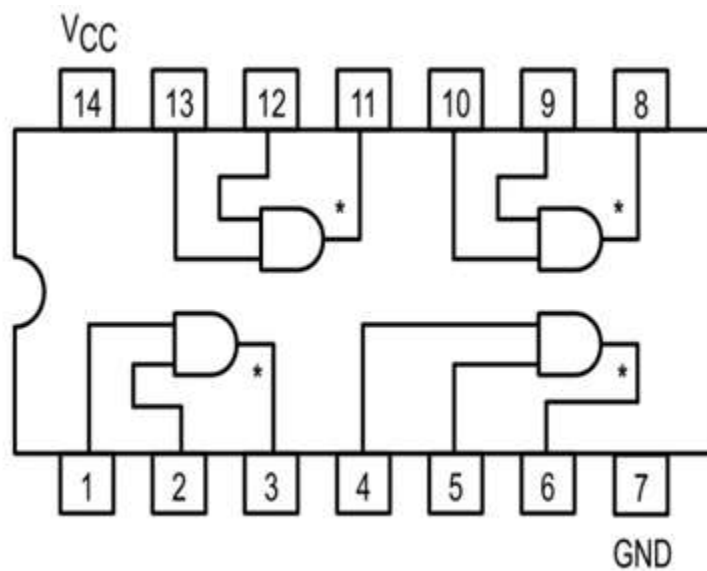


FIG 1: AND GATE

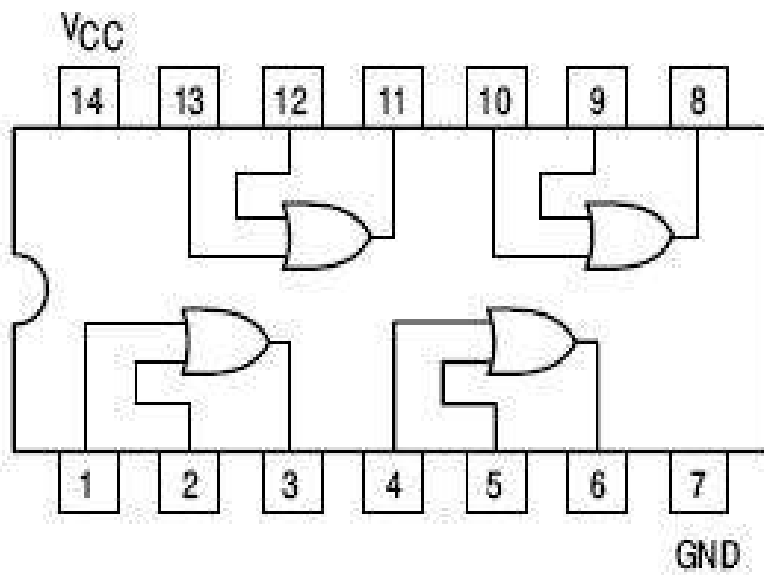


FIG 2: OR GATE

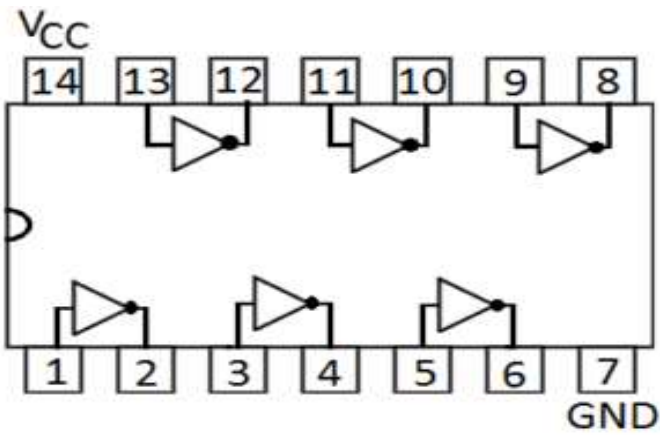


FIG 3: NOT GATE

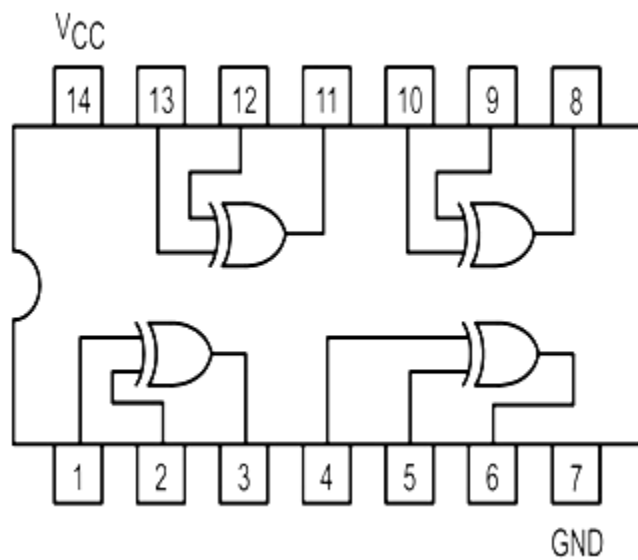


FIG 4: NAND GATE

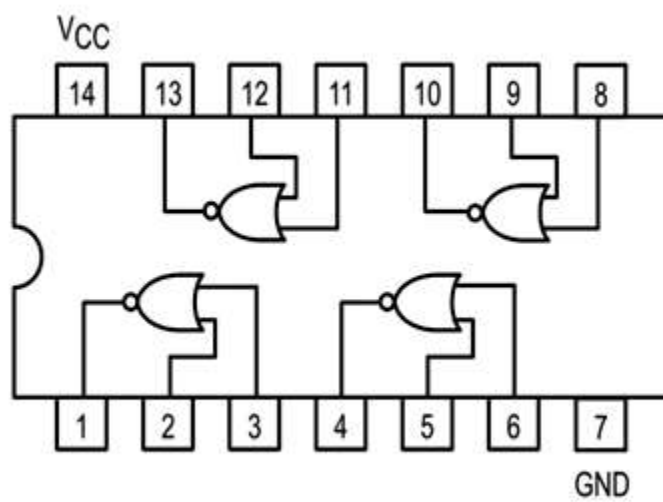


FIG 5: NOR GATE

