

UNIVERSITY OF ASIA PACIFIC

Department of Computer Science & Engineering

Course Title : Digital Logic & System Design Lab

Course Code : CSE 210

Experiment No. : 01

Experiment Name: Test and verify the truth table of following gates: AND gate, OR gate, NOT gate, NAND gate, NOR gate, Exclusive-OR gate.

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Submitted by: Submitted To:

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Problem Statement : Test and verify the truth table of following gates: AND gate, OR gate, NOT gate, NAND gate, NOR gate, Exclusive-OR gate.

Input & Output Variables Specification: We are using **A,B** as input and **Y** as output variable.

Truth Table:

AND Gate

Input		Output
A	В	Y
0	0	0
0	1	0
1	0	0
1	1	1

OR Gate

Input		Output
A	В	Y
0	0	0
0	1	1
1	0	1
1	1	1

NOT Gate

Input	Output
0	1
1	0

NAND Gate

Input		Output
Α	В	Y
0	0	1
0	1	1
1	0	1
1	1	0

NOR Gate

Input		Output
A	В	Y
0	0	1
0	1	0
1	0	0
1	1	0

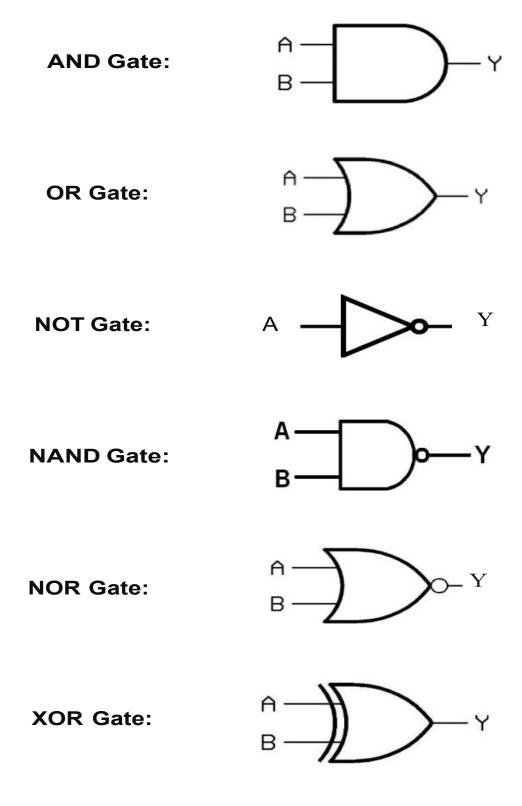
XOR Gate

Input		Output
A	В	Y
0	0	0
0	1	1
1	0	1
1	1	0

Logic Expression:

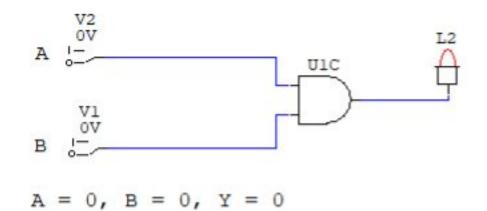
Logic Gate	Logic Expression
AND	Y = A . B
OR	Y = A + B
NOT	Y = A
NAND	Y = A . B
NOR	$Y = \overline{A + B}$
XOR	Y = A ⊕ B

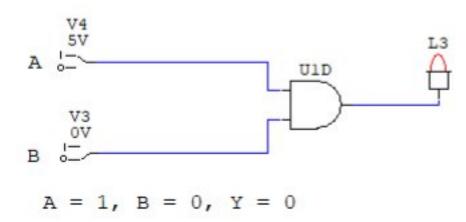
Logic Diagram:



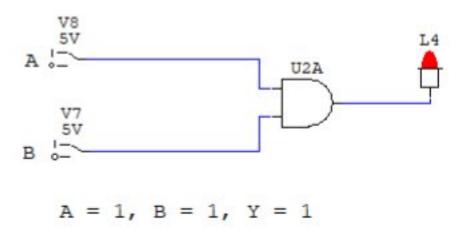
Circuit Diagram:

AND Gate:

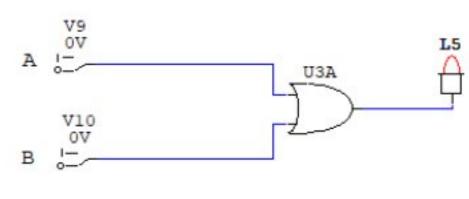




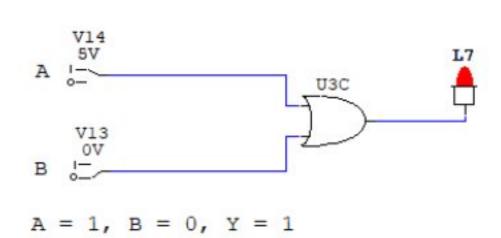
V6 5V В A = 0, B = 1, Y = 0

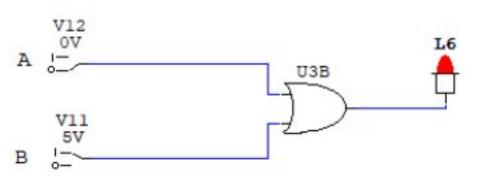


OR Gate:

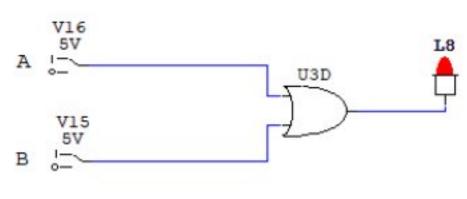


A = 0, B = 0, Y = 0



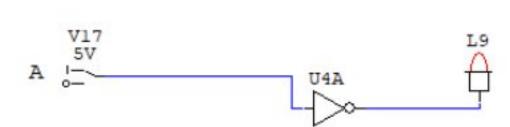


$$A = 0$$
, $B = 1$, $Y = 1$

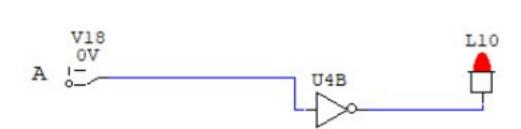


A = 1, B = 1, Y = 1

NOT Gate:

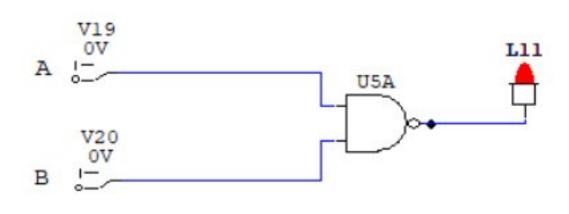


A = 1, Y = 0

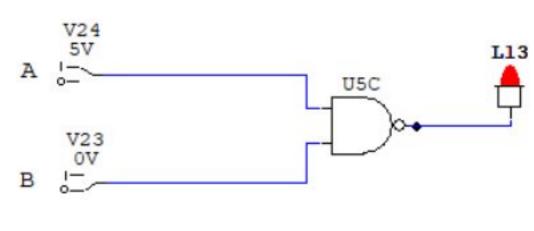


$$A = 0, Y = 1$$

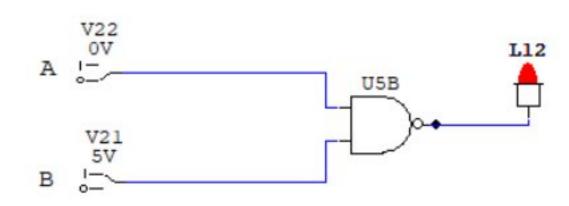
NAND Gate:



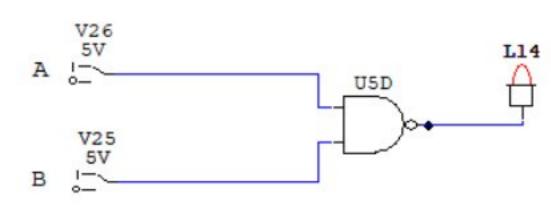
$$A = 0$$
, $B = 0$, $Y = 1$



A = 1, B = 0, Y = 1

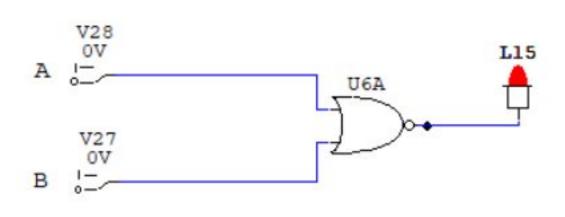


A = 0, B = 1, Y = 1

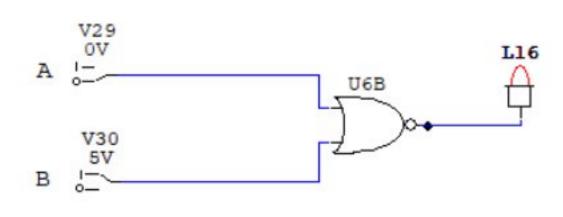


A = 1, B = 1, Y = 0

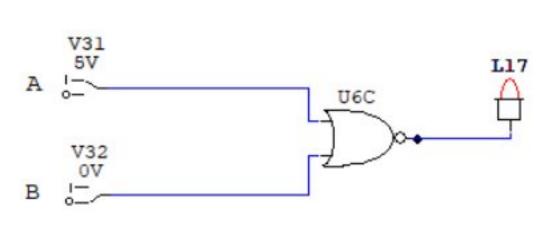
NOR Gate:



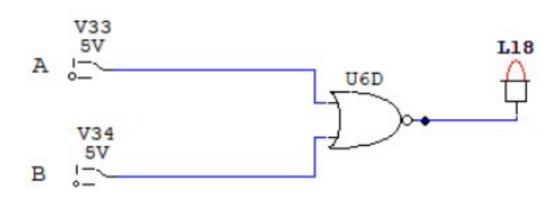
A = 0, B = 0, Y = 1



$$A = 0$$
, $B = 1$, $Y = 0$

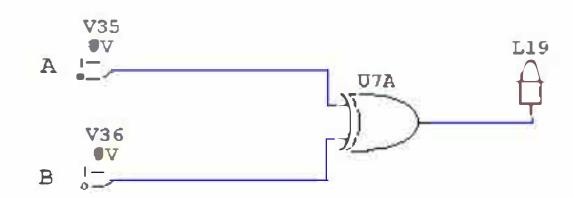


$$A = 1$$
, $B = 0$, $Y = 0$

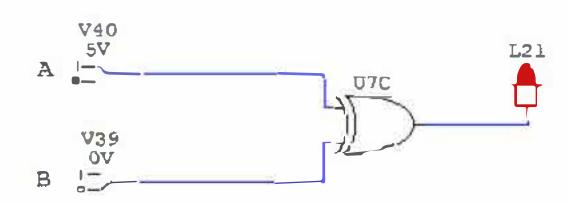


A = 1, B = 1, Y = 0

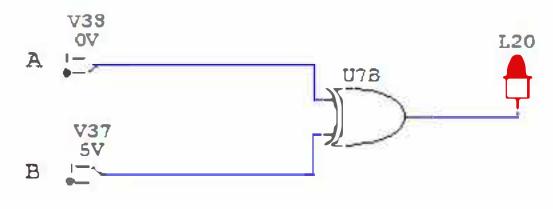
XOR Gate:



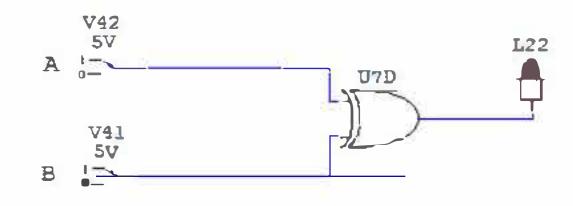
$$A = 0$$
, $B = 0$, $Y = 1$



A = 1, B = 0, Y = 0



A = 0, B = 1, Y = 0



A = 1, B = 1, Y = 1

Pin Configurations-

AND GATE IC-7408

OR GATE IC-7432

NOT GATE IC-7404

NAND GATE IC-7400

NOR GATE IC-7402

XOR GATE IC-7486

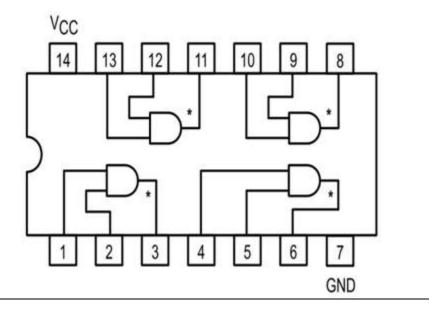


FIG 1: AND GATE

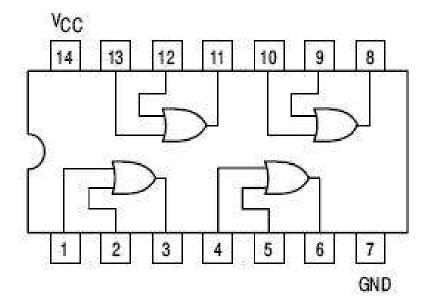


FIG 2: OR GATE

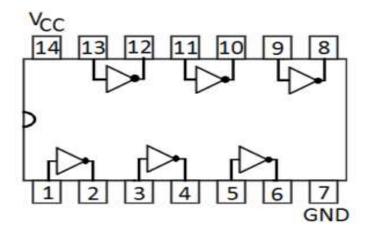


FIG 3: NOT GATE

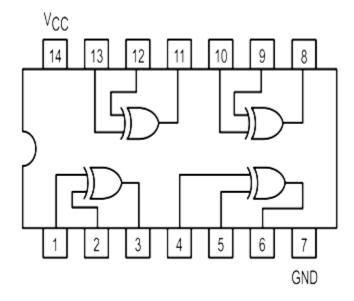


FIG 4: NAND GATE

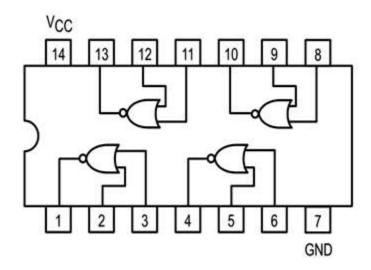


FIG 5: NOR GATE

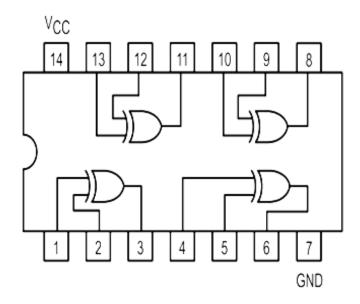


FIG 6: XOR GATE

Discussion:

From the above experiment, we learned about 3 basic gates(AND,OR,NOT) and 3 compound gates (NAND, NOR, XOR). We are representing "1" as High or 5V. and "0" as Low or 0V for input and output. Security protocols has been strictly maintained during the experiment. IC numbers were observed carefully. It can be said after drawing truth table, logical and circuit diagrams-

- 1. AND Gate: Output is HIGH when all inputs are **HIGH**
- 2. OR Gate: Output is HIGH when any input is **HIGH**
- 3. NOT Gate: Output is **REVERSE** to input
- 4. NAND Gate: Output is LOW when all inputs are **HIGH**
- 5. NOR Gate: Output is HIGH when all inputs are **LOW**
- 6. XOR Gate: Output is LOW when all inputs are **HIGH** or all inputs are **LOW**