(1) AND Gate:

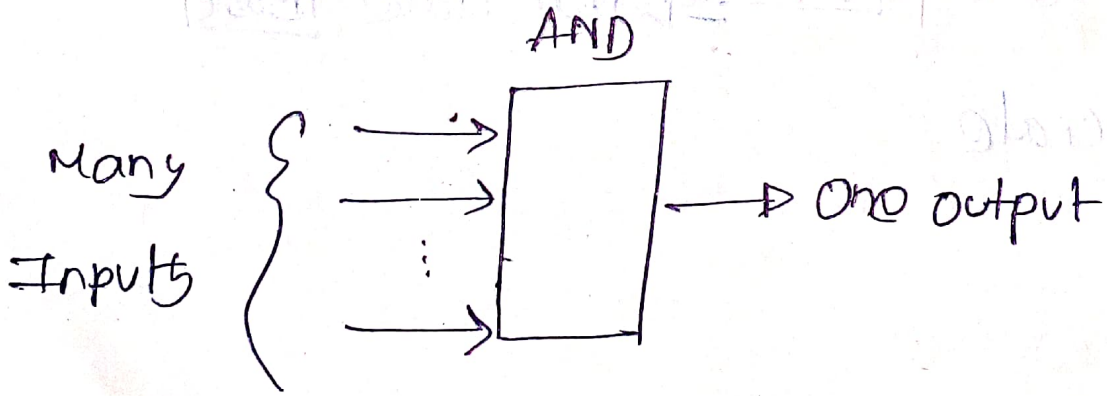
This gate is a device where there are many inputs but only one output.

And output will be high only when all the inputs are high [CAP]. Otherwise output will be low. [CAP]

HIGH → 1, T

[1, T, HIGH]

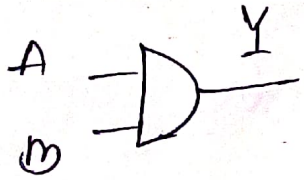
[0, F, LOW]



Truth Table:

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Symbol

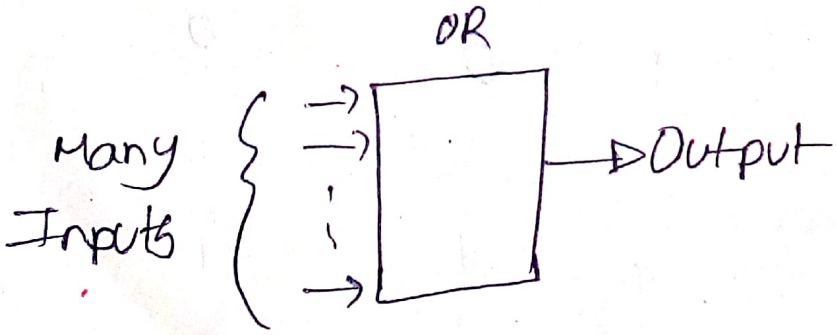


$Y = A \cdot B = AB$

2. OR Gate:

OR Gate is a device where there are many inputs and one output.

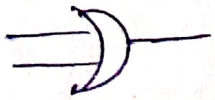
Output will be low only when all the input are LOW; otherwise output will be ~~LOW~~ HIGH.



Truth Table:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

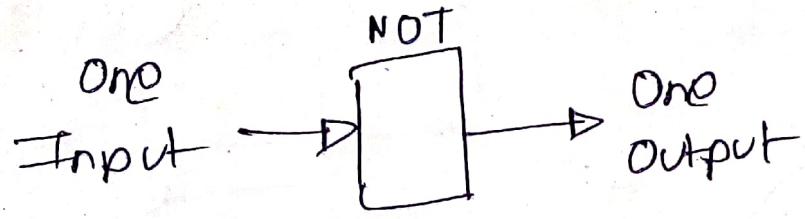
Symbol:



$Y = A + B$

3. NOT Gate: (Inverter)

One Input One Output

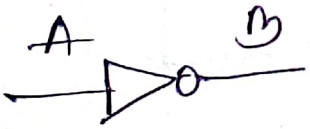


Output is opposite of Input.

Truth Table:

A	B
0	1
1	0

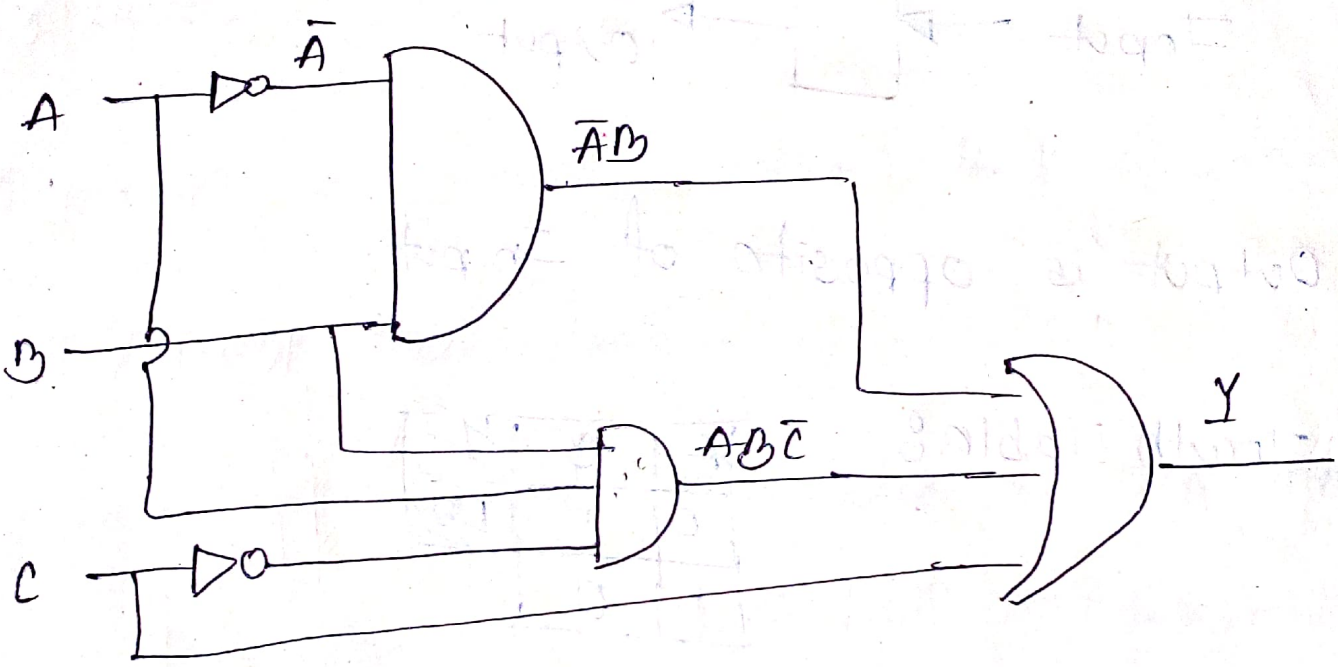
Symbol:



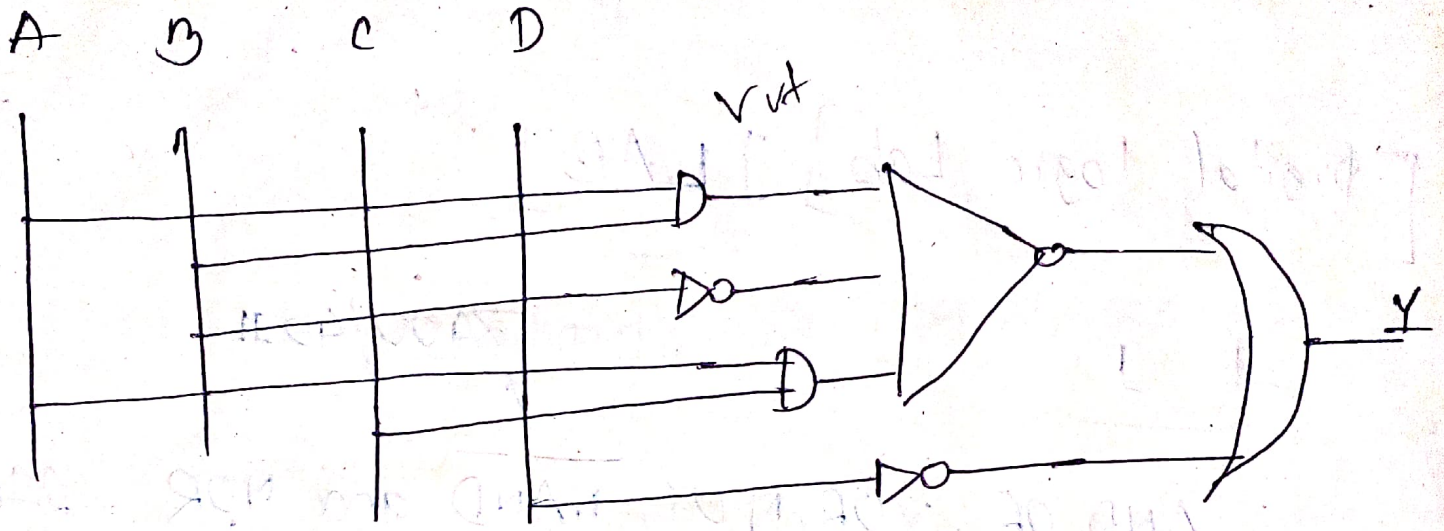
$B = \bar{A}$

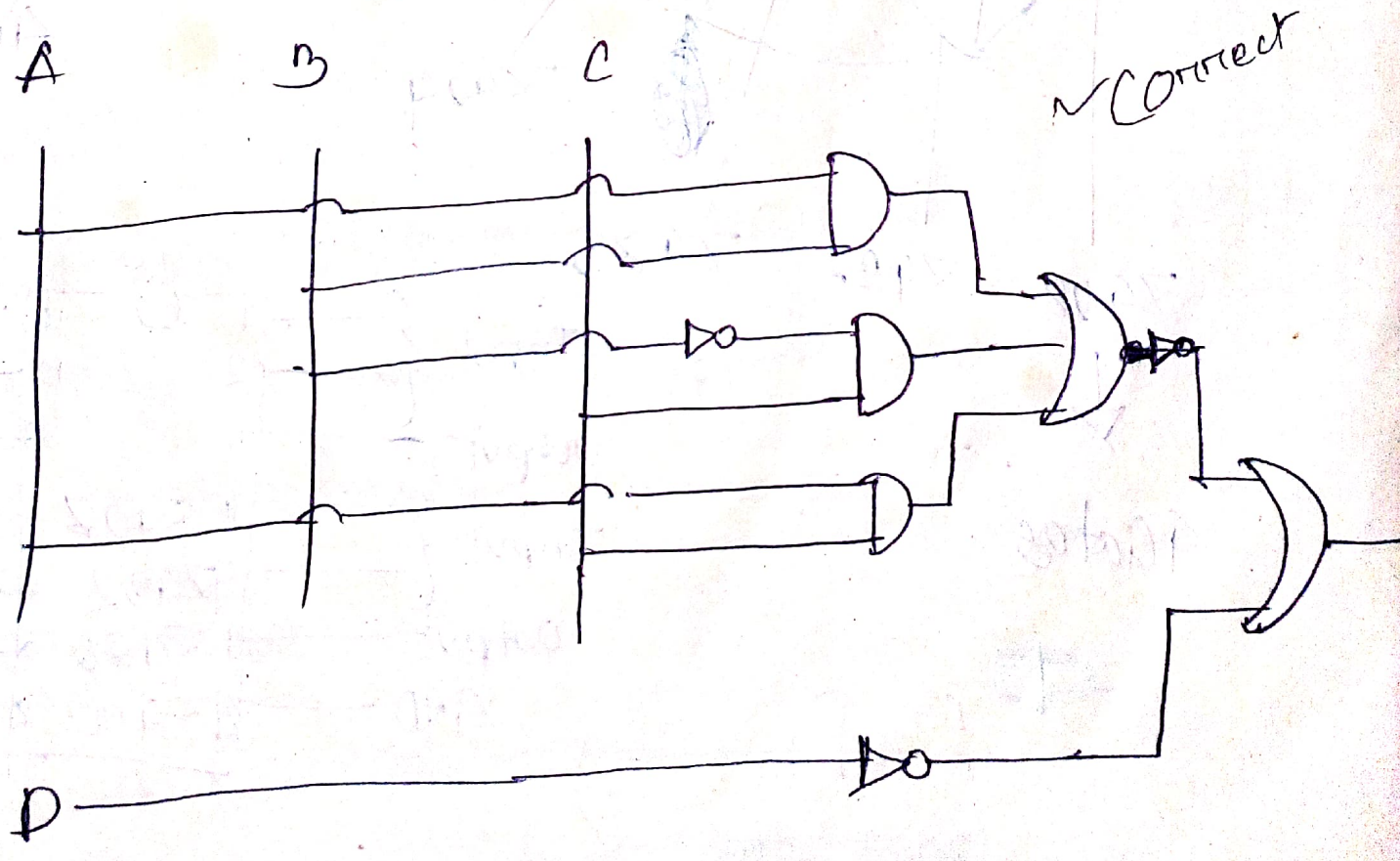
Draw the logic circuit of the following expression

$$Y = \bar{A}B + AB\bar{C} + C$$



$$Y = \overline{(AB + \bar{B}C + AC)} + \bar{D}$$

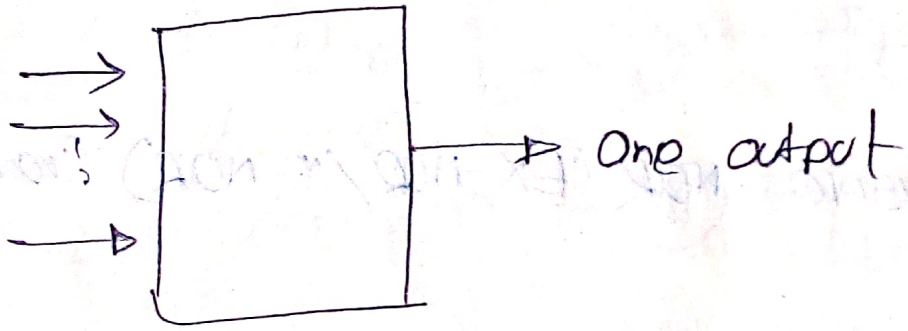




CSE -200 (Theory)

6.

Exclusive OR Gate: (Ex-OR) / (X-OR)

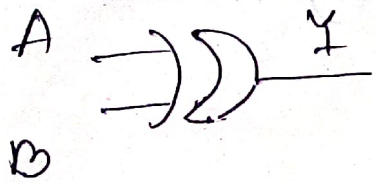


Ex-OR gate is a device, there are many inputs but only 1 output; and output will be low, when all the inputs are same; otherwise output will be high.

TT (Truth table):

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Symbol :



$Y = A \oplus B$

(7) Exclusive NOR (EX-NOR/X-NOR) Gate :

EX - NOR

It is a device where ~~are~~ many input, one output and output will be high when all the inputs are same, otherwise output will be low.

TT :

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Symbol :

$Y = \overline{A \oplus B}$

Boolean Algebra

▷ Don't care Input/Output এর উপর কোনো Allied পড়বে পড়বে না)

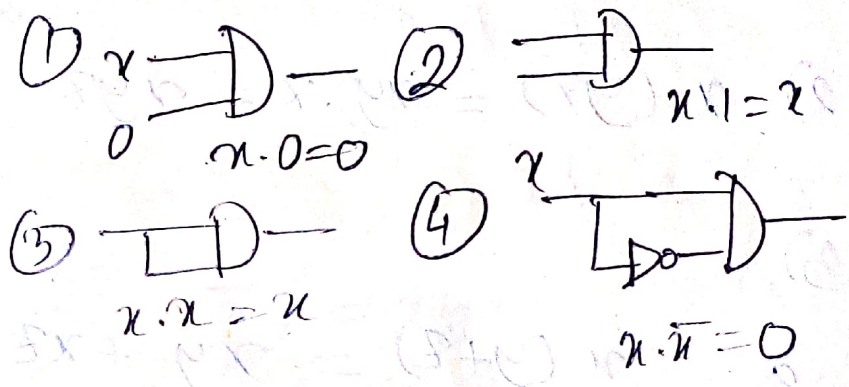
1) $x \cdot 0 = 0$

2) $x \cdot 1 = x$

3) $x \cdot x = x$

4) $x \cdot \bar{x} = 0$

AND



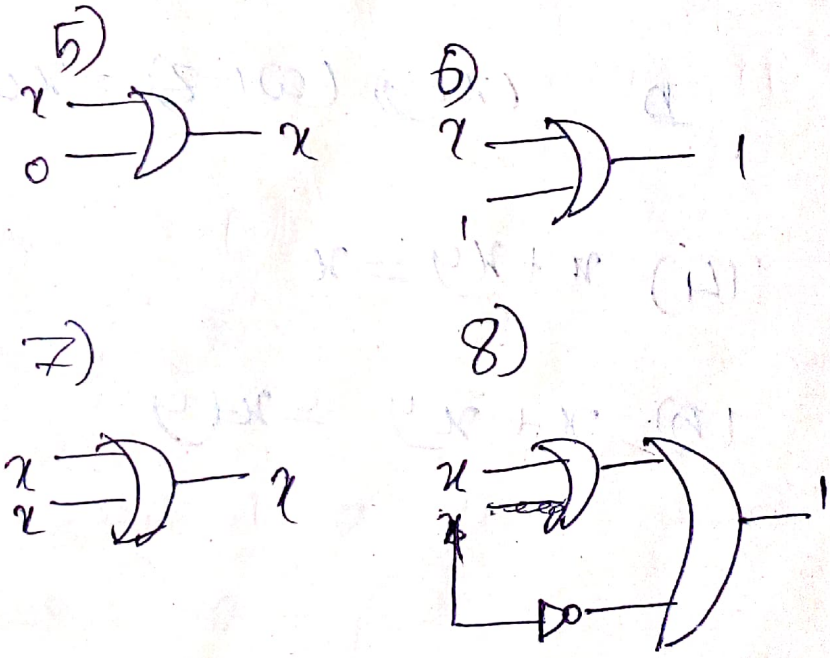
5) $x + 0 = x$

6) $x + 1 = 1$

7) $x + x = x$

8) $x + \bar{x} = 1$

OR



9) $x+y = y+x$

10) $x \cdot y = y \cdot x$

} commutative law

11) $x+(y+z) = (x+y)+z = x+y+z$

12) $x \cdot (yz) = (xy) \cdot z = xyz$

} Associative Law

13)

a $x(y+z) = xy + xz$

b $(x+y)(w+z) = xw + xz + yw + yz$

} Distributive law

14) $x + xy = x$

15). $x + \bar{x}y = x+y$

~~14)~~ 14) $x+xy$

$= x(1+y)$ → Distributive law

$=$

(15)

$x + \bar{x}y$

$= x + xy + \bar{x}y \quad = x + y(x+\bar{x})$

$\cancel{= x(1+y)} \quad = x + y$

(16) $\overline{x+y} = \bar{x}.\bar{y}$

(17) $\overline{xy} = \bar{x}\bar{y} + \bar{y}$ → De Morgan's law

→

$\boxed{16}$

x	y	$x+y$	$\overline{x+y}$	$\bar{x}$	$\bar{y}$	$\bar{x}.\bar{y}$
0	0	0	1	1	1	1
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	0

~~Simply~~

Simplification of Logic Expression:

(1) $y = A\bar{B}D + A\bar{B}\bar{D}$ → 8 logic gate

$= A\bar{B}(D+\bar{D})$

$= A\bar{B} \cdot 1 = A\bar{B}$

(2) $y = (\bar{A}+B)(A+B)$ → 4 logic gate

$= A \cdot \bar{A} + \bar{A}B + AB + B \cdot B$

$= 0 + \bar{A}B + AB + B$

$= B(\bar{A}+A+1)$

$= B$ → 0 logic gate.

(3) $Y = ACD + \bar{A}.BCD$ → logic gate

$= CD(A + \bar{A}B)$

$= CD.(A+B)$

~~$= ACD + ABCD$~~

(4) $Y = \overline{(\bar{A} + C).(B + \bar{D})}$

$= \overline{(\bar{A}+C)} \cdot \overline{(B+\bar{D})}$

$= \bar{\bar{A}} \cdot \bar{C} + \bar{B} \cdot \bar{D} = A\bar{C} + \bar{B} \cdot \bar{D}$

5.

$$Y = ABC + A\bar{B}\,\overline{(\bar{A}\cdot\bar{C})}$$

$$= ABC + A\bar{B}\,(A+C)$$

$$= ABC + \cancel{AB}\ \cancel{A\bar{B}C}\ A\bar{B}\,(A+C)$$

$$\cancel{= AC\,(B+\bar{B}) = AC}$$

$$= ABC + A\bar{B} + A\bar{B}C$$

$$= AC\,(BC + \bar{B} + \bar{B}C)$$

$$=$$

5.

$$Y = ABC + A\bar{B}(\bar{A} \cdot \bar{C})$$

$$= ABC + A\bar{B}(\bar{A} + \bar{C})$$

$$= ABC + A\bar{B} \cdot A + A\bar{B} \cdot C$$

$$= ABC + A\bar{B} + A\bar{B}C$$

$$= AC(B + \bar{B}) + A\bar{B}$$

$$= AC + A\bar{B} = A(C + \bar{B})$$

$\boxed{6}$

$Y = A\bar{B}\bar{C} + A\bar{B}C + ABC$

$= A\bar{B}(\bar{C} + C) + ABC$

$= A\bar{B} + ABC$

$= A(\bar{B} + BC)$ [using the law of absorption

$= A(\bar{B} + C)$ $\bar{A} + AB = \bar{A} + B$]

$= A\bar{B} + AC$ [4 2 1 Gate]

$\boxed{7}$

$Y = \bar{A}C\overline{(\bar{A}BD)} + \bar{A}B\bar{C}\bar{D} + A\bar{B}C$

$= \bar{A}C(\bar{\bar{A}} + \overline{BD}) + \bar{A}B\bar{C}\bar{D} + A\bar{B}C$ [$\because \overline{AB} = \bar{A} + \bar{B}$]

$= \bar{A}C(A + \bar{B} + \bar{D}) + \bar{A}B\bar{C}\bar{D} + A\bar{B}C$ [$\because \overline{AB} = \bar{A} + \bar{B}$]

$= \bar{A} \cdot AC + \bar{A}\bar{B}C + \bar{A}C\bar{D} + \bar{A}B\bar{C}\bar{D} + A\bar{B}C$

$= 0 + \bar{A}\bar{B}C + A\bar{B}C + \bar{A}C\bar{D} + \bar{A}B\bar{C}\bar{D}$ [$\because \bar{A} \cdot A = 0$]

$= C\bar{B}(A+\bar{A}) + \bar{A}\bar{D}(C+B\bar{C})$

$= C\bar{B}\cdot 1 + \bar{A}\bar{D}(B+C)$ $[\because A+\bar{A}B = A+B]$

$= C\bar{B} + \bar{A}B\bar{D} + \bar{A}C\bar{D}$ [12th gate]

$\boxed{8}$

$Y = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$

$= \bar{A}BC + ABC + A\bar{B}C + AB\bar{C}$

$= BC(\bar{A}+A) + A\bar{B}C + AB\bar{C}$

$= BC\cdot 1 + A\bar{B}C + AB\bar{C}$ $[\because \bar{A}+A=1]$

$= C(B+A\bar{B}) + AB\bar{C}$

$= C(A+B) + AB\bar{C}$ $[\because A+\bar{A}B = A+B]$

$= AC + BC + AB\bar{C}$

$= AC + B(C+A\bar{C})$

$= AC + B(A+C)$ [$\because A + \bar{A}B = A+B$]

$= AC + AB + CB$ [5वाँ gate]

13-01-21

Design the logic circuit from given truth table

Sum of Product form:

A	B	C	Y	
0	0	0	1	$\rightarrow \bar{A}\bar{B}\bar{C}$
0	0	1	1	$\rightarrow \bar{A}\bar{B}C$
0	1	0	0	$\rightarrow \boxed{\bar{A}B\bar{C}}$
0	1	1	0	$\rightarrow \boxed{\bar{A}BC}$
1	0	0	1	$\rightarrow A\bar{B}\bar{C}$
1	0	1	1	$\rightarrow A\bar{B}C$
1	1	0	1	$\rightarrow AB\bar{C}$
1	1	1	1	$\rightarrow ABC$

$\cancel{Y = \bar{A}BC + A\bar{B}C}$

$\cancel{+ \bar{A}B\bar{C} + A\bar{B}C}$

$$Y = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C} + A\bar{B}C + AB\bar{C} + ABC$$

$$= \bar{A}\bar{B}(\bar{C}+C) + \bar{A}\bar{B}(A\bar{C}+C) + AB(\bar{C}+C)$$

$$= \bar{A}\bar{B} + \bar{B}(C+A) + AB$$

$$= \bar{A}\bar{B} + A\bar{B} + C\bar{B} + AB$$

$$= \bar{B}(A+\bar{A}) + C\bar{B} + AB$$

$$= \bar{B} + AB + C\bar{B}$$

$$Y = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C} + A\bar{B}C + AB\bar{C} + ABC$$

$$= \bar{A}\bar{B}(\bar{C}+C) + A\bar{B}(\bar{C}+C) + AB(\bar{C}+C)$$

$$= \bar{A}\bar{B} + A\bar{B} + AB$$

$$= \bar{A}\bar{B} + AC = A + \bar{B}$$

A	B	C	Y	
0	0	0	1	$\bar{A}\bar{B}\bar{C}$
0	0	1	1	$\bar{A}\bar{B}C$
0	1	0	1	$\bar{A}B\bar{C}$
0	1	1	1	$\bar{A}BC$
1	0	0	0	
1	0	1	0	
1	1	0	0	
1	1	1	1	ABC

$$Y = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} + \bar{A}BC + ABC$$

$$\cancel{= \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}}$$

$$= \bar{A}\bar{B}(C+\bar{C}) + \bar{A}B\bar{C} + BC(A+\bar{A})$$

$$= \bar{A}\bar{B} + \bar{A}B\bar{C} + BC$$

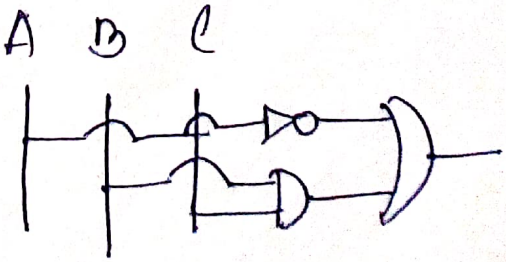
$$= \bar{A}\bar{B} + B(C + \bar{A}\bar{C})$$

$$= \bar{A}\bar{B} + B(C+\bar{A})$$

$$= \bar{A}\bar{B} + BC + \bar{A}B$$

$$= \bar{A}(B+\bar{B}) + BC$$

$$= \bar{A} + BC$$



EX-OR gate

A	B	Y	
0	0	0	
0	1	1	$\rightarrow \bar{A}B$
1	0	1	$\rightarrow A\bar{B}$
1	1	0	

Ex-NOR

Y	
1	$\bar{A}\bar{B}$
0	
0	
1	AB

$Y = A \oplus B$; $Y = \bar{A}B + A\bar{B}$

$\therefore$ $\boxed{A \oplus B = \bar{A}B + A\bar{B}}$

Save 4 logic gates

$\boxed{Y = \overline{A \oplus B} = \bar{A}\bar{B} + AB}$

Save 4 logic gates

Example:

Design the logic circuits from a given statement.

(1) Suppose A B C are inputs and Y is the output. Y will be high [CAP], when majority of inputs are high [CAP]. Design the circuit.

Step: 1 (TT)

A	B	C	Y	
0	0	0	0	
0	0	1	0	
0	1	0	0	
0	1	1	1	$\bar{A}BC$
1	0	0	0	
1	0	1	1	$A\bar{B}C$
1	1	0	1	$AB\bar{C}$
1	1	1	1	ABC

Step 2: Simplification

$Y = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$

$\cancel{= \bar{A}BC +}$

$= \bar{A}BC + A\bar{B}C + AB(C+\bar{C})$

$= \bar{A}BC + A\bar{B}C + AB$

$= \bar{A}BC + A(B + \bar{B}C)$

$= \bar{A}BC + AB + AC$

$= B(A + \bar{A}C) + AC$

$\cancel{= AB + AC + A2AC}$

$\cancel{= B(A+C)}$

$= AB + CB + AC$

16/01/2022

② A, B, C are inputs and Y is the output. Output Y will be HIGH when majority of inputs are LOW. Design the circuit.

Step-1

A	B	C	Y	
0	0	0	1	$\bar{A}\bar{B}\bar{C}$
0	0	1	1	$\bar{A}\bar{B}C$
0	1	0	1	$\bar{A}B\bar{C}$
0	1	1	0	~~$\bar{A}BC$~~
1	0	0	1	$A\bar{B}\bar{C}$
1	0	1	0	
1	1	0	0	
1	1	1	0	

Step-2

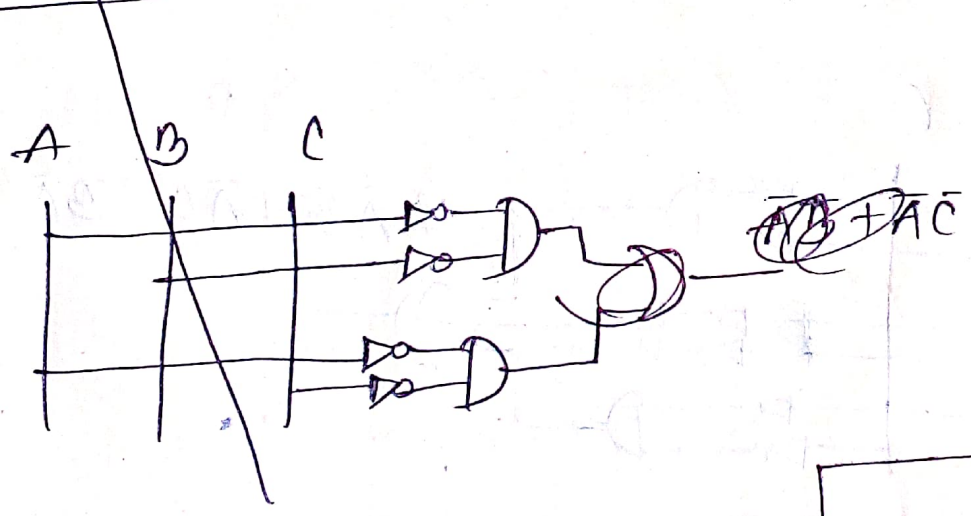
$$\bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C}$$

$$= \bar{A}\bar{B}(\bar{C}+C) + \bar{C}(\bar{A}B + A\bar{B})$$

$$= \bar{A}\bar{B} + \bar{C}(A \oplus B)$$

$$= \bar{A}\bar{B} +$$

Step-3



Step-3

$$\bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C}$$

$$= \bar{A}\bar{B} + \bar{A}B\bar{C} + A\bar{B}\bar{C}$$

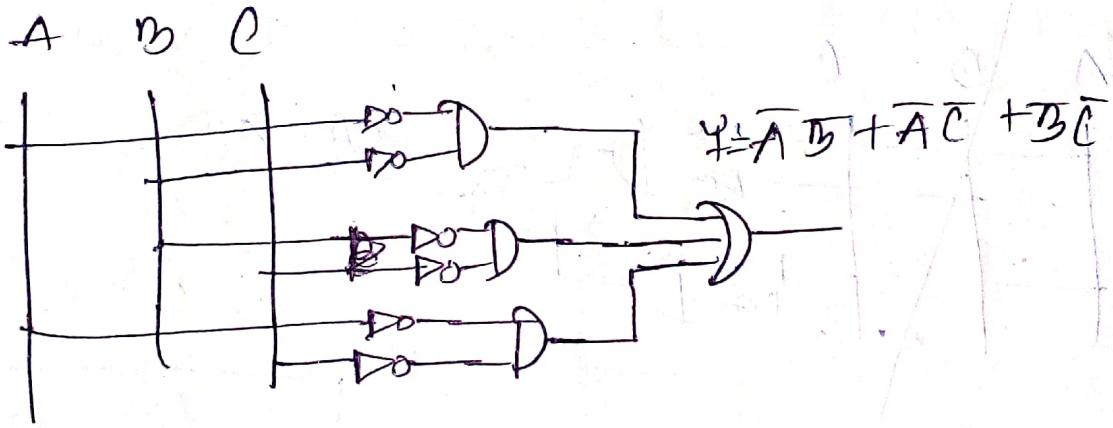
$$= \bar{A}(\bar{B} + B\bar{C}) + A\bar{B}\bar{C}$$

$= \bar{A}(\bar{B}+\bar{C}) + A\bar{B}\bar{C}$

$= \bar{A}\bar{B} + \bar{A}\bar{C} + A\bar{B}\bar{C}$

$= \bar{A}\bar{B} + \bar{A}\bar{C} + \bar{B}\bar{C}$

Step-3



③ A, B, C are inputs and X is the output X will equal to A, when B and C are same. X remain HIGH, when B and C are different. Design the circuit.

Step-1

A	B	C	X	
0	0	0	0	
0	0	1	1	$\bar{A}\bar{B}C$
0	1	0	1	$\bar{A}B\bar{C}$
0	1	1	0	
1	0	0	1	$A\bar{B}\bar{C}$
1	0	1	1	$A\bar{B}C$
1	1	0	1	$AB\bar{C}$
1	1	1	1	ABC

Step-2

$\bar{A}\bar{B}C + A\bar{B}\bar{C} + A\bar{B}\bar{C} + A\bar{B}C + AB\bar{C} + ABC$

$\cancel{= \bar{A}B\bar{C} + \bar{A}B\bar{C} + AB\bar{C} + \bar{A}\bar{B}C + ABC + AB\bar{C} + ABC}$

$\cancel{= \bar{A}\bar{C}(B+\bar{B}) + \bar{A}\bar{B}C}$

$= \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + AB\bar{C} + AB(\bar{C}+C)$

$= \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}(\bar{C}+C) + AB$

$= \bar{A}\bar{B}C + \bar{A}B\bar{C} \cancel{+ A\bar{B} + AB}$

$= A\bar{B} + \bar{A}\bar{B}C + AB + \bar{A}B\bar{C}$

$= \bar{B}(A+\bar{A}C) + B(A+\bar{A}\bar{C})$

$= \bar{B}(A+C) + B(A+\bar{C})$

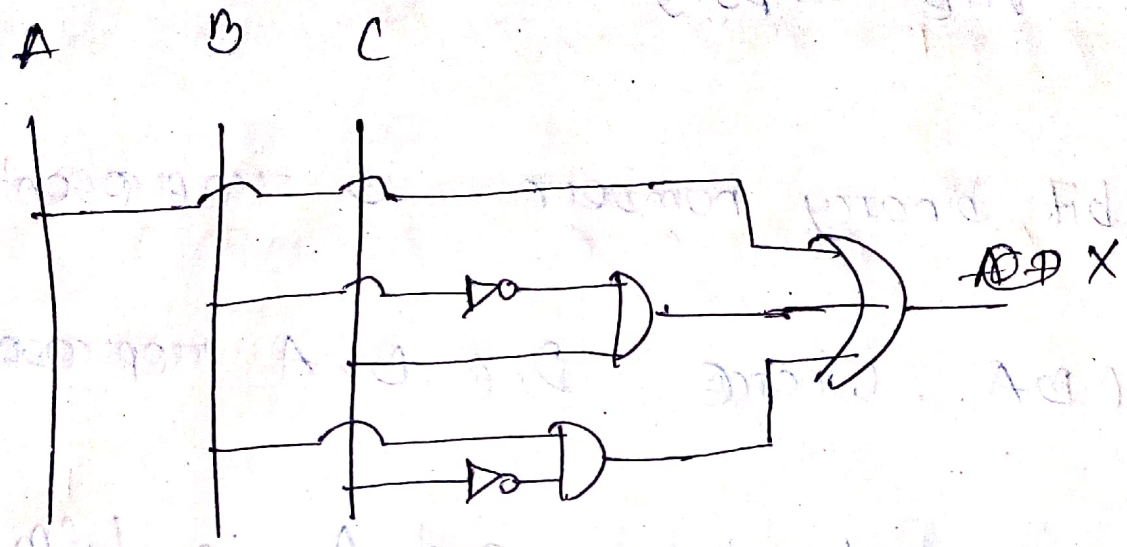
$= A\bar{B} + \bar{B}C + AB + B\bar{C}$

$= A(\bar{B}+B) + \bar{B}C + B\bar{C}$

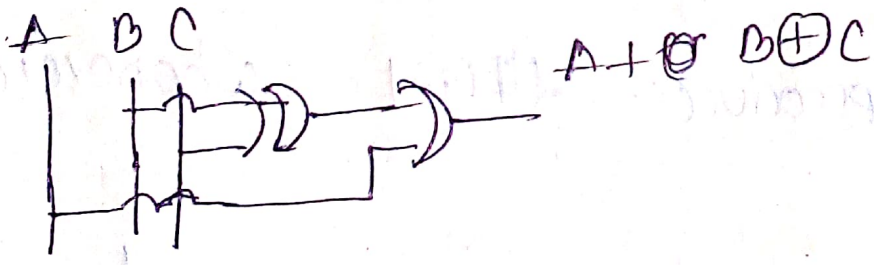
$= A + \bar{B}C + B\bar{C}$

$= A + B \oplus C$

Step-3



or



[9]

~~A, B, C are inputs~~

A 4bit binary number is represented as DCBA. Where D, C, B, A represents the individual bits and A is LSB, D is MSB. Design a logic circuit that will produce HIGH whenever the binary number is greater than 3_{10} and less than 10_{10}.

D	C	B	A		
0	0	0	0		
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0	1	$\cancel{\bar{A}B\bar{C}\bar{D}}$
0	1	0	1	1	$\cancel{\bar{A}B\bar{C}\bar{D}}$
0	1	1	0	1	$\cancel{\bar{A}B\bar{C}\bar{D}}$
0	1	1	1	1	$\cancel{\bar{A}BCD}$
1	0	0	0	1	$\cancel{A\bar{B}\bar{C}\bar{D}}$
1	0	0	1	1	$\cancel{A\bar{B}\bar{C}D}$
1	0	1	0		
1	0	1	1		
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		

$\cancel{= \bar{A}\bar{B}\bar{C}\bar{D} + A\bar{B}C\bar{D} + \bar{A}B\bar{C}\bar{D} + ABCD}$

$Y =$

$\bar{A}\bar{B}C\bar{D} + A\bar{B}C\bar{D} + \bar{A}BC\bar{D} + ABC\bar{D} + \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{C}D$

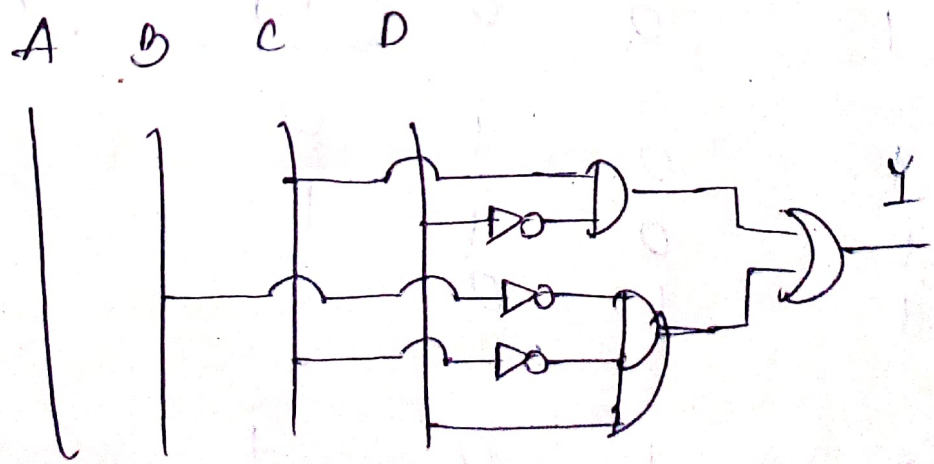
$= \bar{B}C\bar{D}(\bar{A}+A) + BC\bar{D}(\bar{A}+A) + \bar{B}\bar{C}D(\bar{A}+A)$

$= \bar{B}C\bar{D} + BC\bar{D} + \bar{B}\bar{C}D$

$= C\bar{D}(\bar{B}+B) + \bar{B}\bar{C}D$

$= C\bar{D} + \bar{B}\bar{C}D$

Step-3



5 A, B, C, D → inputs

Y → Output

Y is HIGH when A is HIGH at the same time that at least 2 other inputs are HIGH. Design the circuit.

A	B	C	D	Y
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	1 → $A\bar{B}CD$

A	B	C	D	
1	1	0	0	
1	1	0	1	1 → $AB\bar{C}D$
1	1	1	0	1 → $ABC\bar{D}$
1	1	1	1	1 → $ABCD$

$$Y = A\bar{B}CD + AB\bar{C}D + ABC\bar{D} + ABCD$$

$$= A\bar{B}CD + AB\bar{C}D + ABC$$

$$= A\bar{B}CD + AB(C + \bar{C}D)$$

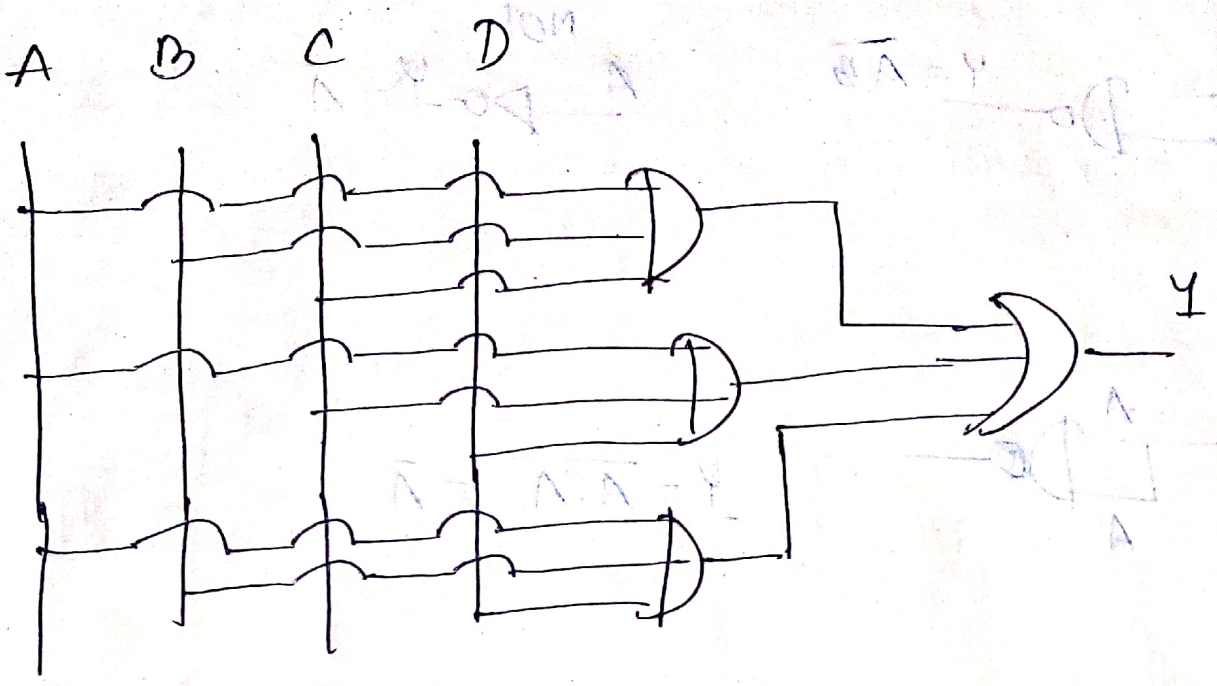
$$= A\bar{B}CD + ABC + ABD$$

$$= AC(B + \bar{B}D) + ABD$$

$$= ACB + ACD + ABD$$

$$= ABC + ACD + ABD$$

Step 3

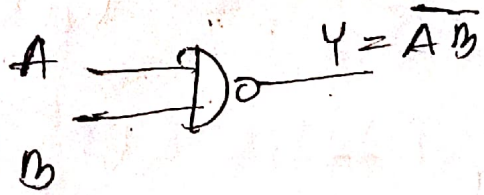


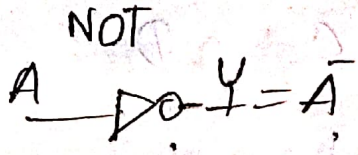
[NAND Gate:]

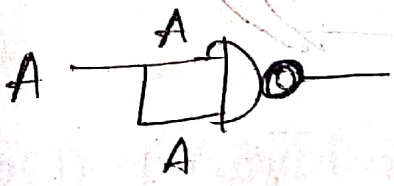
Universality of NAND Gate:

NAND
- NOT
- AND
- OR

① NAND to NOT:

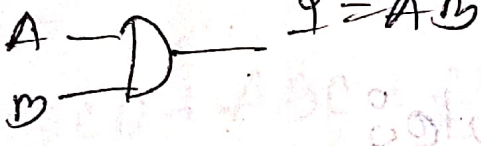


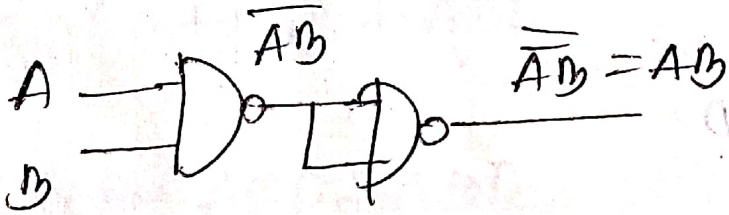




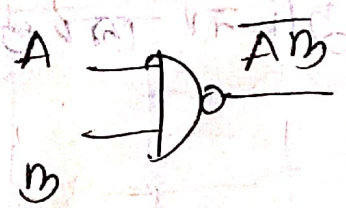
$Y = \overline{A.A} = \bar{A}$

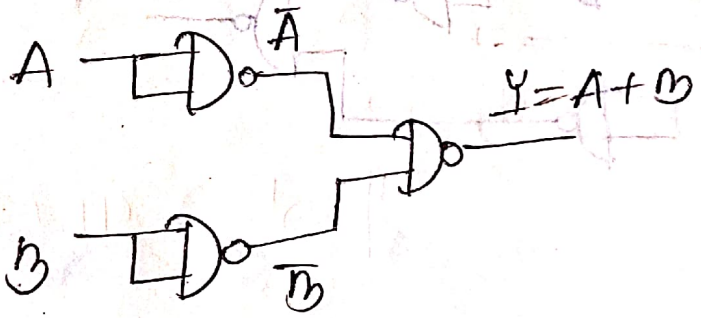
② NAND to AND:





③ NAND to OR





$\bar{A}$) $Y = \overline{\bar{A} \cdot \bar{B}} \Rightarrow Y = \overline{\overline{A+B}}$

বাংলাদেশ

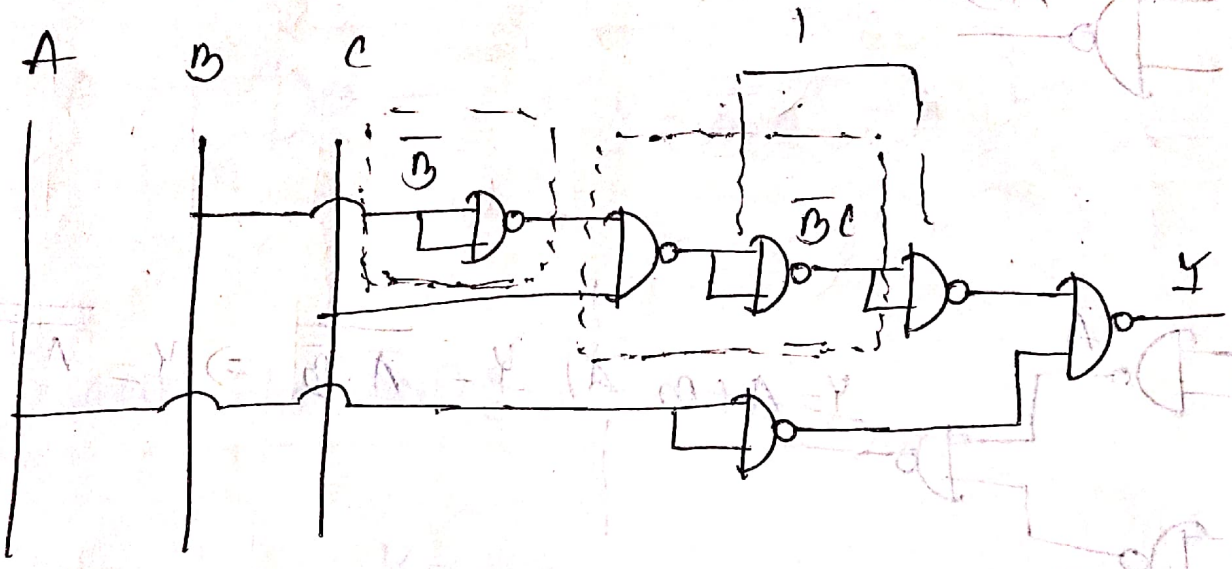
বহু সার্কিটকে বিভাবে NAND Gate বানানো।

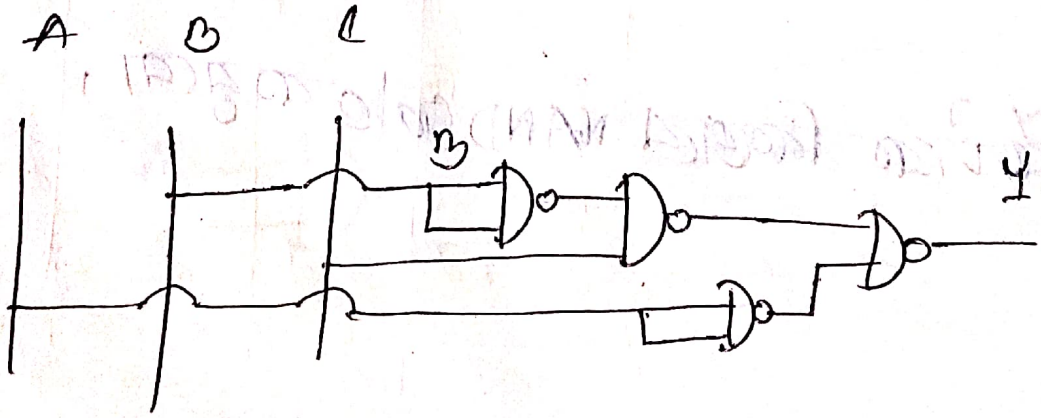
17-01-22

Draw the circuit using NAND gates only.

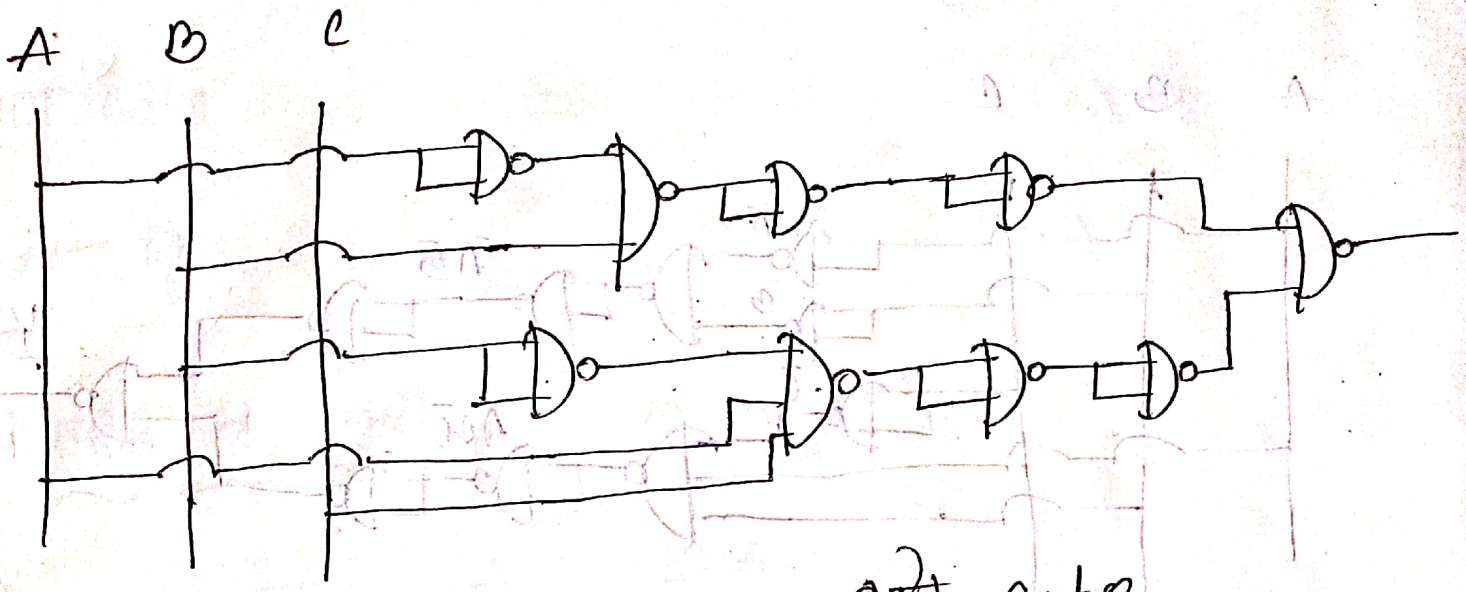
1. $y = \bar{A} + \bar{B}C$

পরপর দুটি না গেট হবে

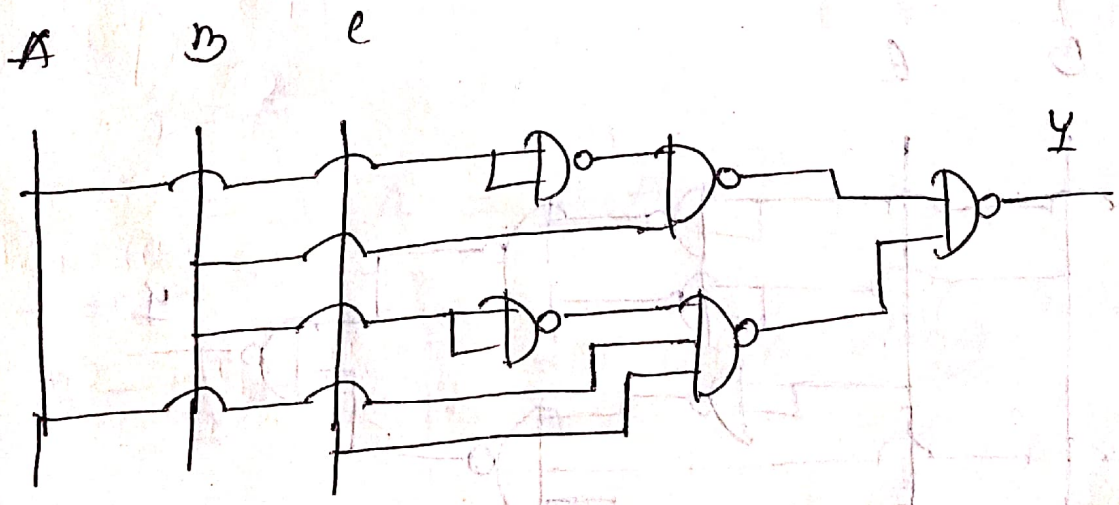




2. $y = \bar{A}B + A\bar{B}C$



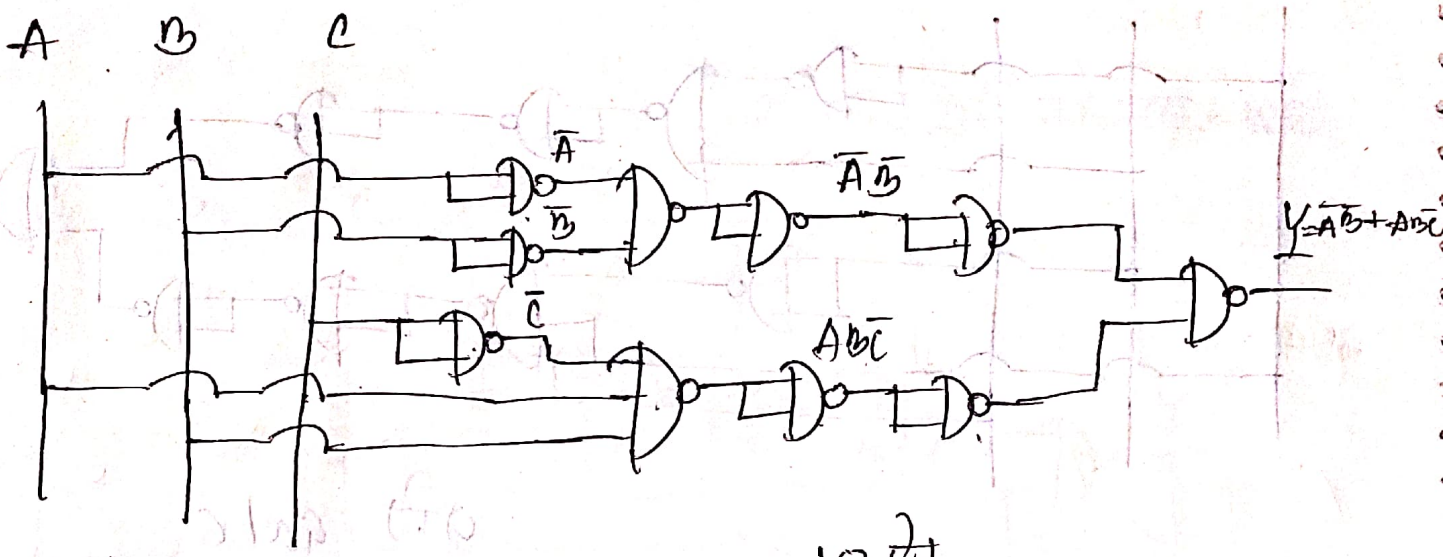
9 no gate



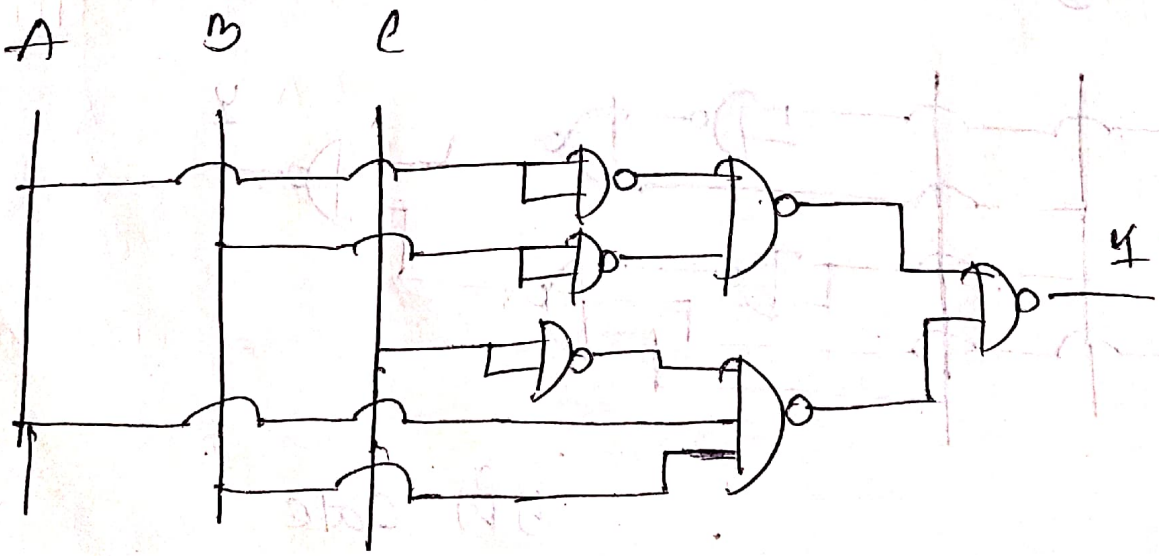
5 no Gate

3.

$Y = \bar{A}\bar{B} + AB\bar{C}$



10 ट्रा



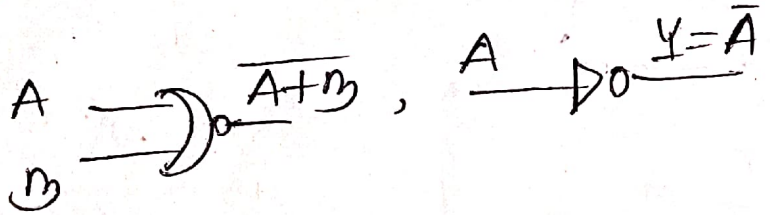
6 ट्रा

NOR Gate is also universal gate:

Universality of NOR gate.

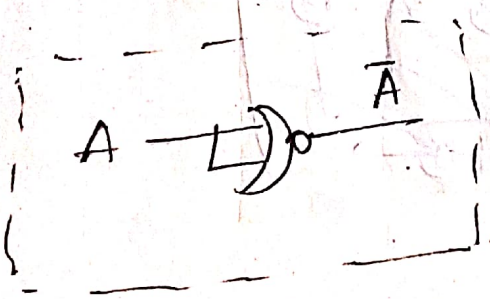
NOT. Gate

① NOR to NOT



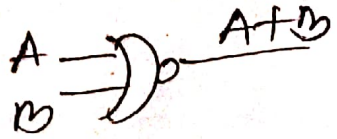
$Y = \bar{A}$

$= \overline{A+A} = \bar{A}\cdot\bar{A} = \bar{A}$



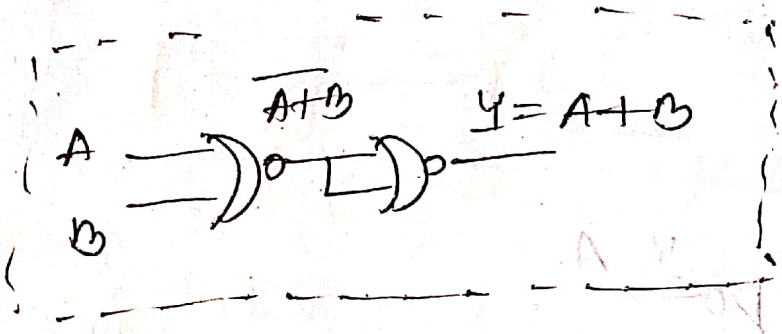
NOT Gate using NOR gate.

② NOR to OR:



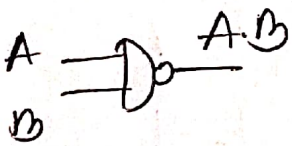
$Y = A + B$

$= \overline{\overline{A+B}}$

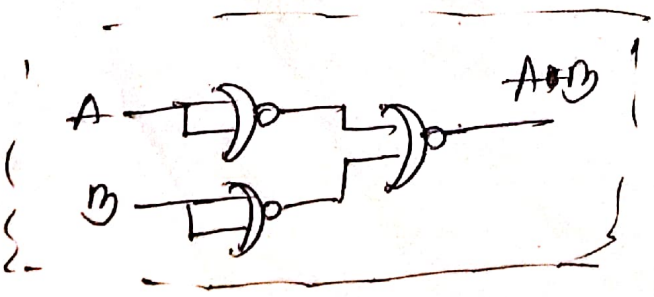


→ OR gate using NOR

③ ~~AND~~ NOR to AND:

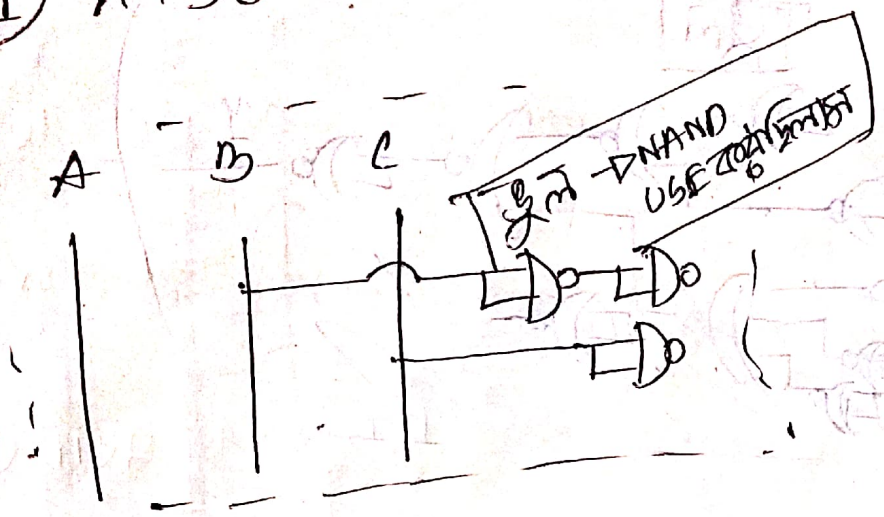


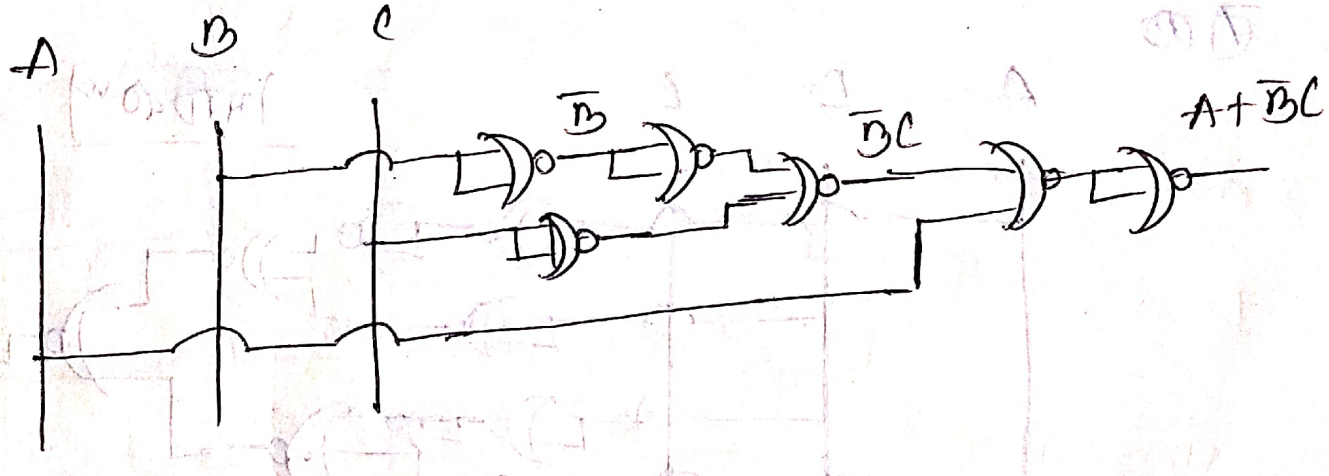
$Y = AB = \overline{\overline{AB}} = \overline{\overline{A}+\overline{B}}$

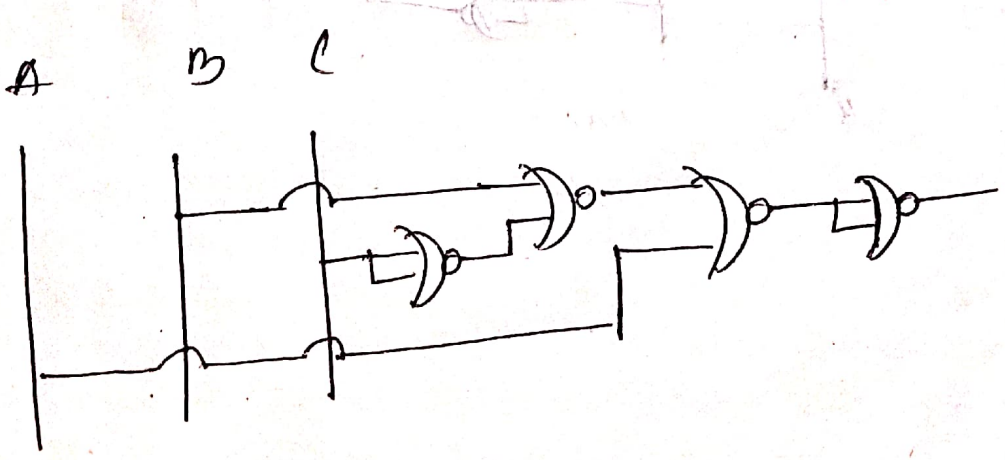


Draw the circuit using NOR gates only

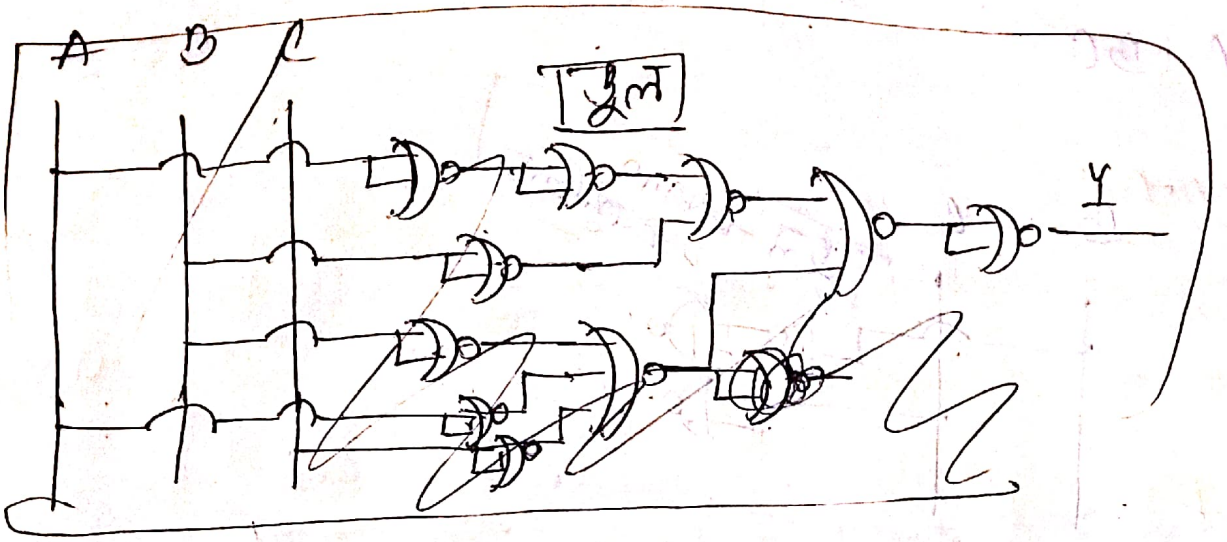
① $A+\bar{B}C$



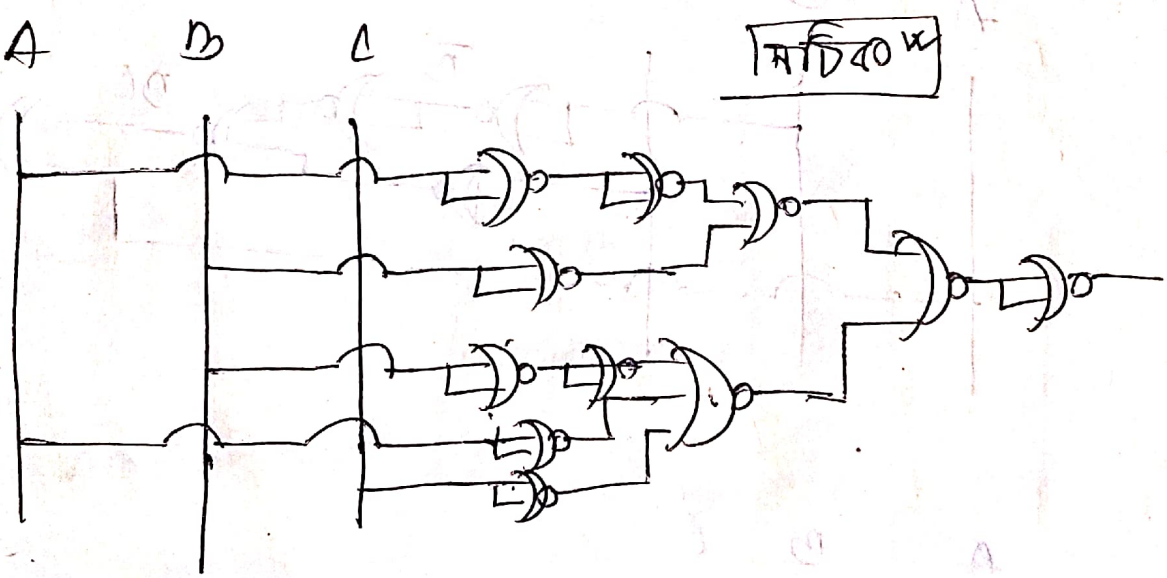




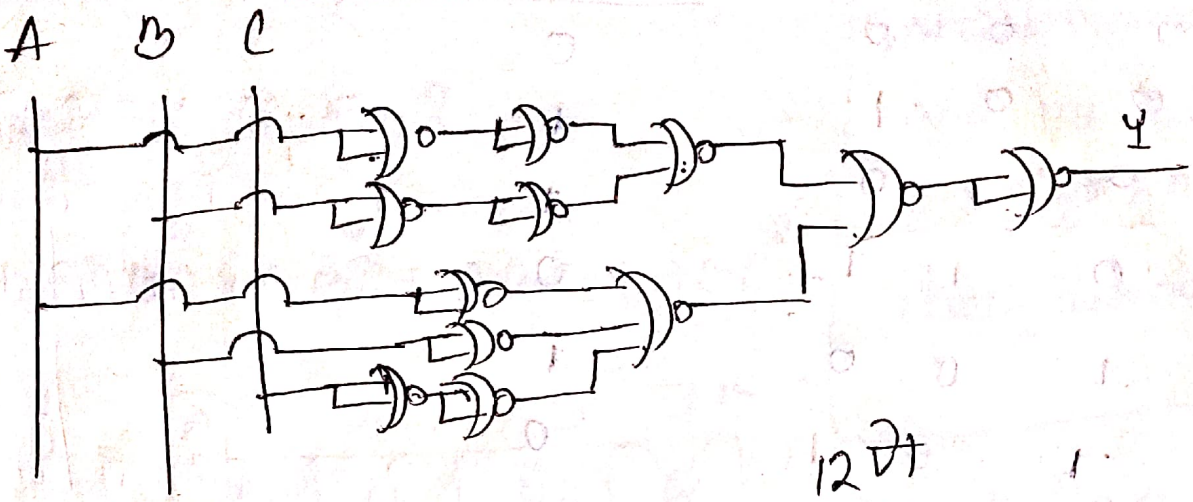
2. $\bar{A}B + A\bar{B}C$



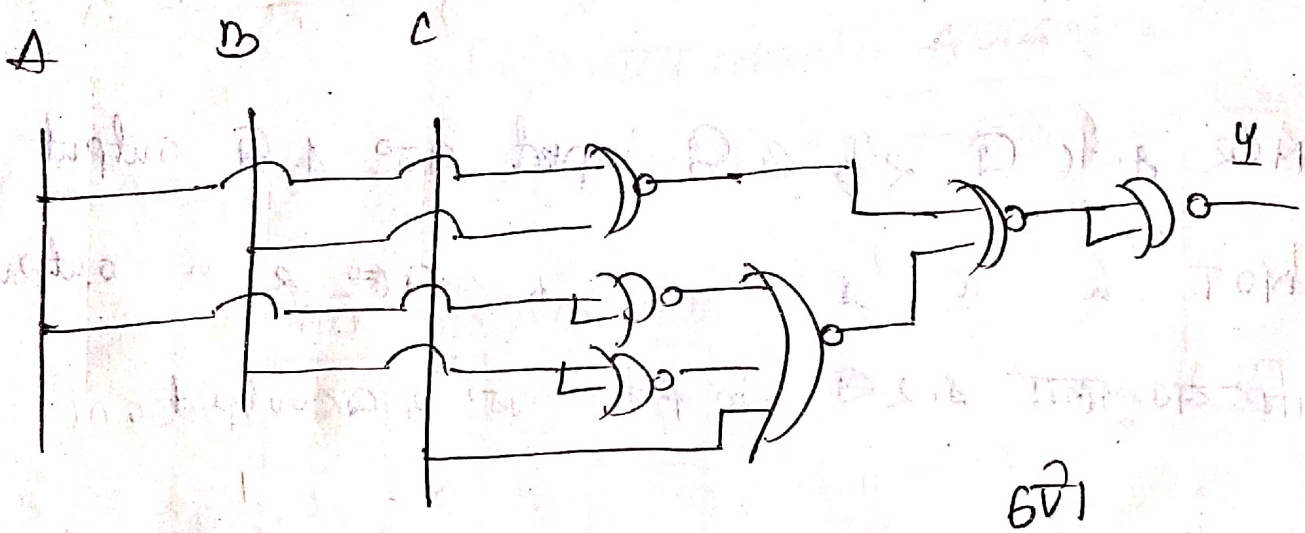
(A)(B)



3) $Y = \bar{A}\bar{B} + AB\bar{C}$



12 ग्टे



6 ग्टे

Truth table

A	B	C	$Y = A \oplus B \oplus C$
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

NOR gate এ 2 & 3 এ input এবং 1 এ output,

NOT " " 1 " " এবং 2 " output

বাকি সবগুলো 1, 2 এ input এবং 3 এ output,

10-01-22

Simplification of Logic Expression using Karnaugh Map (K-Map):

What is K-Map?

$$Y = \bar{A}BC + A\bar{B}C + \bar{A}\bar{B}\bar{C} + ABC$$

variable amount and input possibilities $\rightarrow 2^n$

Here, $n \Rightarrow$ number of inputs

	$\bar{A}\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$
$\bar{C}$	1	0	0	0
C	0	1	1	1

2×4 K-Map

↳ এখানে column A এবং row C — common

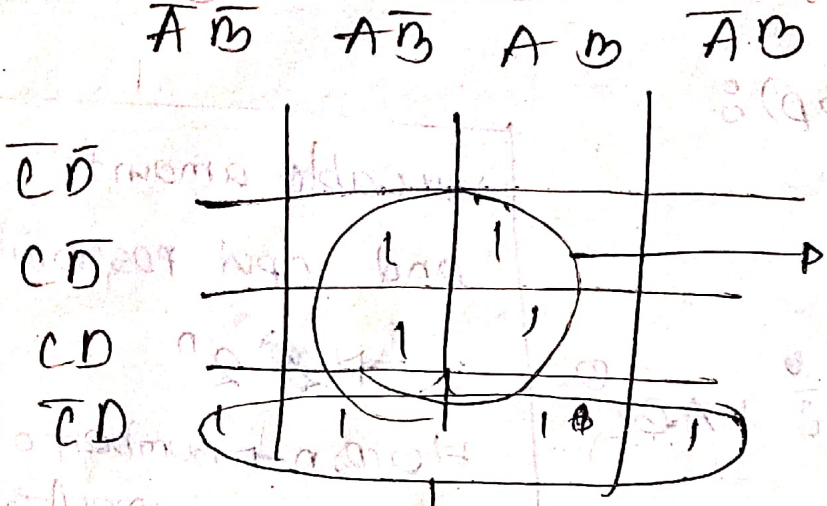
↳ তাই AC এখানে চলবে

$$Y = \bar{A}B\bar{C}D + A\bar{B}\bar{C}D + ABCD + A\bar{B}\bar{C}\bar{D}$$

	$\bar{A}\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$
$\bar{C}\bar{D}$	0	1	0	0
$C\bar{D}$	0	0	0	1
CD	0	0	1	0
$\bar{C}D$	1	1	0	1

4×4 K-Map

Suppose



→ এখানে A common colum এ এবং C বক্সান Row তে তাই উত্তর AC

→ এখানে, colom এ কোনো common নেই। Row তে $\bar{C}D$ common তাই উত্তর $\bar{C}D$ হবে।

Looping :

① Pair ② Quad ③ Octet

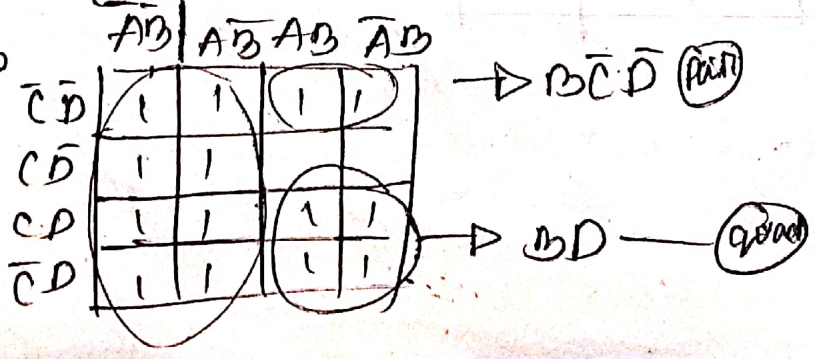
↓ ↓ ↳ 8 adjacent

2 adjacent 4 adjacent 1

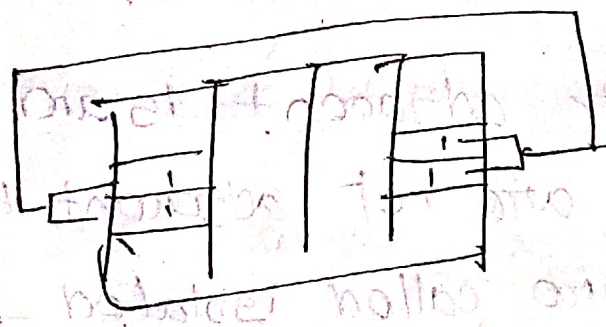
1 1

$\bar{B}$ → কারণ খালি B বক্সান

① Pair :



common বলতে বলতে চাচ্ছি বোঝাচ্ছে লাভ/সাশ্রয়



common বলতে বলছে চাচ্ছে

→ octec best, quad better, pair good

~~or octec better than quad,~~

or, octec > quad > pair > nothing

Algorithm of K-Map:

Step 1: Construct the K-Map according to the number of inputs and place 1s in those squares corresponding to the 1s in the truth table. Place 0s in the other squares

Step 2: Examine the map for adjacent 1s and loop those 1s that are not adjacent to any other 1s. These are called isolated 1s.

Step 3: Next, look for those 1s that are adjacent to only one other 1. Loop any pair containing such a 1.

Step 4: Loop any octet even if it contains some 1s that have already been looped.

Step 5: Loop any quad that contains one or more 1s that have not already been looped, making sure to use the minimum number of loops.

HW.

Example 5: A 4-bit binary number is represented as D C B A, where D, C, B and A represent the individual bits with A equal to the LSB. Design a logic circuit that will produce a HIGH output whenever (the binary number is greater than 0011 and less than 1011) or (all inputs are LOW) or (all inputs are HIGH).

Solve using K-Map.

H.W

solve:

Truth Table:

D	C	B	A (LSB)	Y	
0	0	0	0	1	$\rightarrow \bar{D}\bar{C}\bar{B}\bar{A}$
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0	1	$\rightarrow \bar{D}C\bar{B}\bar{A}$
0	1	0	1	1	$\rightarrow \bar{D}C\bar{B}A$
0	1	1	0	1	$\rightarrow \bar{D}CB\bar{A}$
0	1	1	1	1	$\rightarrow \bar{D}CBA$
1	0	0	0	1	$\rightarrow D\bar{C}\bar{B}\bar{A}$
1	0	0	1	1	$\rightarrow D\bar{C}\bar{B}A$
1	0	1	0	1	$\rightarrow D\bar{C}B\bar{A}$
1	0	1	1		
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1	1	$\rightarrow DCBA$

$$Y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} + A\bar{B}C\bar{D} + \bar{A}BC\bar{D} + ABC\bar{D}$$

$$+ \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{C}D + \bar{A}B\bar{C}D + ABCD$$

	$\bar{A}\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$
$\bar{C}\bar{D}$	1			
$C\bar{D}$	1	1	1	1
CD			1	
$\bar{C}D$	1	1		1

$$Y = \bar{A}\bar{B}\bar{D} + ABC + \bar{B}\bar{C}D + \bar{A}\bar{C}D + C\bar{D}$$

#23-01-2022#

Simplify the following expression using K Map,

$$Y = ABCD + A'B'CD + ABC'D' + ABC + ABCD + A$$

→ 100% okay
You lovely Human Being

	$\bar{A}\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$
$\bar{C}\bar{D}$		1	1	
$C\bar{D}$		1	1	
CD	1	1	1	1
$\bar{C}D$		1	1	

L_2

L_1

$$Y = CD + A$$

Examp

$Y = ABC + A\bar{B}\bar{C} + AB + C$

	$\bar{A}\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$
$\bar{C}$		1	1	
C	1	1	1	1

$ABCD + \bar{A}\bar{B}CD + AB\bar{C}\bar{D} + A\,BC + AB + CD + A$

	$\bar{A}\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$
$\bar{C}\bar{D}$		1	1	
$C\bar{D}$		1	1	
CD	1	1	1	1
$\bar{C}D$		1	1	

Example 10

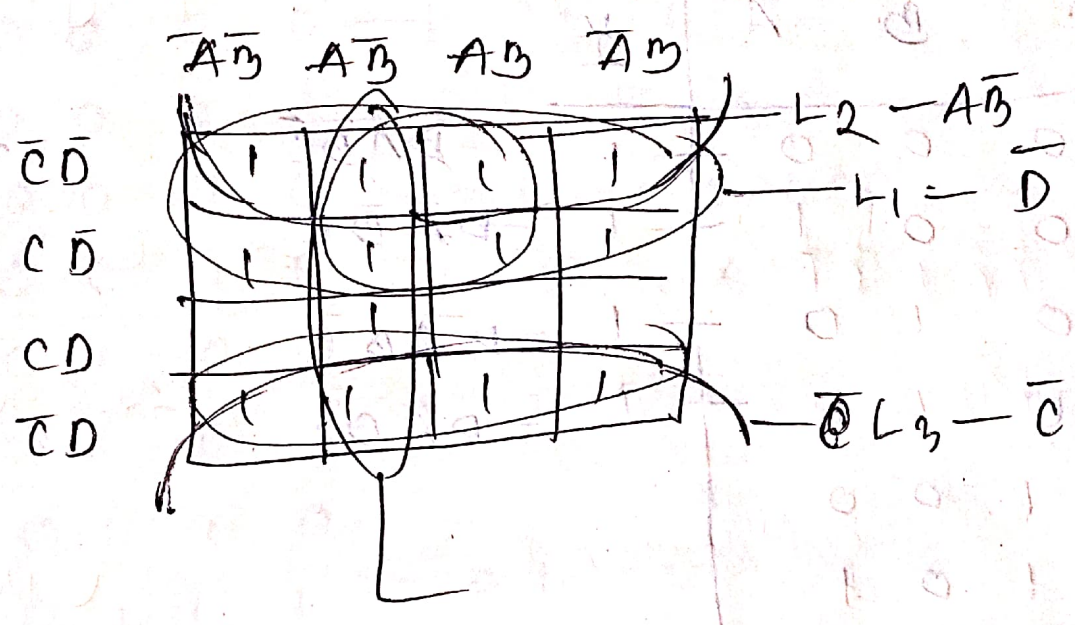
Simplify the following expression using K-Map

$$Y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{C}D + A\bar{B}C + \bar{D}$$

Octet → result

quad → result

pair → result



$$Y = A\bar{B} + \bar{C} + \bar{D}$$

LSM MSB

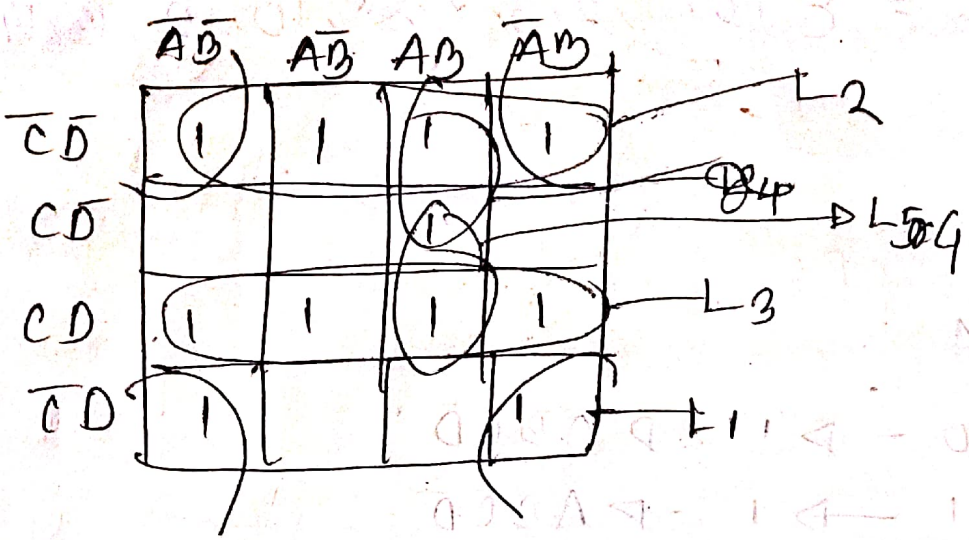
$F(A, B, C) = \{(0, 1, 2, 3, 6, 7)\}$; Simplify using K-Map.

C	B	A	Y	
0	0	0	1	$\rightarrow \bar{A}\bar{B}\bar{C}$
0	0	1	1	$\rightarrow \bar{A}\bar{B}C$
0	1	0	1	$\rightarrow \bar{A}B\bar{C}$
0	1	1	1	$\rightarrow \bar{A}BC$
1	0	0		
1	0	1		
1	1	0	1	$\rightarrow AB\bar{C}$
1	1	1	1	$\rightarrow ABC$

	$\bar{A}\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$
$\bar{C}$	1	1	1	1
C	0	0	1	1

$$F(\overset{LSB}{A}, B, C, \overset{MSB}{D}) = \Sigma(0, 1, 2, 3, 7, 8, 10, 12, 13, 14, 15)$$

D	C	B	A		
0	0	0	0	→ 1	→ $\bar{A}\bar{B}\bar{C}\bar{D}$
0	0	0	1	→ 1	→ $A\bar{B}\bar{C}\bar{D}$
0	0	1	0	→ 1	→ $\bar{A}B\bar{C}\bar{D}$
0	0	1	1	→ 1	→ $AB\bar{C}\bar{D}$
0	1	0	0		
0	1	0	1		
0	1	1	0		→ $\bar{A}BC\bar{D}$
0	1	1	1	→ 1	→ $ABC\bar{D}$
1	0	0	0	→ 1	→ $\bar{A}\bar{B}\bar{C}D$
1	0	0	1		
1	0	1	0	→ 1	→ $\bar{A}B\bar{C}D$
1	0	1	1	→	$AB\bar{C}D$
1	1	0	0	→ 1	→ $\bar{A}\bar{B}CD$
1	1	0	1	→ 1	→ $A\bar{B}CD$
1	1	1	0	→ 1	→ $\bar{A}BCD$
1	1	1	1	→ 1	→ $ABCD$



$Y = \bar{A}\bar{C} + \bar{C}D + CD + ABC$

অথবা $= \bar{A}\bar{C} + \bar{C}\bar{D} + CD + AB\bar{D}$

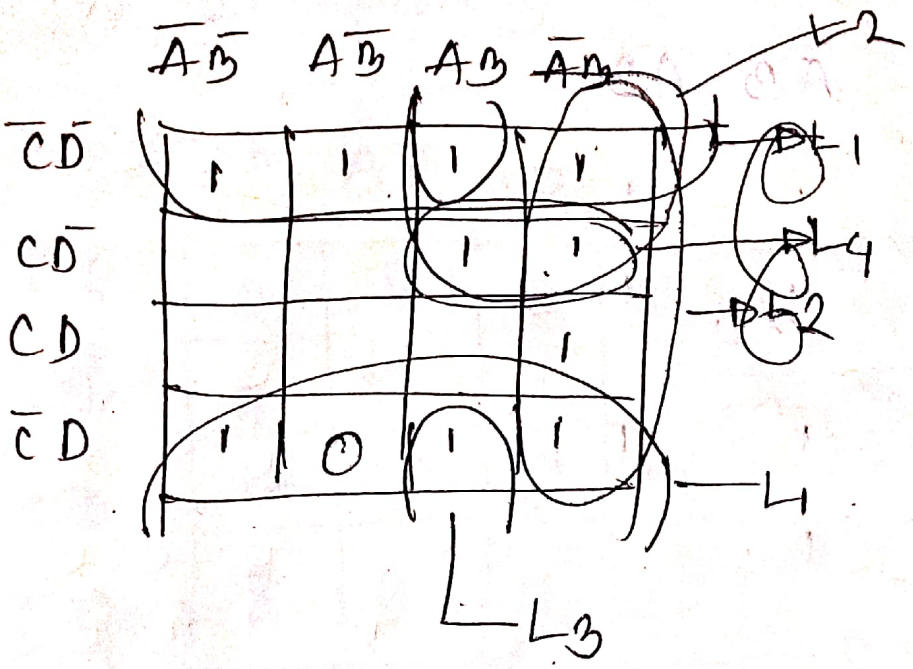
Task –

$F(A, B, C, D) = \Sigma(0, 1, 2, 3, 6, 7, 9, 11, 14, 15)$

$\bar{A}\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} + \bar{A}B\bar{C}\bar{D} + AB\bar{C}\bar{D}$

$+ \bar{A}BC\bar{D} + ABC\bar{D} + \bar{A}B\bar{C}D + AB\bar{C}D$

$+ \bar{A}BCD + ABCD$



$$Y = \bar{C} + \bar{A}B + AB\bar{C} + BC\bar{D}$$

$$= \bar{C} + B(\bar{A} + A\bar{C}) + BC\bar{D}$$

$$= \bar{C} + B(\bar{A} + \bar{C}) + BC\bar{D}$$

$$= \bar{C} + \bar{A}B + B\bar{C} + BC\bar{D}$$

	$\bar{A}\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$
$\bar{C}\bar{D}$	1	1	1	1
$C\bar{D}$			1	1
CD			1	1
$\bar{C}D$		1	1	

$$F(A, B, C, D) = \bar{C}\bar{D} + BC + A\bar{C}$$

		00	10	11	01
		$\bar{A}\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$
00	$\bar{C}\bar{D}$	0	2	3	1
10	$C\bar{D}$	4	6	7	5
11	CD				
01	$\bar{C}D$				

K-Map cell Numbering

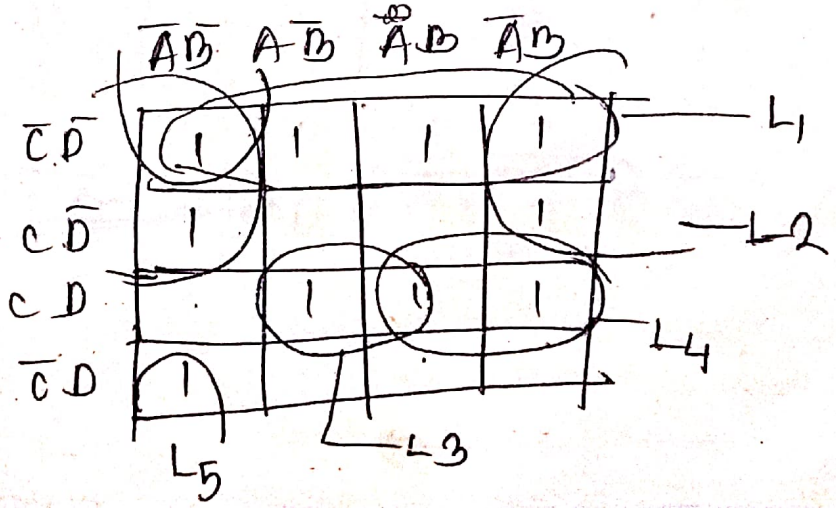
	$\bar{A}\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$
$\bar{C}\bar{D}$	0	1	3	2
$C\bar{D}$	4	5	7	6
CD	12	13	15	14
$\bar{C}D$	8	9	11	10

→ $F(A,B,C) = \Sigma(0, 1, 4, 6, 7)$

	$\bar{A}\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$
$\bar{C}$	1	1	0	0
C	1	0	1	1

→ $F(A,B,C,D) = \Sigma(0, 1, 2, 3, 4, 6, 8, 13, 14, 15)$

$Y = \bar{C}\bar{D} + \bar{A}\bar{D} + BCD + ACD + \bar{A}\bar{B}\bar{C}$



24-01-23

Indexing :

2×4 K-Map

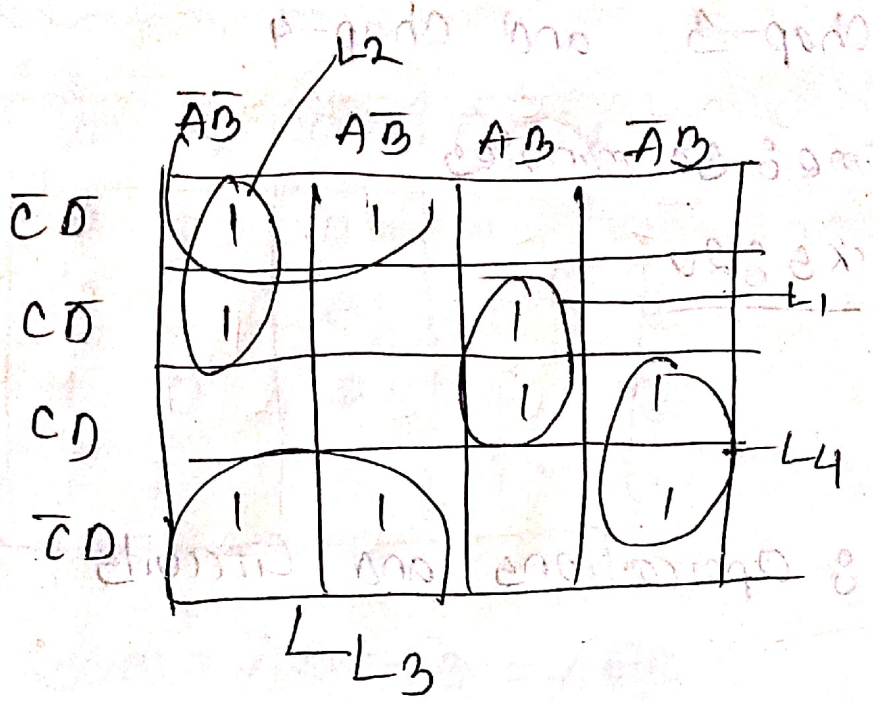
	$\bar{A}\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$
$\bar{C}$	0	1	3	2
C	4	5	7	6

4×4 K-Map

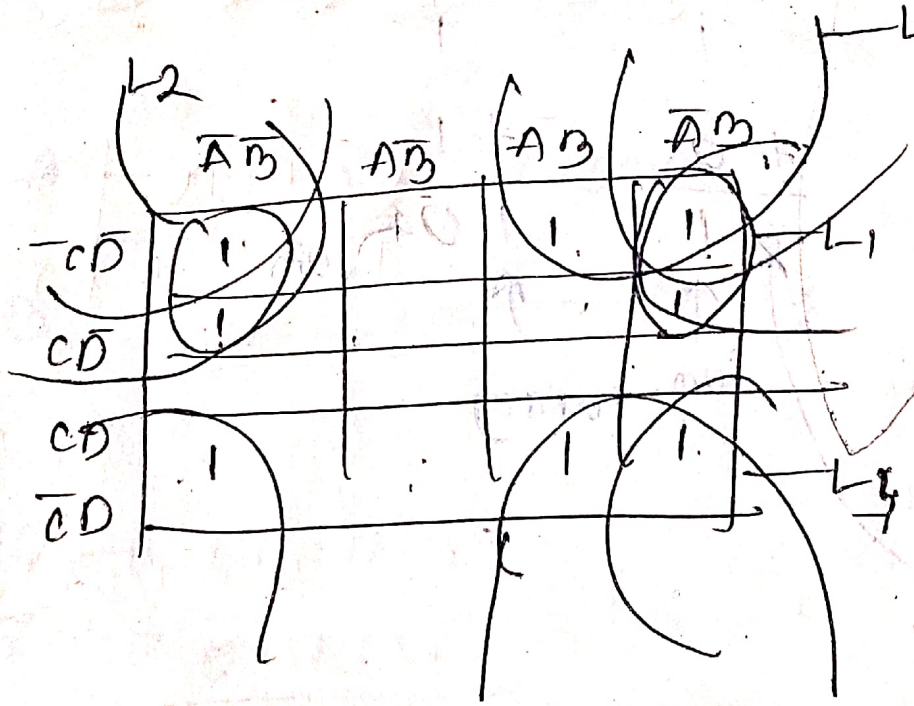
	$\bar{A}\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$
$\bar{C}\bar{D}$	0	1	2	3
$C\bar{D}$	4	5	7	6
CD	12	13	15	14
$\bar{C}D$	8	9	10	11

—x—

$F(A,B,C,D) = \Sigma(0,1,4,7,8,9,10,14,15)$



$Y = ABC + \bar{A}\bar{B}\bar{D} + \bar{B}\bar{C} + \bar{A}BD$



$Y = \bar{A}\bar{D} + \bar{A}\bar{C} + B\bar{C}$

$Y = \cancel{\bar{A}B\bar{D} + AB\bar{D}} + \bar{A}\bar{C} + B\bar{C}$

CT 4 : Date : 26-01-2022

Syllabus : Chap-3 and Chap-4

Class Time : 30 minutes

Marks : 20

Chapter 6 :

Digital Arithmetic : Operations and Circuits

Addition :

$$\begin{array}{r} 0 \\ +\,0 \\ \hline 0\,0 \end{array} \qquad \begin{array}{r} 0 \\ +\,1 \\ \hline 0\,1 \end{array} \qquad \begin{array}{r} 1 \\ +\,0 \\ \hline 0\,1 \end{array} \qquad \begin{array}{r} 1 \\ +\,1 \\ \hline 1\,0 \end{array}$$

sum sum sum carry sum

carry

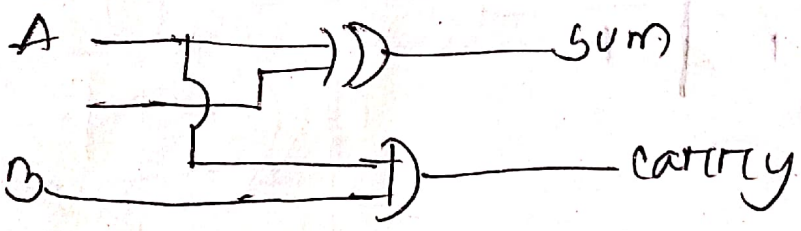
→ Design the half adder

Half Adder :

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$Sum = \bar{A}B + A\bar{B} = A \oplus B$

$Carry = AB$



10 → 1010
7 → 0111
17 → 10001

Design the Full Adder →

Full Adder:

Truth Table

A	B	Cin (Carry in)	Sum	Cout (Carry out)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Sum →

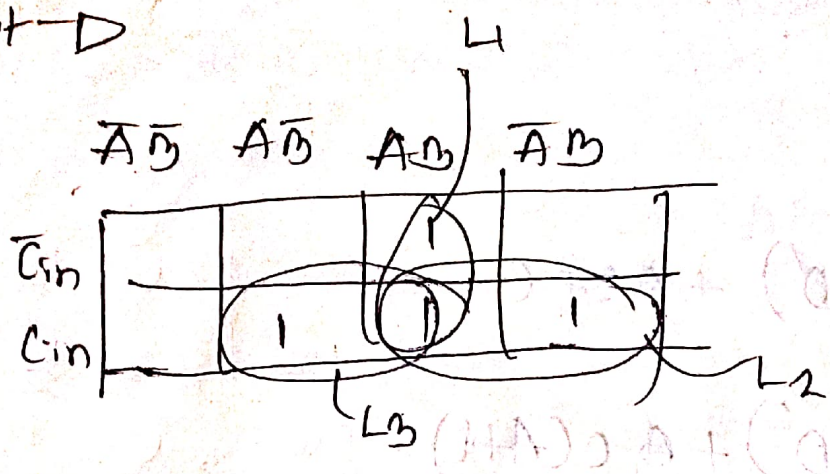
	$\bar{A}\bar{B}$	$\bar{A}B$	AB	$A\bar{B}$
$\bar{C}_{in}$	0	1	0	1
C_{in}	1	0	1	0

$$Sum = \bar{A}\bar{B}C + \bar{A}B\bar{C} + ABC + A\bar{B}\bar{C}$$

$$= \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

$$= \bar{A}(B \oplus C) + A\overline{(B \oplus C)} = A \oplus B \oplus C_{in}$$

Cout →

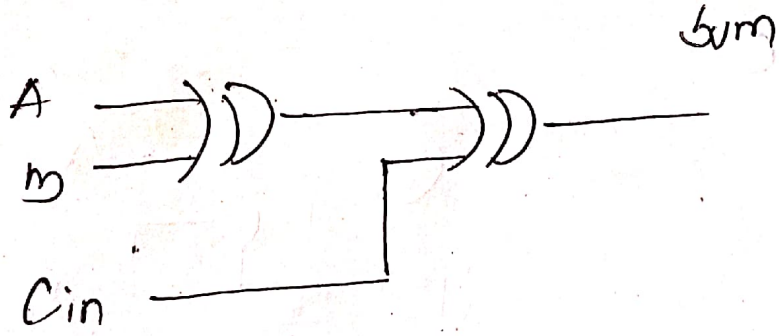


$Cout = AB + AC + BC$ · এভাবে লিখি $AB + BCin + ACin$

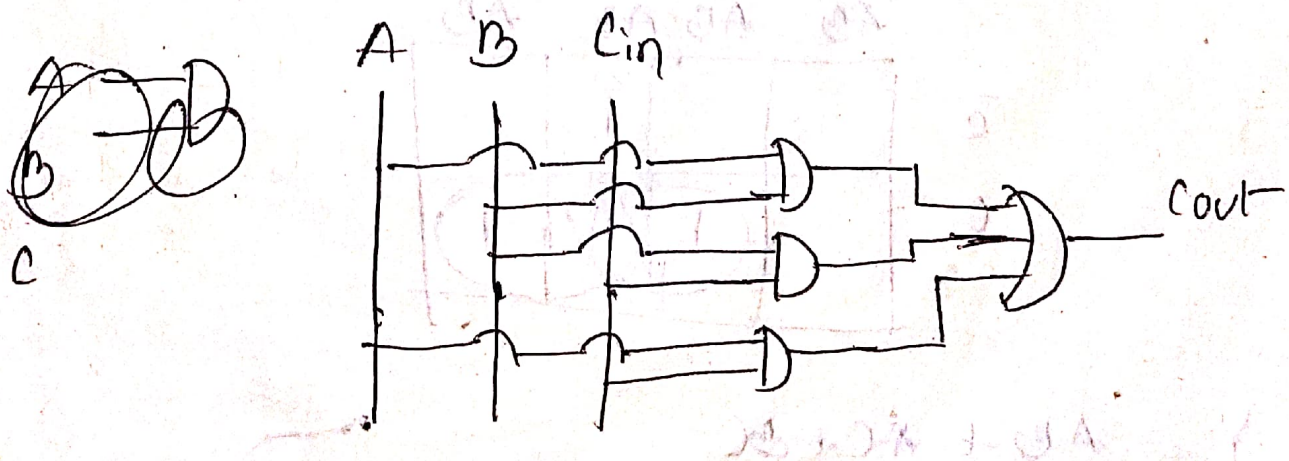
$= A(B+C) + BC$

Circuit

Sum



Cout



25-01-2022

CSE-210 (LAB)

(a)(b)

① $(A+C)(AD+AD') + AC + C$

$= (A+C)\,A(D+D') + C(A+1)$

$= (A+C)\,A + C$

$= (A+AC) + C$

$= A(1+C) + C$

$= A + C$

(b2). $A'BC + AB'C + ABC' + ABC$

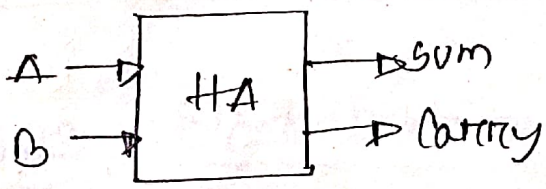
	$\bar{A}\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$
$\bar{C}$			1	
C		1	1	1

$Y = AB + AC + BC$

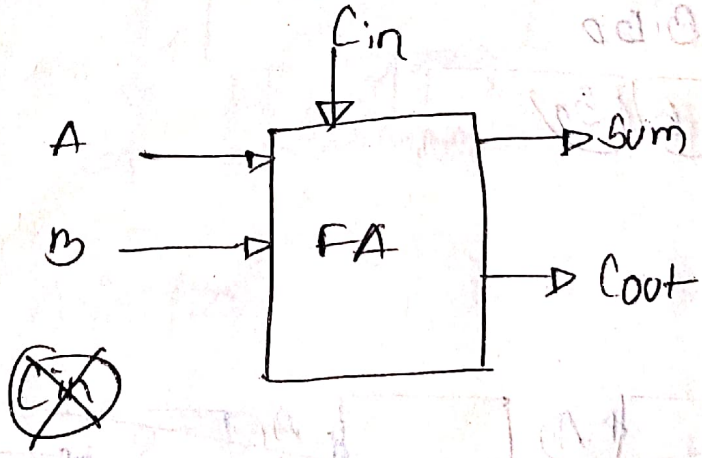
30-01-2022

Block Diagram:

Half adder:



Full adder:



4 bit parallel Adder:

13	→ 1101	04
11	→ 1011	
24	→ 11000	

4 bit Parallel Adder

```
                1  1  1  1
B  →            1  1  0  1   ← Cin
A  →            1  0  1  1
-----------------------------
24 →           11 000
```

Carry জন্য full Adder প্রয়োজন

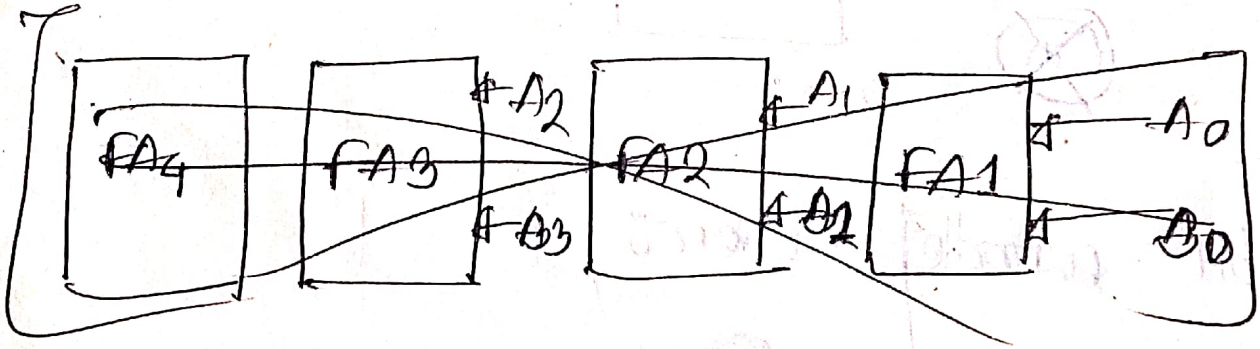
↓

কারণ Cin

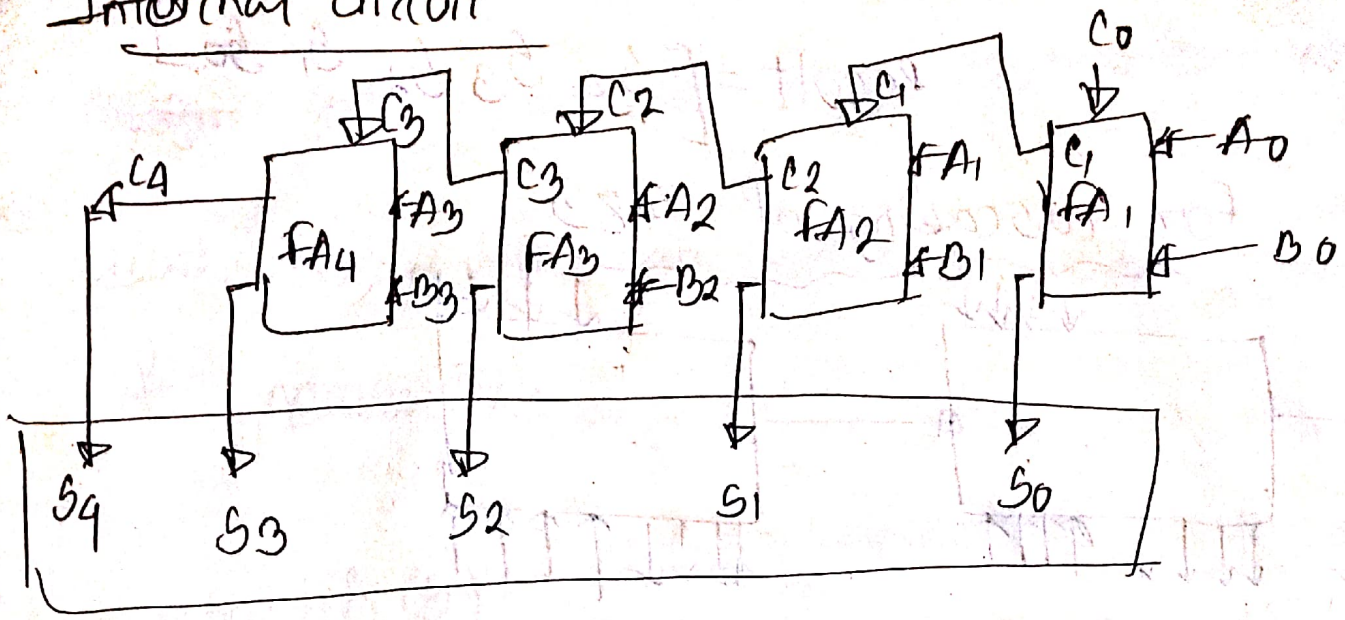
Internal Circuit:

```
          C4 C3 C2 C1 C0
[A] → |A3 A2 A1 A0
[B] → |B3 B2 B1 B0
-----------------------
[A]+[B] → S4 S3 S2 S1 S0
```

← 4টি full Adder লাগবে।

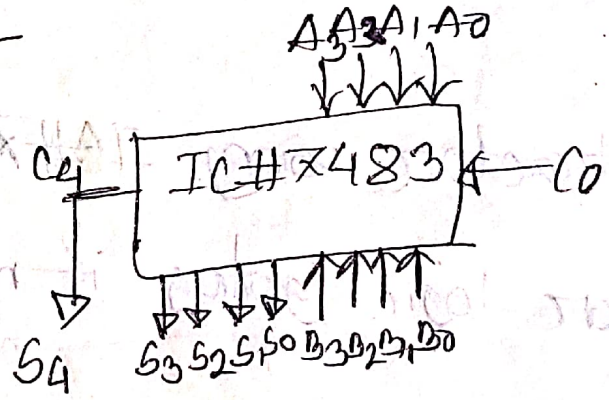


Internal Circuit



IC# 7483 : Block Diagram :

operation –



Inside Arrow
↳ Input

Outside Arrow
↳ Output

for Addition

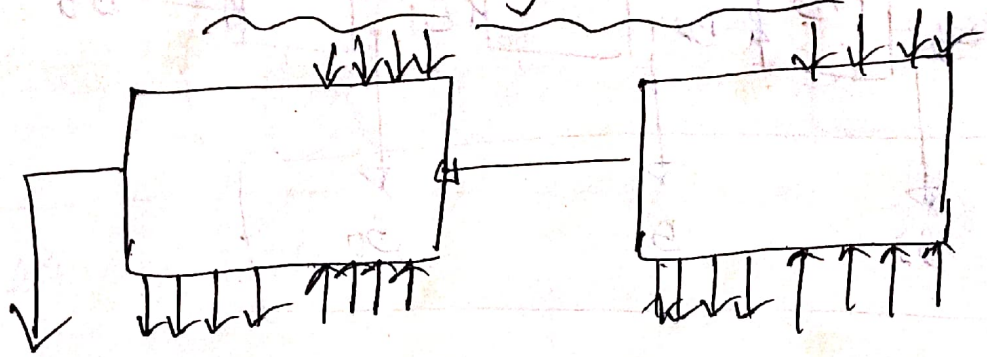
$C_0 = 0$

$[A_3\ A_2\ A_1\ A_0] = [1\ 1\ 0\ 1]$

$[B_3\ B_2\ B_1\ B_0] = [1\ 0\ 1\ 1]$

Result = $[S_4\ S_3\ S_2\ S_1\ S_0]$

for cascading of 7483



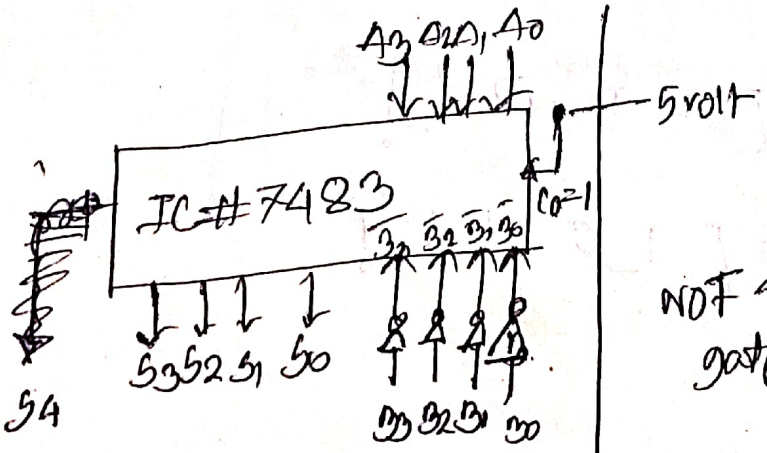
for addition of more than 4-bits.

Design 4-bit subtractor using IC#7483.

You can use other logic gates if necessary.

$\Rightarrow A - B = A + (-B)$; $B = [B_3\ B_2\ B_1\ B_0]$

2's complement



$0111 \rightarrow +7$

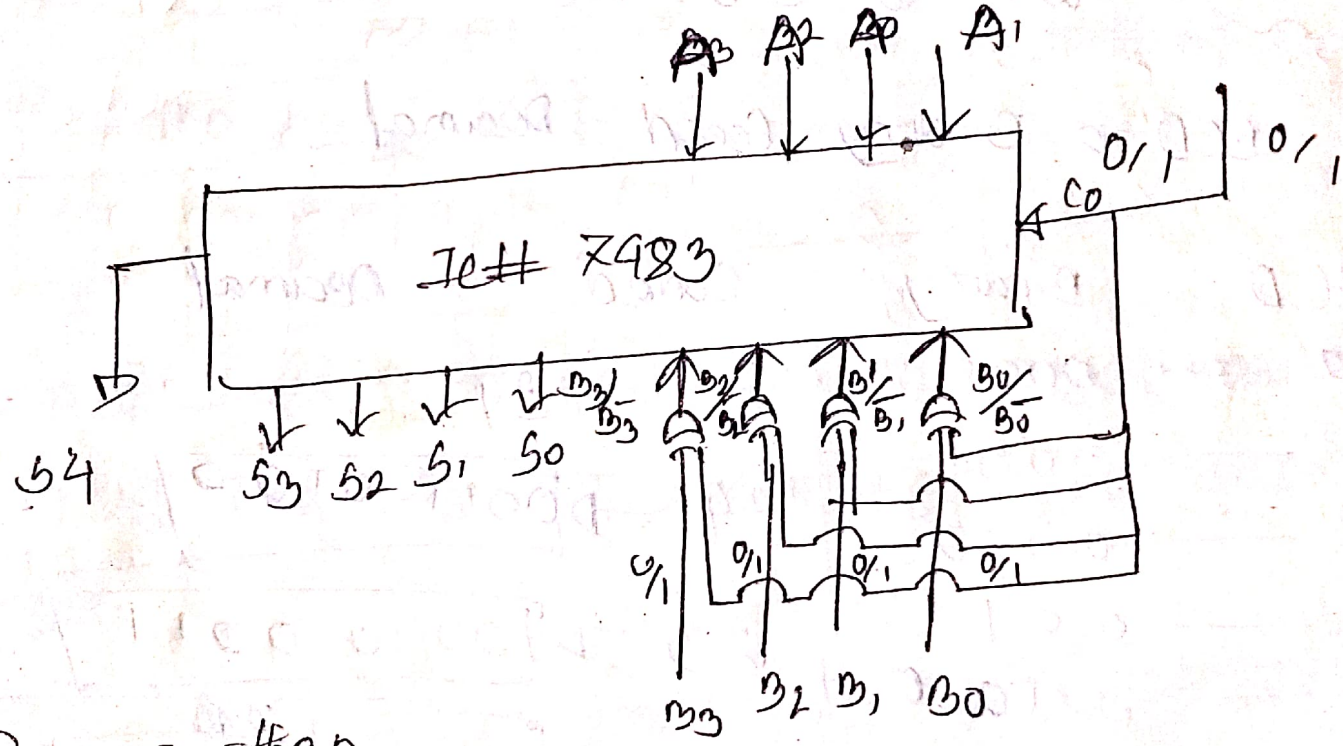
NOT gate $\leftarrow 1000 \rightarrow$ 1's complement

$+1 \rightarrow \boxed{C_0 = 1}$

$(-7) \rightarrow 1001 \rightarrow$ 2's complement

Design 4-bit parallel Adder/Subtractor using IC# 7483. You can use other logic gates if necessary.

→ Switch (S) → S=0 → Adder
→ S=1 → Subtractor



If S=0 then,

First inputs are A_3, A_2, A_1, A_0

Second inputs are $\bar{B}_3, \bar{B}_2, \bar{B}_1, \bar{B}_0$ and $C_0=0$

therefore this is addition.

If $S=1$, then 1st inputs are A_3, A_2, A_1, A_0

and second inputs are $\overline{B_3}, \overline{B_2}, \overline{B_1}, \overline{B_0}$

and $C_0 = 1$.

BCD: What is BCD?

BCD → Binary Coded Decimal

BCD	Binary	Coded Decimal
0 —	0000	
1 —	0001	
2 —	0010	
3 —	0011	
4 —	0100	
5 —	0101	
6 —	0110	
7 —	0111	
8 —	1000	
9 —	1001	

34

34 → $\boxed{0011\ 0100}$

23 → $\boxed{0010\ 0011}$

+

57 → $\boxed{0101}\ \boxed{0111}$

31-01-2022 (BCD adder)

47 - 0100 0111

85 = 1000 0101

132 - 0001 0011 0010

47 → 0 1 0 0 0 1 1 1

\+ 85 → 1 0 0 0 0 1 0 1

9 এর চেয়ে বড় (12)

1100 1100

তাই +6

0110 0110

0000 1110 0010

যদি কখনো দুটো BCD কোড যোগ করলে result 9 এর চেয়ে বড় হয় তাহলে +6 (0110) করতে হবে।

→ এখানে +6 এইজন্য যে 10 - 15 এর কোড exist করে না। তাই +6 করে 16 পর্যন্ত skip করা হচ্ছে।

Suppose $[A] = A_3 A_2 A_1 A_0$

$[B] = B_3 B_2 B_1 B_0$

$[S] = S_4 S_3 S_2 S_1 S_0$

If sum is > 9 add 6 → 0 11 0

If sum ≤ 9 then add 0 → 0 0 0 0

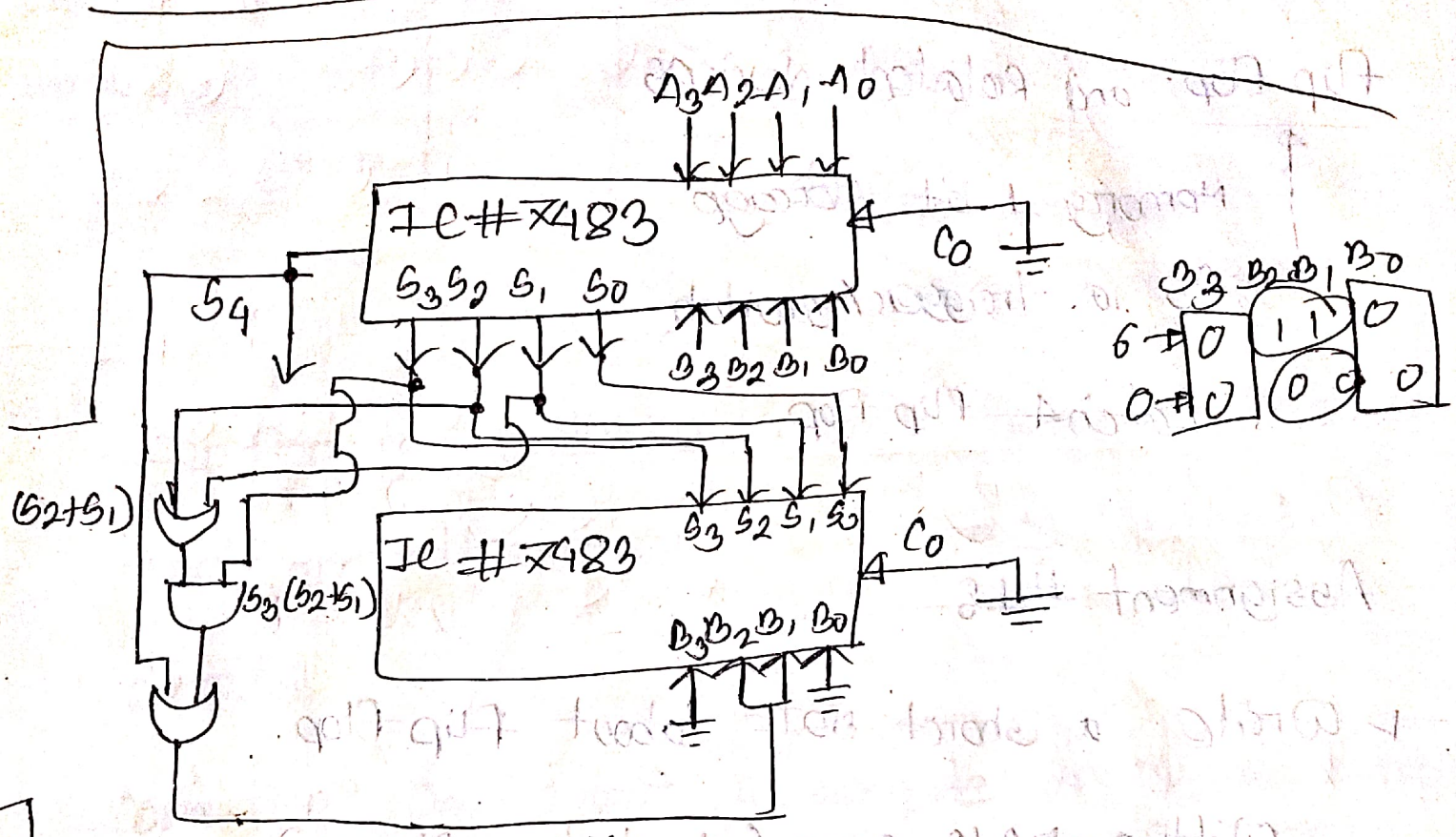
S_4	S_3	S_2	S_1	S_0	
0	0	0	0	0	
0	0	0	0	1	
0	0	0	1	0	0
0	0	0	1	1	1
0	0	1	0	0	Add 0
0	0	1	0	1	
0	0	1	1	0	
0	0	1	1	1	
0	1	0	0	0	
0	1	0	0	1	
0	1	0	1	0	1
0	1	0	1	1	1
0	1	1	0	0	
0	1	1	0	1	add 6
0	1	1	1	0	
0	1	1	1	1	
1	0	0	0	0	

Error Correction

x: If, x = 1 then add 6 →

If, x = 1 then add 0.

10001	
10010	



More than 9

$\boxed{S_4 = 1}$ OR

$S_3 = 1$ AND $(S_2 = 1$ OR $S_1 = 1)$

$$X = S_4 + S_3 \cdot (S_2 + S_1)$$

02-02-2022

Chapter-5

Flip-flop and Related devices

- Memory & bit storage
- As a trigger/switch

Latch & flip flop

Assignment #1:

→ Write a short NOTE about flip-flop.

Within → 3/4 page (Including Digram)
↳ Excluding cover page

→ font size (12)

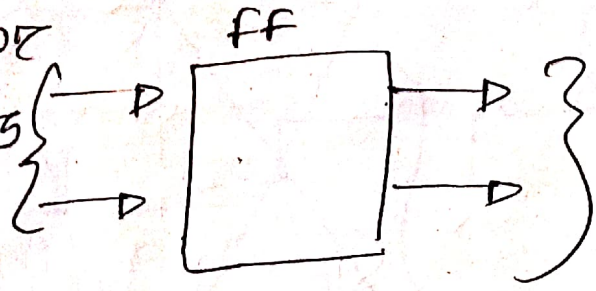
→ Single space (Word File)

Submission Date: 09.02.2022

within 12:30pm

Flip-Flop

One input or many inputs



Always to output

—x—

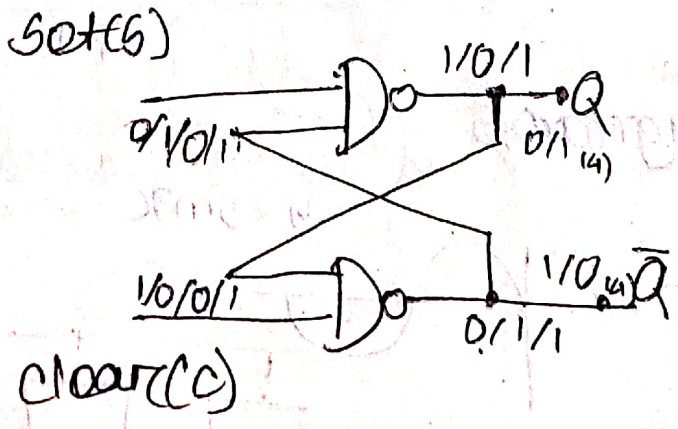
And One output is the opposite to another

Flip flop is a device where there is one input or there are many inputs but only 2 outputs.

Condition: One output is opposite of other outputs

NAND Latch:

Internal Circuit:



TT

S	C	Q
0	1	1
1	0	0
0	0	Invalid
1	1	NO Change

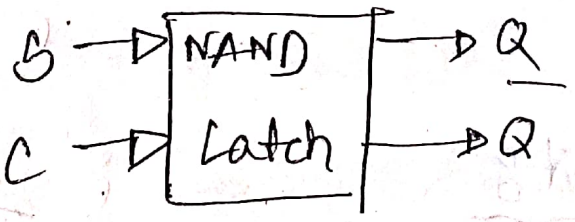
NAND Gate

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

(1,1): If Initially Q=0, then finally Q=0

(1,1): If Initially Q=1, then finally Q=1

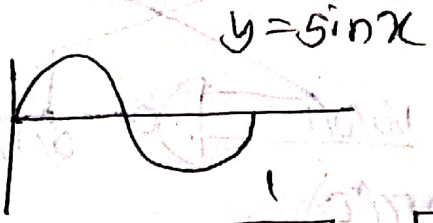
Block Diagram:



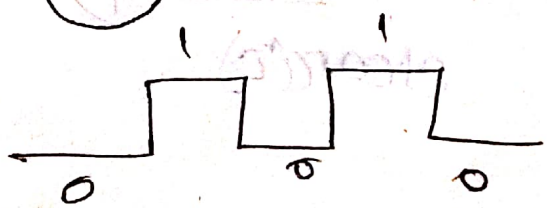
S	C	→ Q
0	0	→ Invalid
0	1	→ 1
1	0	→ 0
1	1	→ No change

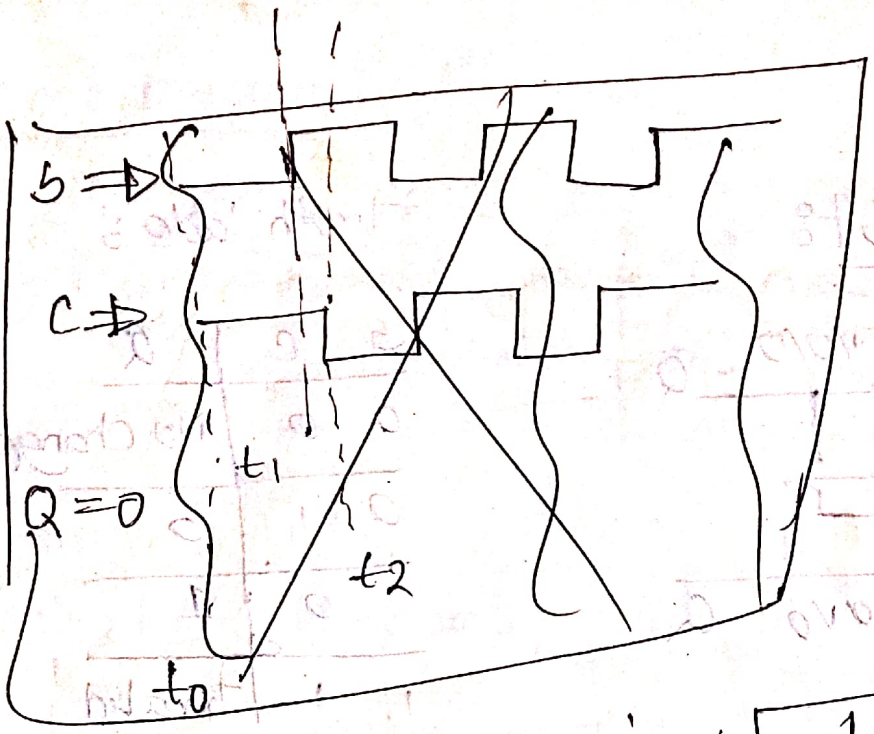
Waveform diagram:

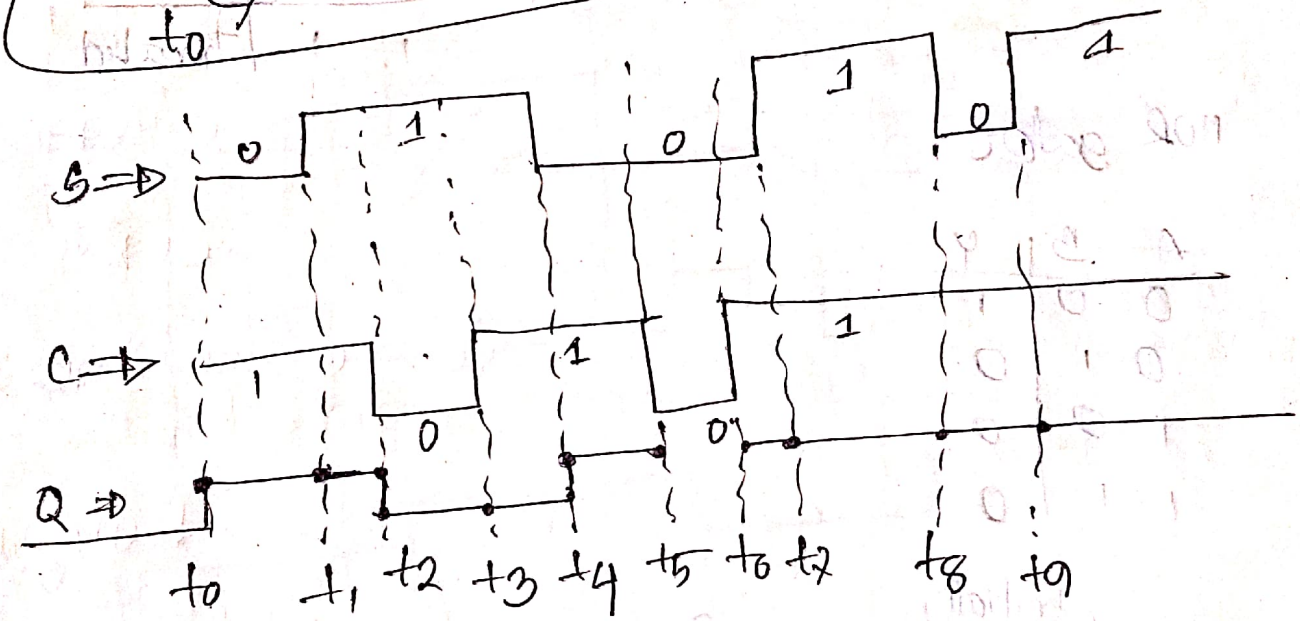
Sine wave

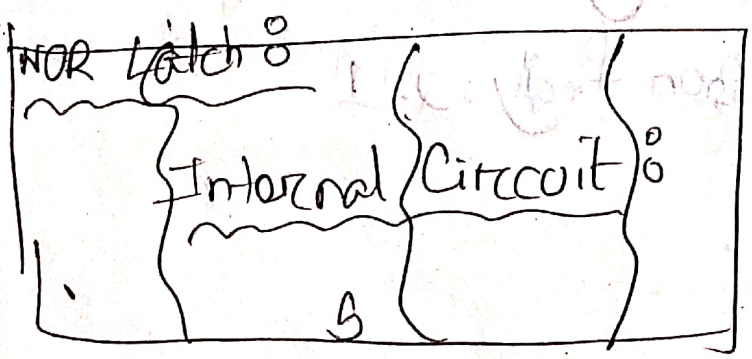


Square wave



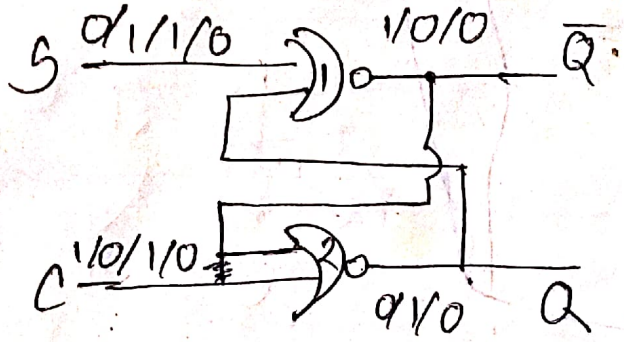

S
C
Q=0
t1
t2
t0


S
C
Q
0
1
0
1
0
1
0
1
1
0
0
1
t0
t1
t2
t3
t4
t5
t6
t7
t8
t9


NOR Latch
Internal Circuit
S

NOR Latch:

Internal Circuit:



Truth Table:

S	C	Q
0	0	No Change
0	1	0
1	0	1
1	1	Invalid

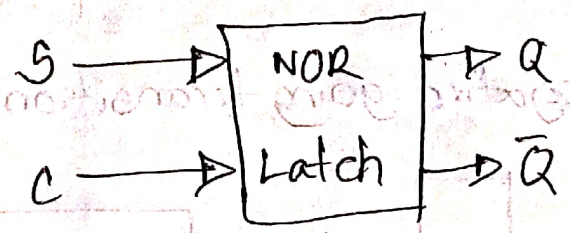
NOR gate:

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

(0,0) If Initially Q=0, then finally Q=0,

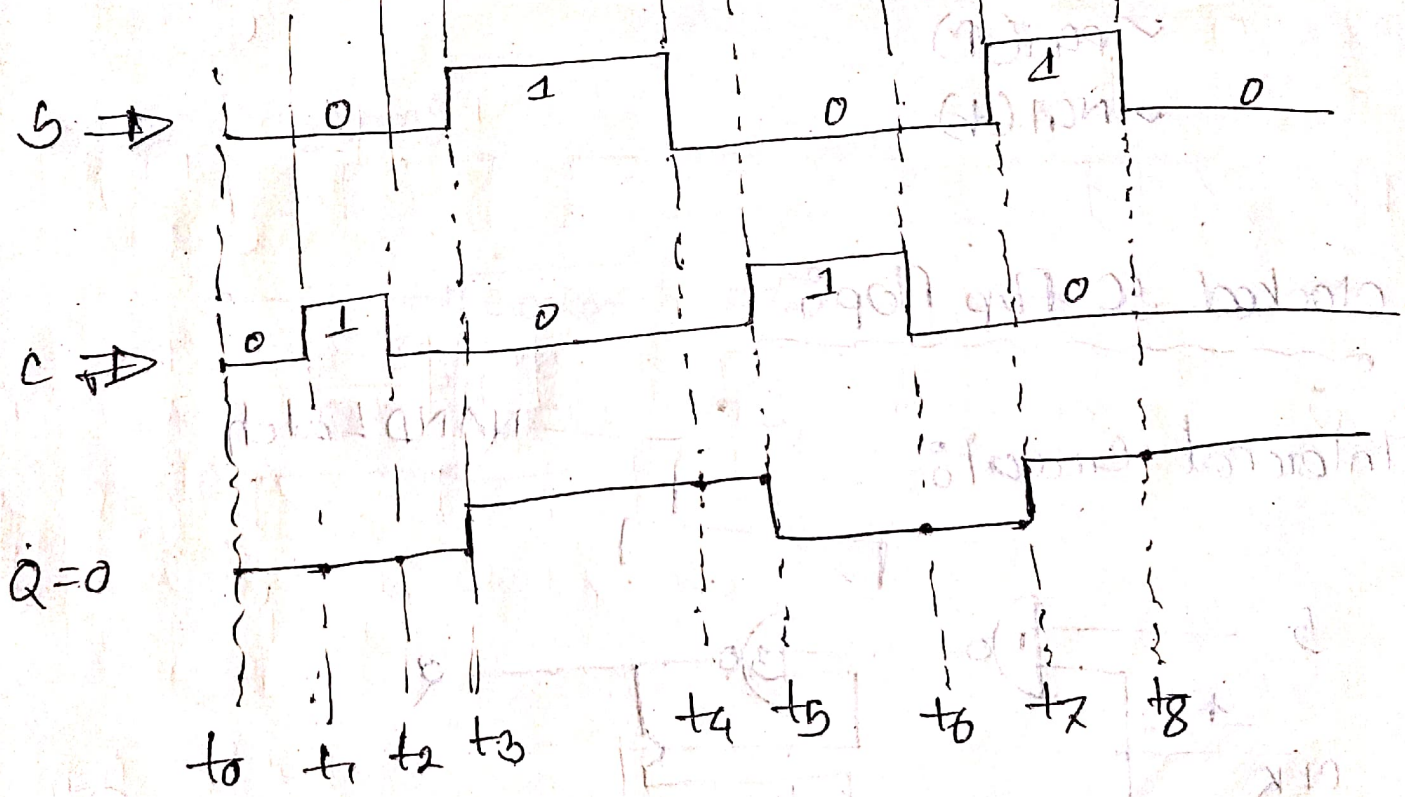
(0,0) If Initially Q=1, then finally, Q=1

Block Diagram:



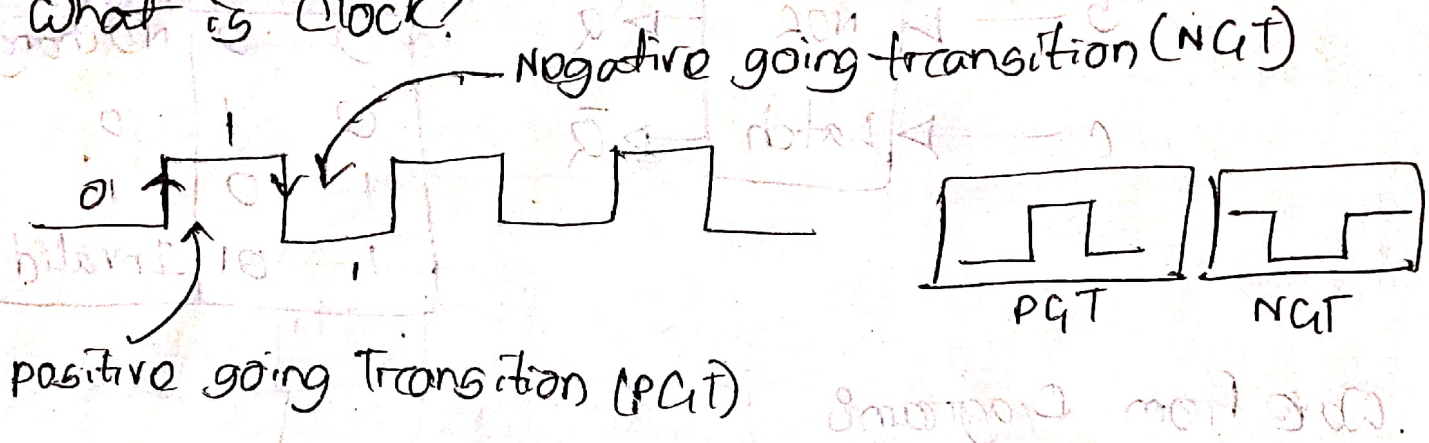
S	C	Y
0	0	No change
0	1	0
1	0	1
1	1	Invalid

Wave from Diagram:



Clock :

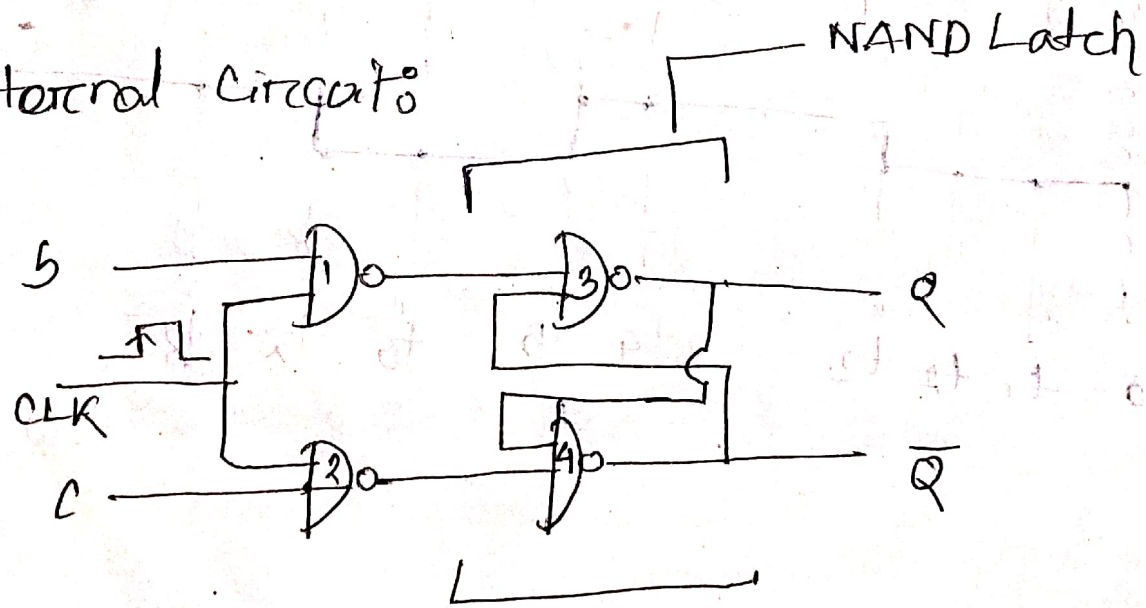
What is Clock?



- ✓ PGT(↑)
- ✓ NGT(↓)

Clocked SC Flip flop :

Internal Circuit :



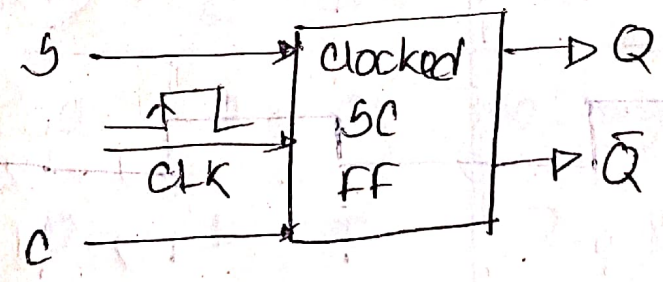
TT

S	C	CLK	Q
0	0	↑	No change
0	1	↑	0
1	0	↑	1
1	1	↑	Invalid

NAND Latch

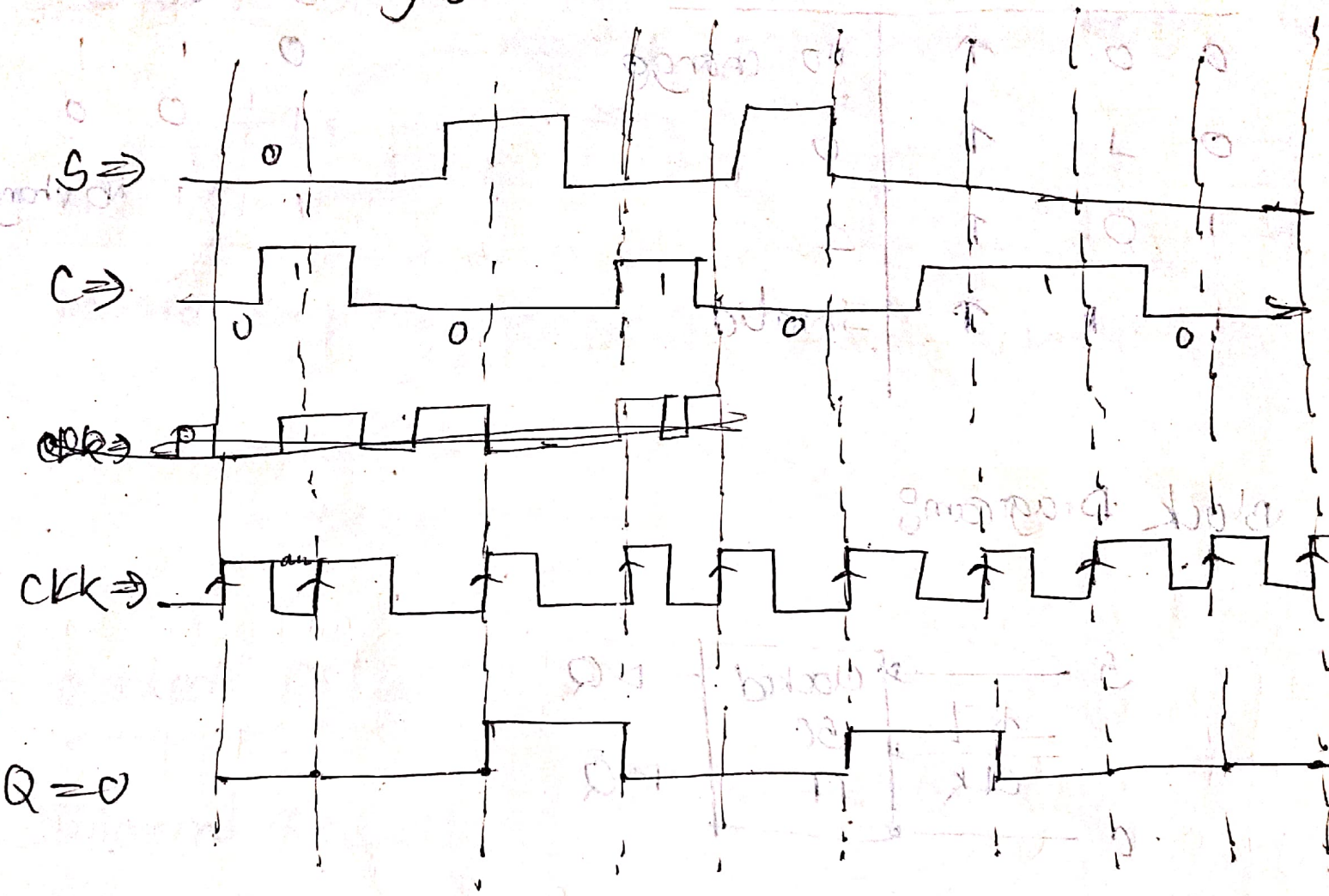
S	C	Q
0	0	Invalid
0	1	1
1	0	0
1	1	No chang

Block Diagram:



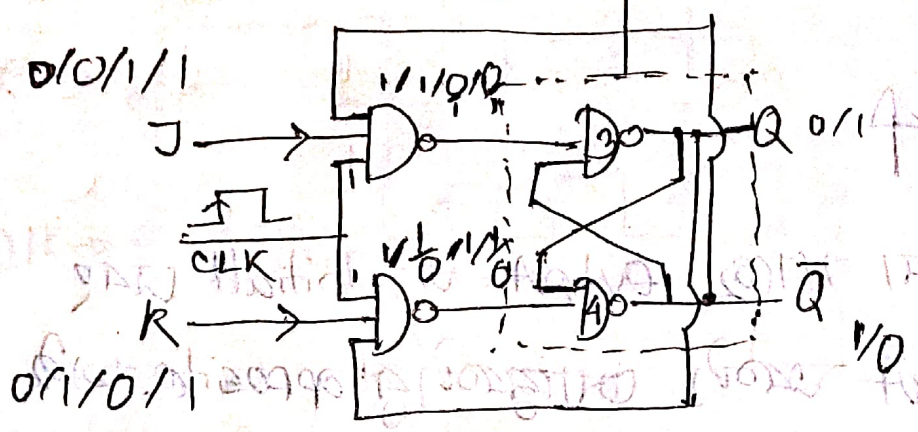
06-02-2022

Waveform diagram of Clocked S-R Flip Flop:



Clocked JK Flip Flop:

Internal Circuit:



NAND Latch

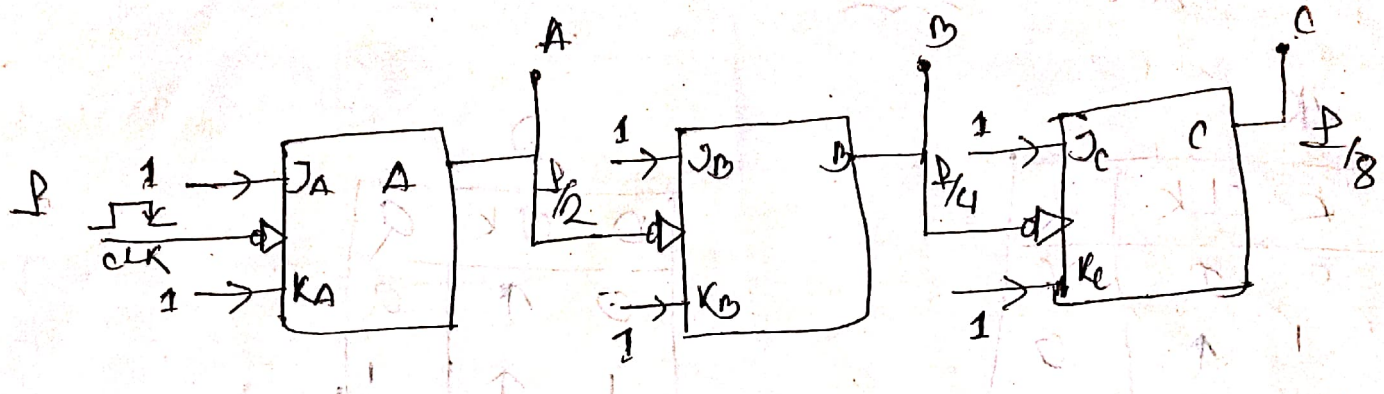
S	C	Q
0	0	Invalid
0	1	1
1	0	0
1	1	N.C

Truth Table:

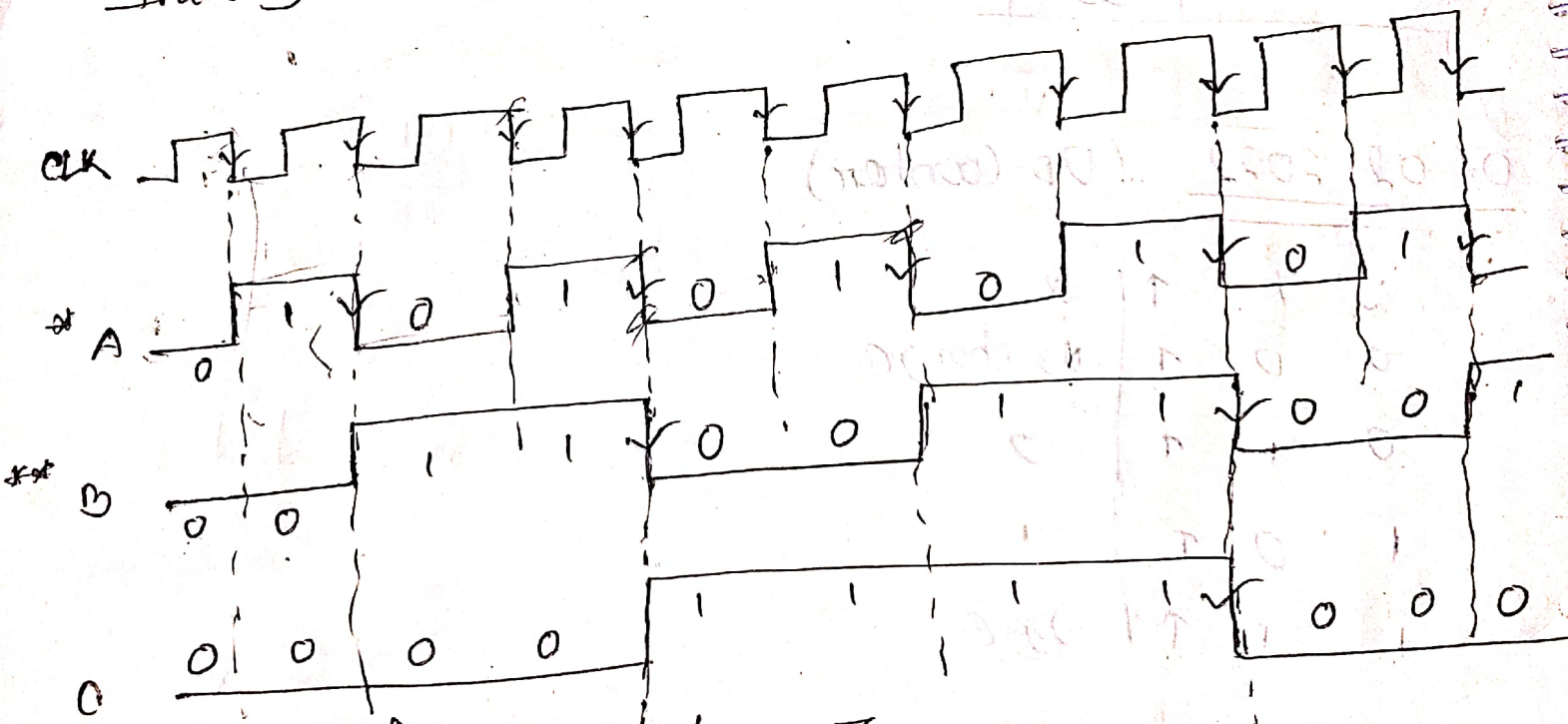
J	K	CLK	Q
0	0	↑	No Change
0	1	↑	0
1	0	↑	1
1	1	↑	Toggle

(0,1) = If initially Q=0, finally Q=0
If " Q=1, " Q=1

(1,0) = If initially Q=0, finally Q=1
If initially Q=1 finally Q=1



Initially A = B = C = 0



It counts from 0 to 7

frequency is number of cycles per second.

$$\text{Output frequency} = \frac{f.F}{2^N}$$

N → Number of inputs

Convert "JK" flipflop to "D" flipflop:

JK

J	K	CLK	Q
0	0	↑	NC
0	1	↑	0
1	0	↑	1
1	1	↑	Toggle

D

D	CLK	Q
0	↑	0
1	↑	1

07-02-2022 (Up-Counter)

J	K	↑	Q
0	0	↑	No change
0	1	↑	0
1	0	↑	1
1	1	↑	Toggle

Application of Flip Flop:

Frequency division and Counting

(P.T.O)

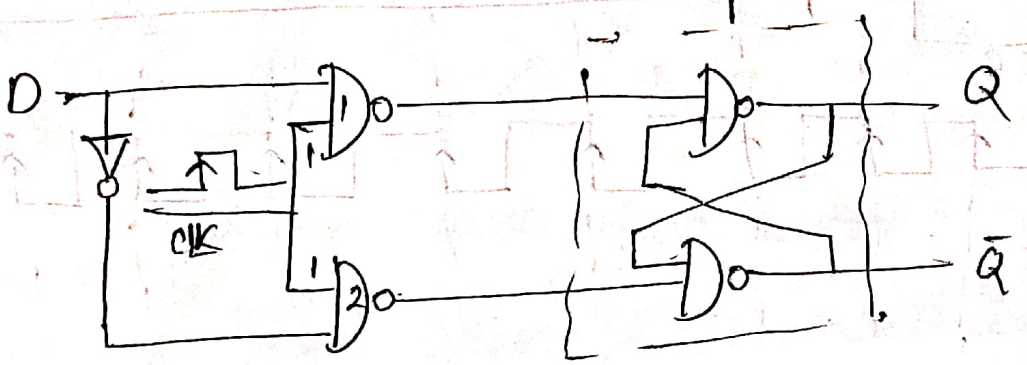
Mod 8 Counter: (Up counter)

Clocked D flip flop:

Internal Circuit

NAND Latch

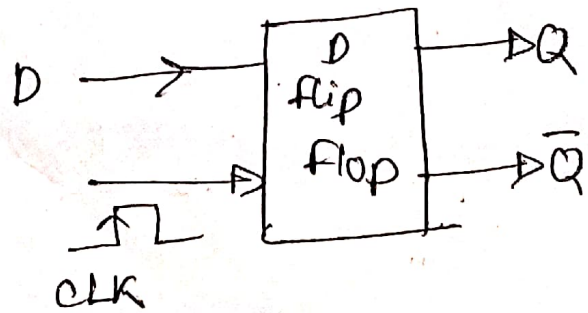
0	0	Invalid
0	1	1
1	0	0
1	1	NC

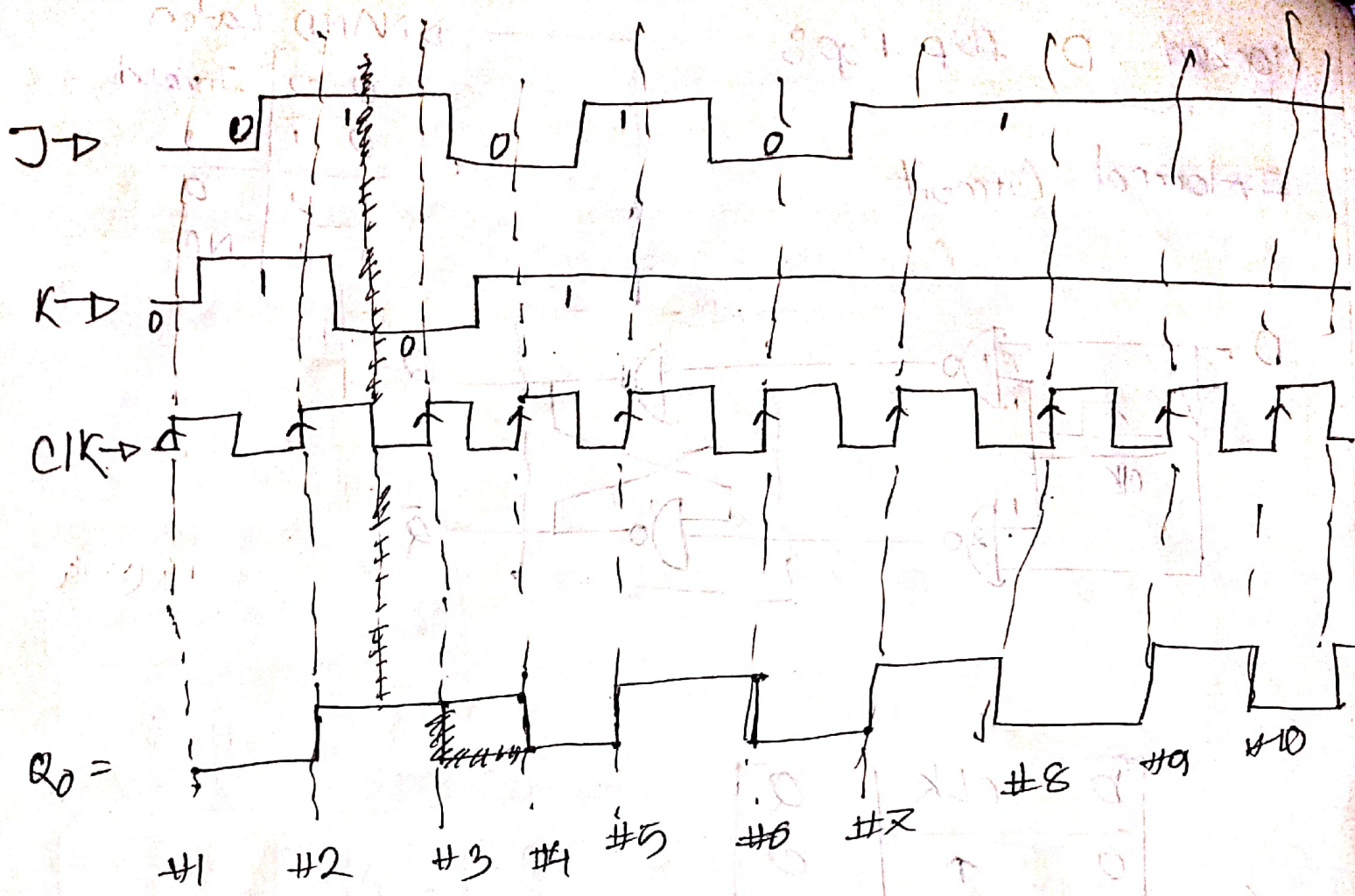


D	CLK	Q
0	↑	0
61	↑	1

operation:

Block Diagram:

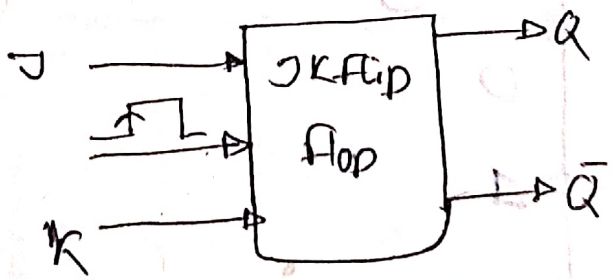



J
K
CLK
Q_0 =
#1
#2
#3
#4
#5
#6
#7
#8
#9
#10

(1, 1) ⇒ [If Initially Q = 0, finally Q = 1
If Initially Q = 1, finally Q = 0]

[এখানে দেখা যাচ্ছে, ~~output এ~~ Initial এবং final output এদের একে অপরের opposite তাই একে Toggle বলা যায়/হয়]

▸ Block Diagram:



Truth Table:

J	K	clk	Q
0	0	↑	NC
0	1	↑	0
1	0	↑	1
1	1	↑	Toggle

Waveform diagram:

(P.T.O)

Mod Number is the number of different steps of the counter.

No. of FFs	Mod Number	Range
2	4 $= 2^2$	
3	8 $= 2^3$	→ 0 to 7
4	16 $= 2^4$	→ 0 to 15
5	32 $= 2^5$	→ 0 to 31
6	64 $= 2^6$	→ 0 to 63

Mod Number of any counter $= 2^n$

Here,
n = number of flip flop

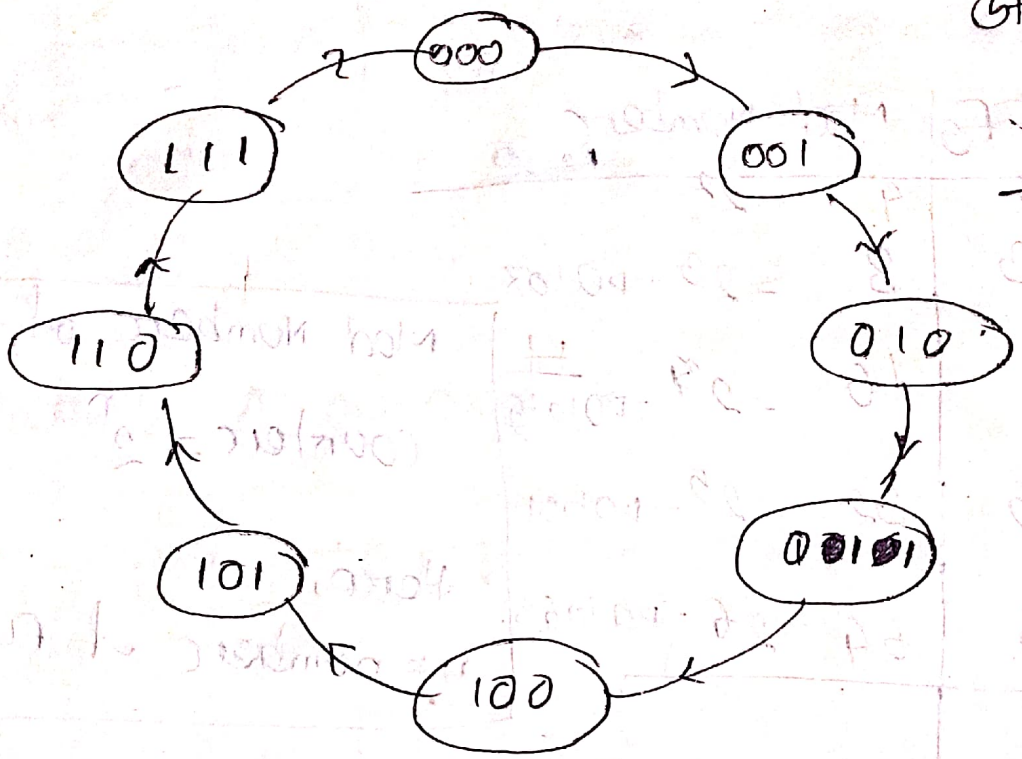
$$\boxed{\text{Output frequency of the counter} = \frac{\text{Input freq}}{\text{Mod Number}}}$$

Range of Counter = 0 to Mod Number − 1

or = 0 to $2^n - 1$, n is the NO of Inputs

State transition Diagram:

For Mod 8 counter



If initial state is 000, find the state after 11 pulses

50%8 = 2

State: 010

Step তত্ত্ব Binary number to তত্ত্ব Ans.

Initial state is 101 the state after 105 pulse,

105+5 = 110

110%8 = 6 তত্ত্ব Binary

State: 110

$$\begin{array}{r|l} 6 & 110 \quad 13 \\ & 8 \\ \hline & 30 \\ & 24 \\ \hline & 6 \end{array}$$

Question 1

(a) Mod Num $= 2^6 = 64$

(b) Output freq $= \frac{\text{Input freq}}{64} = \frac{1 \times 10^3 \text{ KHz}}{64}$ ~~= 15.625Hz~~

$= 15.625$ KHz

(c) Range → 0 to 63

(d) 0+ 129 = 138 138%64

$$\begin{array}{r|l|l} 64 & 138 & 2 \\ & 128 & \\ \hline & 10 & \end{array}$$

State : 001010

#

Considere a counter circuit that contains 5x FFs wired in the arrangements Q5 Q4 Q3 Q2 Q1 Q0

(a) Determined the counters MOD number.

(b) Determine the output frequency in KHz when input freq in 1 MHz

(c) Range of the counter

(d)

~~1024~~ (a) ~~512~~ ~~512~~ $2^{10} \rightarrow 1024 \rightarrow 10$

(b) $\frac{2 \times 10^3 \times 10^3}{10} = 3.906$ KHz $\quad$ 1953.125 Hz

$= 3906$ Hz

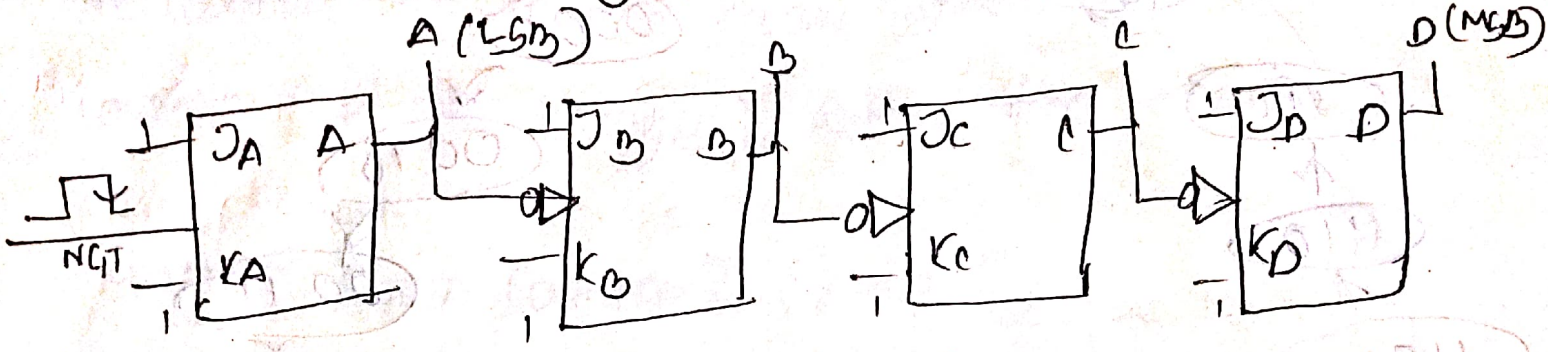
(c) 1024 $\quad$ $2^n = 1024$

(d) 1100 12

Next week Quiz Chapter 5.6

09-02-2022

Draw the circuit diagram of MOD 16 counter?



Q

(1) Consider a MOD 16 counter

$2^4 = 16$

- If initially 1011 state determine the output after 83 pulses.

⇒ ⊙# 1011 = 11

50, ~~1~~ 11 + 83 = 94

50, 94 % 16 = 14

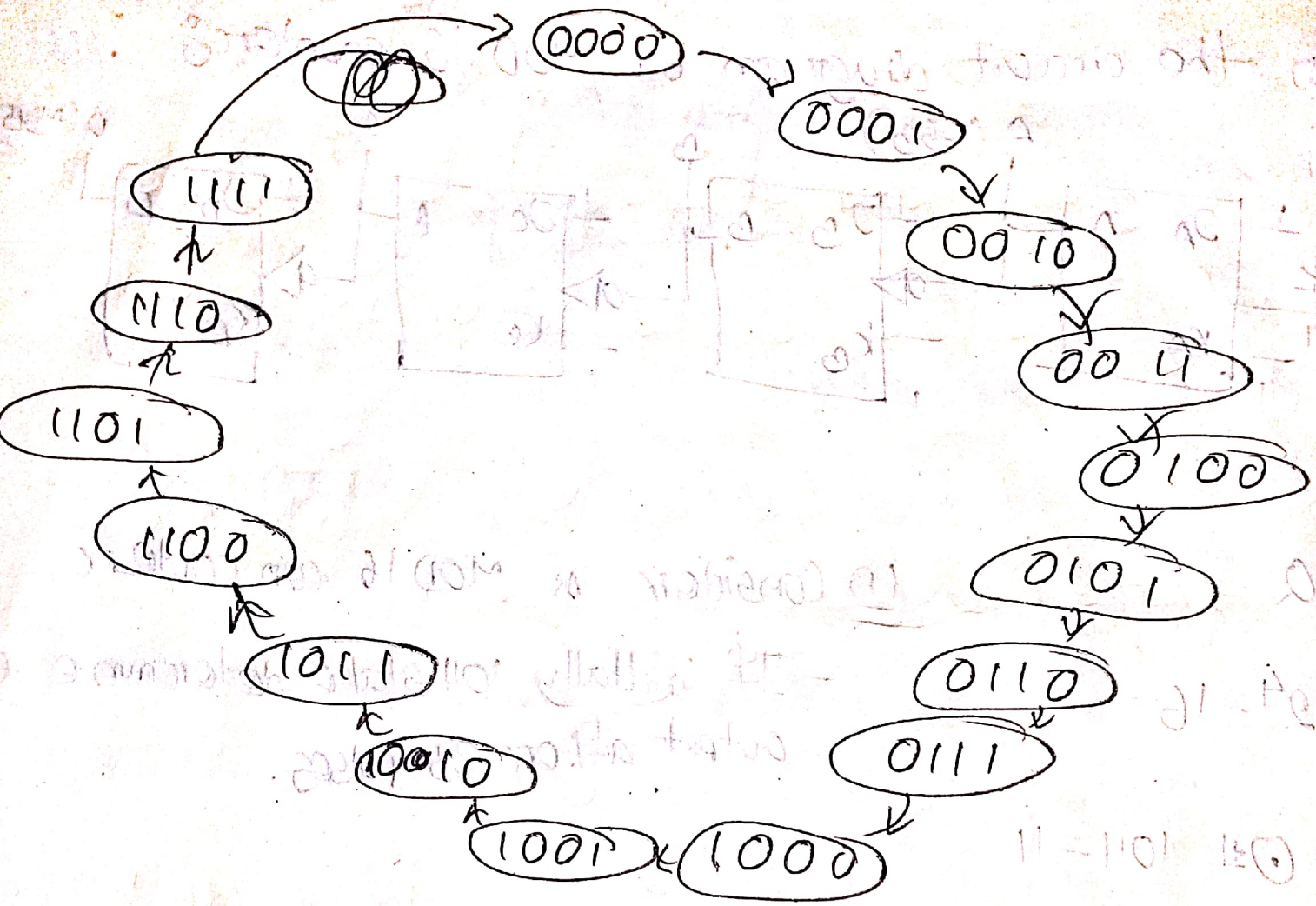
50, 1110

(2) If the input 10MHz, what is the output in KHz

- $\frac{10 \times 10^3}{16} = 625$ KHz

(3) Draw the state transition diagram of the counter.

(3)

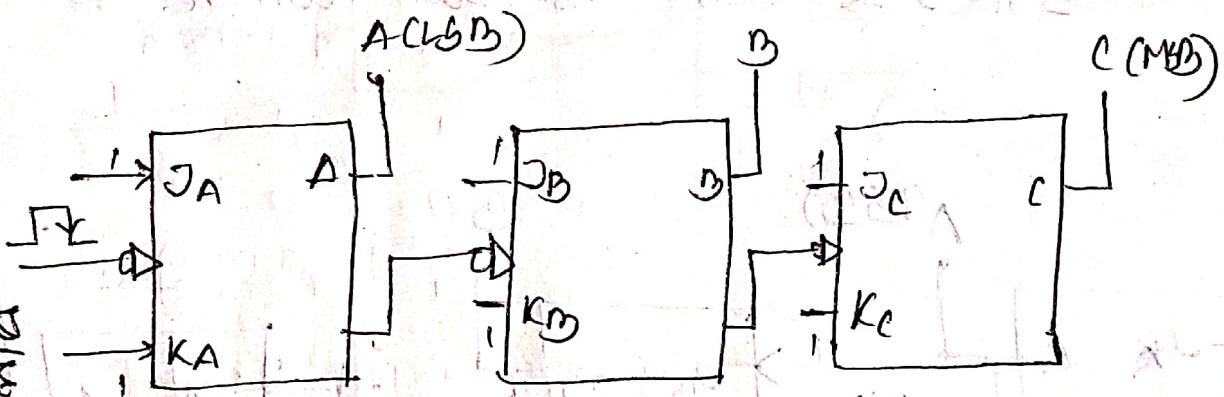

0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111

Down Counter

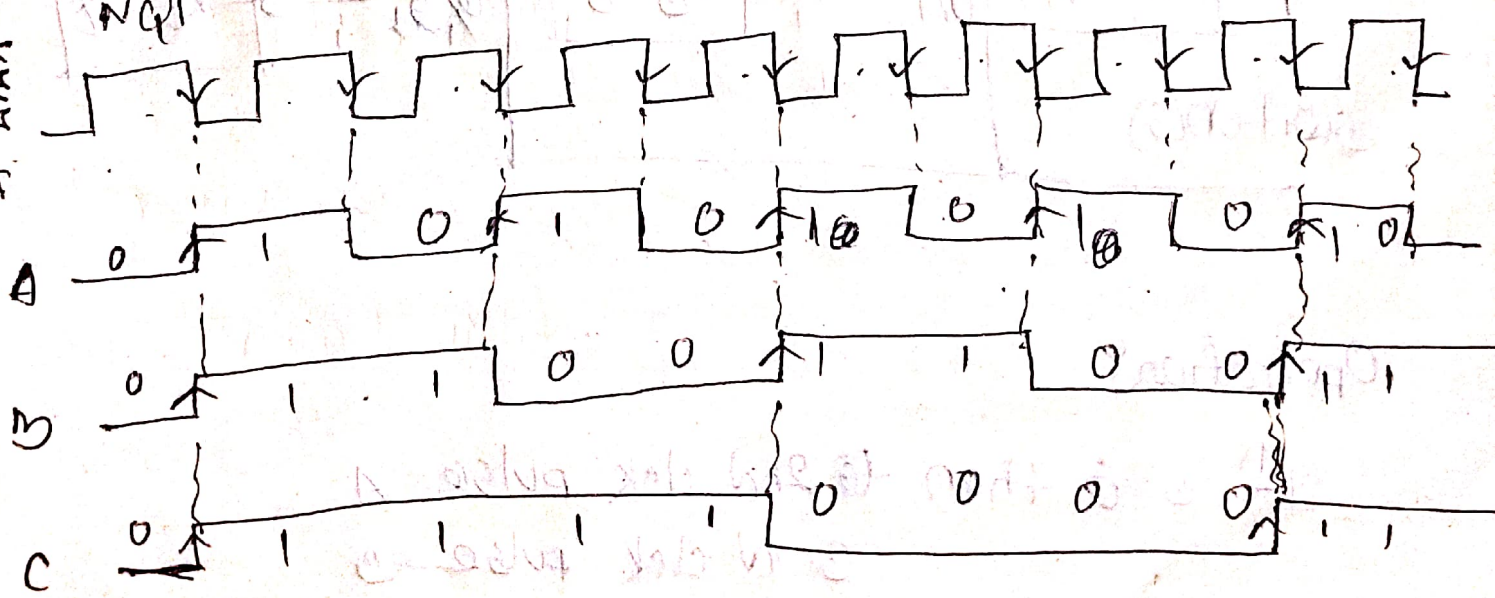
The counter that counts from highest number to the lowest (of the range) within the range

MOD 8 Down Counter: (7 to 0)

Circuit Diagram



Initially A=B=0



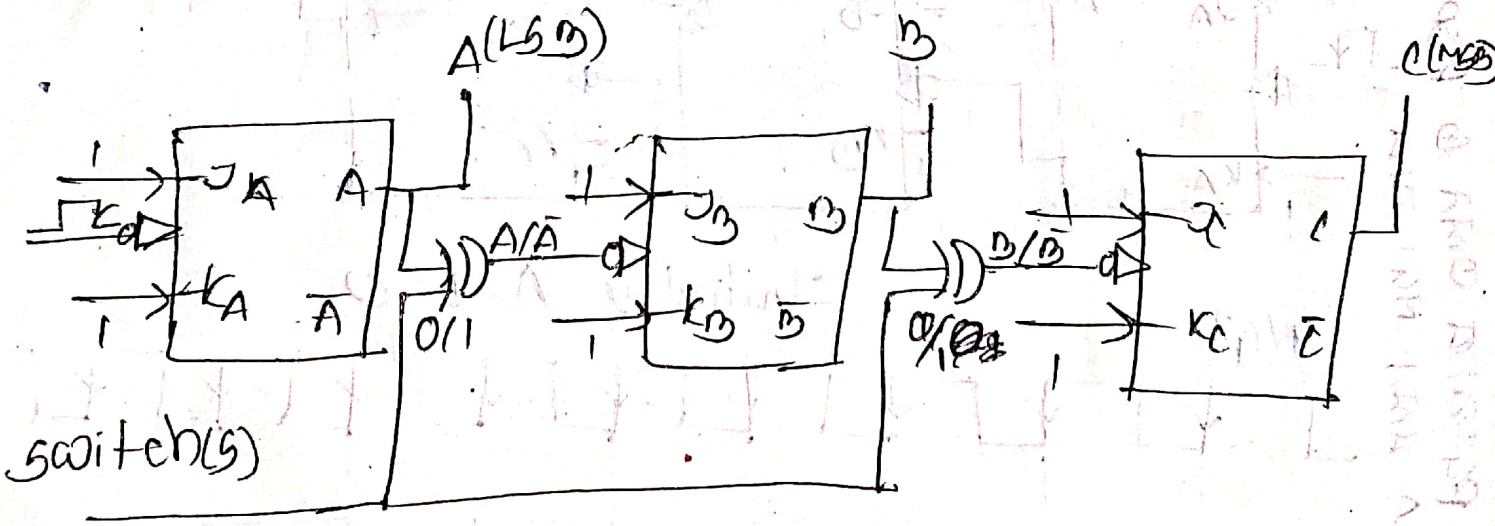
It counts 7 to 0. Therefore it is MOD 8

Down counter

Design a MOD 8 counter (up/Down) using JK flipflops.

You can use other logic gates if you necessary.

⇒ Switch(S): If S=0, then MOD 8 up counter
If S=1, then MOD 8 down counter



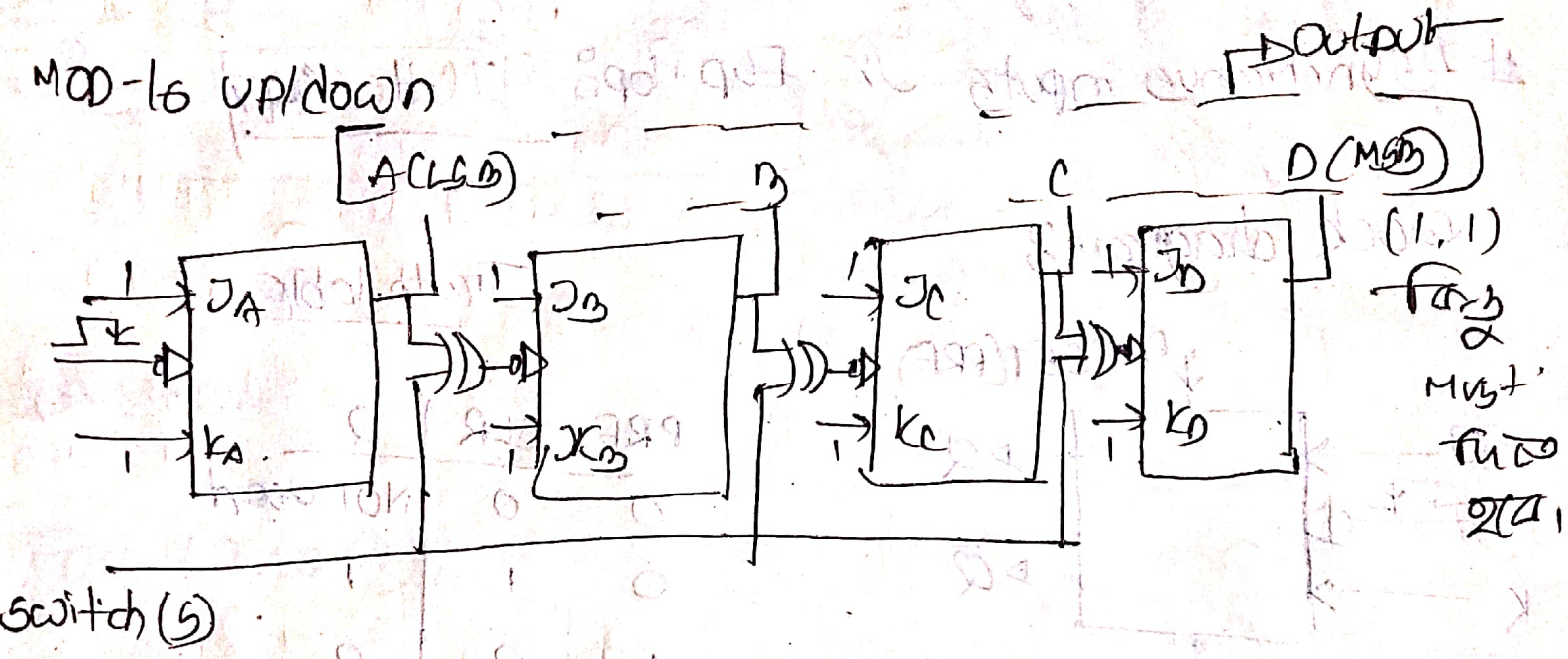
Operation:

If S=0 then 2nd clck pulse = A
3rd clck pulse = B

∴ Therefore this is up counter.

If S=1, then 2nd clk pulse = $\bar{A}$
then 3rd clk pulse = $\bar{B}$ } counter is down counter.

MOD-16 up/down



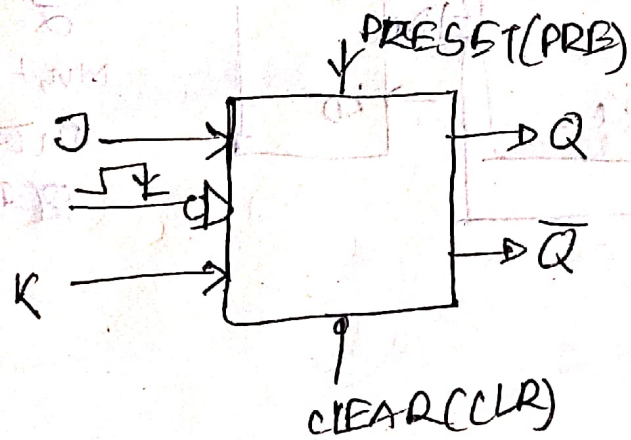
10-02-2022

MOD 8, MOD 16, MOD 32, MOD 64, MOD 128

2^N counter

Asynchronous inputs JK flip flop: IC# 7476

block diagram:

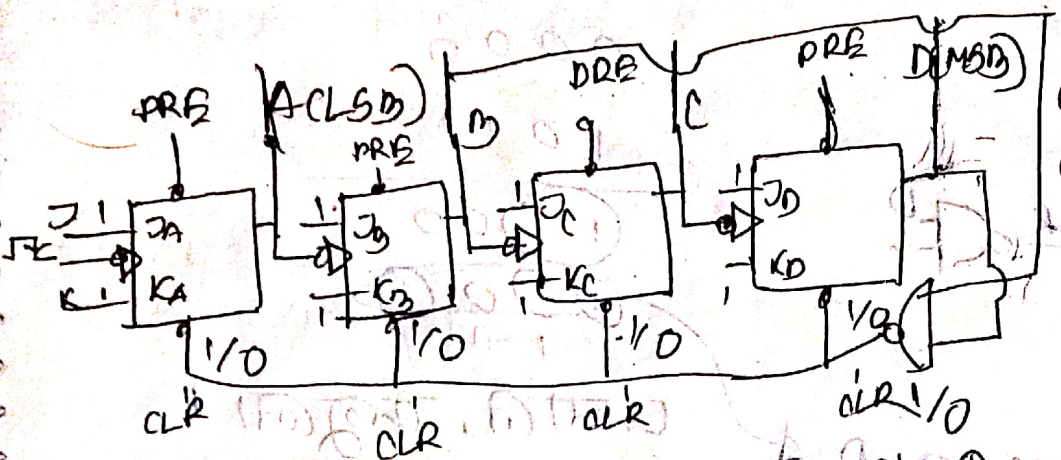


Truth Table

PRE	CLR	Q
0	0	NOT USED
0	1	1
1	0	0
1	1	Normal clock operation

Design MOD 10 up counter:

(P.T.O)



Truth table

D	C	B	A	
0	0	0	0	PRE=1
0	0	0	1	CLR=1
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
0	0	0	0	DRE=1
1	0	1	0	CLR=0

অবশ্য

(অ) সাধ কোনো

operation:

For (0 to 9):

PRE=1, CLR=1,

Normal clock operation

It counts from 0 to 9

For 10: PRE=1, CLR=0,

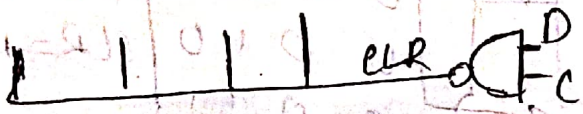
A=B=C=D=0

It counts 0

therefore the counter count from 0 to 9.

So this is MOD 10 up counter

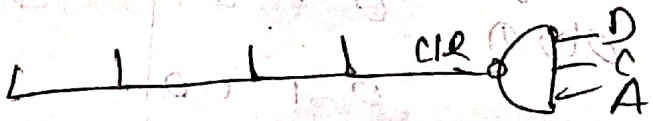
MOD 12 up counter:



D	C	B	A
0	0	0	0
1	0	1	1
1	1	0	0
1	1	0	1

যেখানে, সেগুলো 1 থাকে তা NAND এ Input বলে দিবো।

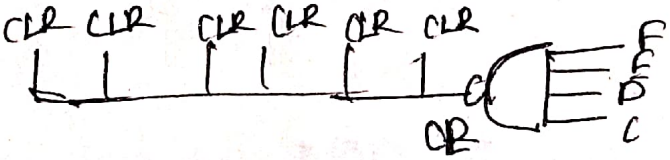
MOD 13 up-C:



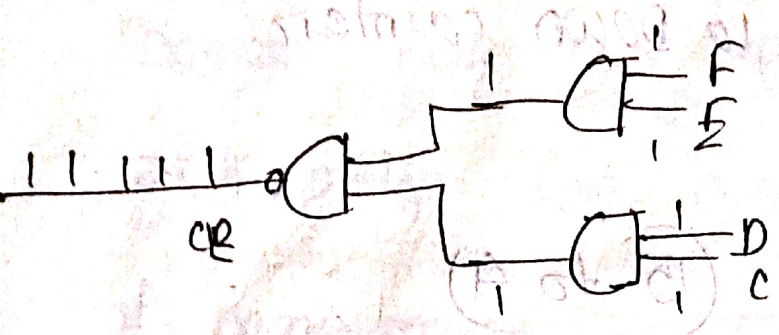
MOD 60: (0 to 59)

60

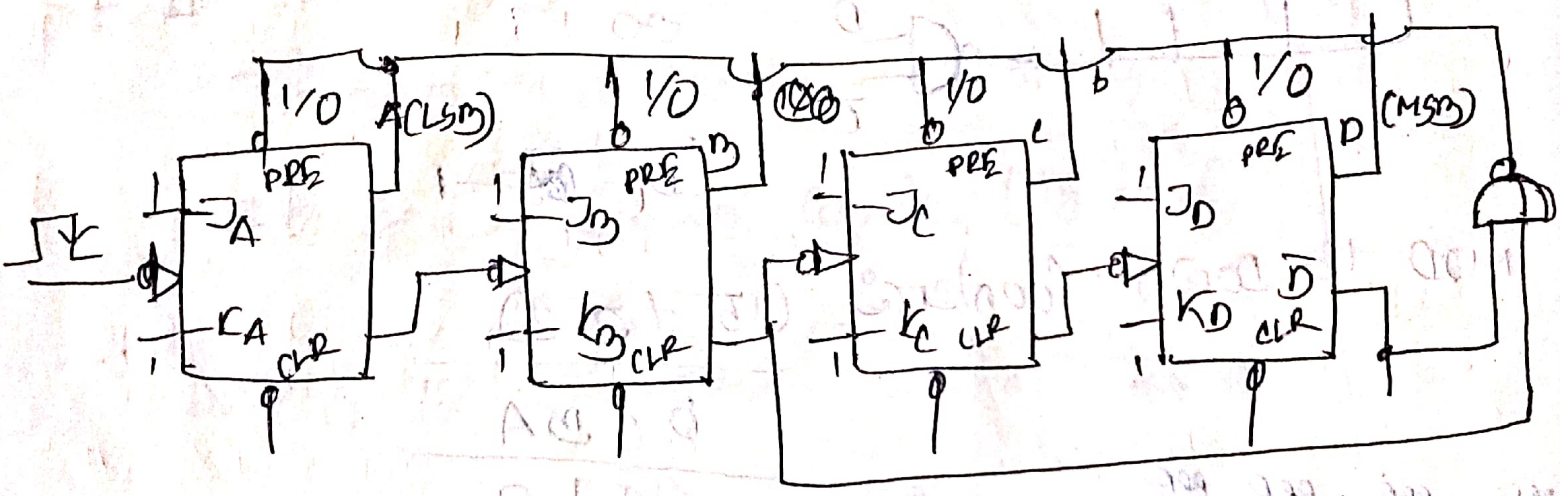
32	16	8	4	2	1
1	1	1	1	0	0
F	E	D	C		



2 Input NAND gate:



Asynchronus
MOD 10 Down counter:



operation:

For 15 to 6: PRE=1, CLR=1

∴ It counts from 15 to 6.

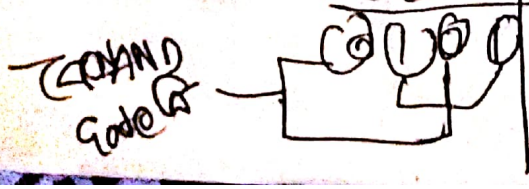
For 5: PRE=0, CLR=1,

∴ A=B=C=D=1

∴ It counts 1111, 22 15, 0 (D.T.O)

D	C	B	A
1	1	1	1
1	1	1	0
1	1	0	1
1	1	0	0
1	0	1	1
1	0	1	0
1	0	0	1
1	0	0	0
0	1	1	1
0	1	1	0

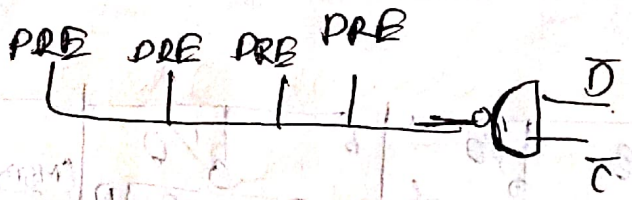
DCBA
0101



→ The counter counts from 15 to 6.

It is MOD 10 DOWN counter

MOD 12 DOWN Counter: (15 to 4)

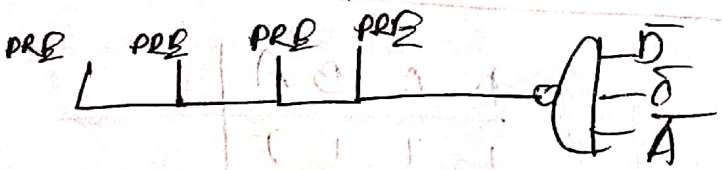


D	C	B	A
0	0	1	1

$\overline{D} = \overline{C} = 1$

MOD 13 DOWN Counter: (15 to 3)

D	C	B	A
0	0	1	0



$\overline{D} = \overline{C} = \overline{A} = 1$

Assigment Number 28

Design MOD 10 Asynchronous up/Down Counter using JK FlipFlop. You can use other logic gates, if necessary.

⇒ Switch (S):

If S=0, UD counter (0 to 9)

If S=1, Down counter (15 to 6)

Date: 17.02.2022 within 2P.M

13-02-2022

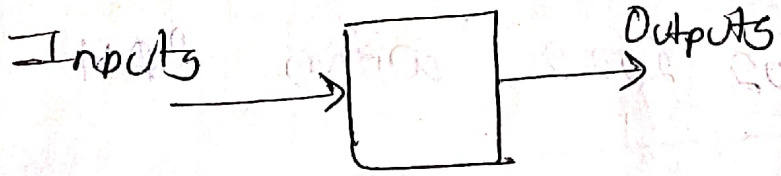
Propogation Delay (tpd):

What is tpd?

For any devices to ~~get~~ give the ~~ip~~ inputs and

response for output, it takes some time. This

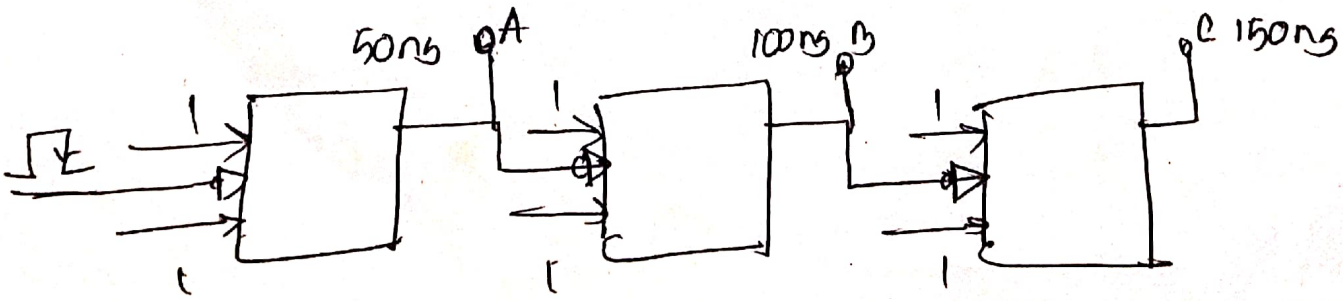
time is called propogation delay.



JK flip flop ⇒ tpd ⇒ 50 ns $= 50 \times 10^{-9}$ seconds

AND gate ⇒ tpd ⇒ 20 ns $= 20 \times 10^{-9}$ seconds

MOD 8 asynchronus up counter:



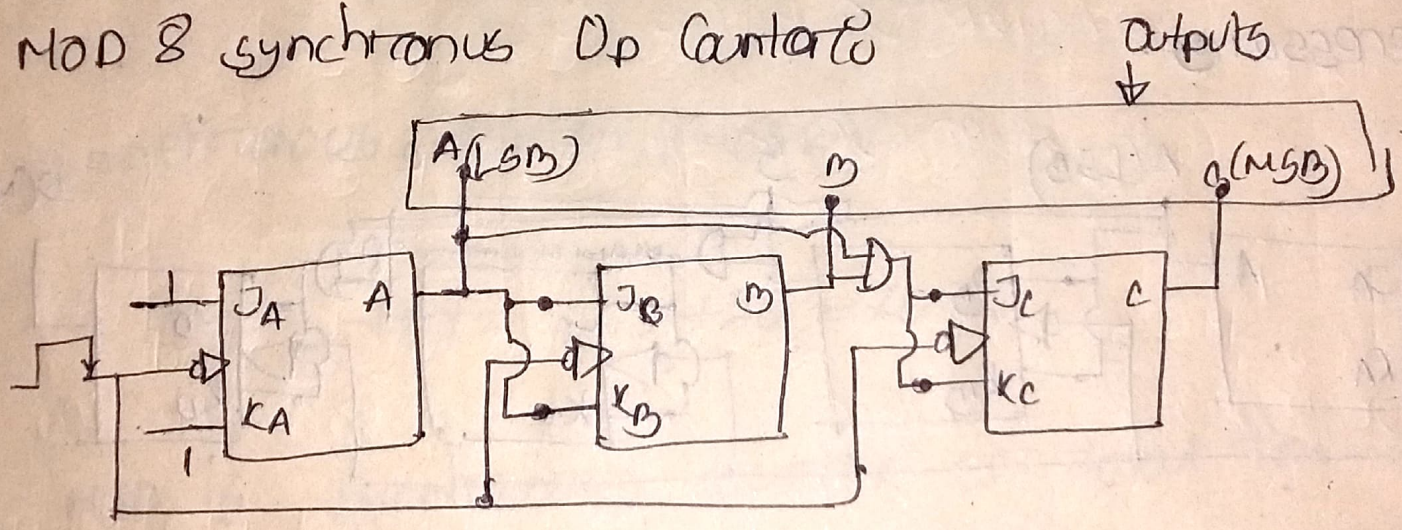
Asynchronus Counter: All the outputs do not response together.

[All counter before this are asynchronus]

Synchronus counter:

All the outputs response together

MOD 8 synchronus Up Counter:



Initially $A = B = C = 0$

A: Toggle

$\rightarrow J_A = K_A = 1$

B: If A=0, then, No change

J_B	K_B
0	0
1	1

If A=1, then

$\therefore J_B = K_B = A$

J	K	clk	Q
0	0	↓	N.C
0	1	↓	0
1	0	↓	1
1	1	↓	Toggle

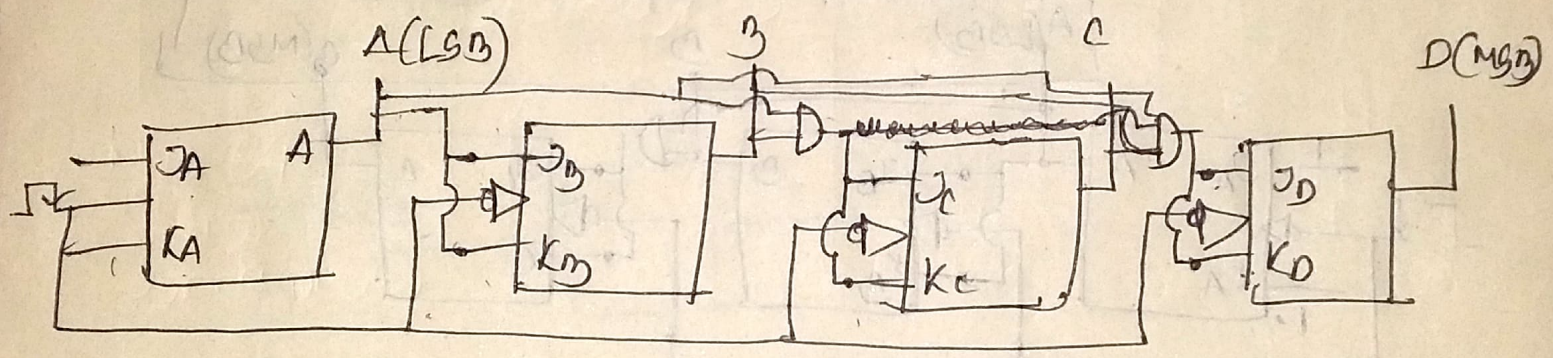
	C	B	A
	0	0	0
#1	0	0	1
#2	0	1	0
#3	0	1	1
#4	1	0	0
#5	1	0	1
#6	1	1	0
#7	1	1	1
#8	0	0	0

.C: If $A=B=1$, then toggle

J_C	K_C
1	1
0	0

otherwise, $J_C = K_C =$ ~~No chang~~ AB

Design MOD 16 synchronus up Counter using JK Flip Flop. You can use other logic gates if necessary.



D: If $A=B=C=1$ then toggle

J_C	K_C
1	1
0	0

otherwise $J_C = K_C = ABC$

MOD 8 asynchronous counter

Total delay = 50×3 = 150ns

In general:

For asynchronous counter, (MOD 8)

Total t_{pd} = t_{pd} for one JK FF × NO of FF

synchronous counter, (MOD 8)

Total t_{pd} = 50 + 20 = 70 ns

MOD 16 synchronous counter ⇒ Total t_{pd} = 70 ns

In general,

For any synchronous counter,

Total t_{pd} = t_{pd} for one JK FF + t_{pd} for one NAND gate

$f = \frac{1}{T}$, Frequency = $\frac{1}{\text{Total } t_{pd}}$

Advantage and Disadvantage:

Synchronous:

Less t_{pd} ← Adv

Disadvantages → More costly

Asynchronous:

Advantage → Less costly

Disadvantage → More t_{pd}.

MOD 64:

Synchronous counter: total delay = 50+20 = 70ns

$$f = \frac{1}{70 \times 10^{-9}} Hz = \frac{1}{70} \times 10^{9}$$

$$= \frac{1}{70} \times 10^{3} MHz$$

$$= 14.3 MHz$$

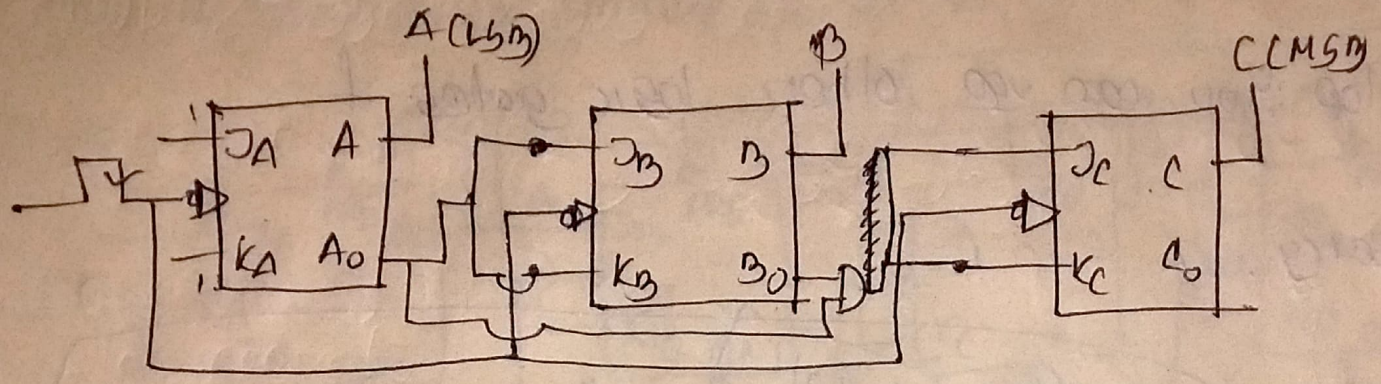
Asynchronous total t_{pd} = 50×6

= 300 ns

$$f = \frac{1}{300 \times 10^{-9}} Hz = \frac{1}{300} \times 10^{9} Hz = \frac{1}{300} \times 10^{3} MHz$$

$$= 3.33 MHz$$

MOD 8 synchronous Down Counter:



Initially $A=B=C=1$,

A: Always toggle.

$\therefore J_A = K_A = 1$

B: If $A=0$, then J_B K_B
1 1

If $A=1$, then 0 0

$\therefore J_B = K_B = \bar{A}$

C: If $A=B=0$, then $J_C = K_C$ (Toggle)
1 1

0 0,

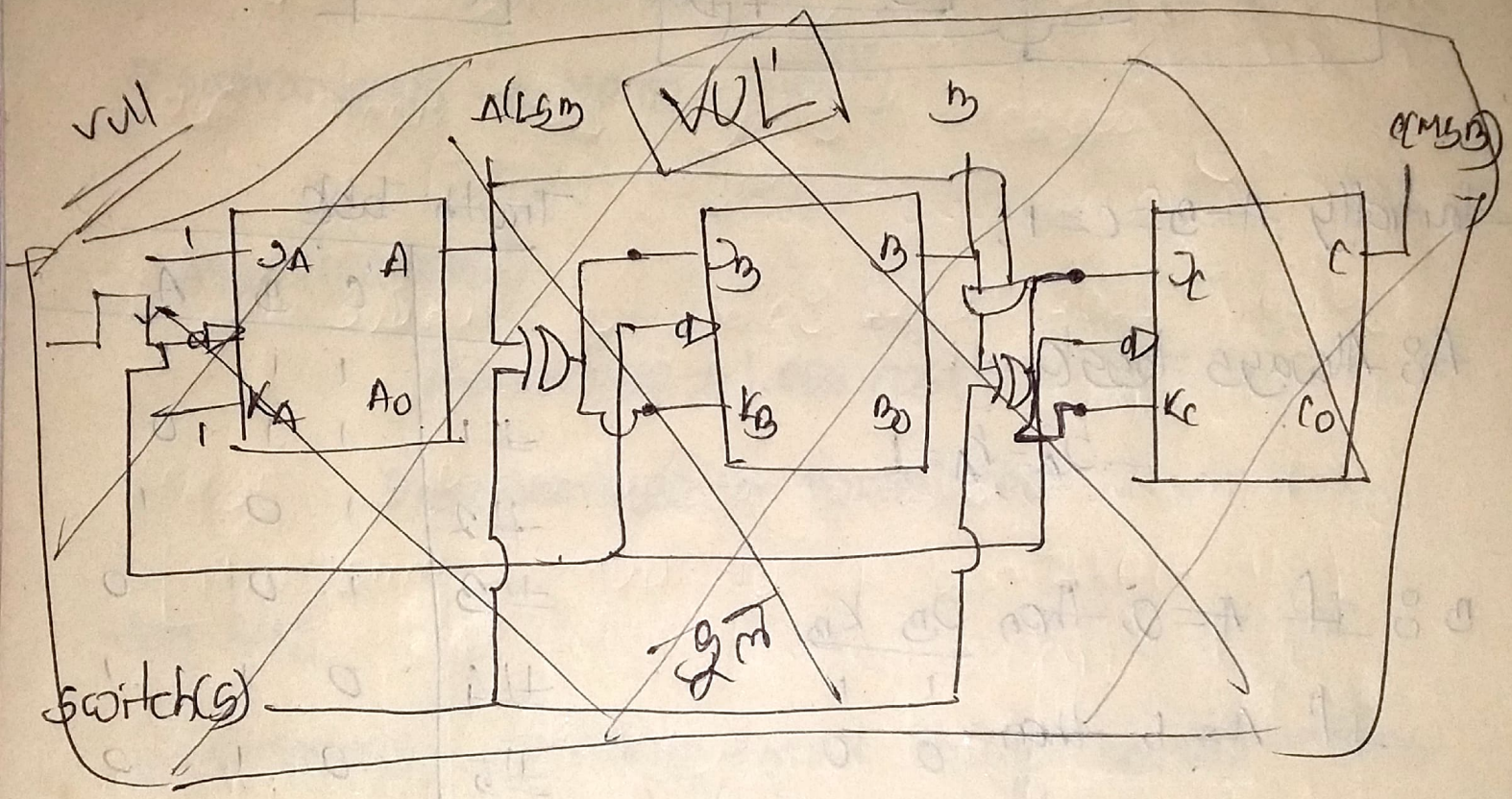
otherwise

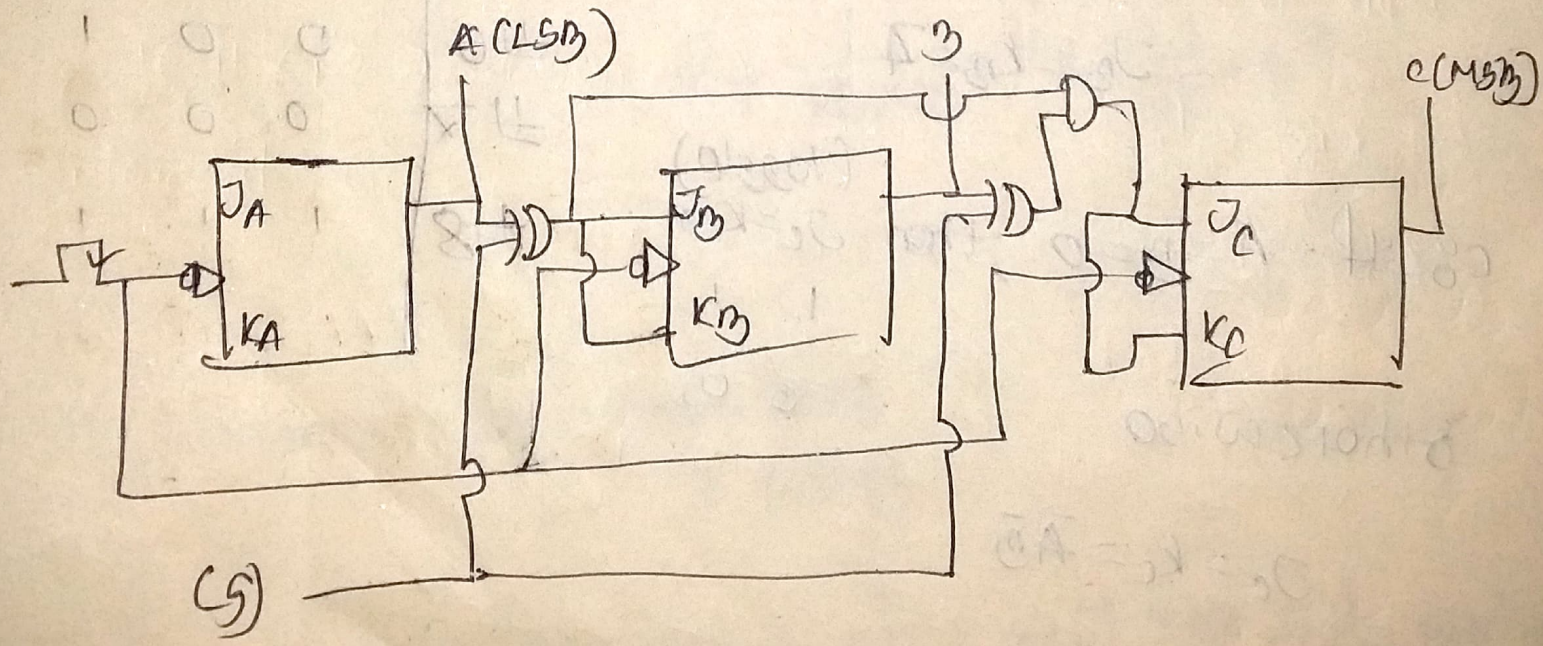
$J_C = K_C = \bar{A}\bar{B}$

Truth table

	C	B	A
	1	1	1
#1	1	1	0
#2	1	0	1
#3	1	0	0
#4	0	1	1
#5	0	1	0
#6	0	0	1
#7	0	0	0
#8	1	1	1

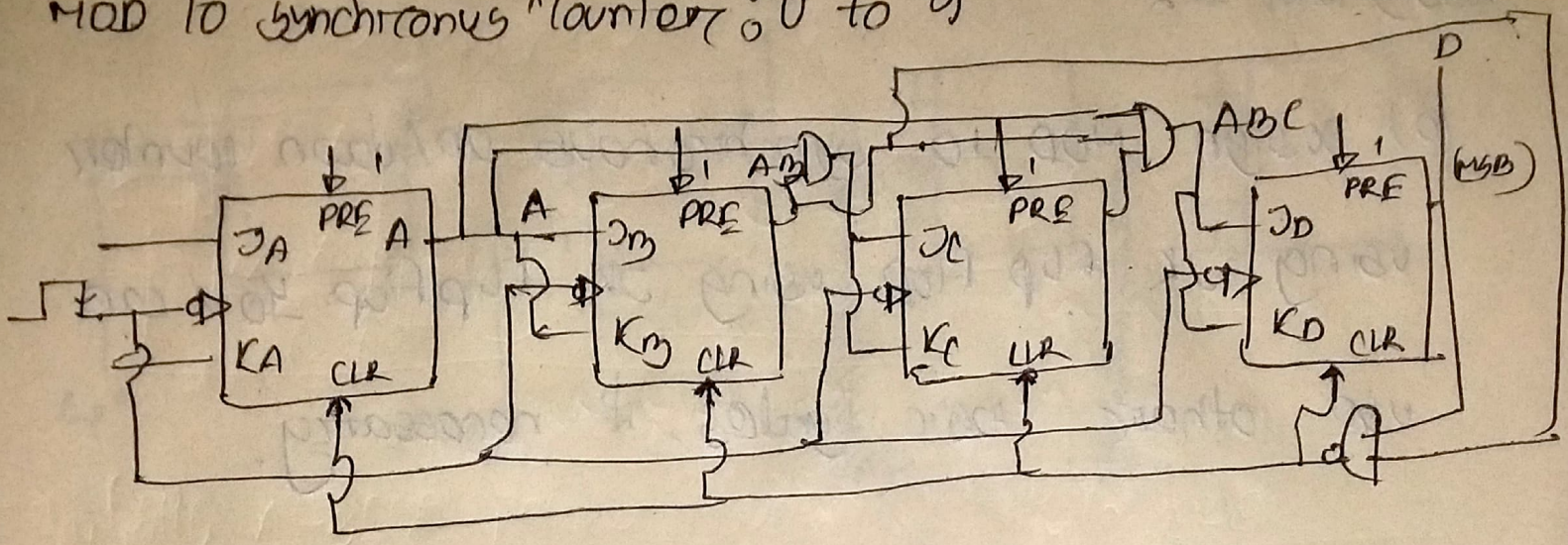
Design MOD 8 synchronous up/down counter using JK Flipflop. You can use other logic gates if necessary.





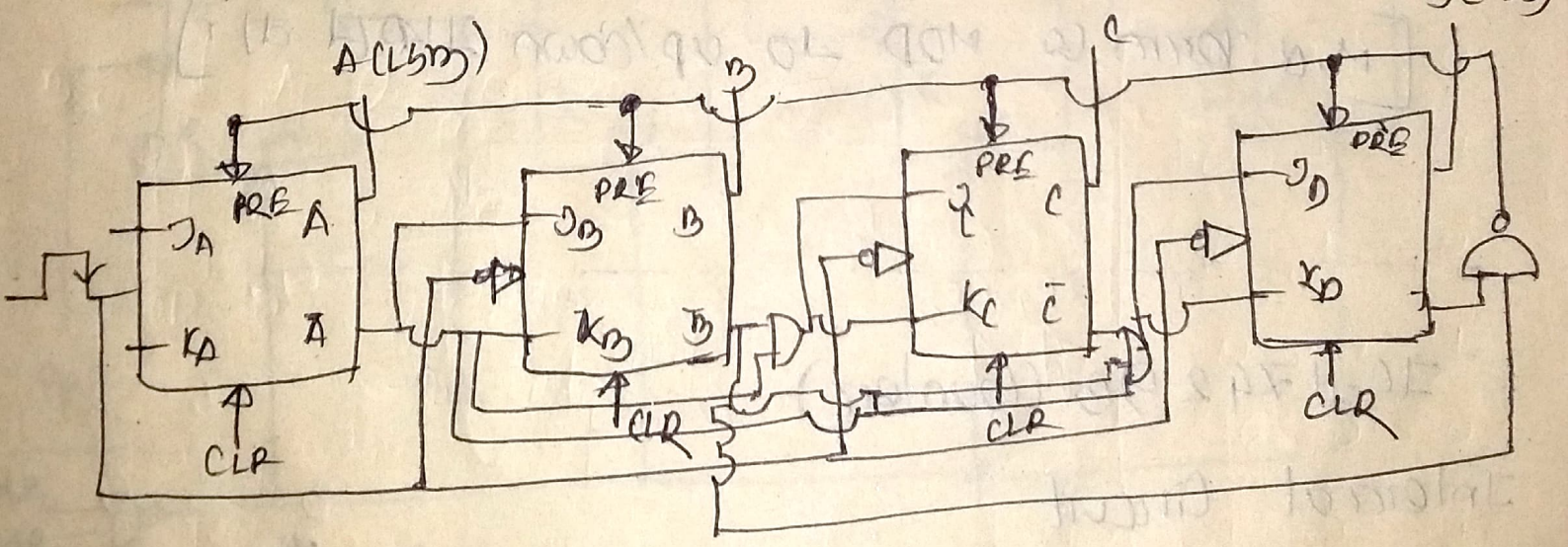
16-02-2022

MOD 10 synchronus UP Counter: 0 to 9



	D	C	B	A
10	1	0	1	0

MOD 10 synchronus Down Counter:



Assigment #2

(b) Design MOD 10 synchronous up/down counter using JK flip flop using JK flip flop. You can use other logic gates, if necessary.

Submit last date: 22.02.2022 Tuesday

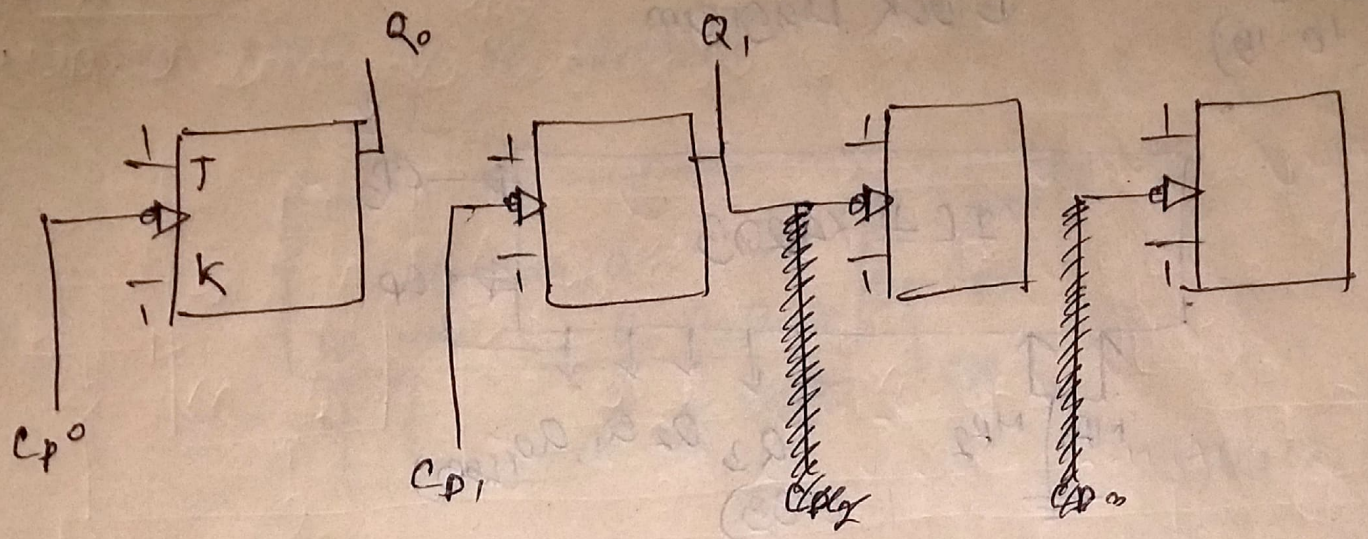
11 PM

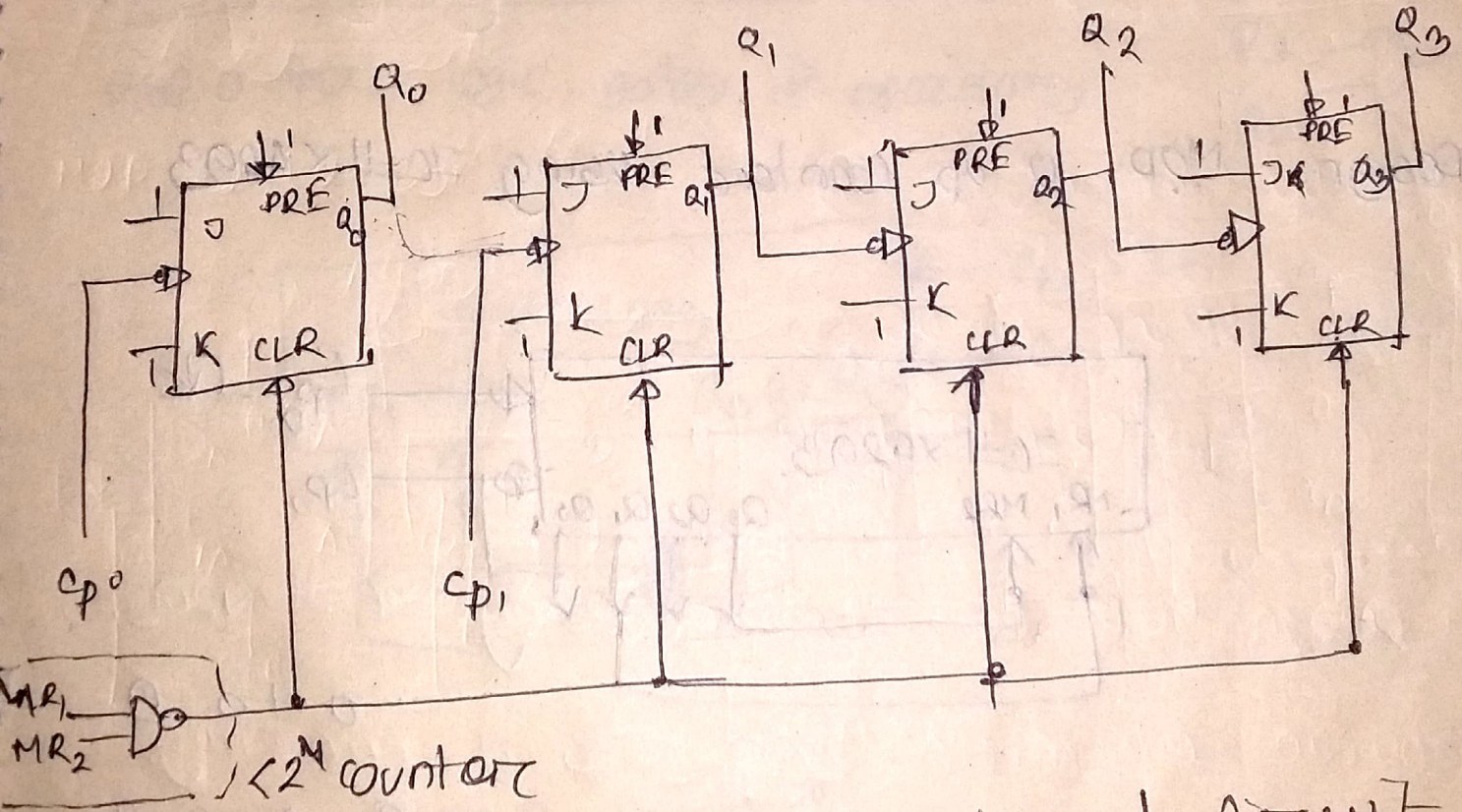
[Mid Term এ MOD 10 up/down আসবে না]

IC #74293 (Counter)

Internal Circuit

(P.T.O)





$CP_0 \rightarrow$ clock pulse 0

$CP_1 \rightarrow$ clock pulse 1

$MR_1 \rightarrow$ Master Reset 1

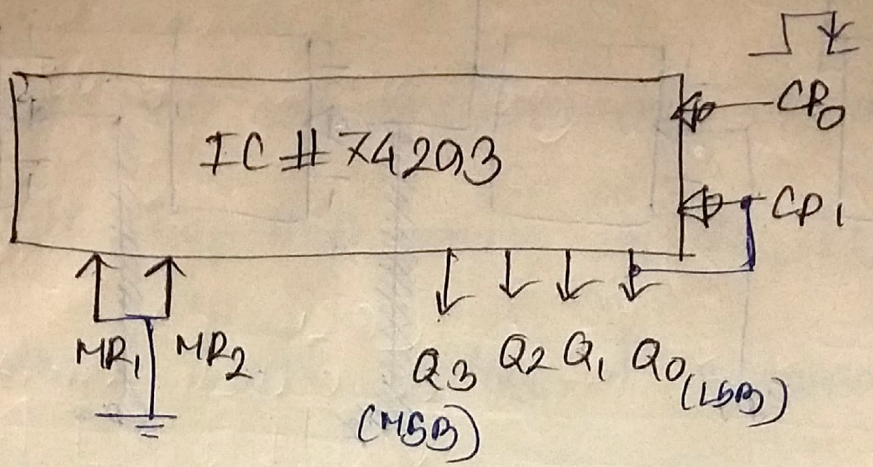
$MR_2 \rightarrow$ Master Reset 2

Internal circuit

Q_0 ও CP_1 connected থাকে যদি কোনো কিছু গণনা করতে হয় তখন।

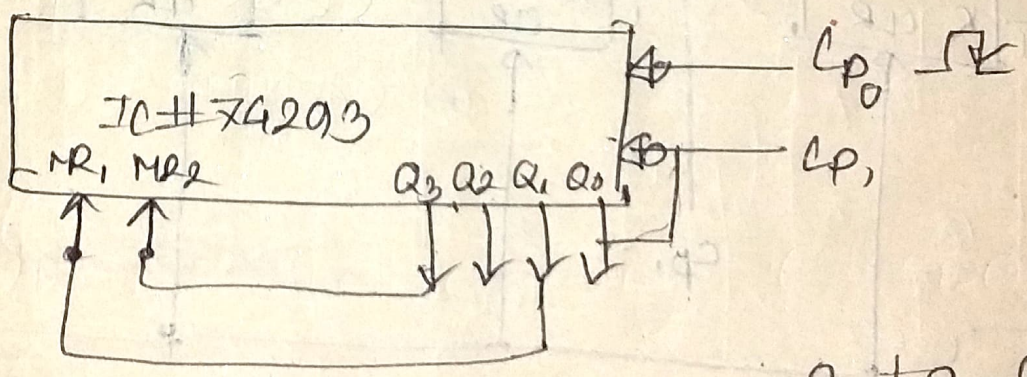
MOD 16
(0 to 15)

Block Diagram



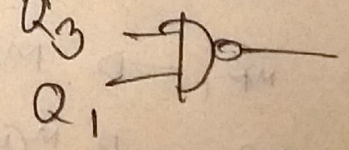
Blue color is to make MOD 16

Design MOD 10 up counter using IC # 74293

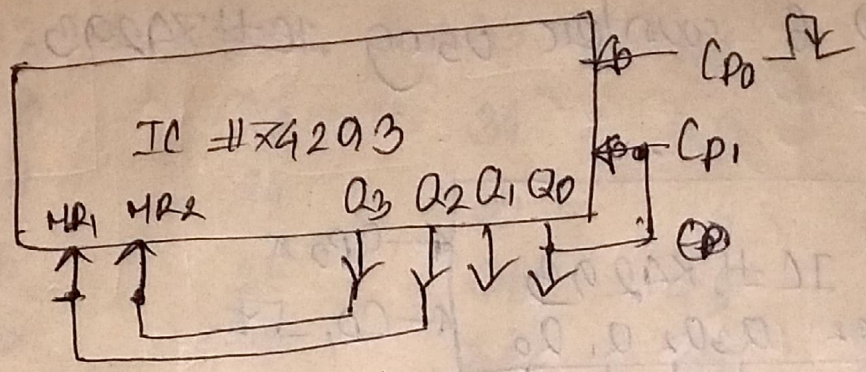


0 to 9

Q_3	Q_2	Q_1	Q_0
1	0	1	0

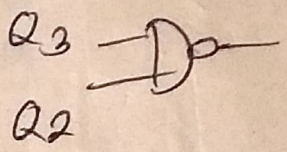


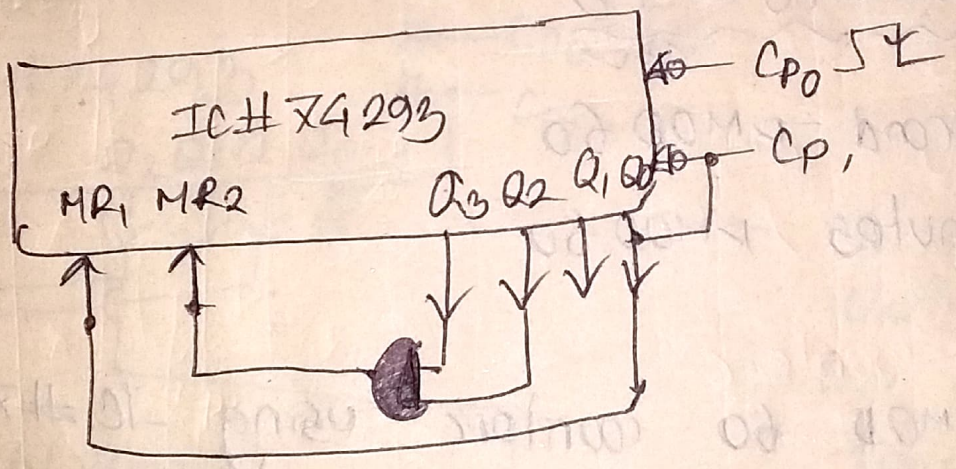
Design MOD 12 up Counter



Q_3	Q_2	Q_1	Q_0
1	1	0	0

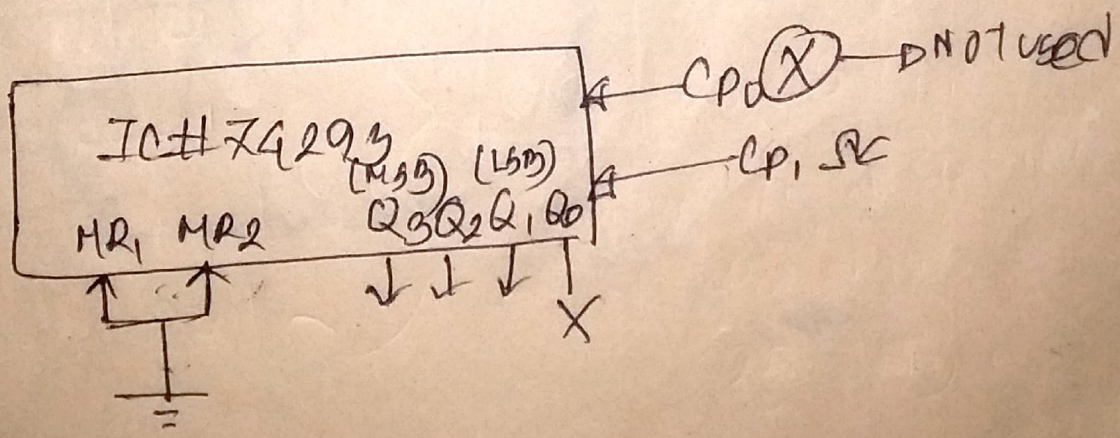
Design MOD 13 up Counter: You can use other logic gates if necessary





1101

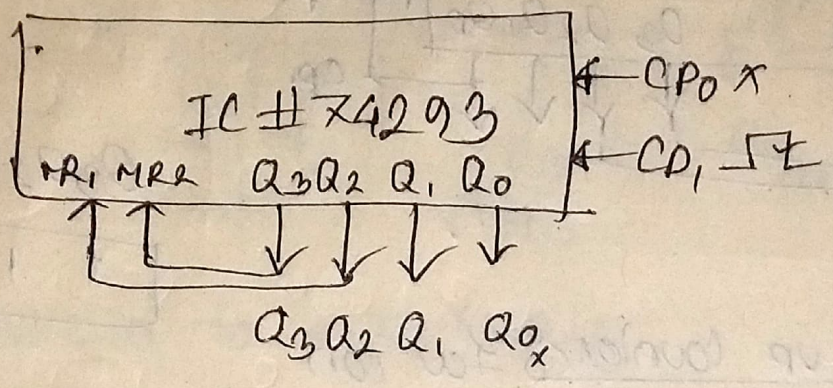
Design MOD 8 Counter:



17-02-2022

#

Design MOD 6 counter using IC # 74293.



Q_3	Q_2	Q_1
1	1	1

MOD 60 counter: (0-59)

Second → MOD 60

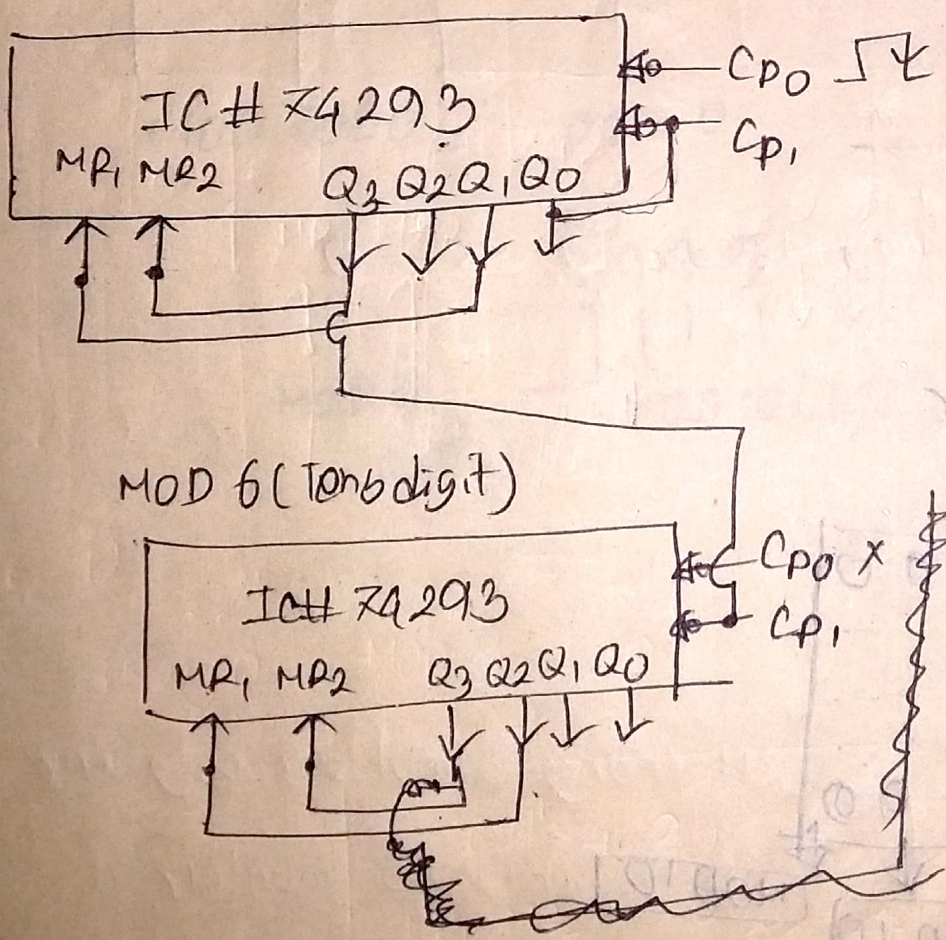
Minutes → MOD 60

[Q] Design MOD 60 counter using IC # 74293

You can use other logic gates if necessary

TU	TU	TU	TU	TU	TU	
00	10	20	30	40	50	00
01	11	21	31	41	51	01
02	12	22	32	42	52	
03	13	23	33	43	53	
04	14	24	34	44	54	
05	15	25	35	45	55	
06	16	26	36	46	56	
07	17	27	37	47	57	
08	18	28	38	48	58	
09	19	29	39	49	59	

MOD 10 (Units digit)



U → Units

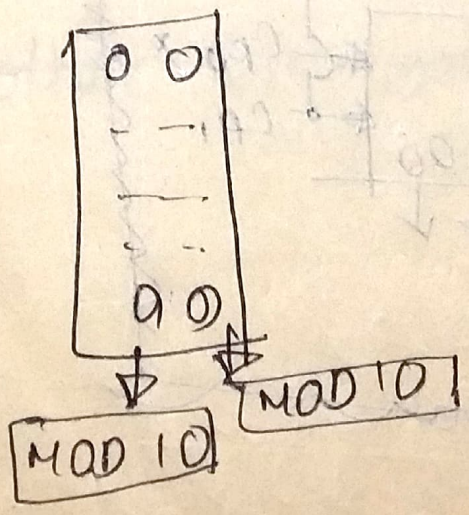
T → Tens

Units → MOD 10 counter

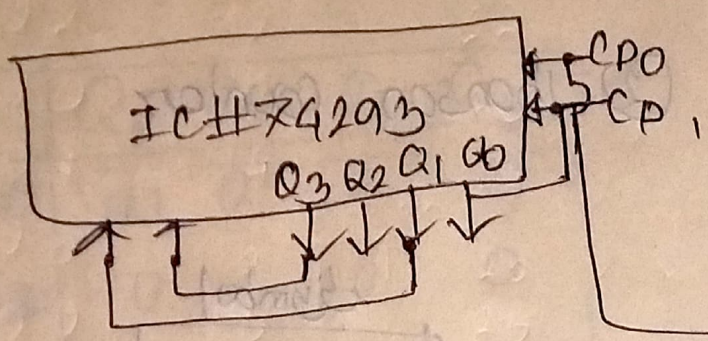
Tens → MOD 6 counter

Q_3	Q_2	Q_1	Q_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
0	0	0	0

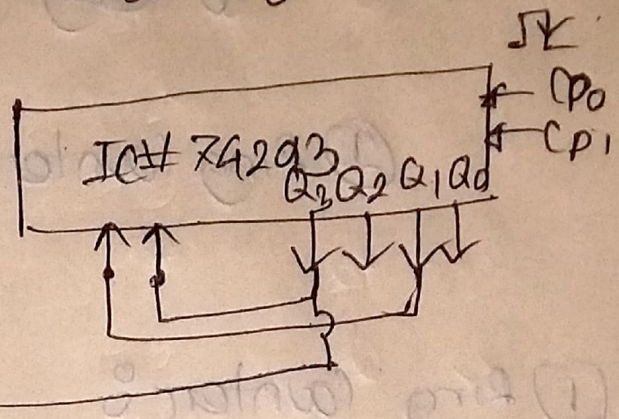
MOD 100 Counter



MOD 10



MOD 10



MOD 1000:

000
⋮
999

MOD 10 → 3

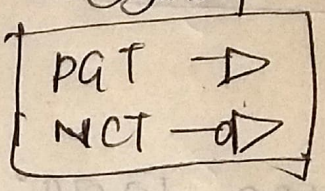
MOD 6000: 0000
⋮
5999
| | | |
MOD 6 (↓↑) MOD 10 (3↑)

Shift Counter: ~~Ring~~

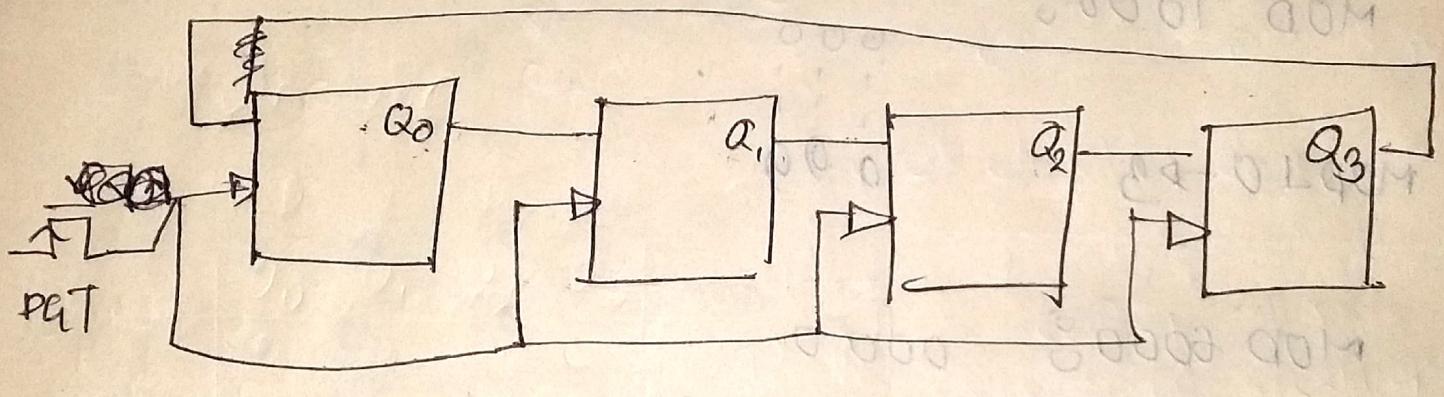
① Ring Counter ② Johnson Counter

① Ring Counter:

Symbol



MOD 4 Ring Counter



Initially $Q_0 = 1$; $Q_1 = Q_2 = Q_3 = 0$

Operation:

After giving pulse:

$Q_0 = Q_3$;
$Q_1 = Q_0$;
$Q_2 = Q_1$;
$Q_3 = Q_2$;

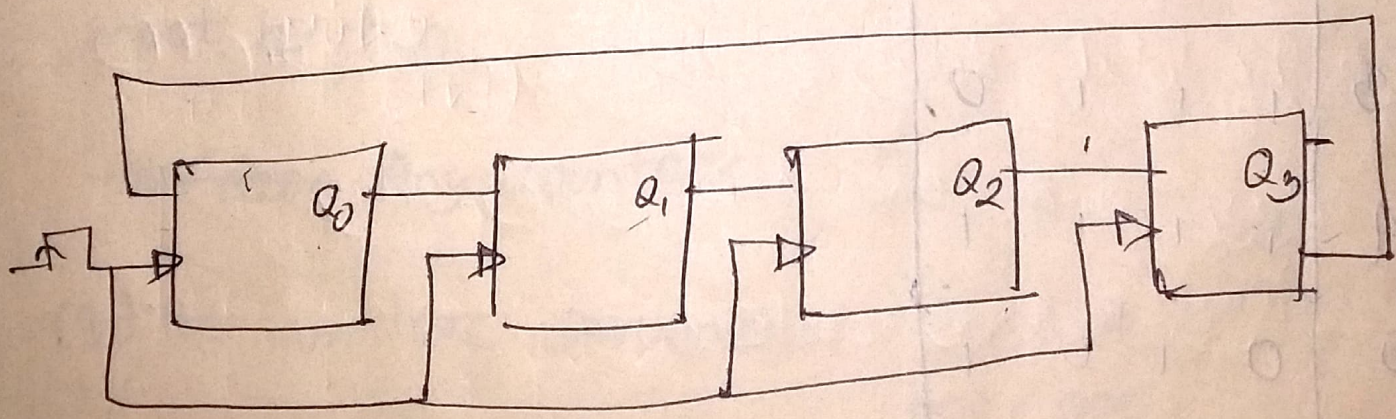
→ will change simultaneously since it's synchronous counter

Truth Table:

	Q_0	Q_1	Q_2	Q_3
#0	1	0	0	0
#1	0	1	0	0
#2	0	0	1	0
#3	0	0	0	1
#4	1	0	0	0

MOD no of Ring Counter = No of Flip flop

[2] Jhonson Counter: MOD 8 Jhonson Counter



~~Initially~~
$Q_0 =$
$Q_1 =$
$Q_2 =$
$Q_3 =$

Initially $Q_0 = Q_1 = Q_2 = Q_3 = 0$

After giving the pulse

$Q_0 = \overline{Q_3}$;

$Q_1 = Q_0$;

$Q_2 = Q_1$;

$Q_3 = Q_2$;

Truth Table

	Q_0	Q_1	Q_2	Q_3
	0	0	0	0
#1	1	0	0	0
#2	1	1	0	0
#3	1	1	1	0
#4	1	1	1	1
#5	0	1	1	1
#6	0	0	1	1
#7	0	0	0	1
#8	0	0	0	0

For Jhonson counter

MOD no = 2× Number of ~~Fl~~ Flip-flop

27-02-2022

For each of the following statements, indicate the type's of counter being described

(1) Each FF is clocked at the same time

- synchronous / parallel counter

(2) Each FF divides the frequency at its clock input by two.

- ~~up/down~~ Any counter

(3) The counter sequence is 111, 110, 101, 100, 011, 010, 001, 000.

- MOD 8 down counter

(4) The counter has ten (10) distinct states

- MOD 10 counter / BCD counter

(5) The total delay is sum of individual FF's delay

- Asynchronous counter / Ripple counter

(6) The counter can count in either direction.

- Up/down counter

(7) The counter counts from 0 to 9.

- MOD 10 UP counter

(8) The MOD number is always twice the number of FFs.

- Jhonson counter

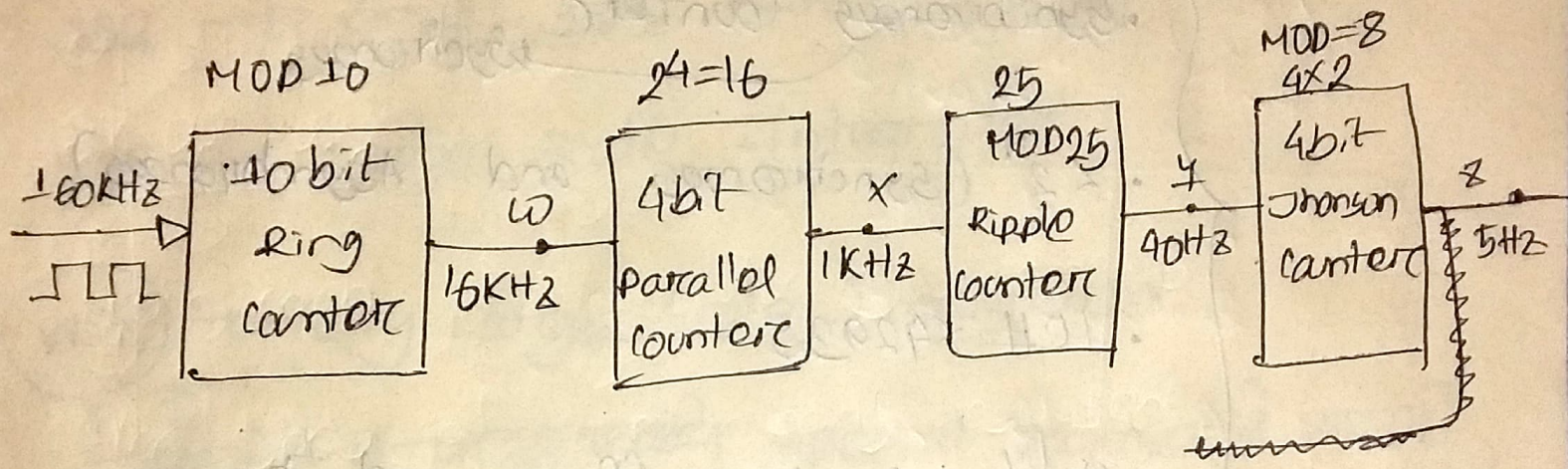
(9) The total delay is the sum of one FF's delay and one AND gate's delay.

- Synchronous counter

(10) The MOD number is always equal to the number of FFs.

- Ring Counter

$\boxed{\text{Output frequency} = \dfrac{\text{Input frequency}}{\text{MOD NO.}}}$



→ Find the values of w, x, y and z.

$$w = \frac{160\ kHz}{10}$$

$$= 16\ kHz$$

$$x = \frac{16}{16}\ kHz = 1000\ Hz$$

$$y = \frac{1000\ Hz}{25} = 40\ Hz$$

$$z = \frac{40}{8} = 5\ Hz$$

End of Counters:

CT3: only counters

- ~~Synchronous~~ Counter → Shift, Sychronous
- $< 2^N$ (Synchronous and Asynchronous)
- IC# 742938 ---
- Shift counter (Ring and Jhonson

(1) Chapter 9

(2) Counter (Any sequence) $\boxed{0, 1, 3, 5, 2, \ldots}$

(3) SAPI (Simple as Possible)

(4) ALU

→ MID SYLLABUS END

Chapter 9: MSI logic circuits

MSI → Medium Scale Integrated

SSI → Small Scale Integrated

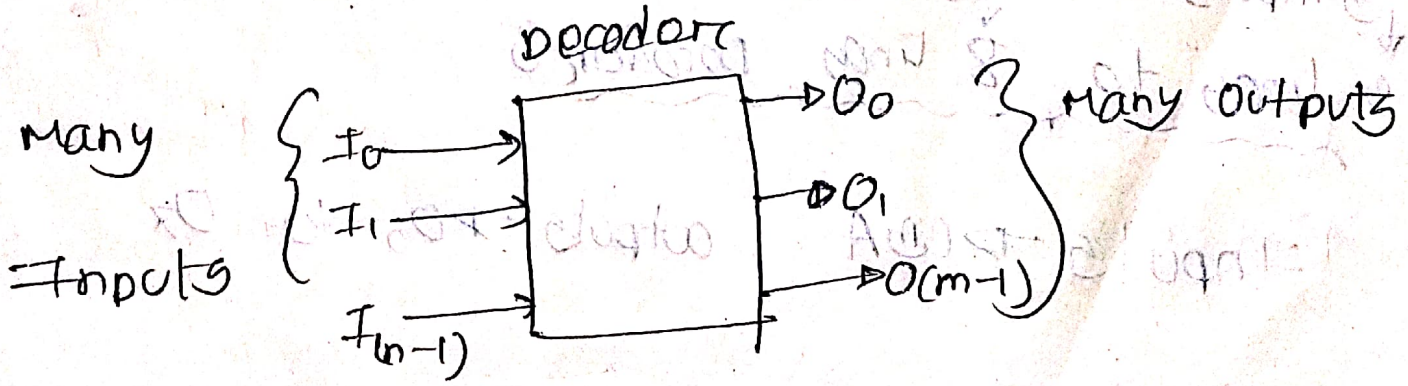
LSI → Large Scale Integrated

VLSI → Very Large Scale Integrated.

↳ [(4-2/4-1) → এগুলো special course এ আছে]

(1) Decoder (2) Multiplexer (MUX) (3) Demultiplexer (DEMUX)

(1) Decoder:



At a time only one of the output will be active according to the corresponding

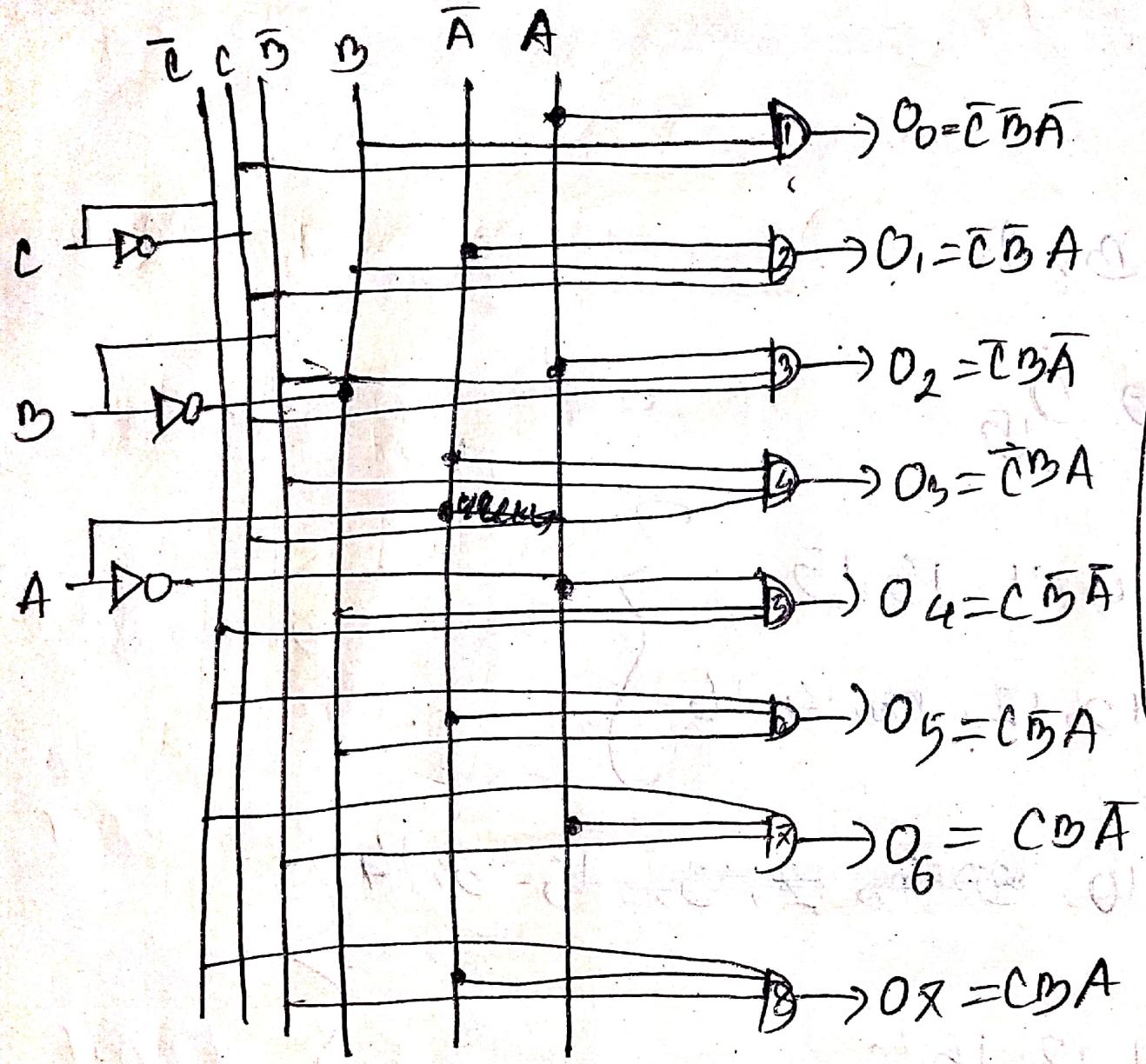
combination of inputs.

No of Input	No. of Output
2	$4 = 2^n$
3	$8 = 2^3$
4	$16 = 2^4$
5	$32 = 2^{16}$

$$\boxed{\text{No outputs} = 2^{\text{number of inputs}}}$$

3 inputs → 3 lines to 8 outputs → 8 lines Decoder:

Inputs → CBA , outputs → O_0 to O_7



Active

	C B A	Output
$\bar{C}\bar{B}\bar{A}$	0 0 0	O_0
$\bar{C}\bar{B}A$	0 0 1	O_1
$\bar{C}B\bar{A}$	0 1 0	O_2
$\bar{C}BA$	0 1 1	O_3
$C\bar{B}\bar{A}$	1 0 0	O_4
$C\bar{B}A$	1 0 1	O_5
$CB\bar{A}$	1 1 0	O_6
CBA	1 1 1	O_7

Active high output

28-02-2022

Inputs → D, C, B, A

Outputs → O_0 to O_{15}

$\bar{A}$ → 1, 3, 5, 7, 9, 11, 13, 15

A → 2, 4, 6, 8, 10, 12, 14, 16

$\bar{B}$ → 1, 2, 5, 6, 9, 10, ~~12, 13, 16~~ 13, 14

B → 3, 4, 7, 8, 11, 12, 15, 16

$\bar{C}$ → 1 to 4, 9 to 12

C → 5 to 8, then 13 to 16

$\bar{D}$ → 1 to 8

D → 9 to 16

4 inputs → 4 lines to 10 line decoder ← 10 outputs

Input → D, C, B, A

Outputs → O_0 to O_9

10 AND Gates (1 to 9)

$\overline{A}$ → 1, 3, 5, 7, 9
A → 2, 4, 6, 8, 10

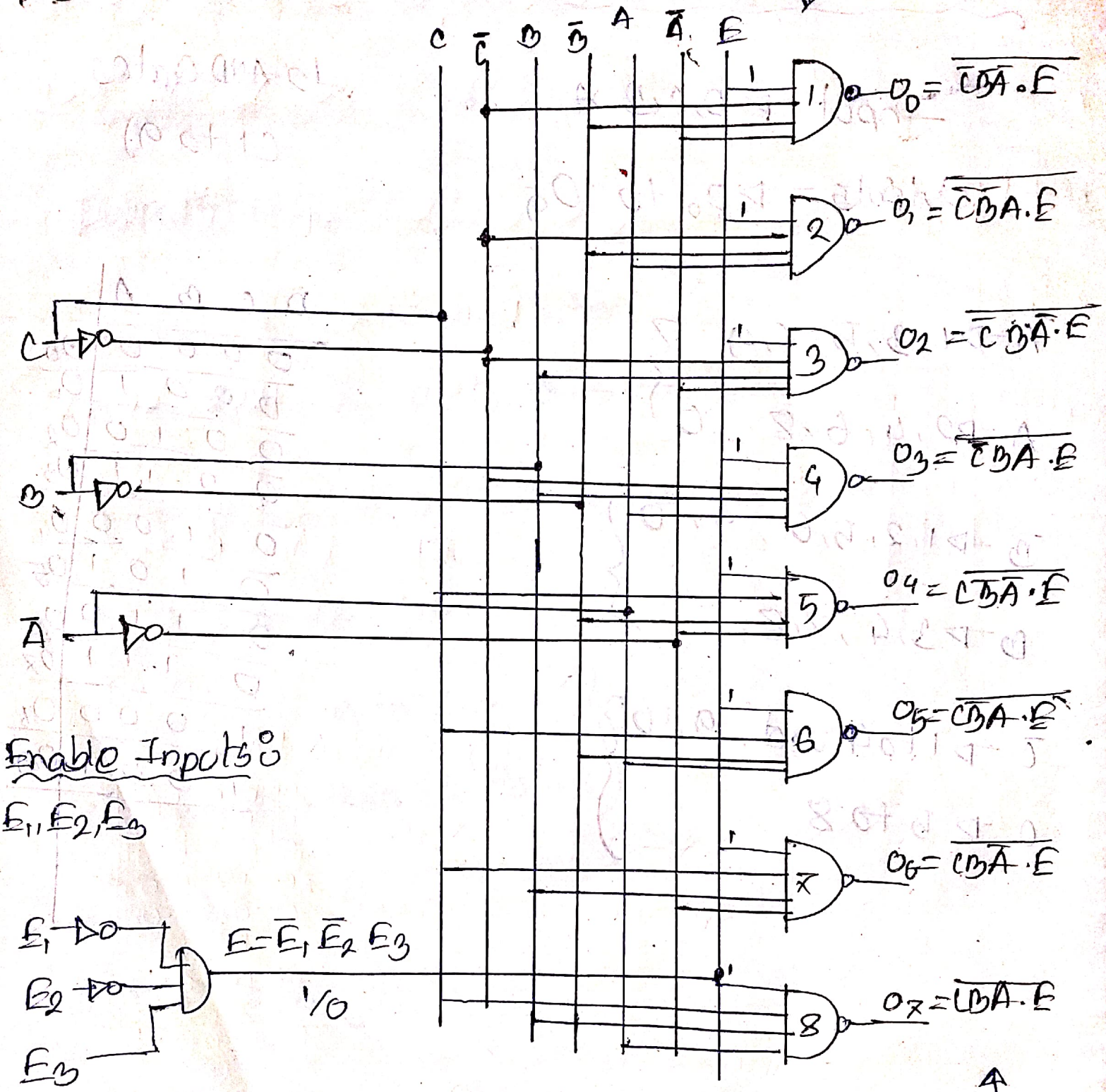
$\overline{B}$ → 1, 2, 5, 6, 9, 10
B → 3, 4, 7, 8,

$\overline{C}$ → 1 to 4 and 9, 10
C → 5 to 8

D	C	B	A	
0	0	0	0	O_0
0	0	0	1	O_1
0	0	1	0	O_2
0	0	1	1	O_3
0	1	0	0	O_4
0	1	0	1	O_5
0	1	1	0	O_6
0	1	1	1	O_7
1	0	0	0	O_8
1	0	0	1	O_9

IC # 74138 (Decoder) Internal Circuit

এখানে আমরা NAND use করবো



Enable Inputs:

E_1, E_2, E_3

Active Mode:

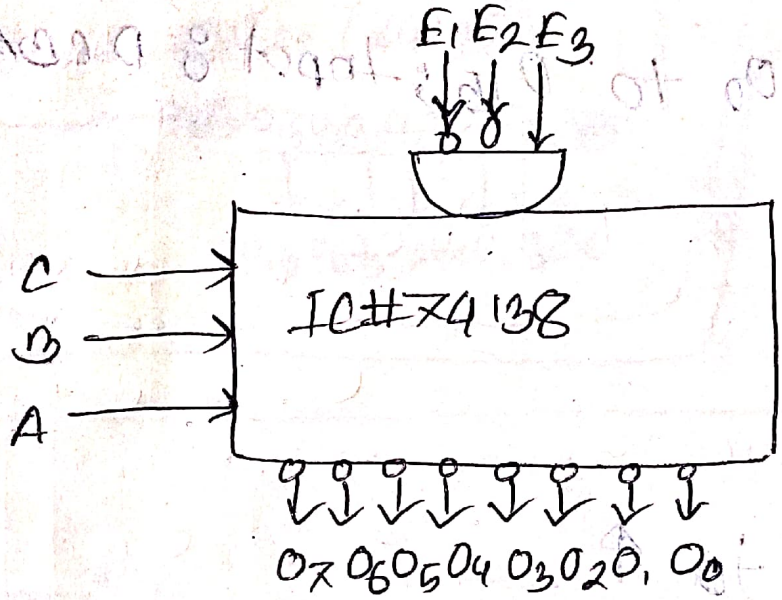
$E = 1$, ~~$E_1 = 0$~~

$\boxed{E_1 = 0,\ E_2 = 0,\ E_3 = 1}$

other combination IC will be inactive

Active low output

Block Diagram of IC#74138:



Ex-1

$E_1 = E_2 = 0,\ E_3 = 1$ → Active Mode

$C = B = 1,\ A = 0$

→ Which ~~what~~ output will be Active?

Ans: O_6

Ex-2

$E_1 = 0,\ E_2 = 1,\ E_3 = 1$ → Inactive Mode

$C = 1,\ B = 0,\ A = 1$

→ Which output will be active?

Ans: No output will be active.

Design 4 lines to 16 lines Decoder Using IC #74138.

You can use other logic gates, if necessary.

⇒ 2 IC's Output O_0 to O_{15}; Input: D C B A

02-02-2021

Design 4 lines to 16

Truth Table

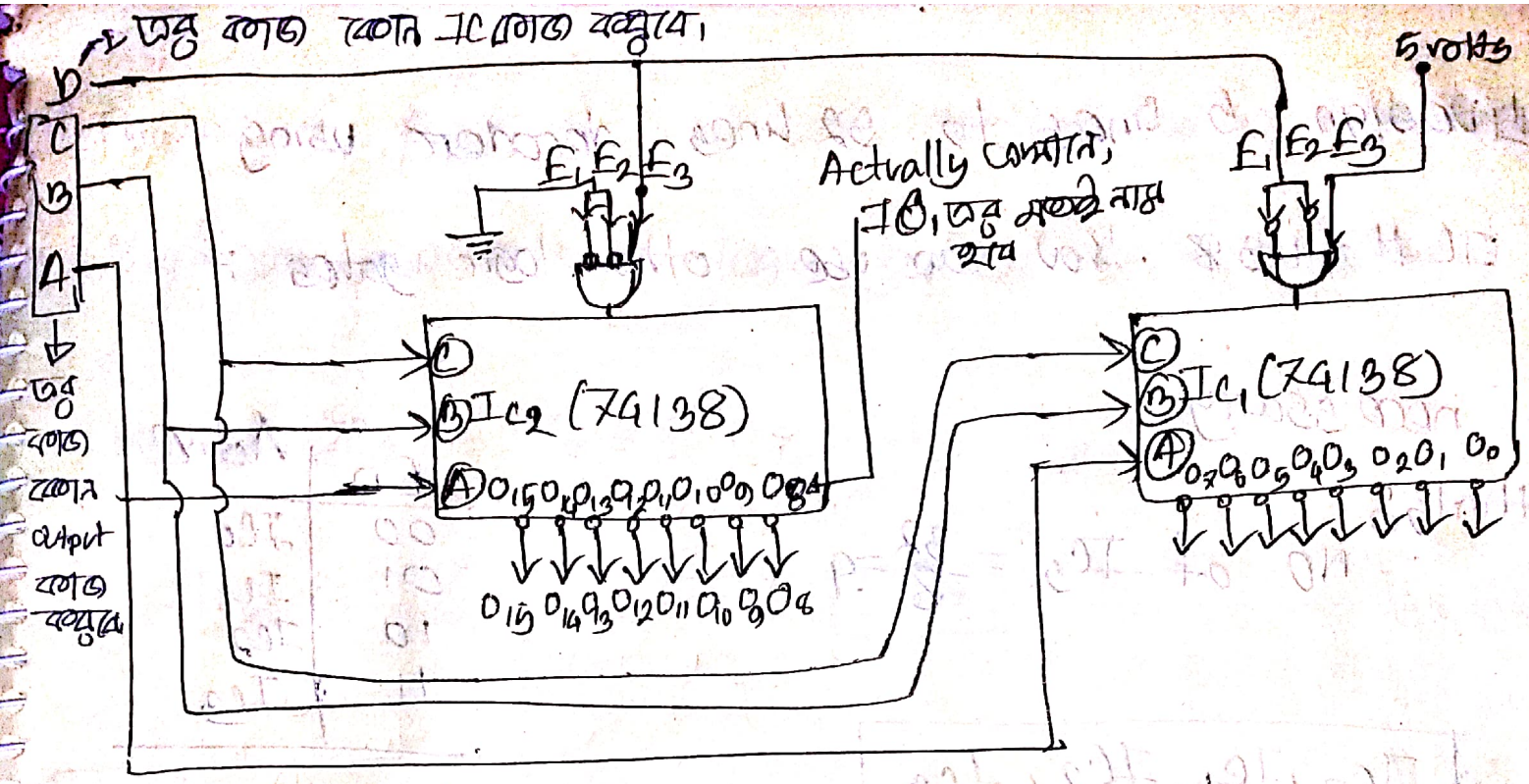
D	C	B	A	Active Output
0	0	0	0	O_0
0	0	0	1	O_1
0	0	1	0	O_2
0	0	1	1	O_3
0	1	0	0	O_4
0	1	0	1	O_5
0	1	1	0	O_6
0	1	1	1	O_7
1	0	0	0	O_8
1	0	0	1	O_9
1	0	1	0	O_{10}
1	0	1	1	O_{11}
1	1	0	0	O_{12}
1	1	0	1	O_{13}
1	1	1	0	O_{14}
1	1	1	1	O_{15}

IC_1 ✓ → Active

IC_2 ✗ → Inactive

IC_1 ✗ → Inactive

IC_2 ✓ → Active



Operation :

If D=0,

then for IC_1 $E_1 = E_2 = 0$, $E_3 = 1$

for IC_2 $E_1 = E_2 = E_3 = 0$

$\therefore$ IC_1 is active & IC_2 is inactive

If D=1,

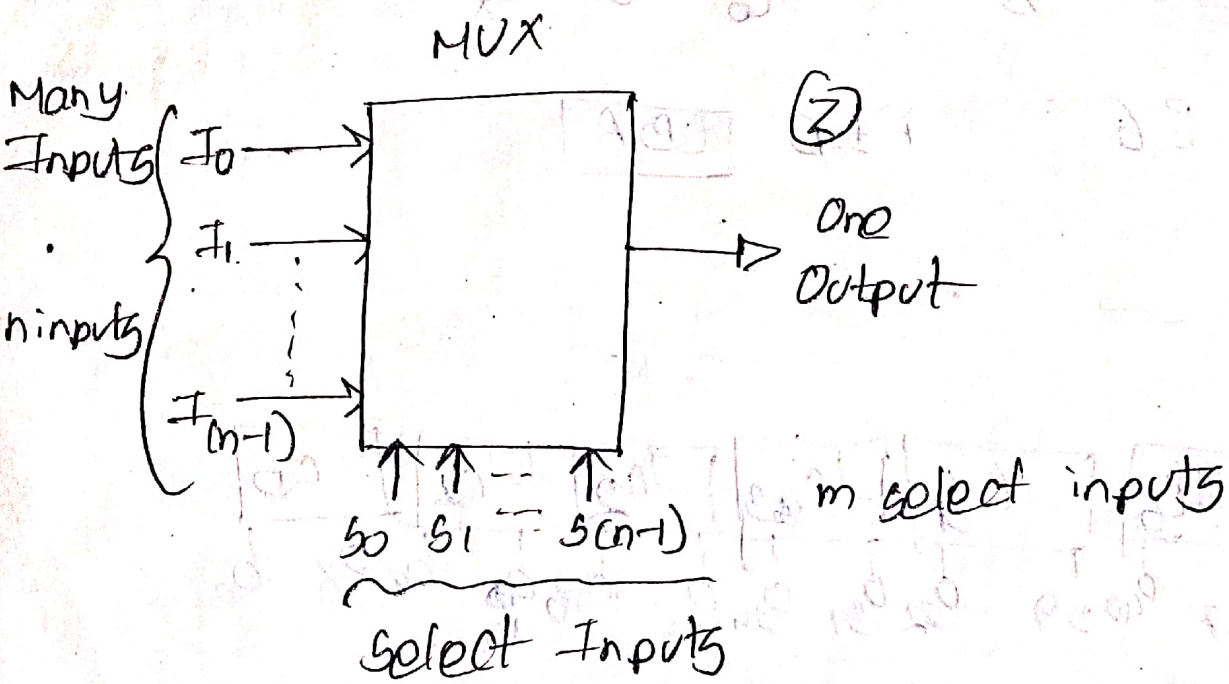
then for IC_1 $E_1 = E_2 = E = 1$

$\therefore$ for IC_2 $E_1 = E_2 = 0$, $E_3 = 1$

$\therefore$ IC_1 is inactive and IC_2 is active

Multiplexer ও Input থেকে Output নেয়।

(2) Multiplexer (MUX):



MUX is a device where there are many inputs one output and some select inputs. At a time one of the inputs goes to the output according to the corresponding combination of select inputs.

No of select Inputs	No of Normal Inputs
2	$4 = 2^2$
3	$8 = 2^3$
4	$16 = 2^4$
5	$32 = 2^5$

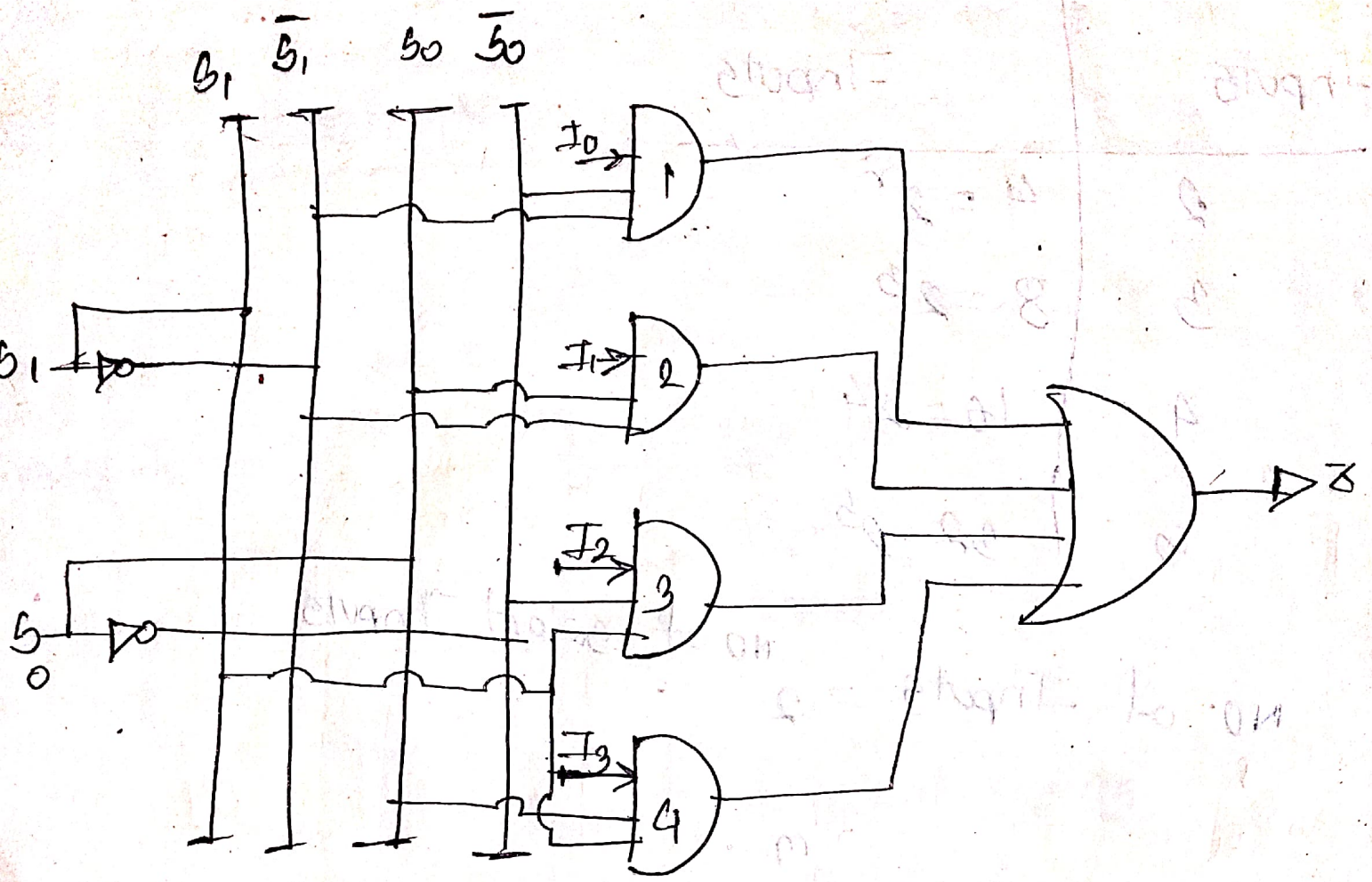
$$\text{No of Inputs} = 2^{\text{No of select Inputs}}$$

$$\therefore n = 2^m$$

4 inputs MUX:

$$Z = \overline{S_1}\,\overline{S_0} \cdot I_0 + \overline{S_1} S_0 . I_1 + S_1 . \overline{S_0} \cdot I_2 + S_1 S_0 I_3$$

S_1	S_0	$Z =$
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3



4 Input MUX

DLSD:

Chapter [3 - 7] [Mid term syllabus] ⊛

06-03-2022

8 input MUX:

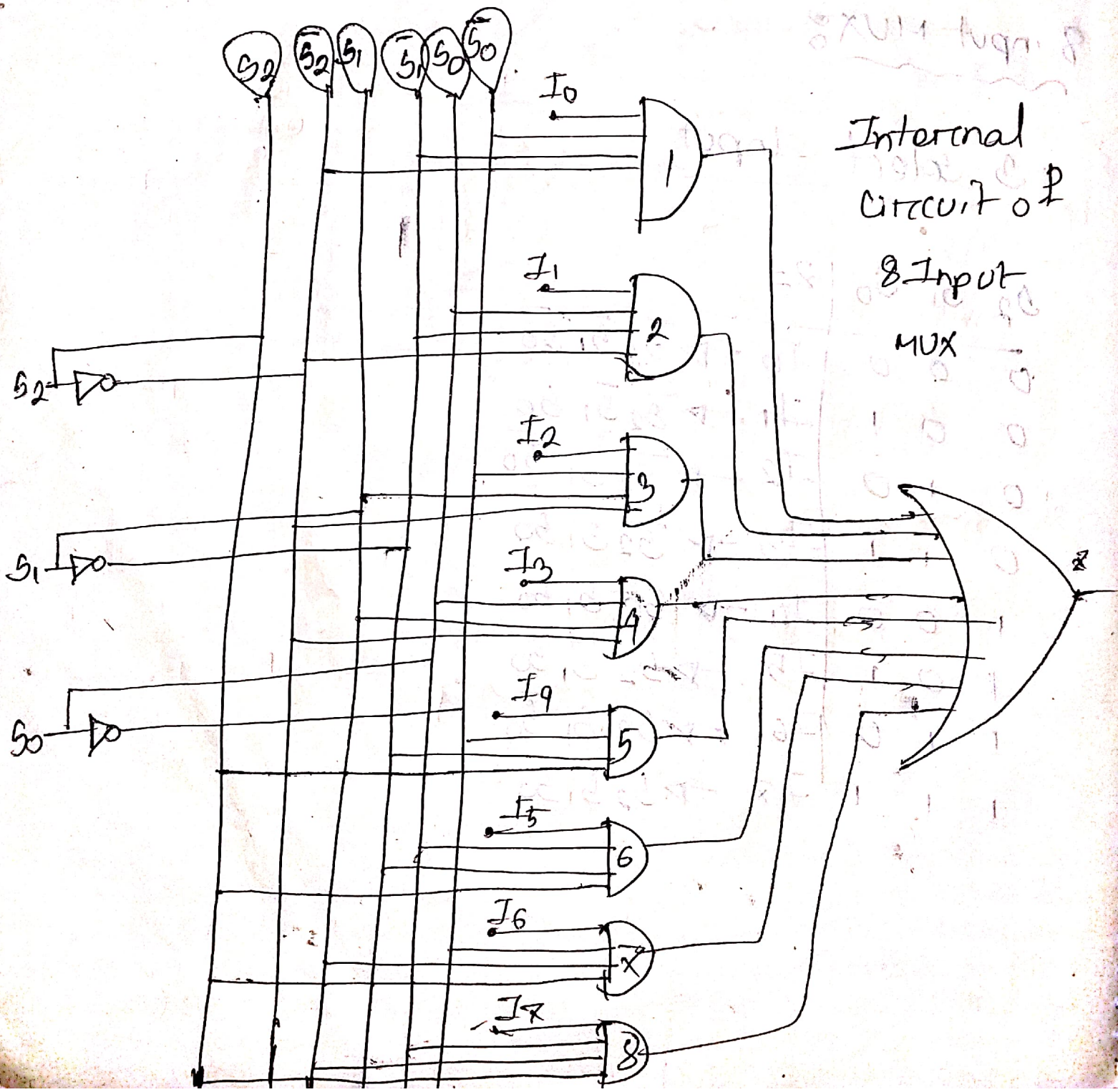
3 select Input

S_2	S_1	S_0	$Z =$
0	0	0	$I_0 \rightarrow \overline{S_2}\,\overline{S_1}\,\overline{S_0}$
0	0	1	$I_1 \rightarrow \overline{S_2}\,\overline{S_1}\,S_0$
0	1	0	$I_2 \rightarrow \overline{S_2}\,S_1\,\overline{S_0}$
0	1	1	$I_3 \rightarrow \overline{S_2}\,S_1\,S_0$
1	0	0	$I_4 \rightarrow S_2\,\overline{S_1}\,\overline{S_0}$
1	0	1	$I_5 \rightarrow S_2\,\overline{S_1}\,S_0$
1	1	0	$I_6 \rightarrow S_2\,S_1\,\overline{S_0}$
1	1	1	$I_7 \rightarrow S_2\,S_1\,S_0$

$$Z = \bar{S}_2\bar{S}_1\bar{S}_0 \cdot I_0 + \bar{S}_2\bar{S}_1 S_0 \cdot I_1 + \bar{S}_2 S_1 \bar{S}_0 \cdot I_2 + \bar{S}_2 S_1 S_0 \cdot I_3$$

$$+ S_2\bar{S}_1\bar{S}_0 \cdot I_4 + S_2\bar{S}_1 S_0 \cdot I_5 + S_2 S_1 \bar{S}_0 \cdot I_6$$

$$+ S_2 S_1 S_0 \cdot I_7$$

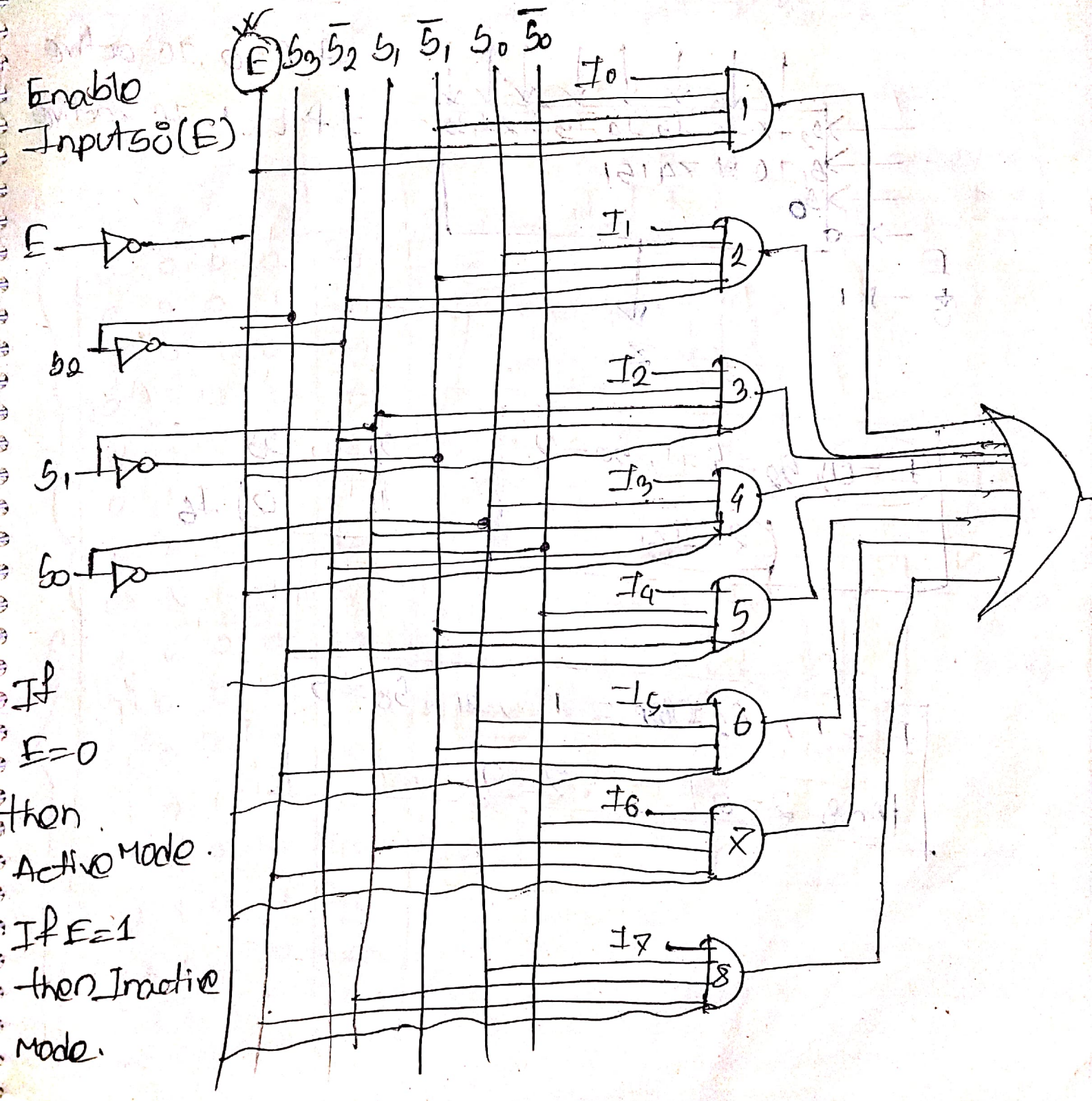


Internal circuit of 8 Input MUX

IC#74151

নিচের ছবিতে Internal circuit বিদ্যমান।

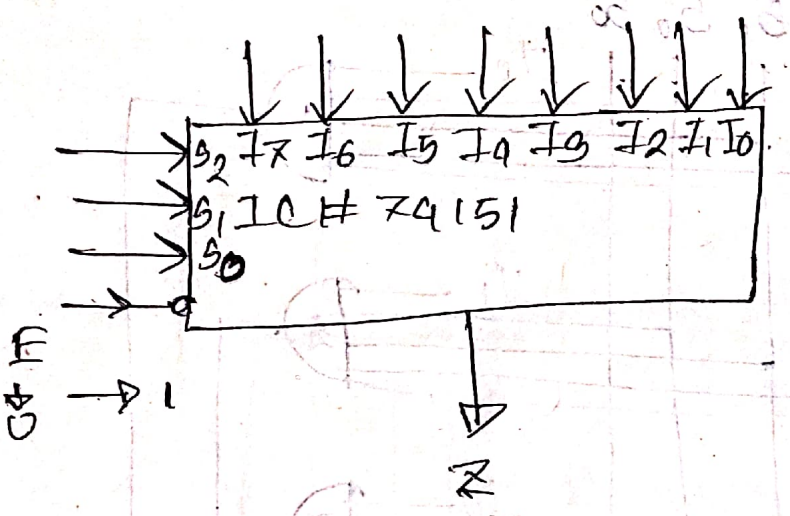
#Internal circuit of IC#74151#



If E=0 then Active Mode.

If E=1 then Inactive Mode.

Block Diagram : (শুধু Input এবং Output দিয়ে আঁকা diagram)



If E=0, IC active

If E=1, IC inactive

$E=0$, $S_2=S_1=1$, $S_0=0$

$Z=I_6$

S_2	S_1	S_0	
1	1	0	I_6

$E=1$, $S_2=1$, $S_1=S_0=0$

$Z=?$

Ans: $Z=0$

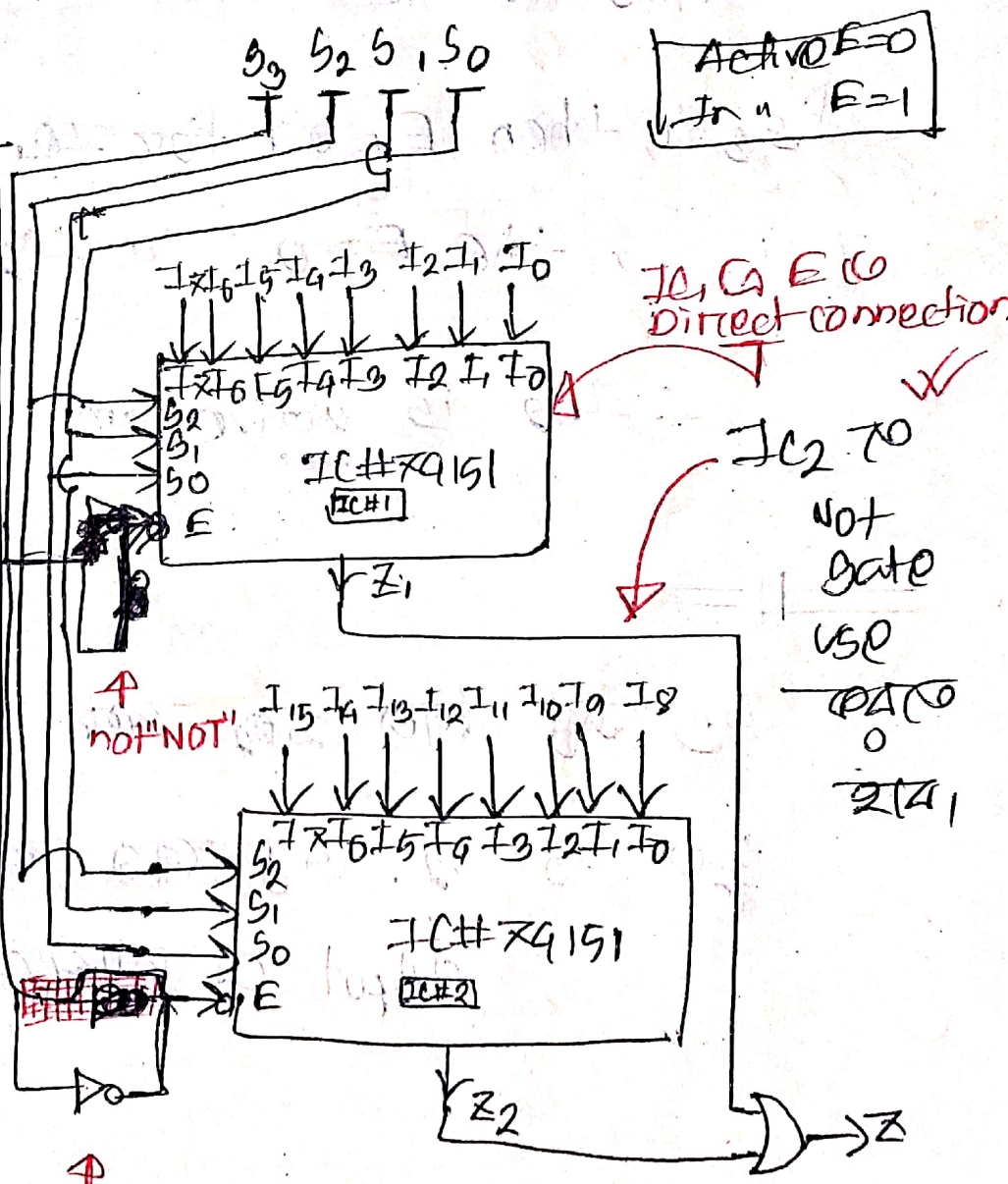
23-03-23

Design 16 input MUX using IC# 74151. You can use other logic gates, if necessary.

→ No of IC $= \frac{16}{8} = 2$; Select input → S_3, S_2, S_1, S_0

Inputs → I_0 to I_15

S_3	S_2	S_1	S_0	Z
0	0	0	0	I_0
0	0	0	1	I_1
0	0	1	0	I_2
0	0	1	1	I_3
0	1	0	0	I_4
0	1	0	1	I_5
0	1	1	0	I_6
0	1	1	1	I_7
1	0	0	0	I_8
1	0	0	1	I_9
1	0	1	0	I_{10}
1	0	1	1	I_{11}
1	1	0	0	I_{12}
1	1	0	1	I_{13}
1	1	1	0	I_{14}
1	1	1	1	I_{15}



operation:

If $S_3 = 0$, then $E = 0$ for IC_1

If $S_3 = 1$, the $E = 1$ for IC_2

$\therefore IC_1$ is active and IC_2 is inactive.

If $S_3 = 1$, then $E = 1$ for IC_1

" , the $E = 0$ " IC_2,

$\therefore IC_2$ is active and IC_1 is inactive.

S_3 এর মান 0 হলে কোন IC active হবে

এবং $S_0 - S_2$ এর মান কত নিয়ে Input

Output এ আসবে।

27-03-2022

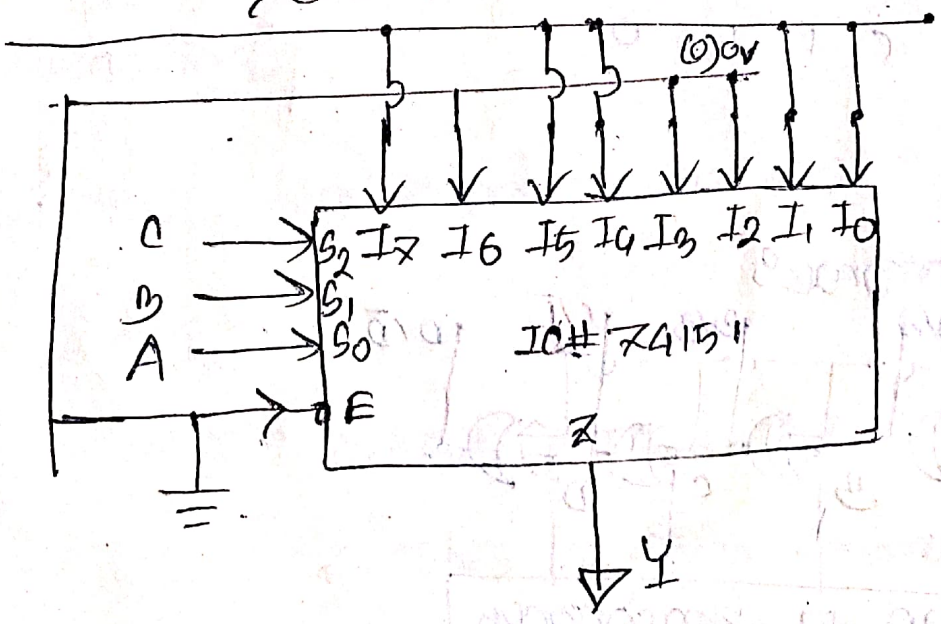
Application of MUX:

(i) Logic Function generation

$$Y = \overline{A}\,\overline{B}C + \overline{A}B\overline{C} + AB\overline{C} + A\overline{B}C + A\overline{B}\,\overline{C}$$

IC# 74151

5 volts (1)

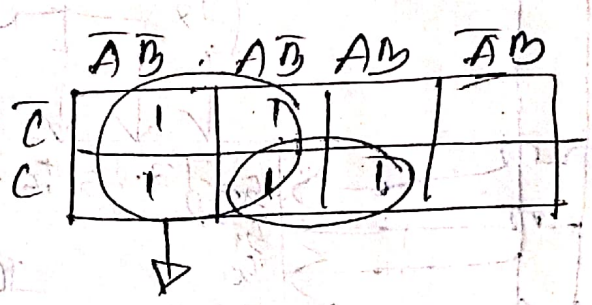


C | B | A

S_2	S_1	S_0	Z
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

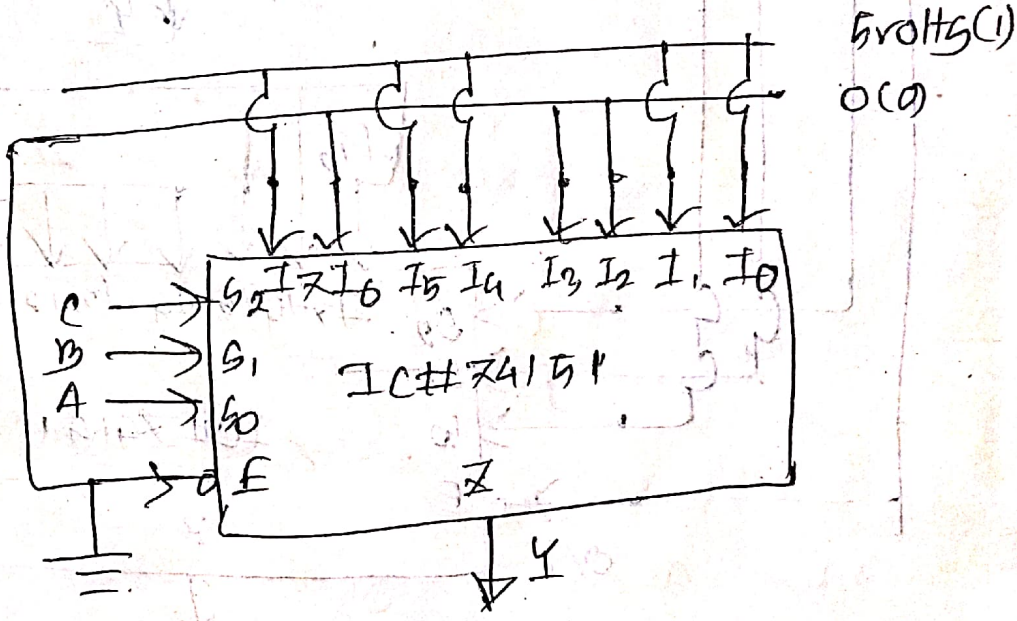
C	B	A	Y
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

Implement $F(A, B, C) = \Sigma(0, 1, 4, 5, 7)$ using IC#74151

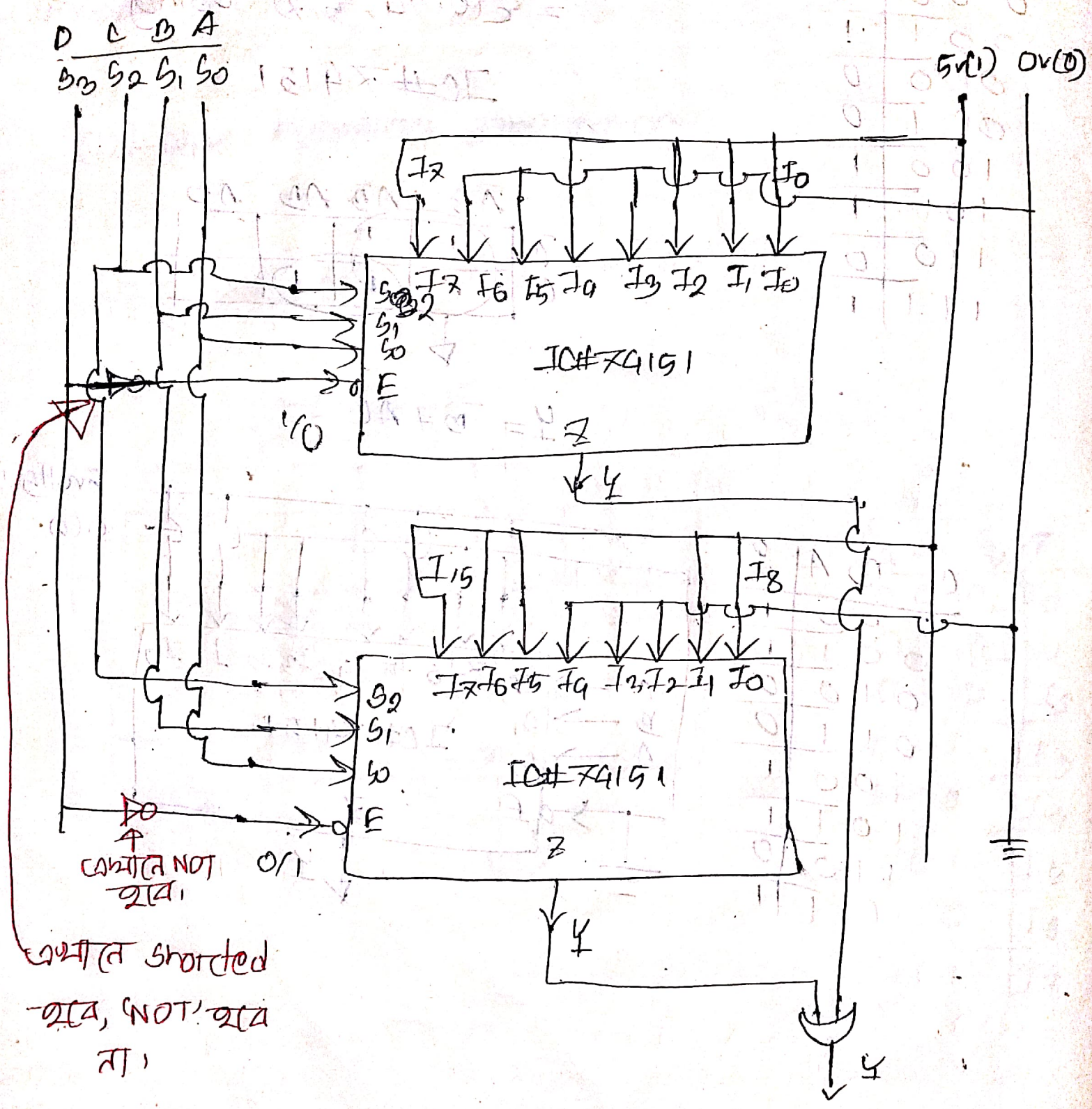


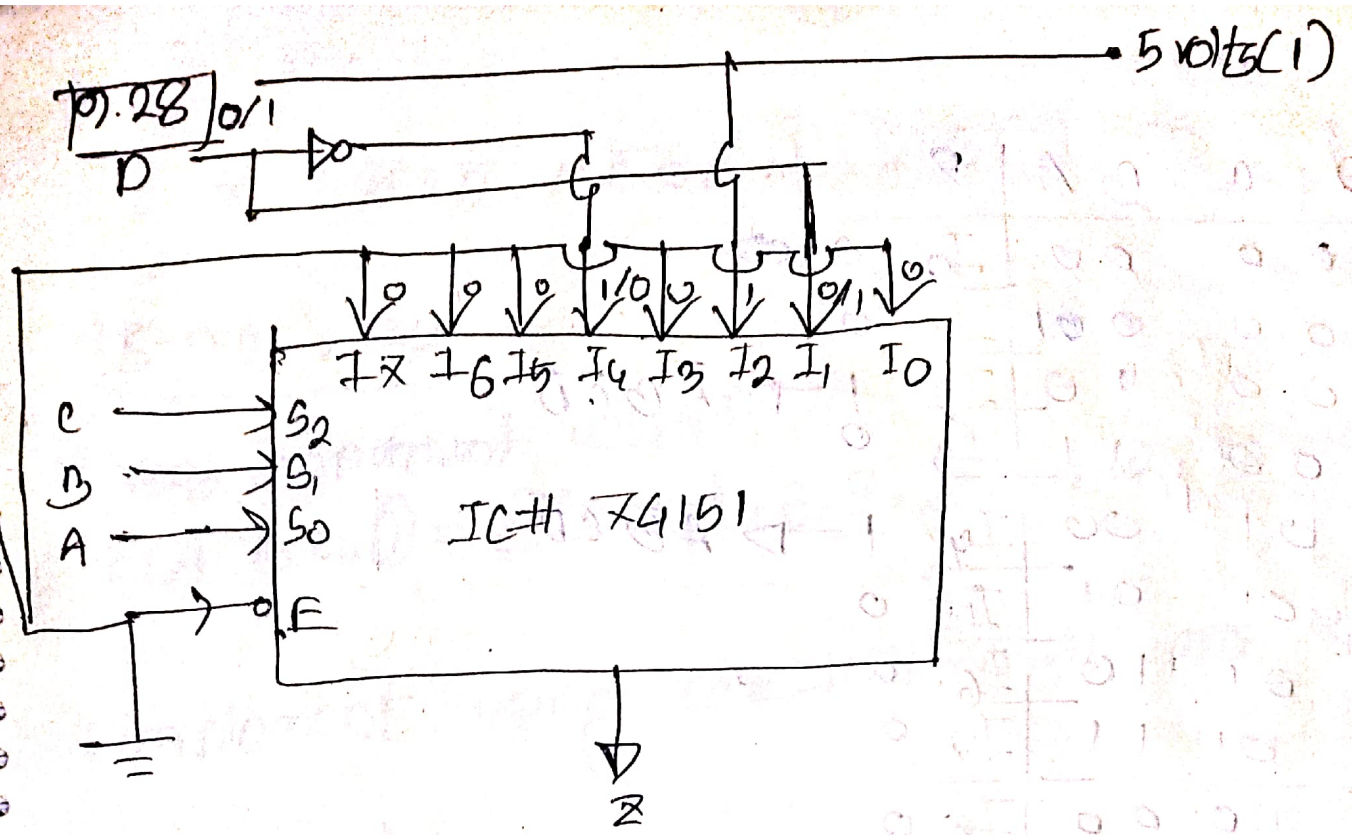
$Y = \bar{B} + AC$

C	B	A	Y
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1



[# $F(A, B, C, D) = \Sigma(0, 1, 2, 4, 7, 8, 9, 13, 14, 15)$]





(a) Draw truth table

(b) Simplify using K-Map or otherwise

(a) $I_1 =$

D	C	B	A	
0	0	0	0	I_0
0	0	0	1	I_1
0	0	1	0	I_2 —(1)→ $\bar{A}B\bar{C}$
0	0	1	1	I_3
0	1	0	0	I_4
0	1	0	1	I_5
0	1	1	0	I_6
0	1	1	1	I_7

D	C	B	A	Z	
0	0	0	0	I_0 0	
0	0	0	1	I_1 0	
0	0	1	0	I_2 1	$\rightarrow \bar{A}B\bar{C}\bar{D}$
0	0	1	1	I_3 0	
0	1	0	0	I_4 1	$\rightarrow \bar{A}\bar{B}C\bar{D}$
0	1	0	1	I_5 0	
0	1	1	0	I_6 0	
0	1	1	1	I_7 0	
1	0	0	0	I_8 0	
1	0	0	1	I_9 1	$\rightarrow A\bar{B}\bar{C}D$
1	0	1	0	I_{10} 1	$\rightarrow \bar{A}B\bar{C}D$
1	0	1	1	I_{11} 0	
1	1	0	0	I_{12} 0	$\rightarrow \bar{A}\bar{B}CD$
1	1	0	1	I_{13} 0	
1	1	1	0	I_{14} 0	
1	1	1	1	I_{15} 0	

~~when D=0,~~

(b)

$$Z = \bar{A}B\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} + A\bar{B}\bar{C}D + \bar{A}B\bar{C}D \cancel{+ \bar{A}\bar{B}CD}$$

	$\bar{A}\bar{B}$	$\bar{A}B$	AB	$A\bar{B}$
$\bar{C}\bar{D}$	0	0	0	1
$C\bar{D}$	1	0	0	0
CD	0	0	0	0
$\bar{C}D$	0	1	0	1

$= \bar{A}\bar{B}C\bar{D} + A\bar{B}\bar{C}D + \bar{A}B\bar{C}$

28-03-2022

very Important ডিগ্রি

$F(A,B,C,D) = \Sigma(0,1,4,6,7,8,10,12,13,14,15)$

Implement using one IC#74151 and NOT gates, if necessary.

Portion কুড common

	D	C	B	A	Y		
D=0	0	0	0	0	1	I_0	
	0	0	0	1	1	I_1	
	0	0	1	0	0	I_2	
	0	0	1	1	0	I_3	
	0	1	0	0	1	I_4	
	0	1	0	1	0	I_5	
	0	1	1	0	1	I_6	
	0	1	1	1	1	I_7	
D=1	1	0	0	0	1	$I_8 \to I_0$	
	1	0	0	1	0	$I_9 \to I_1$	
	1	0	1	0	1	$I_{10} \to I_2$	
	1	0	1	1	0	$I_{11} \to I_3$	
	1	1	0	0	1	$I_{12} \to I_4$	
	1	1	0	1	1	$I_{13} \to I_5$	
	1	1	1	0	1	$I_{14} \to I_6$	
	1	1	1	1	1	$I_{15} \to I_7$	

$1 = I_0 = I_4 = I_6 = I_7$

$0 = I_3$; $\bar{D} = I_1$

$D = I_2, I_5$

when D=0, then $I_1 = 1$

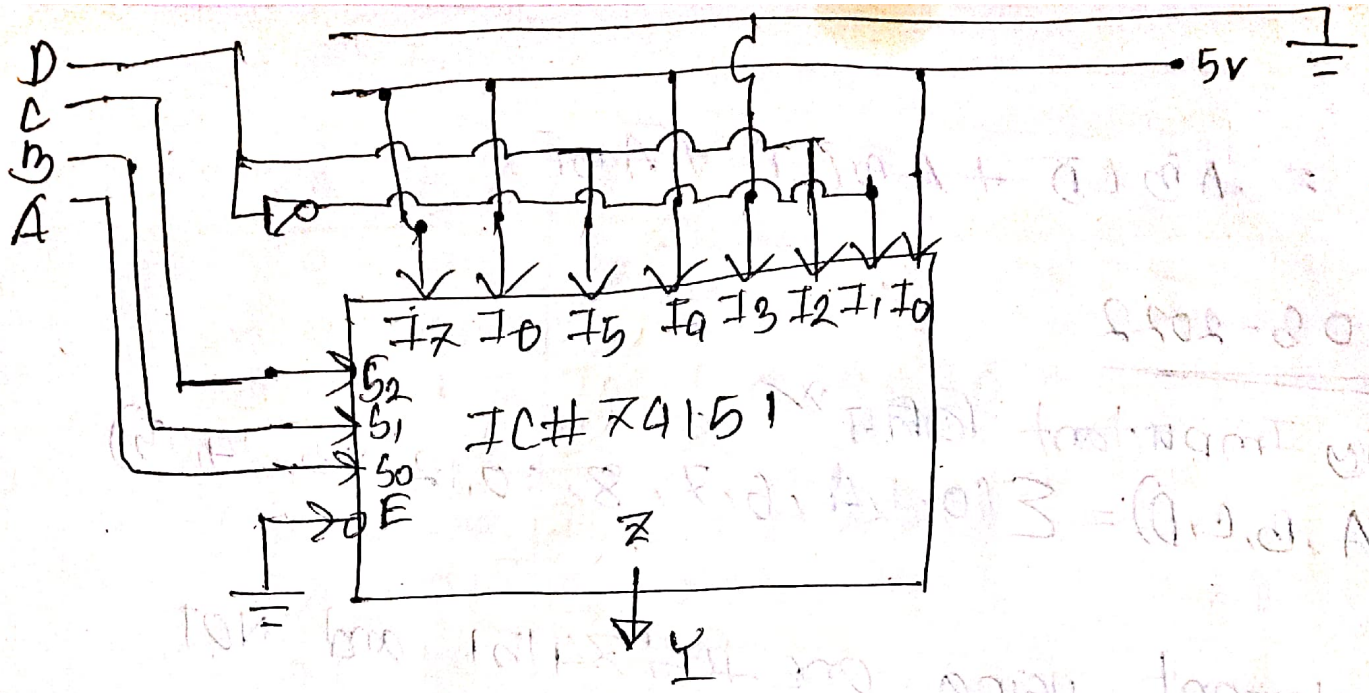
" , D=1, then $I_1 = 0$

when D=0, then $I_2 = 0$

when D=1, then $I_2 = 1$

when D=0, then $I_5 = 0$

" D=1, " $I_5 = 1$



D=0

	0	1	2	3	4	5	6	7
	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
	1	0	1	0	0	1	0	1

D=1

	8	9	10	11	12	13	14	15
	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
	1	1	0	1	1	0	0	1

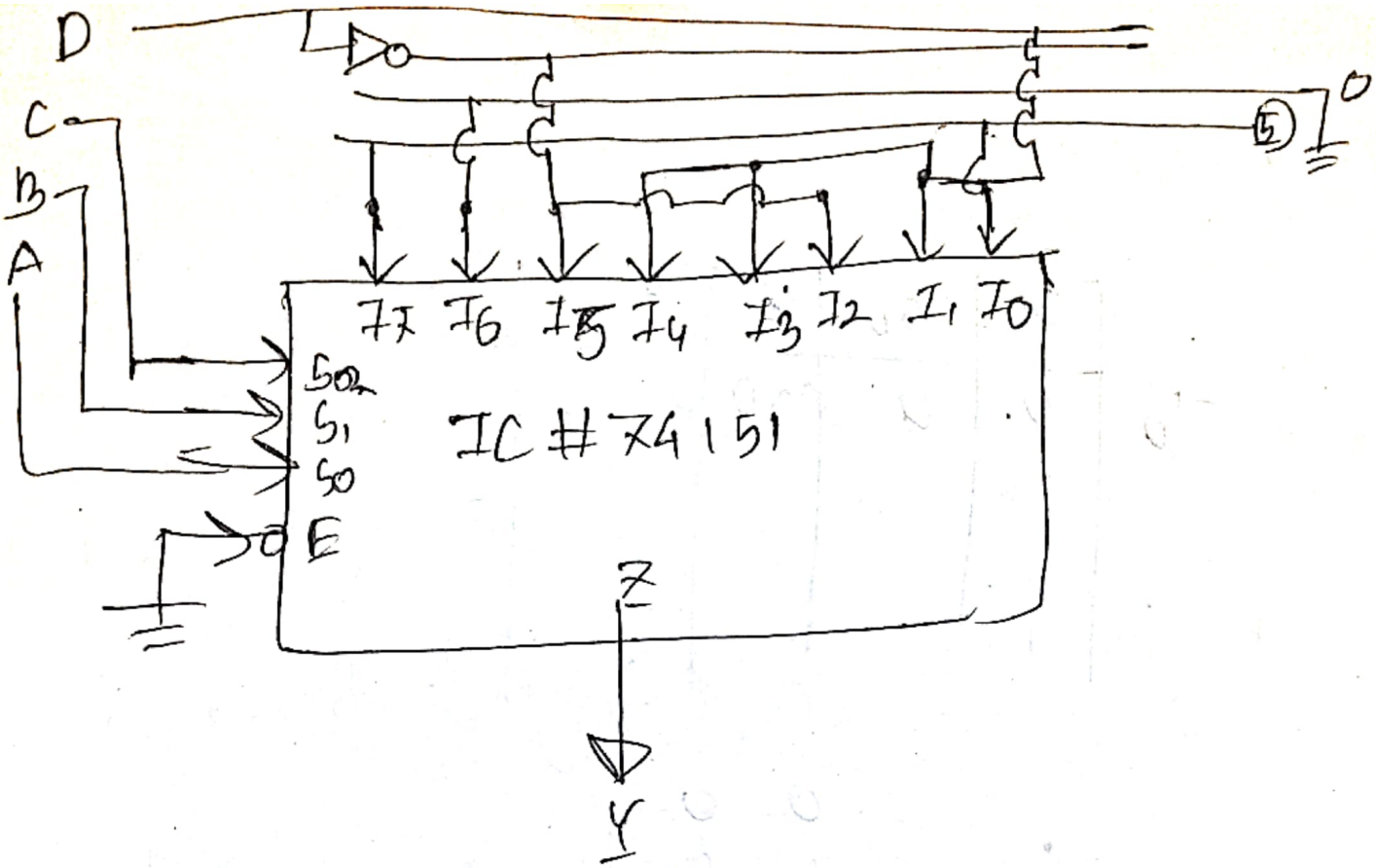
$F(A, B, C, D) = \Sigma(0, 2, 5, 7, 8, 9, 11, 12, 15)$

$1 = I_7, I_0$

$0 = I_6$

$D = I_1, I_3, I_4$

$\bar{D} = I_2, I_5$



→ SAP4 → Next class

↳ Simple As Possible Computer

48 1 MUX — IC#74153

12:50 PM | 30-03-2022

DESIGN AND IMPLEMENTATION OF (SAP-1)

SAP → Simple As possible computer

- 2 operation (Logical and Arithmetic)

→ Addition and subtraction (Arithmatic)

⊞ SAP(-1) ⇒ Logical possible না

→ Programming (Assembly Language)

Machine Language

MATHEMATICS

(SAP-1) Slide Page-3

program counter

↳ এ কাজ currently আমি কোন লাইনে আছি

- এ কোন Line এ Jump করবে।

size 4 so Maximum 16 লাইন লেখা যাবে।

→ Only counts OP.

Accumulator

↳ এতে প্রথমে একটা value থাকতে হয়, যাকে যোগ করবো তাকে B তে রাখবো। Adder কল দিলে যোগ করবে। ↳ Register

Subtractor কল দিলে বিয়োগ করবে।

→ প্রতিটি operation শেষ করার পরে Registered Result "Accumulator" এ যাবে। Output কল দিলে তা পরে Output Register এ যাবে।

Add/Sub unit is 8-bit numbers.

Accumulator – "A"

Register – "B"

Adder/Subtractor

↳ "A+B" OR "A-B"

After the end of the operation Accumulator contains the answer

MAR → Memory Address Register

LDA → Load Accumulator ← ACC ← RAM [MAR]

ADD → Addition → Add Ram data to accumulator
ACC ← ACC + B

SUB → Subtraction → Subtract RAM data
↳ ACC ← ACC − B

OUT → OUT ← ACC

HLT → CLK ← 0

HLT → Halt

↑
অবশ্যই capital letter এ লিখতে হবে।

=

LDA 8H → Hexadecimal

↳ means 8 নম্বর location এ 8 যে value আছে তাকে Load করো।

LDA FH → ~~load~~ load the accumulator with contents of memory location FH.

FH কেও বলতে হবে Hexa decimal এ

⊞ LDA stands for Load the Accumulator.

⊞ LDA, ADD, SUB are called memory reference instructions because they use data stored in the memory.

Mnemonics

LDA	ADD	SUB	OUT	HLT
0000	0001	0010	1110	1111

OP code

OP code stands for operation code.

Program in Assembly

Address

0H to FH

1. ACC ← RAM[9H]
2. ACC ← 10H
3. ACC ← 10H + 18H
4. ACC ← 10H + 18H + 20H
5. ACC ← 10H + 18H + 20H − 14H
6. OUT ← ACC[ ].

10H + 18H + 20H − 14H

~~ACC ← 10~~

Maximum 7 operation :

① + ①

কেন? OUT, HLT

16-2 = 14 ~~op~~

এখন প্রতি ~~operation~~ Add/sub এ 2টি করে operation লাগে তাই $\frac{14}{2}$ = 7 operation possible.

blank থাকলে operation এর op code এ

All ফিল্ড 2টি। [1111]

03-04-22

SAP1 :- ▷ only Addition and Subtraction

MRE

1. LDA : Load to the Accumulator

		OPP code
LDA 8H	ACC ← RAM[8H]	0000

2. ~~Ad~~ ADD : Addition

		OPP code
ADD AH	ACC ← ACC + RAM[AH]	0001

3. SUB : Subtraction

		OPP code
SUB 9H	ACC ← ACC - RAM[9H]	0010

NOT MRE

			OPP code
4. OUT : Output	OUT ← ACC	1110	~~0010~~
5. HLT : Halt	Stop the program		OPP code 1111

* SAP1 থেকে 25 Marks এর Question থাকবে।

#Write the assembly language program and machine lang. that perform the following operations: 10H + 18H + 20H - 14H

Assembly language

Address	Contents
0H	LDA FH
1H	ADD EH
2H	ADD DH
3H	SUB CH
4H	OUT FH
5H	HLT FH
6H	FFH
7H	FFH
8H	FFH
9H	FFH
AH	FFH
BH	FFH
CH	14H
DH	20H
EH	18H
FH	10H

Machine Language

Address	Content (in binary)		Contents in Hex (Optional)
0000	0000	1111	0FH
0001	0001	1110	1EH
0010	0001	1101	1DH
0011	0010	1100	2CH
0100	1110	1111	EFH
0101	1111	1111	FFH
0110	1111	1111	FFH
0111	1111	1111	FFH
1000	1111	1111	FFH
1001	1111	1111	FFH
1010	1111	1111	FFH
1011	1111	1111	FFH
1100	0001	0100	14H
1101	0010	0000	20H
1110	0001	1000	18H
1111	0001	0000	10H

→ Hex to Binary এর জন্য Address এর per digit এর BCD লিখে দিলেই চলে।

Create a SAP1 assembly language program and then generate the machine code for following expression

52+28-38+72-12. These number is in decimal form.

→ Decimal to Hexa তে করতে হবে এমনটা।

D : 52+28-38+72-12

H : 34H+1CH-26H+48H ~~0CH~~ -0CH

; zero

Assembly Language		Machine Language		
Address	Contents	Address	Content (In Binary)	Content (in Hex)
0 H	LDA FH	0000	0000 1111	0 FH
1 H	ADD EH	0001	0001 1110	1 EH
2 H	SUB DH	0010	0010 1101	2 DH
3 H	ADD CH	0011	0001 1100	1 CH
4 H	SUB BH	0100	0010 1011	2 BH
5 H	OUT FH	0101	1110 1111	E FH
6 H	HLT FH	0110	1111 1111	FFH
7 H	FFH	0111	1111 1111	FFH.
8 H	FFH	1000	1111 1111	FFH
9 H	FFH	1001	1111 1111	FFH
A H	FFH	1010	1111 1111	FFH
B H	0CH	1011	0000 1100	0CH
C H	48 H	1100	0100 1000	48H
D H	26H	1101	0010 0110	26 H
E H	1CH	1110	0001 1100	1CH
F H	34H	1111	0011 0100	34H

Create a SAP1 assembly language Program and then generate the machine code for the expression of 18-20+35+37-8. These number is in decimal form.

D: 18 -20 +35+37-8

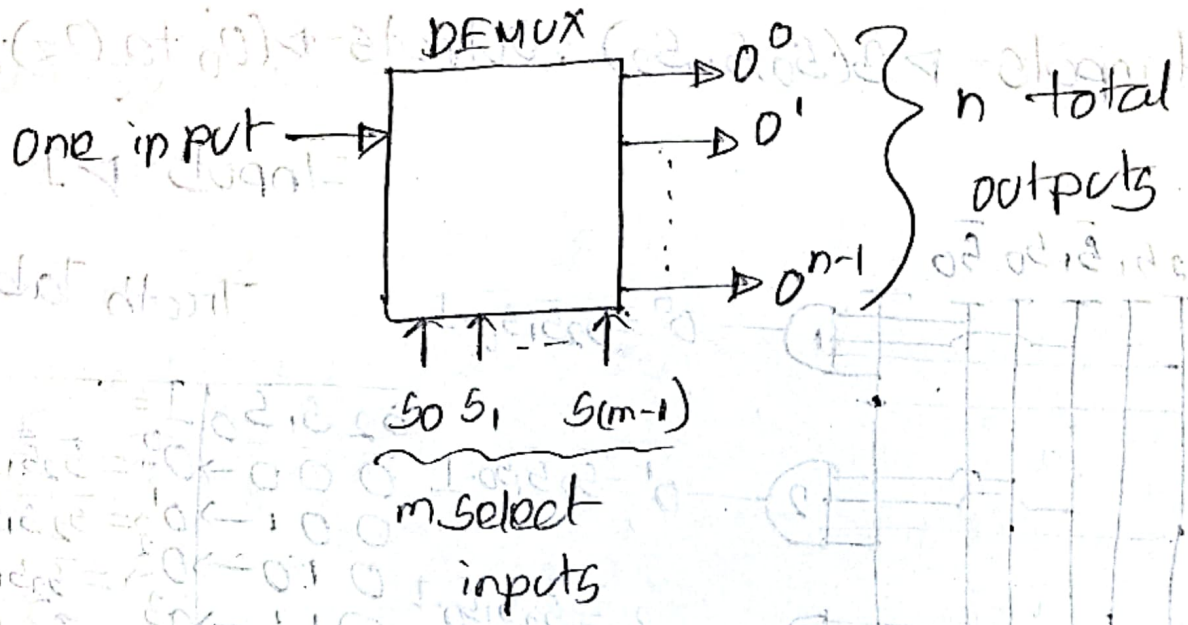
H: 12H - 14H + 23H + 25H - 8H

Assembly Language		Machine Language		
Address	Contents	Address	Contents (In Binary)	Contents (In H
0H	LDA FH	0000	0000 1111	0FH
1H	SUB EH	0001	0010 1110	2 ~~D~~E
2H	ADD DH	0010	0001 1101	1 DH
3H	ADD CH	0011	0001 1100	1 CH
4H	SUB BH	0100	0010 1011	2 BH
5H	OUT FH	0101	1110 1111	E F~~A~~H
6H	HLT FH	0110	1111 1111	FFH
7H	FFH	0111	1111 1111	FFH
8H	FFH	1000	1111 1111	FFH
9H	FFH	1001	1111 1111	FFH
A~~B~~H	FFH	1010	1111 1111	FFH
B~~A~~H	08H	1011	0000 1000	08H
C~~D~~H	25H	1100	0010 0101	25H
D~~C~~H	23H	1101	0010 0011	23H
E~~F~~H	14H	1110	0001 0100	14H
F~~E~~H	12H	1111	0001 0010	12H

③ Demultiplexer (DEMUX):

06-03-2022

What is DEMUX?



At a time input goes to the one of the outputs according to corresponding combination of select inputs.

No of select inputs	No of outputs
2	4
3	8
4	16
5	32

$\therefore$ No of outputs $= 2^{(\text{No of select inputs})}$

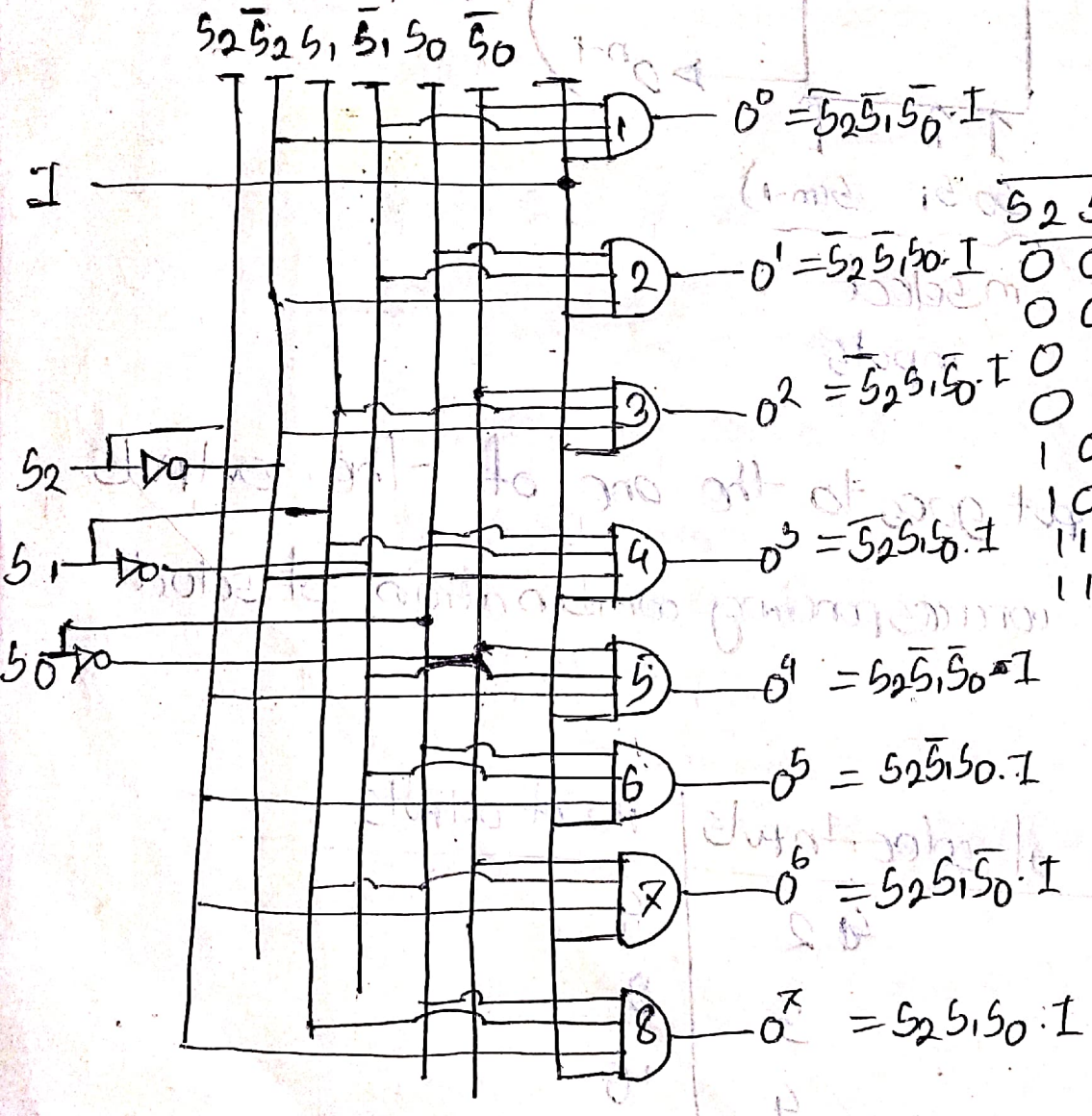
$\therefore n = 2^m$

1 of 8 DEMUX → DEMUX:

(1 line to 8 line DEMUX)

Select inputs → 3 (S_0, S_1, S_2) ; Outputs → (O_0 to O_7);

Inputs → I

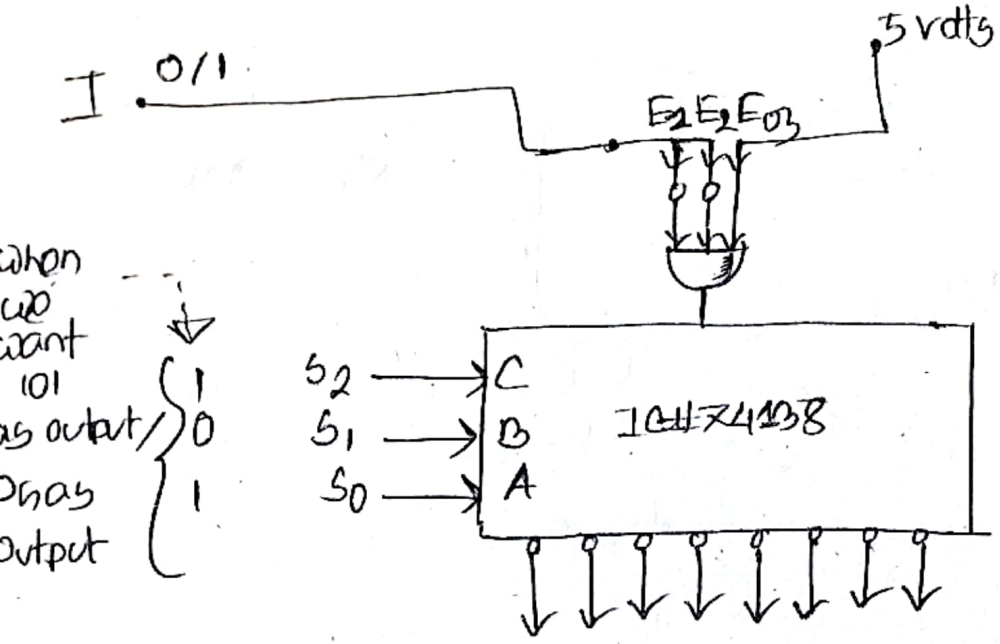


Truth Table

S_2 S_1 S_0	I =
0 0 0 →	$O^0 = \bar{S}_2\bar{S}_1\bar{S}_0 \cdot I$
0 0 1 →	$O^1 = \bar{S}_2\bar{S}_1 S_0 \cdot I$
0 1 0 →	$O^2 = \bar{S}_2 S_1 \bar{S}_0 \cdot I$
0 1 1 →	$O^3 = \bar{S}_2 S_1 S_0 \cdot I$
1 0 0 →	$O^4 = S_2\bar{S}_1\bar{S}_0 \cdot I$
1 0 1 →	$O^5 = S_2\bar{S}_1 S_0 \cdot I$
1 1 0 →	$O^6 = S_2 S_1 \bar{S}_0 \cdot I$
1 1 1 →	$O^7 = S_2 S_1 S_0 \cdot I$

IC#74138 দিয়ে Decoder / DEMUX দুটো একত্রে বানাতে পারি।

Design 1 of 8 (1 line to 8 lines) DEMUX using IC#74138.



Active low output means

0 → Active
1 → Inactive

অর্থাৎ 0 হলে তবে Active, 1 হলে Inactive

IC Active:

Active: $E_1 = E_2 = 0$; $E_3 = 1$.

when $I = 0$, $O_5 = 0$

" $I = 1$, $O_5 = 1$

when $I = 0$ then IC is Active

when $I = 1$ then IC is Inactive.

END of chapter-9

MSI logic circuits #

10-04-2022

Chapter 6:

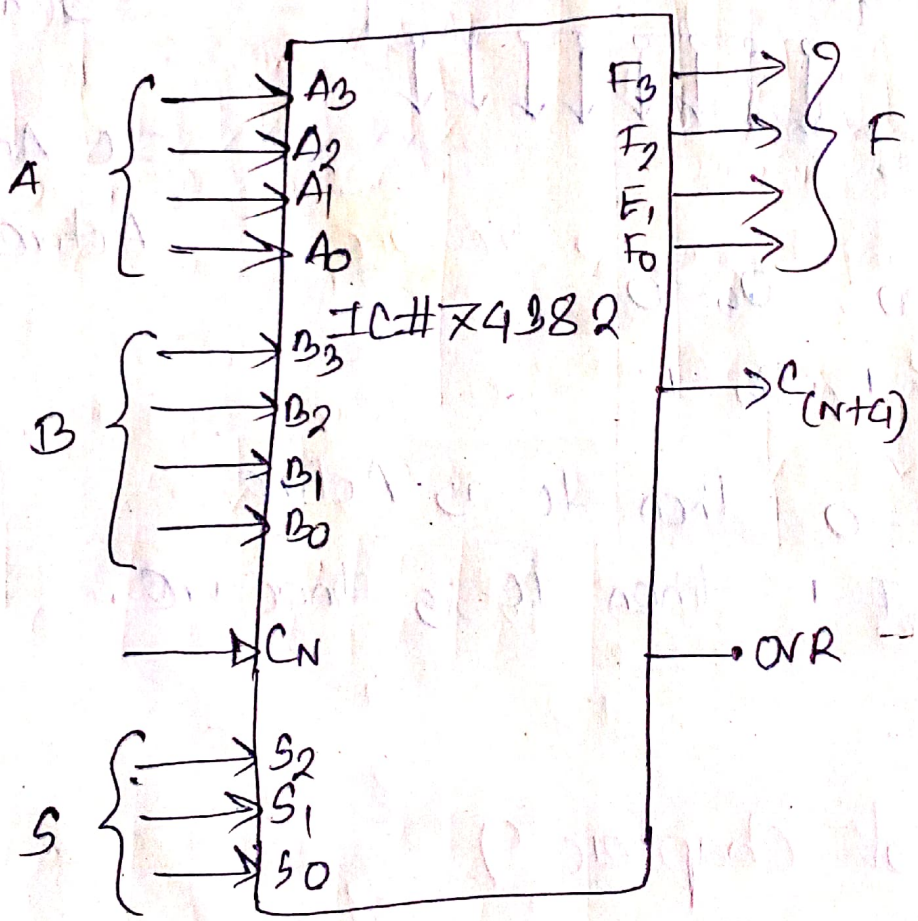
ALU: (Arithmetic Logic Unit)

IC#1
N=0

IC#2
N=4
C_4 = Carry In
C_8 = Carry Out

IC# 74382: (4 bit ALU)

Block Diagram:



A: 4-bit input Number

B: 4 bit input number

S: 3 bit select input

C_N: carry input

(overflow)

F: 4-bit output number

$C_{(N+4)}$: Carry output

OVR: overflow

Function Table:

	S_2	S_1	S_0	operation	comments
	✓0	0	0	CLEAR	$F_3F_2F_1F_0=[0000]$
Arithmetic OP	0	0	1	B minus A	C_N has to be 1 কেননা subtraction এ Addition এ আবার লাগে
	0	1	0	A minus B	C_N has to be 1; $C_N=1$
	0	1	1	A plus B	$C_N=0$
Logical OP	1	0	0	A XOR B ($A \oplus B$)	Ex-OR operation
	1	0	1	A OR B ($A+B$)	OR operation
	1	1	0	AB (A and B)	AND operation
	✓1	1	1	PRESET	$F_3F_2F_1F_0=[1111]$

$A_3A_2A_1A_0=[1011]$

$B_3B_2B_1B_0=[1101]$

$\rightarrow S_2S_1S_0=[100]$

$F_3F_2F_1F_0$

$=[0110]$

$S_3S_2S_1=[011]$ $\quad C_N=0$

$F_3F_2F_1F_0=[1000]$

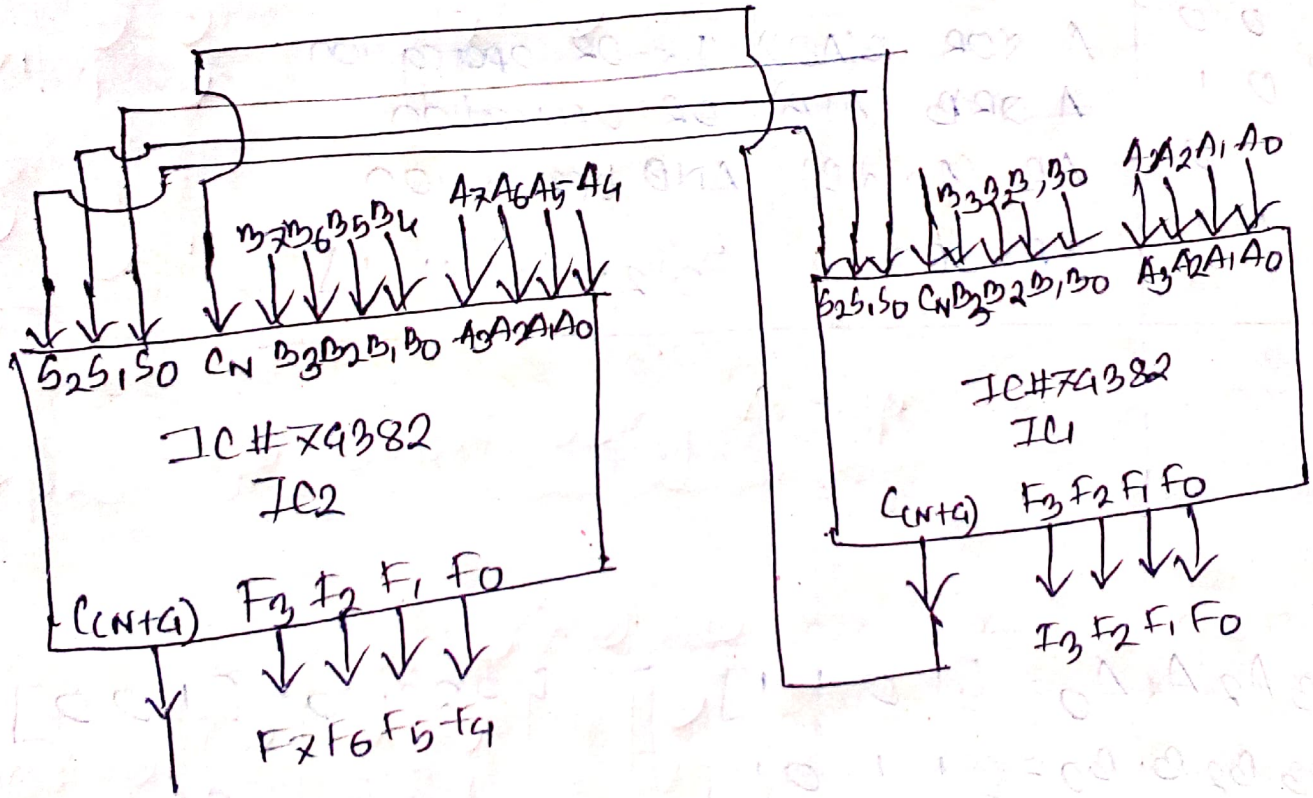
$C_{(N+4)}=1$

Design 8 bit ALU using IC# 74382:

$A_7\ A_6\ A_5\ A_4\ A_3\ A_2\ A_1\ A_0$

$B_7\ B_6\ B_5\ B_4\ B_3\ B_2\ B_1\ B_0$

$[F_7\ F_6\ F_5\ F_4\ F_3\ F_2\ F_1\ F_0]$



13-04-22

Synchronous counter design for any random sequence [Final এ অবশ্যই আসবে] VVI

Ex $\boxed{0, 1, 3, 5, 7}$, 0 ...

~~Before Pulse | After Pulse~~

C	B	A	C	B	A
0	0	0	0	0	1
0	0	1	0	1	1
0	1	0	1	0	1
0	1	1	1	0	1
1	0	0			
1	0	1			
1	1	0			
1	1	1			

(*) Undesired states

If undesire state comes then it starts from 000.

Circuit excitation table

Step 1:

J	K	clk	
0	0	↓	No change
0	1	↓	0
1	0	↓	1
1	1	↓	Toggle

Before Pulse	After Pulse							
C B A	C B A	J_C	K_C	J_B	K_B	J_A	K_A
0 0 0	0 0 0	0	x	0	x	1	x
0 0 1	0 0 1	0	x	1	x	x	0
(*) 0 1 0	0 0 0	0	x	x	1	0	x
0 1 1	1 0 1	1	x	x	1	x	0
(*) 1 0 0	0 0 0	x	1	0	x	0	x
1 0 1	1 1 1	x	0	1	x	x	0
(*) 1 1 0	0 0 0	x	1	x	1	0	x
1 1 1	0 0 0	x	1	x	1	x	1

Truth Table of JK:

	J	K	clk	QJ	K
0→0	0 0	0 1		0	x
0→1	1 1	0 1		1	x
1→1	0 1	0 0		x	0
1→0	1 0	1 1		x	1

Step 2: Simplification using K-Map

$J_C = AB$;

	$\bar{A}\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$
$\bar{C}$	0	0	1	0
C	x	x	x	x

$K_C = \bar{A} + B$;

x	x	x	x
1	0	1	1

$J_B = A$;

0	1	x	x
0	1	x	x

$K_B = 1$;

	$\bar{A}\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$
$\bar{C}$	x	x	1	1
C	x	x	x	1

$J_A = \bar{B}\bar{C}$;

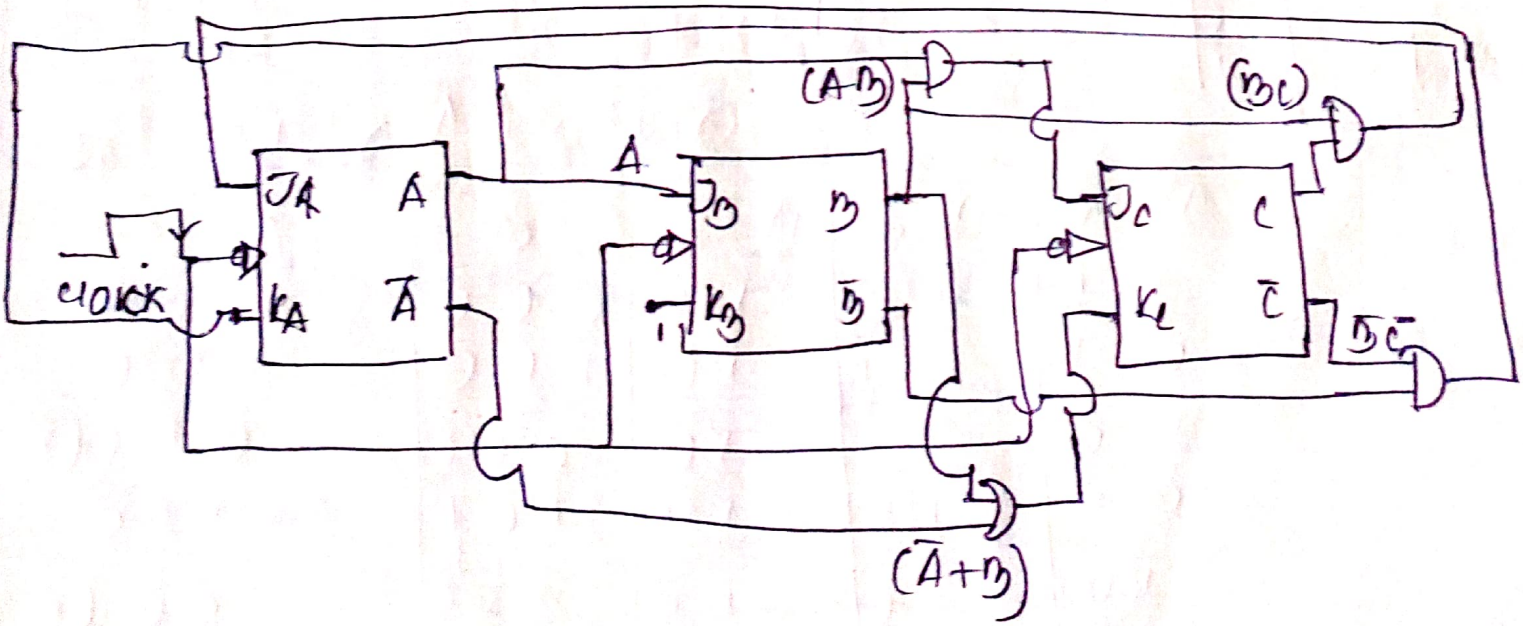
1	x	x	0
0	x	x	0

$K_A = BC$;

x	0	0	x
x	0	1	x

Step 3: Circuit Diagram

MOD8 = $J_A = K_A = 1$; $J_B = K_B = A$; $J_C = K_C = AB$ Instead of → $J_A = \bar{B}\bar{C}$, $K_A = BC$; $J_B = A$, $K_B = 1$; $J_C = AB$, $K_C = \bar{A}+B$



17-04-2022

$F(A,B,C) = \Sigma$

Sequence: $\boxed{0, 1, 4, 6, 7,}$ 0, 1 ---

Step-1: Circuit excitation table

Before pulse	After pulse	J_C K_C	J_B K_B	J_A K_A
000	001	0 x	0 x	1 x
001	100	1 x	0 x	x 1
010	000	0 x	x 1	0 x
011	000	0 x	x 1	x 1
100	110	x 0	1 x	0 x
101	000	x 1	0 x	x 1
110	111			1 x
111	000	x 0	x 0	x 1
		x 1	x 1	

Step2: Simplification Using K-Map

$J_C = \bar{A}\bar{B}$;

	$\bar{A}\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$
T	0	1	0	0
C	x	x	x	x

$K_C = A$;

	$\bar{A}\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$
$\bar{C}$	x	x	x	x
C	0	1	1	0

$J_B = \bar{A}\,C$;

0	0	x	x
1	0	x	x

$K_B = \bar{C} + A$;

x	x	1	1
x	x	1	0

$J_A = B\bar{C} + BC$
$= \overline{B \oplus C}$;

1	x	x	0
0	x	x	1

$K_A = 1$;

x	1	1	x
x	1	1	x

Sequence : 0, 1, 3, 5, 7, 9, 10, 13, 14, 15, 0,

Step 1 : Circuit excitation table

DCBA before pulse	DCBA After pulse	J_D K_D	J_C K_C	J_B K_B	J_A K_A
0000	0001	0 x	0 x	0 x	1 x
0001	0011	0 x	0 x	1 x	x 0
* 0010	0000	0 x	0 x	x 1	0 x
0011	0101	0 x	1 x	x 1	x 0
* 0100	0000	0 x	x 1	0 x	0 x
0101	0111	0 x	x 0	1 x	x 0
* 0110	0000	0 x	x 1	x 1	0 x
0111	1001	1 x	x 1	x 1	x 0
* 1000	0000	x 1	0 x	0 x	0 x
1001	1010	x 0	0 x	1 x	x 1
1010	1101	x 0	1 x	x 1	1 x
* 1011	0000	x 1	0 x	x 1	x 1
* 1100	0000	x 1	x 1	0 x	0 x
1101	1110	x 0	x 0	1 x	x 1
1110	1111	x 0	x 0	x 0	1 x
* 1111	0000	x 1	x 1	x 1	x 1

Step2: Simplification using K-Map

$J_D = ABC$;

	$\bar{A}\bar{B}$	$\bar{A}B$	AB	$A\bar{B}$
$\bar{C}\bar{D}$	0	0	0	0
$C\bar{D}$	0	0	1	0
CD	x	x	x	x
$\bar{C}D$	x	x	x	x

$K_D = \bar{A}\bar{B} + AB$;

$= \overline{A \oplus B}$

x	x	x	x
x	x	x	x
1	0	1	0
1	0	1	0

$J_C =$;

$AB\bar{D} + \bar{A}BD$

0	0	1	0
x	x	x	x
x	x	x	x
0	0	x	1

$K_C = \bar{A}\bar{B} + AB + \bar{A}B$

$= \overline{A \oplus B} + \bar{A}B$

x	x	x	x
1	0	1	1
1	0	1	0
x	x	x	x

$J_B = A$;

0	1	x	x
0	1	x	x
0	1	x	x
0	1	x	x

$K_B = \bar{D} + A + \bar{C}$;

x	x	1	1
x	x	1	1
x	x	1	0
x	x	1	1

$J_A = BD + \bar{B}\bar{C}\bar{D}$;

1	x	x	0
0	x	x	0
0	x	x	1
0	x	x	1

$K_A = D$;

x	0	0	x
x	0	0	x
x	1	1	x
x	1	1	x