UNIVERSITY OF ASIA PACIFIC

Department of Computer Science & Engineering

Course Title : Digital Logic & System Design Lab

Course Code : CSE 210

Experiment No. : 06

Experiment Name : a) Test and verify the truth table of Clocked D flip-flop (IC#7474)
b) Implement a clocked D flip-flop.
c) Test and verify the truth table of Clocked JK flip-flop (IC#7476).
d) Implement a clocked JK flip-flop.

Date of Performance : 22-02-2022

Date of Submission : 27-02-2022

Submitted by:

Name : Sheikh Nafez Sadnan

Reg. No. : 20101106

Roll No. : 106

Section : B (2)

Submitted To:

Shammi Akhtar

Assistant Professor

Department of CSE

University of Asia Pacific

A.

Problem Statement: a) Test and verify the truth table of Clocked D flip-flop (IC#7474)

b) Implement a clocked D flip-flop.

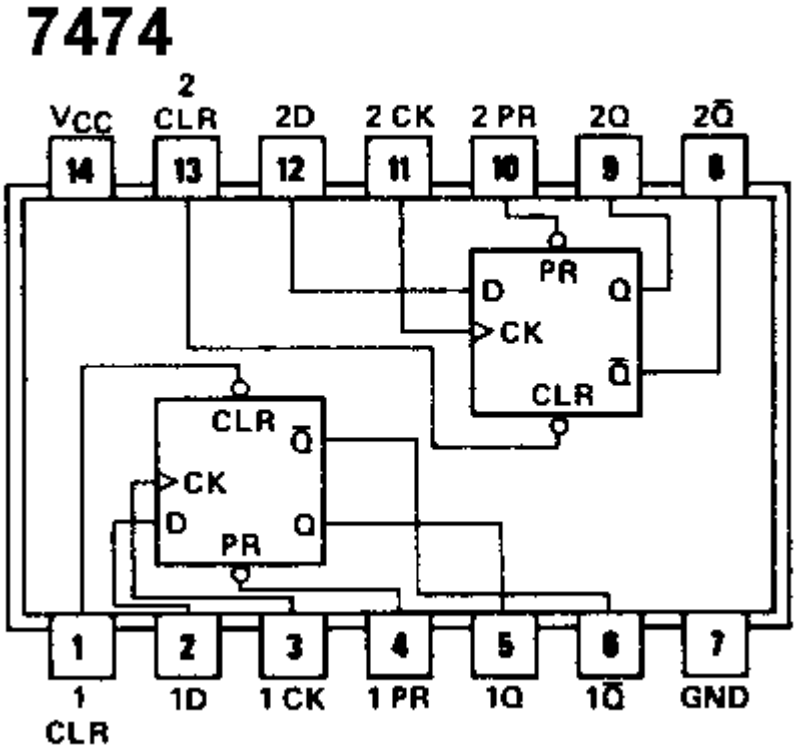
c) Test and verify the truth table of Clocked JK flip-flop (IC#7476).

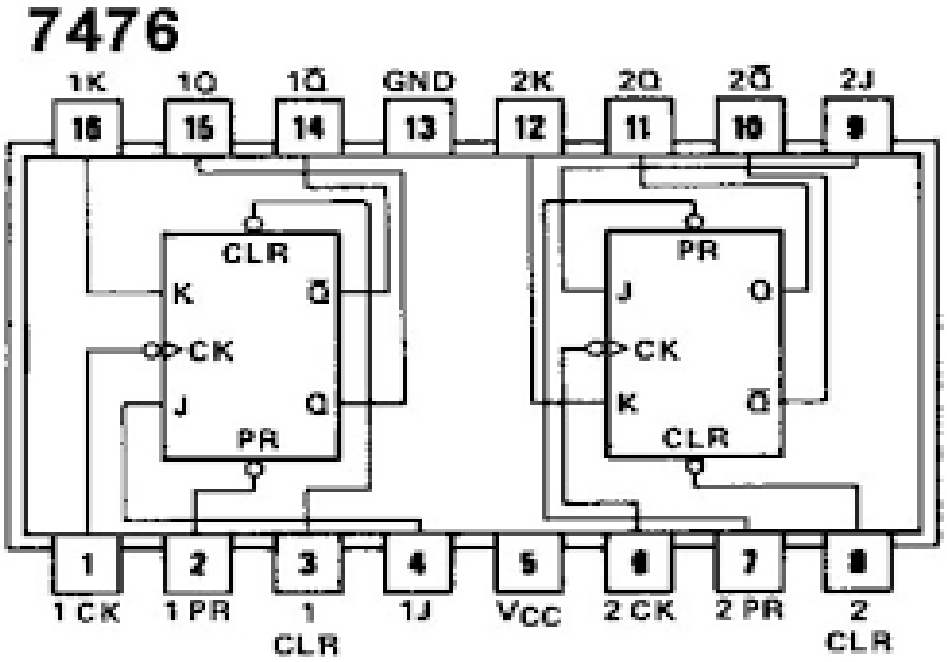
d) Implement a clocked JK flip-flop.

Instruments (Used in This Experiment):

i. IC-7474 (D Flip Flop)
ii. IC-7476 (JK Flip Flop)
iii. IC-7408 (AND GATE)
iv. IC-7432 (OR GATE)
v. IC-7404 (NOT GATE)
vi. IC-7411 (NAND GATE)
vii. Pulse Generator
viii. Wires
ix. Trainer board

IC Diagram:





Truth Table:

D Flip Flop:

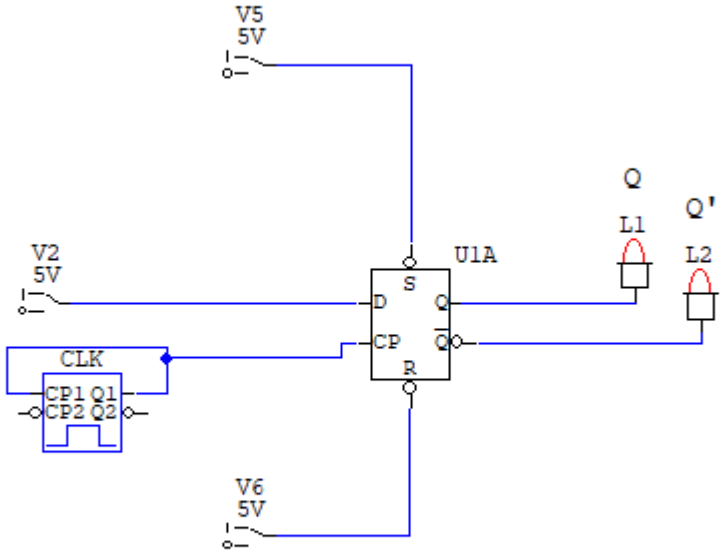
D	CLK	Q	Q’
0	↑	0	1
1	↑	1	0

J K Flip Flop:

J	K	CLK	Q	Q’
0	0	↑	NC	NC
0	1	↑	0	1
1	0	↑	1	0
1	1	↑	Toggle	Toggle

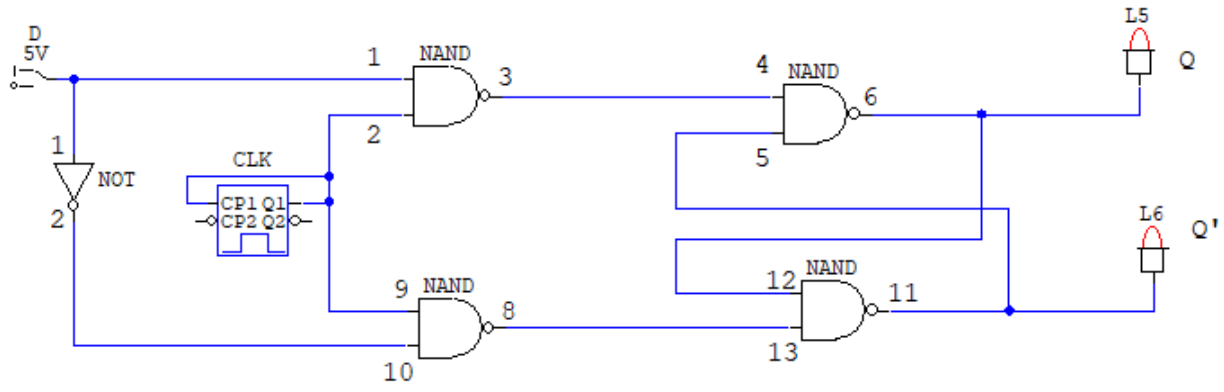
Logic Diagram:

D Flip Flop IC:



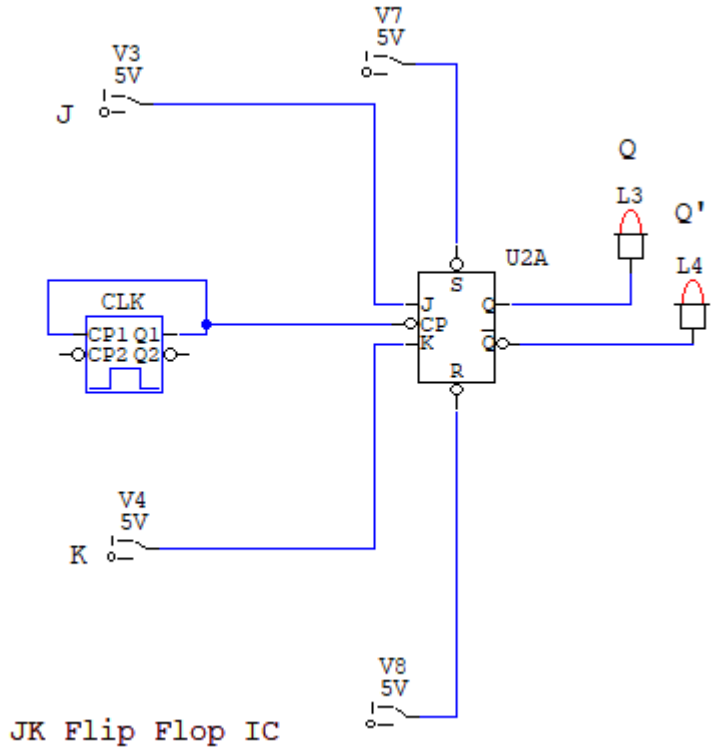
D Flip Flop IC

D Flip Flop with Logic Gates:

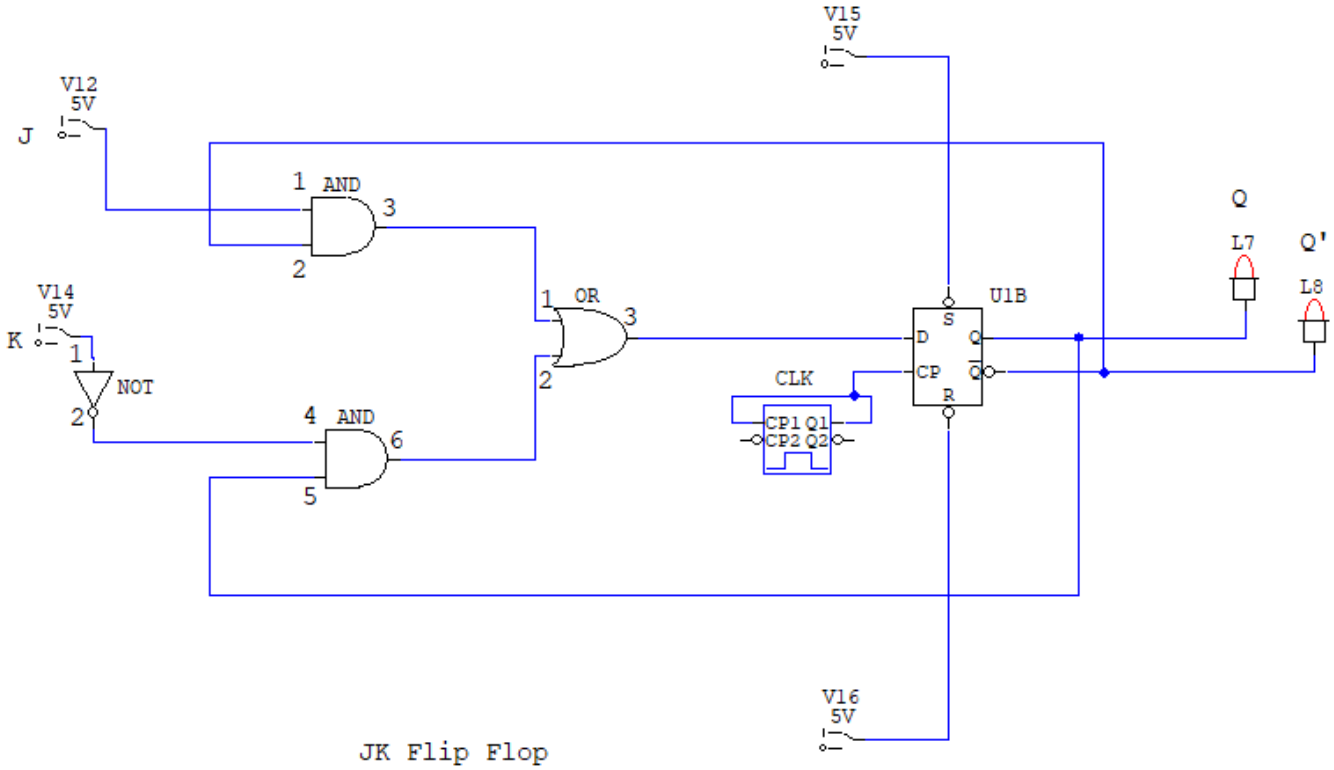


D Flip Flop

JK Flip Flop IC:



JK Flip Flop with Logic Gates:



Discussion: In this experiment, we learned how to design IC of D and JK flip-flops. Also we verified our circuits via truth table. We analyzed behave of flip-flops under the condition of clocked. Safety issues were strictly maintained during the experiment.