



UNIVERSITY OF ASIA PACIFIC

Department of Computer Science & Engineering

Course Title : Digital Logic & System Design Lab

Course Code : CSE 210

Experiment No. : 03

Experiment Name : Test and verify the universality of -
a) NAND gate
b) NOR gate

Date of Performance : 01-02-2022

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A.

Problem Statement: Test and verify the universality of -

- a) NAND gate
- b) NOR gate

Input and Output Variables:

Here A,B is input and Y is output

Instruments (Used in This Experiment):

- i. IC-7400 (NAND GATE)
- ii. IC-7402 (NOR GATE)
- iii. Wires
- iv. Trainer board

Truth Table:

AND Gate

Input		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

OR Gate

Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

NAND Gate

Input		Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

NOR Gate

Input		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

XOR Gate

Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

NOT Gate

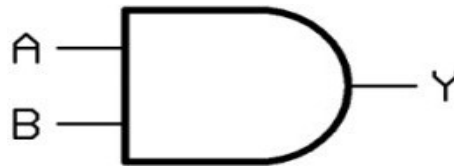
Input	Output
0	1
1	0

Logic Expression:

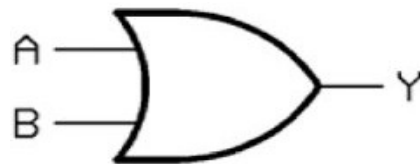
Logic Gate	Logic Expression
AND	$Y = A \cdot B$
OR	$Y = A + B$
NOT	$Y = \overline{A}$
NAND	$Y = \overline{A \cdot B}$
NOR	$Y = \overline{A + B}$
XOR	$Y = A \oplus B$

Logic Diagram:

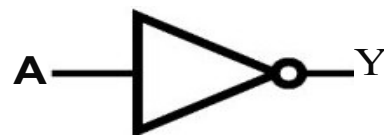
AND Gate:



OR Gate:



NOT Gate:



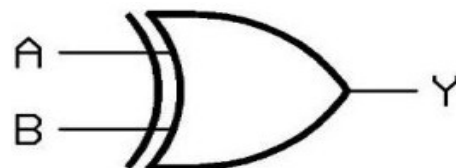
NAND Gate:



NOR Gate:



XOR Gate:

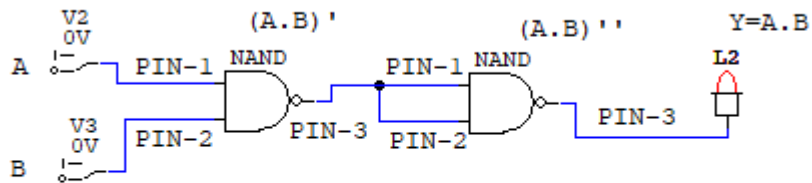


Circuit Diagram: (with logical equation)

Using NAND Gate:

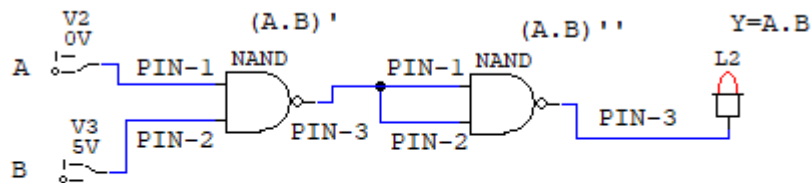
a) AND

Input A=0, B=0



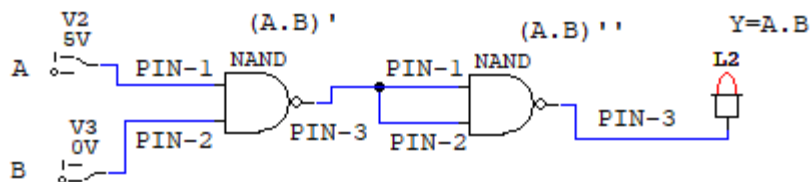
NAND TO AND

Input A=0, B=1



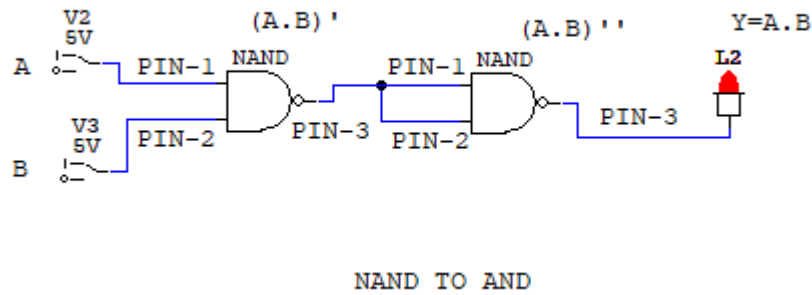
NAND TO AND

Input A=1, B=0



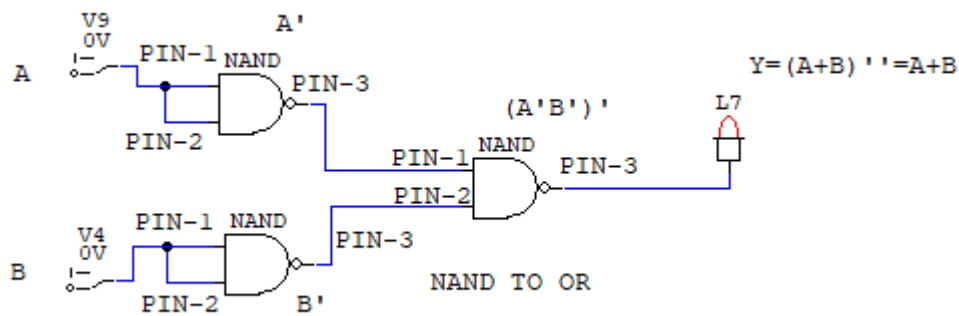
NAND TO AND

Input A=1, B=1

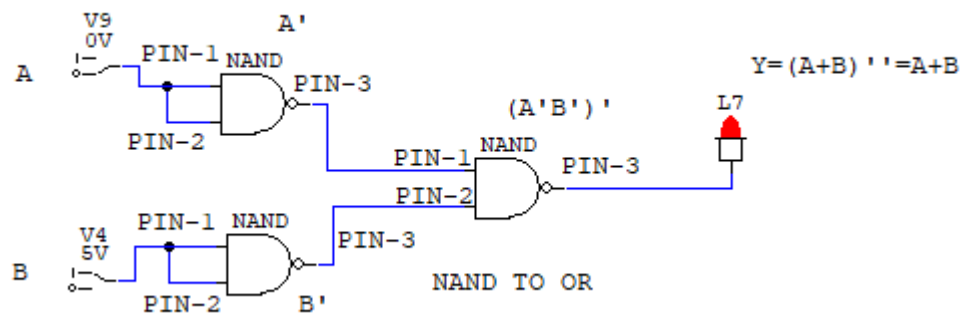


b) OR : $A + B = ((A.A)' . (B.B)')'$

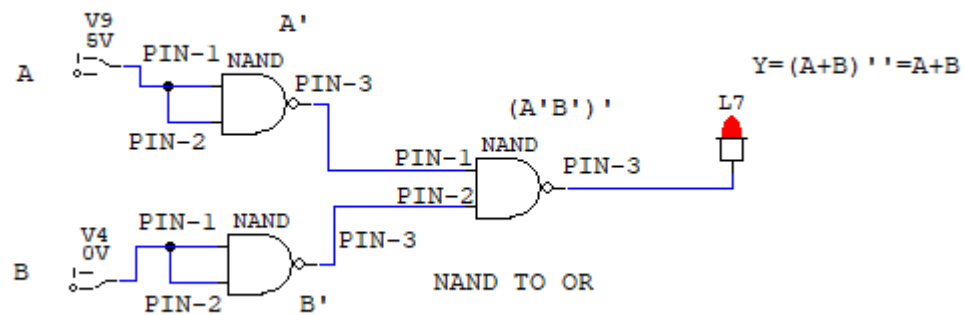
Input A=0, B=0



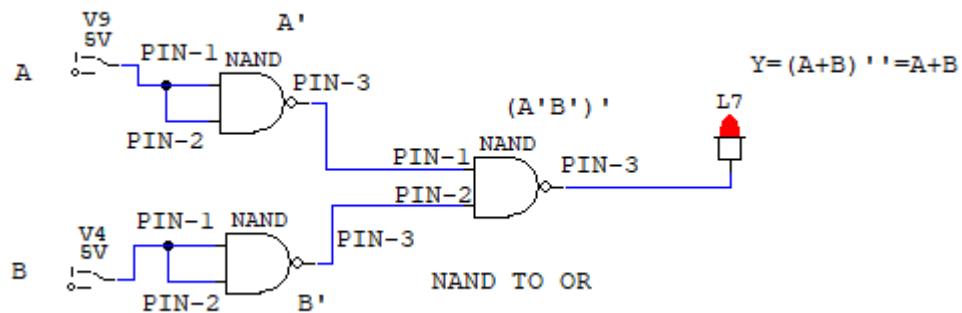
Input A=0, B=1



Input A=1, B=0

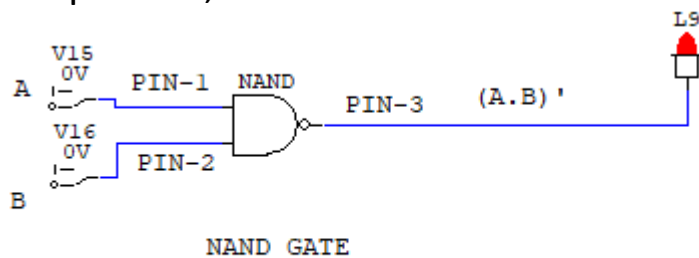


Input A=1, B=1

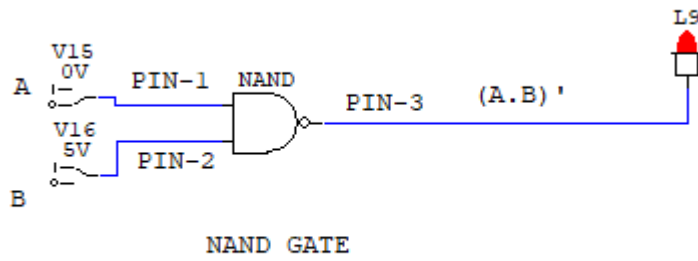


c) NAND

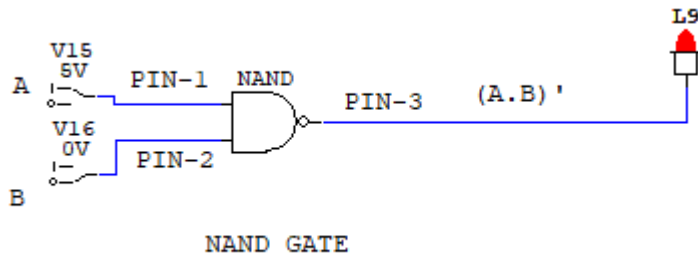
Input A=0, B=0



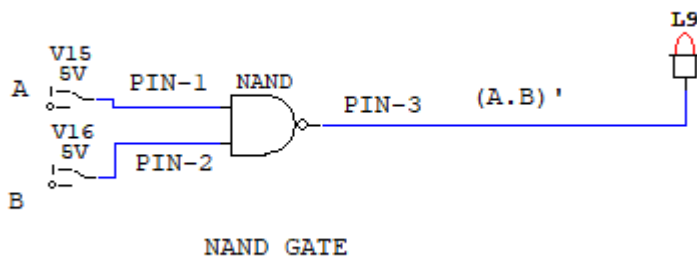
Input A=0, B=1



Input A=1, B=0

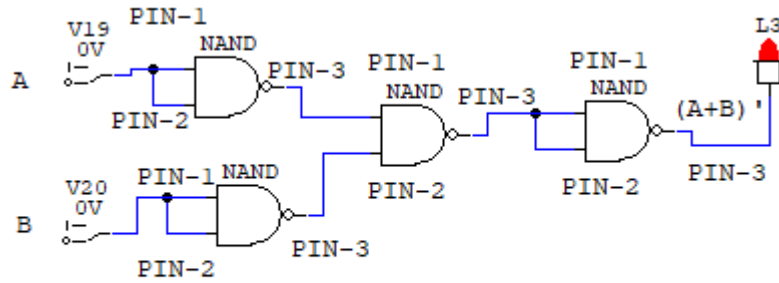


Input A=1, B=1



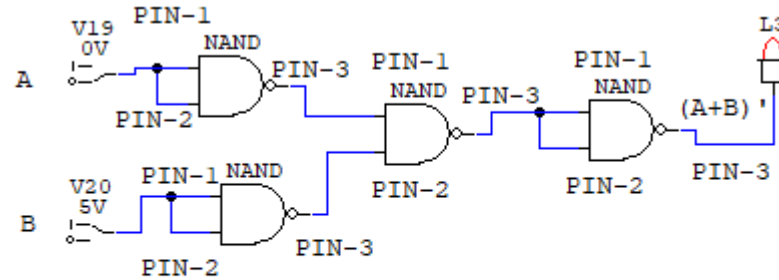
d) NOR

Input A=0, B=0



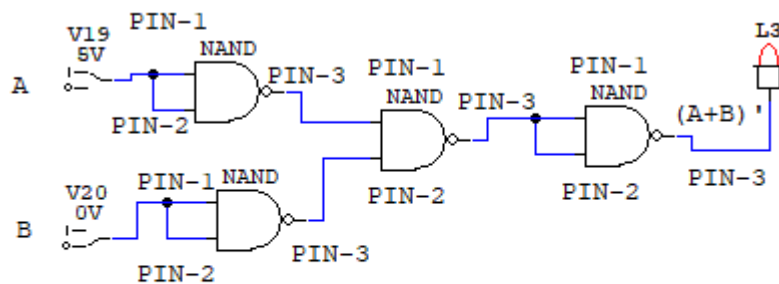
NAND TO NOR

Input A=0, B=1



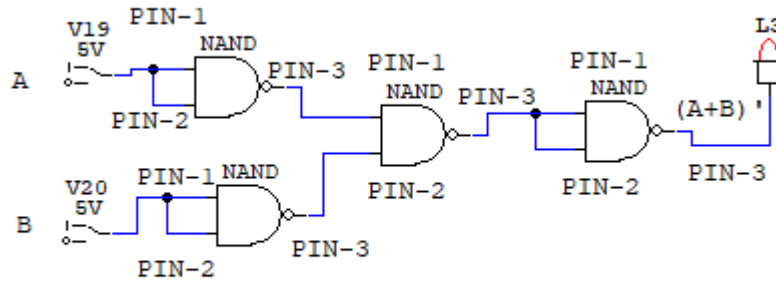
NAND TO NOR

Input A=1, B=0



NAND TO NOR

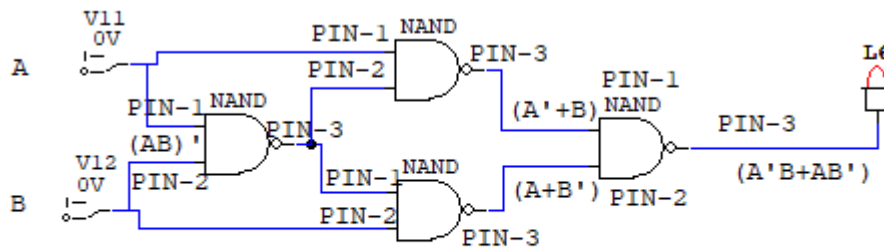
Input A=1, B=1



NAND TO NOR

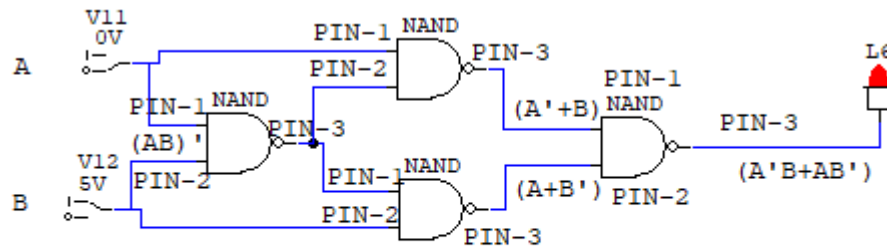
e) XOR

Input A=0, B=0



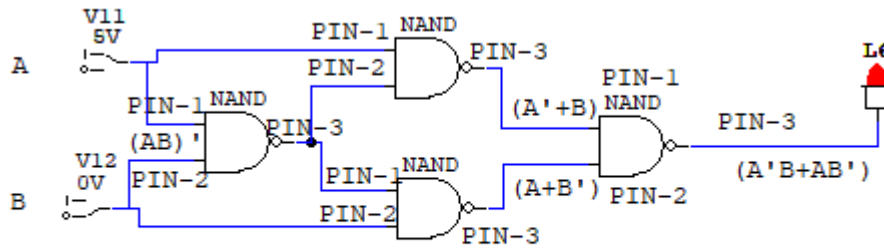
NAND TO XOR

Input A=0, B=1



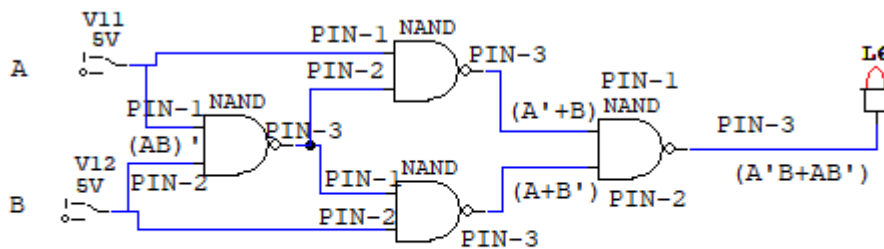
NAND TO XOR

Input A=1, B=0



NAND TO XOR

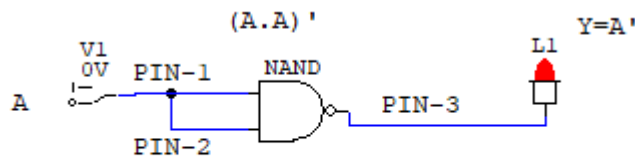
Input A=1, B=1



NAND TO XOR

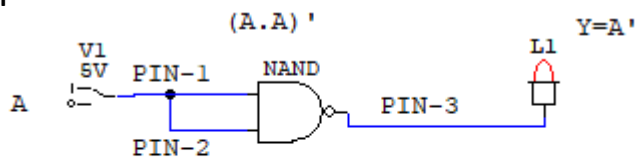
f) NOT : $A' = (A.A)'$

Input A=0



NAND TO NOT

Input A=1

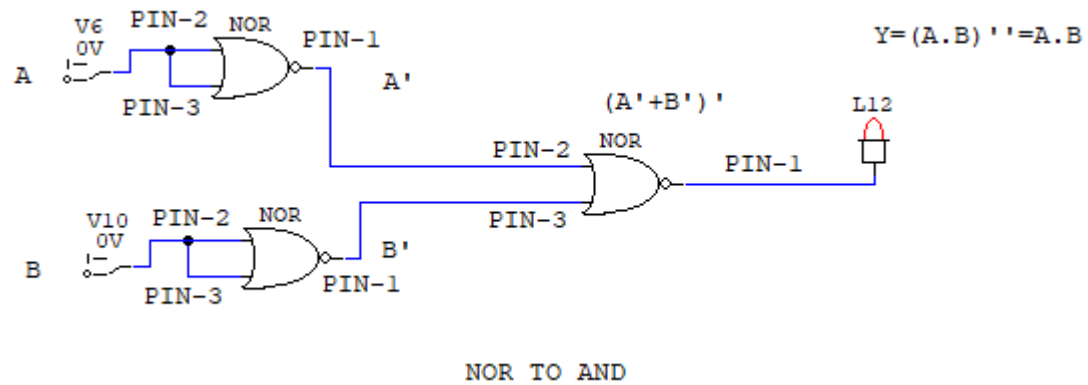


NAND TO NOT

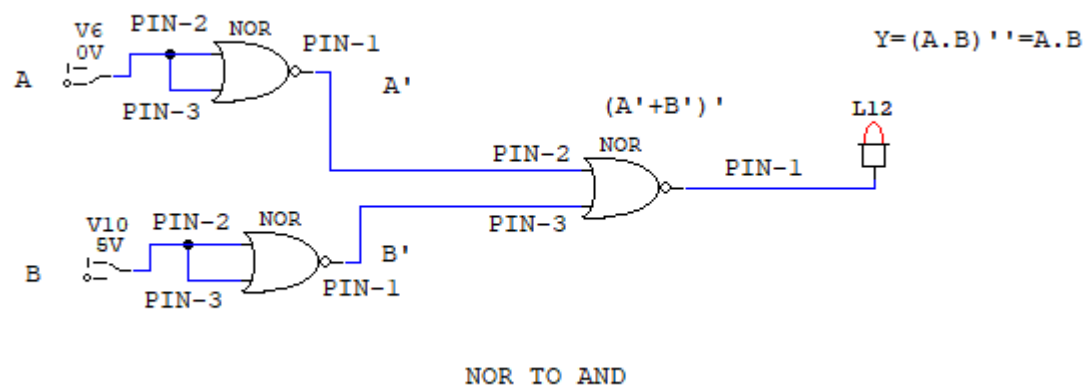
Using NOR Gate:

a) AND

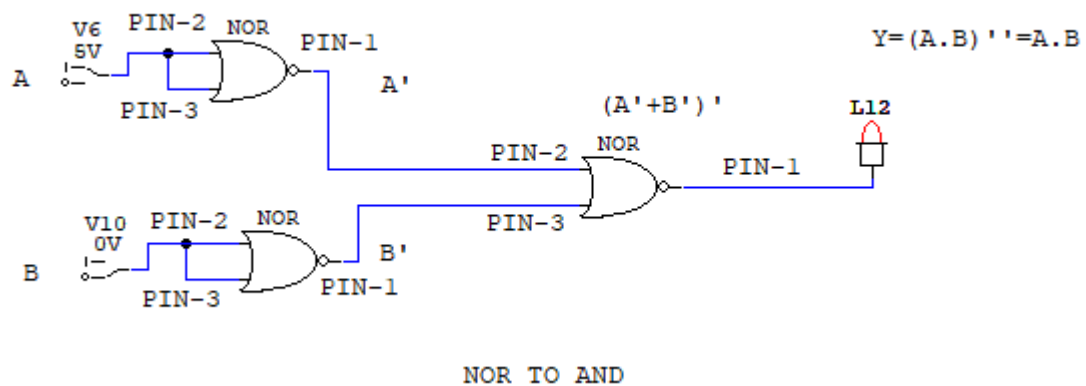
Input A=0, B=0



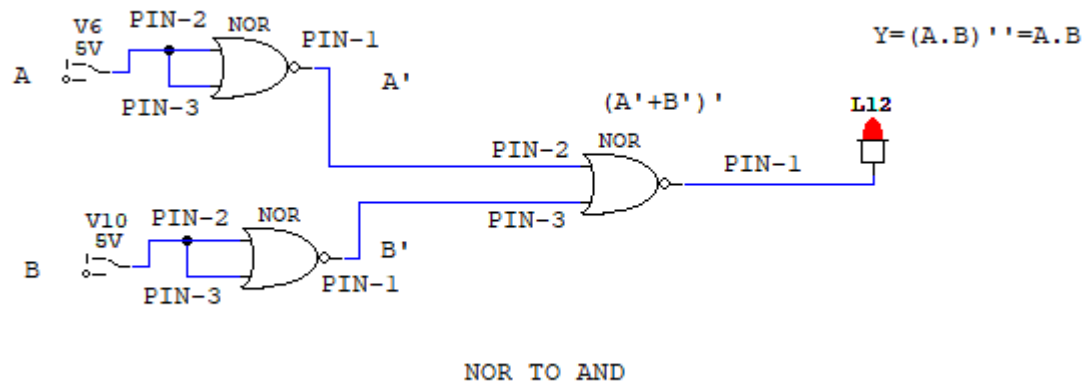
Input A=0, B=1



Input A=1, B=0

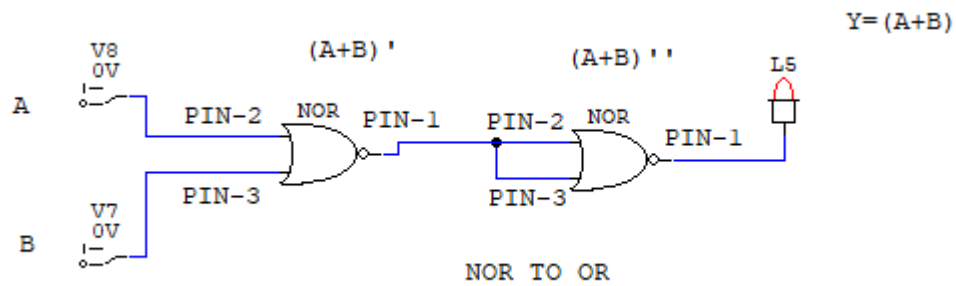


Input A=1, B=1

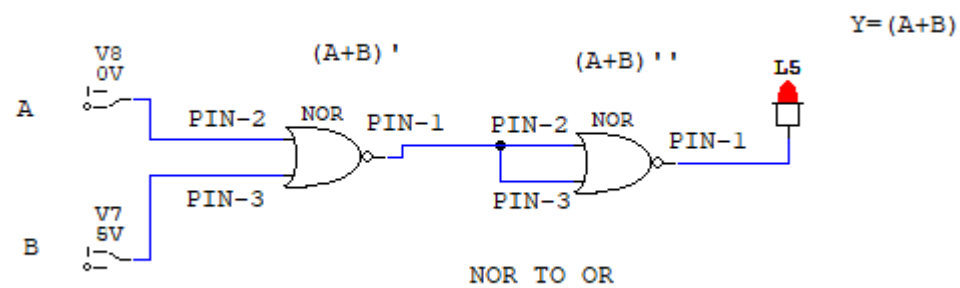


b) OR : $A + B = ((A.A)' . (B.B)')'$

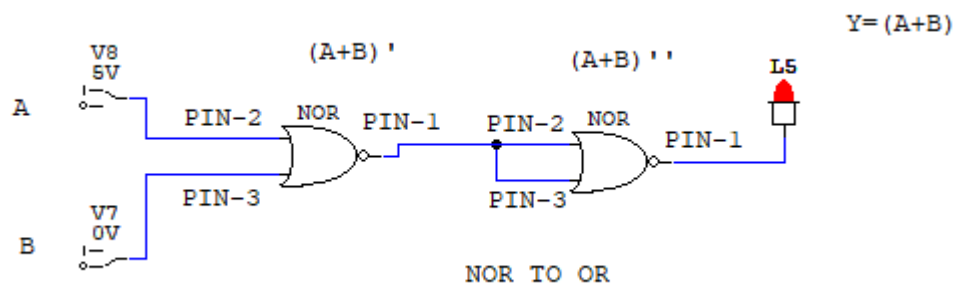
Input A=0, B=0



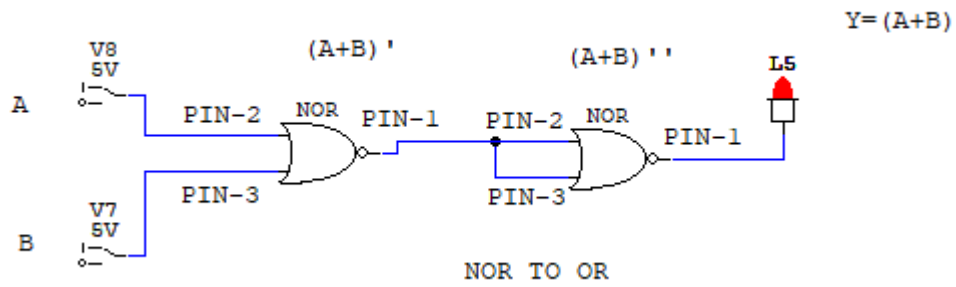
Input A=0, B=1



Input A=1, B=0

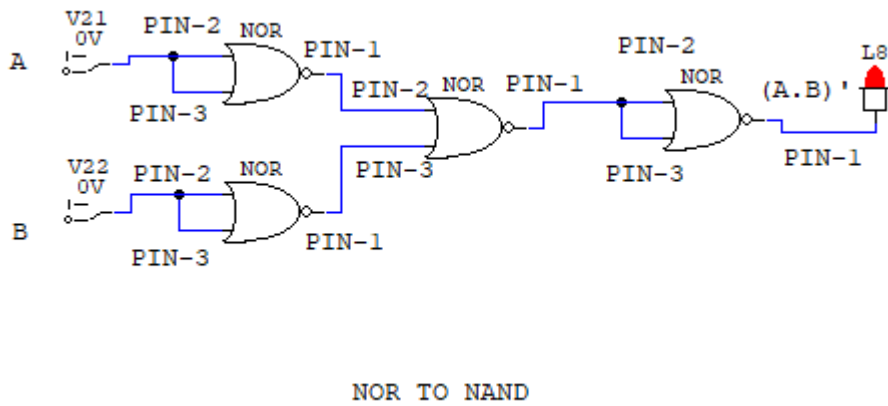


Input A=1, B=1

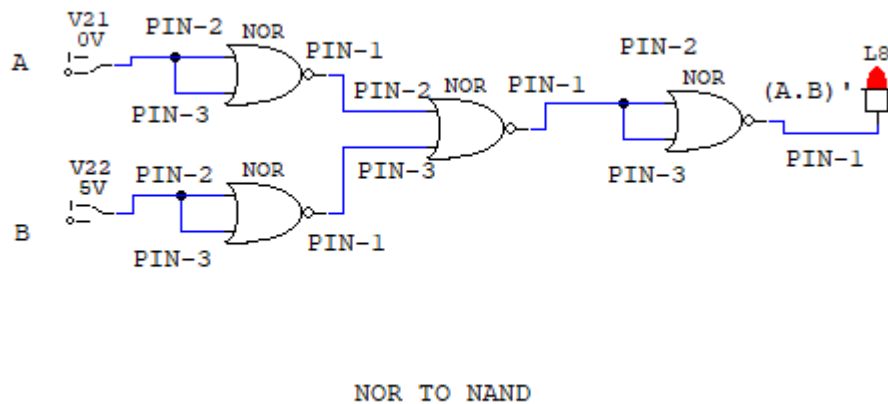


c) NAND

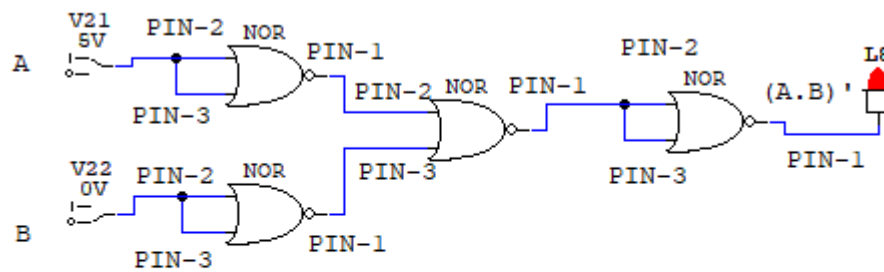
Input A=0, B=0



Input A=0, B=1

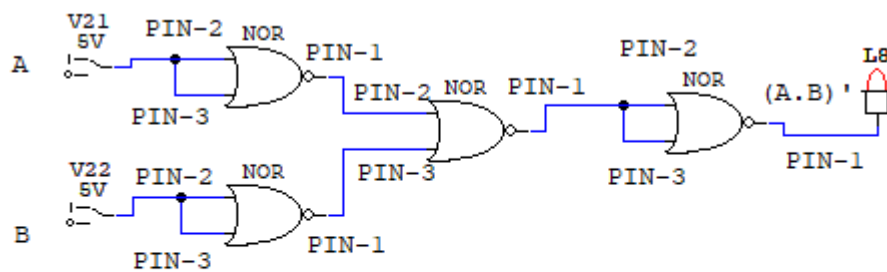


Input A=1, B=0



NOR TO NAND

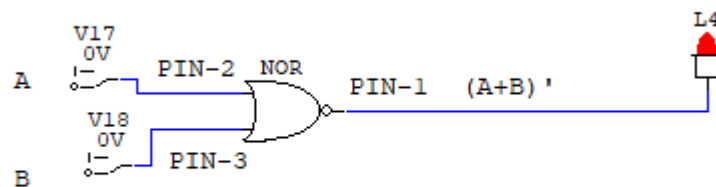
Input A=1, B=1



NOR TO NAND

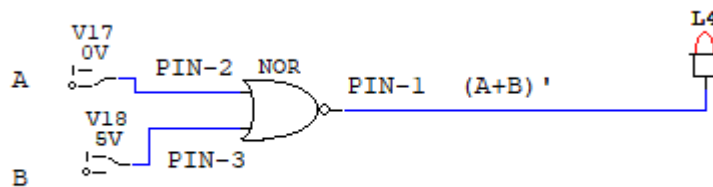
d) NOR

Input A=0, B=0



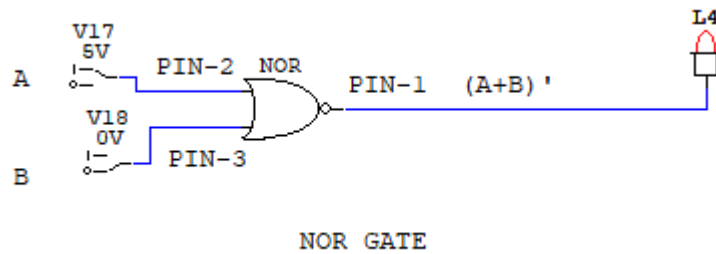
NOR GATE

Input A=0, B=1

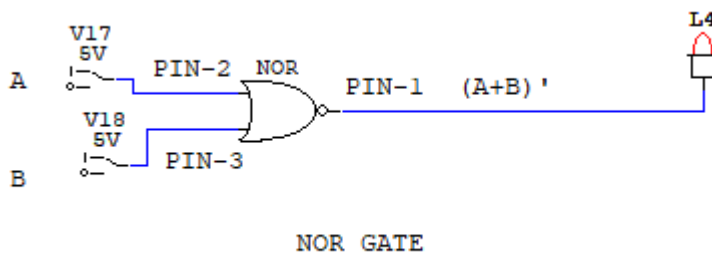


NOR GATE

Input A=1, B=0

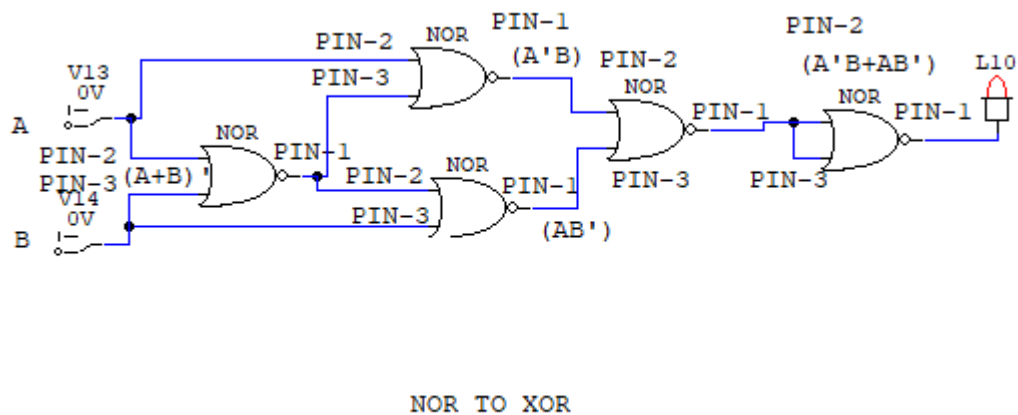


Input A=1, B=1

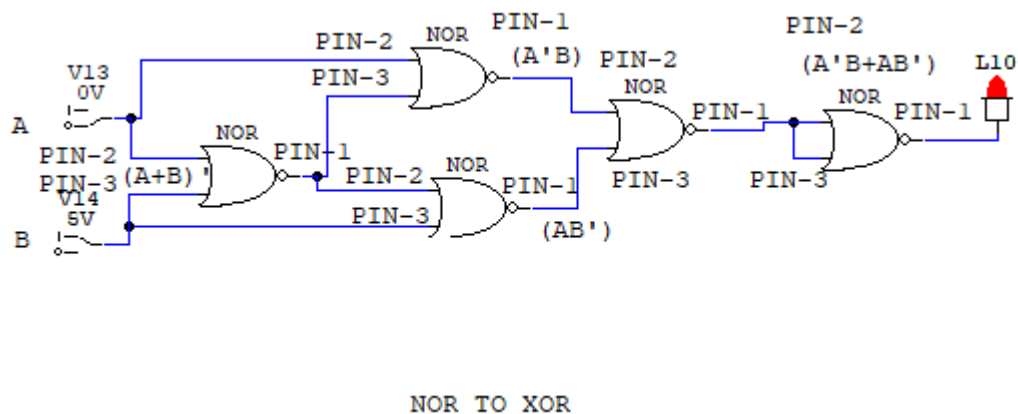


e) XOR

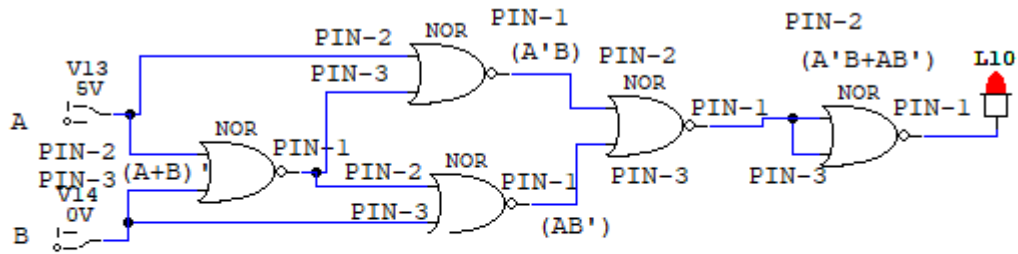
Input A=0, B=0



Input A=0, B=1

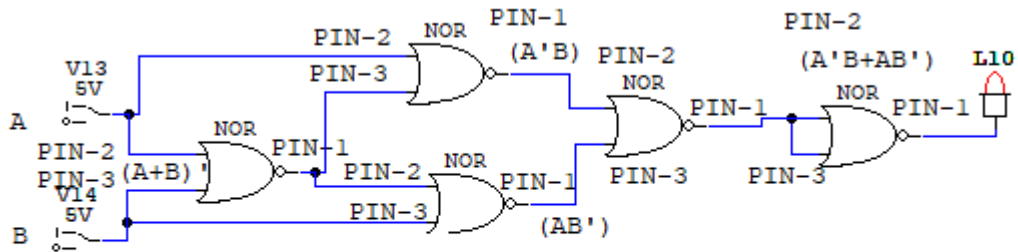


Input A=1, B=0



NOR TO XOR

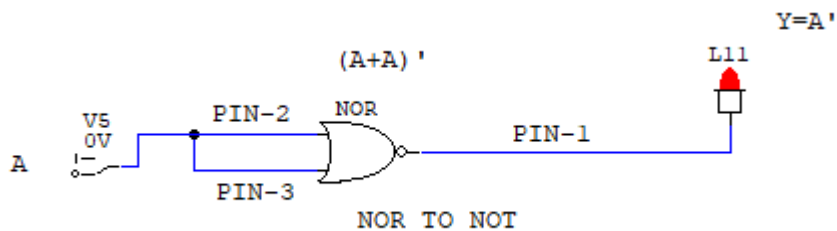
Input A=1, B=1



NOR TO XOR

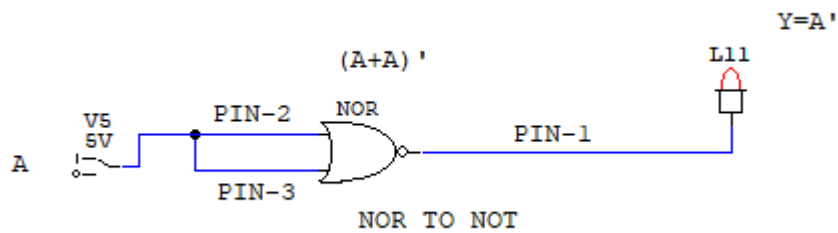
f) NOT : $A' = (A.A)'$

Input A=0



NOR TO NOT

Input A=1



Discussion: In this experiment, we proved and verified the universality of NAND and NOR gate. We have used NAND gate & NOR gate to make circuits of basic gates (AND,OR,NOT) and XOR gate. Security protocols were strictly maintained during the experiment. We have verified our outputs created in trainer board by following truth table outputs.