UNIVERSITY OF ASIA PACIFIC

Department of Computer Science & Engineering

Course Title : Digital Logic & System Design Lab

Course Code : CSE 210

Experiment No. : 02

Experiment Name : **A) Design a logic circuit from a given truth table.**
B) Simplify the given logic expression and verify the truth table.

Date of Performance : 25-01-2022

Date of Submission : 31-01-2022

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A.

Problem Statement : Design a logic circuit from a given truth table.

Inputs			Outputs	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Instruments (Used in This Experiment):

i. IC-7404 (NOT GATE)
ii. IC-7408 (AND GATE)
iii. IC-7432 (OR GATE)
iv. IC-7486 (X-OR GATE)
v. Wires
vi. Circuit board

Simplification of the Equation:

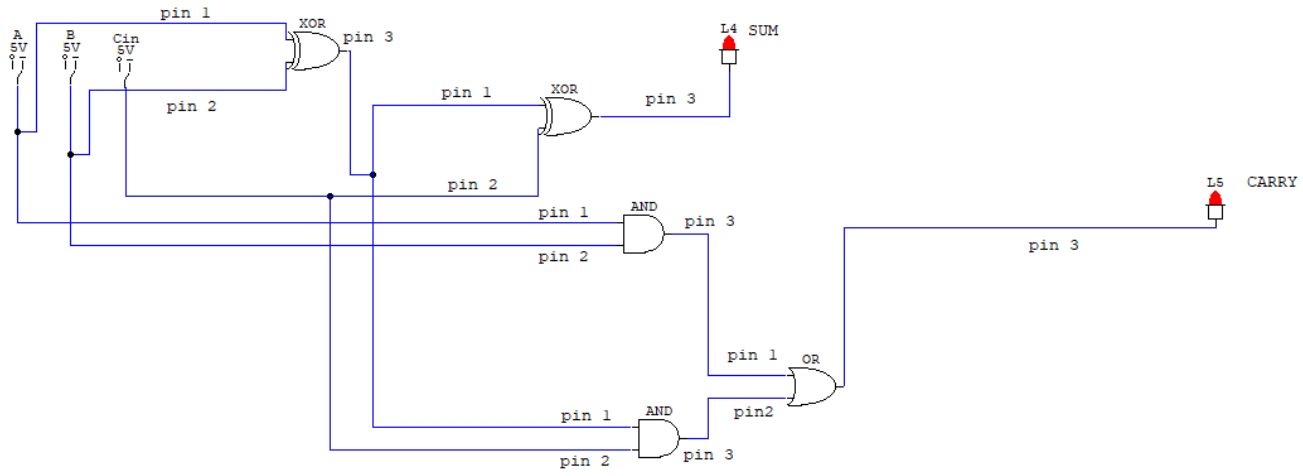
For "Sum": $A'B'C_{in} + AB'C_{in}' + ABC_{in} + A'BC_{in}'$

$= A \oplus B \oplus C_{in}$

For "Carry": $A'BC_{in} + AB'C_{in} + ABC_{in}' + ABC_{in}$

$= C_{in}(A \oplus B) + AB$

Circuit Diagram of the Equation:



Discussion: Here, SUM is HIGH when only one input is HIGH or all the inputs are HIGH. And carry will be HIGH when at least two inputs are HIGH.

B.

Problem Statement: Simplify the given logic expression and verify the truth table.

i. **(A + C) (A D + A D') + A C + C**

ii. **A' B C + A B' C + A B C' + A B C (Using K-map)**

Instruments (Used in This Experiment):

i. IC-7404 (NOT GATE)
ii. IC-7408 (AND GATE)
iii. IC-7432 (OR GATE)
iv. IC-7486 (X-OR GATE)
v. Wires
vi. Circuit board

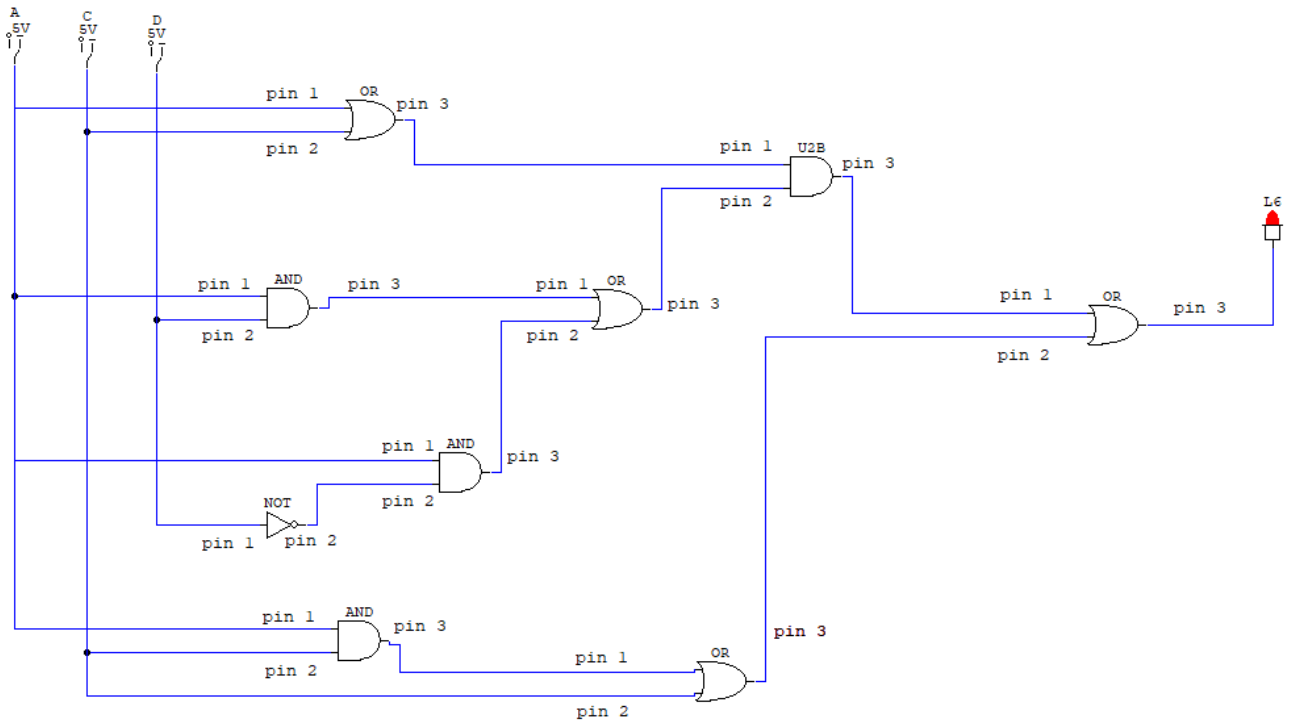
Simplification of the Equation:

i) (A + C) (A D + A D') + A C + C

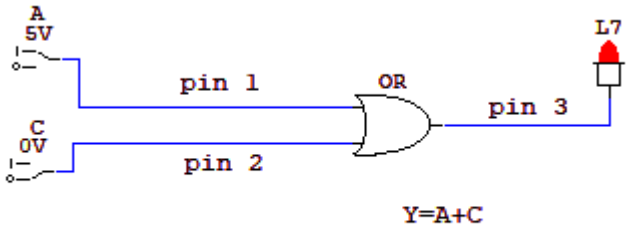
= AD + AD' + ACD + ACD' + AC + C
= A + AC + AC + C
= A + AC + C
= A + C

Circuit Diagram:

Before Simplification:



After Simplification:



Y=A+C

Truth table
Before Simplification:

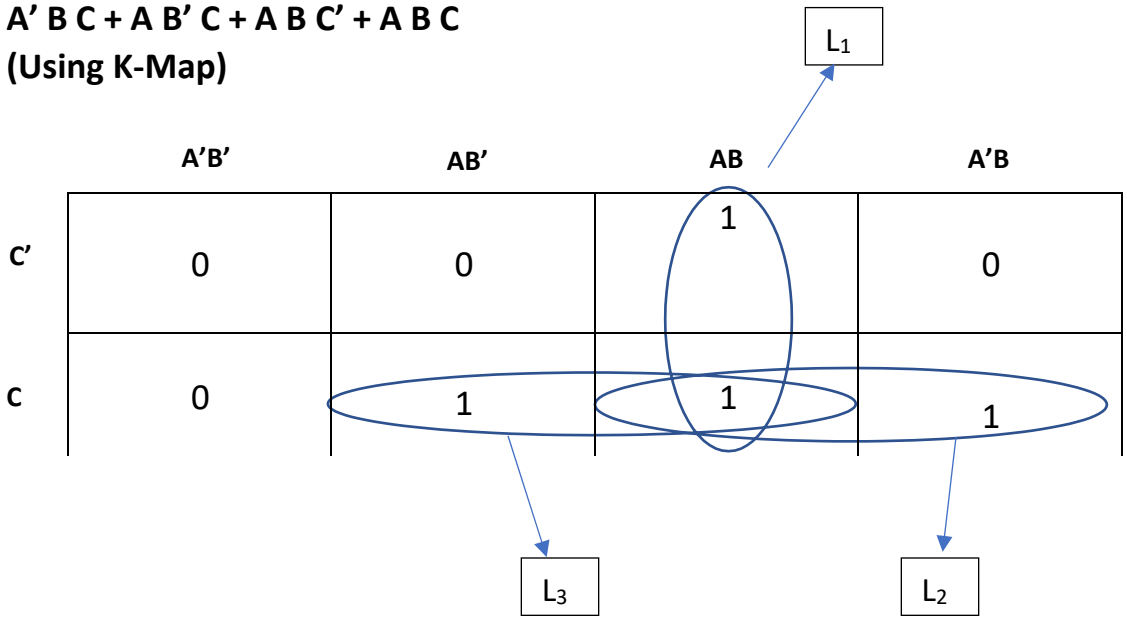
A	C	D	Y = (A + C) (AD + AD') + AC + C
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

After Simplification:

A	**C**	**Y= A+C**
0	0	0
0	1	1
1	0	1
1	1	1

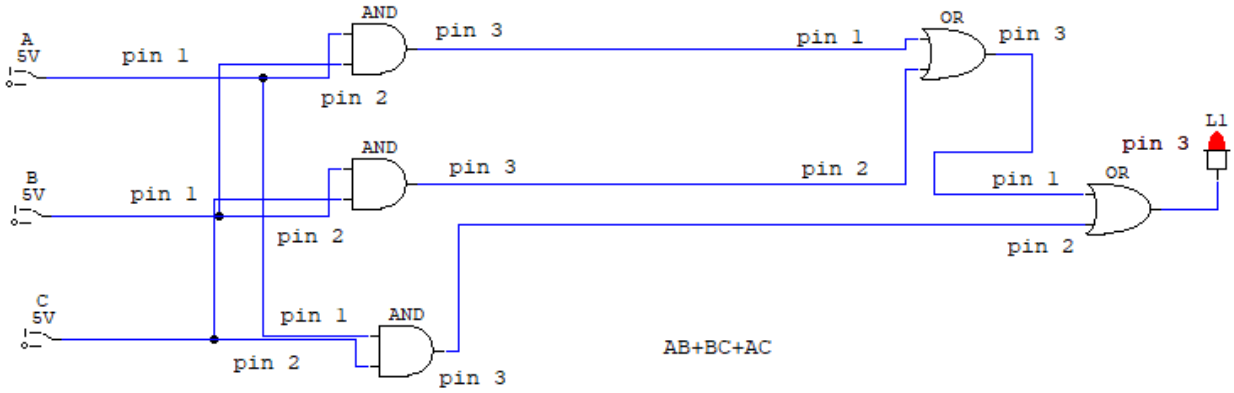
Discussion: In this experiment we need at least 8 gates but after simplification we need only one OR gate. Output will be HIGH when either A or C or both are HIGH.

ii) **A’ B C + A B’ C + A B C’ + A B C**
(Using K-Map)



Analyzing K-map, we got : **AB + BC + AC**

Circuit Diagram (by using K-Map):



Truth table before simplification:

A	B	C	Y=A’BC+AB’C +ABC’+ABC
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Truth table after simplification (by using K-Map):

A	B	C	Y=AB+AC+BC
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Here both tables have same output because equal number of inputs.

Discussion: Here we have simplified the equation using K-map. Both truth tables simplified or not simplified are the same. The output is HIGH when at least two inputs are HIGH.

Additional work for Lab-2:

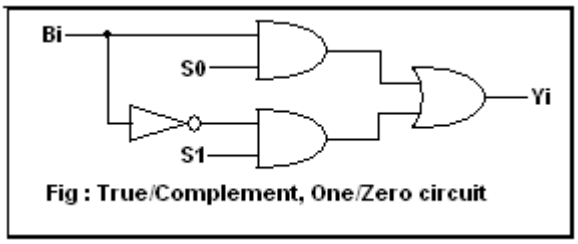


Fig : True/Complement, One/Zero circuit

i) Logical expression for above circuit:

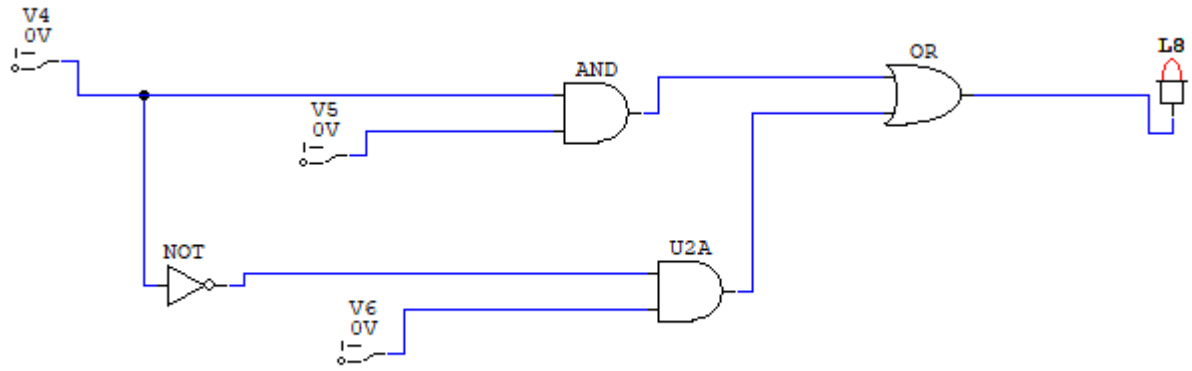
Y = BiS0 + Bi'S1

ii) Truth table:

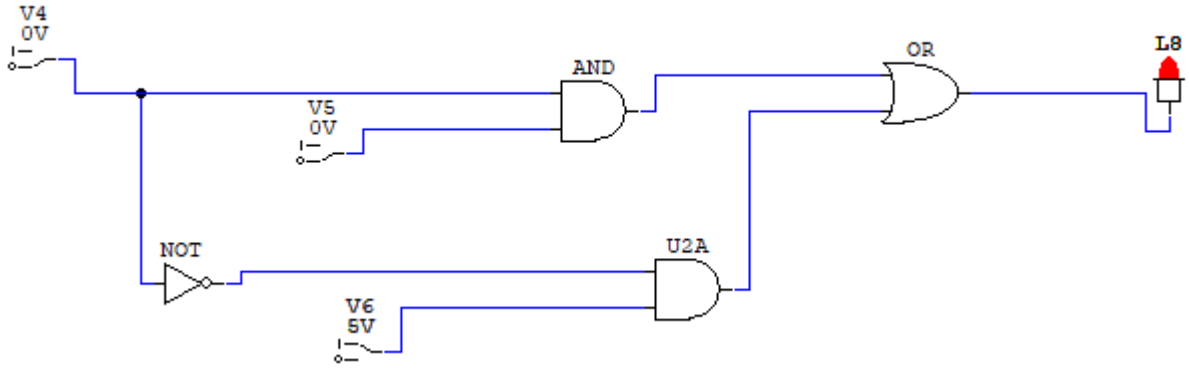
Bi	S0	S1	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Verification of truth table:

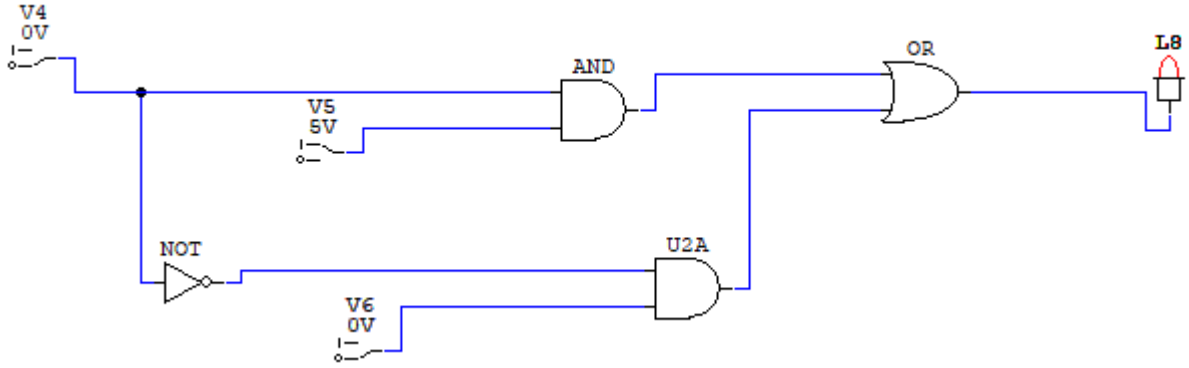
For input 0 0 0



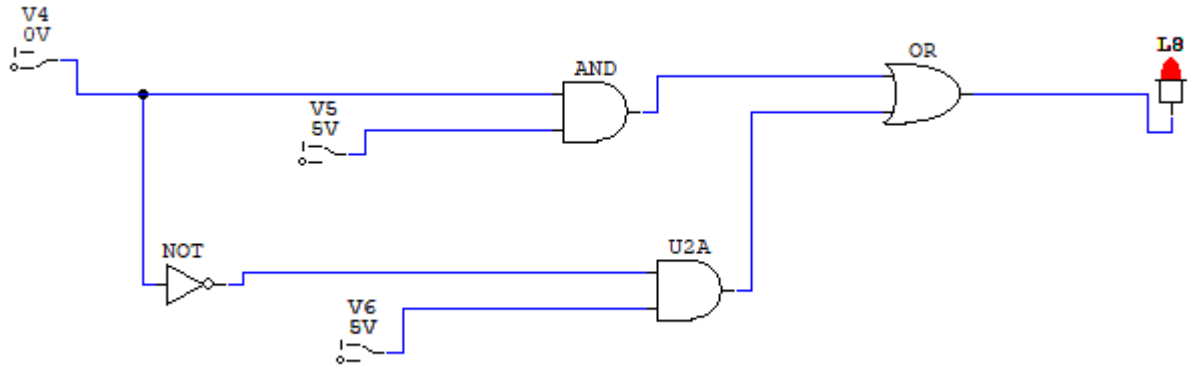
For input 0 0 1



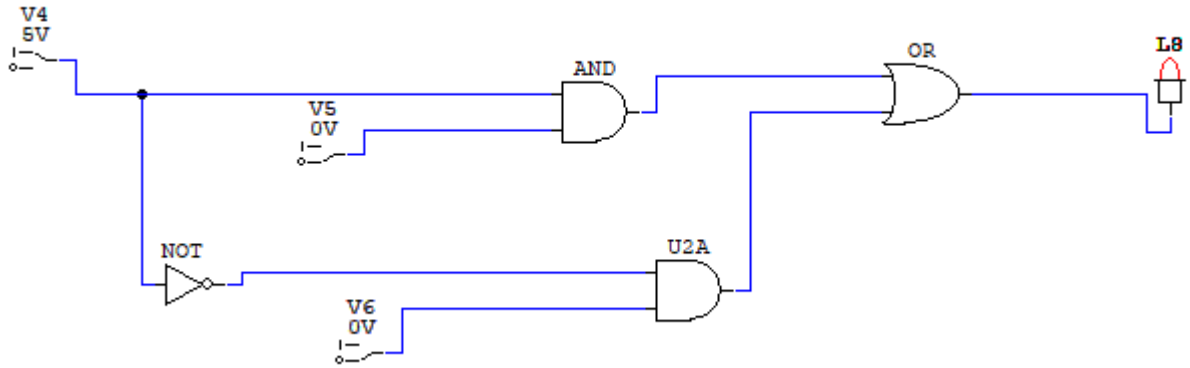
For input 0 1 0



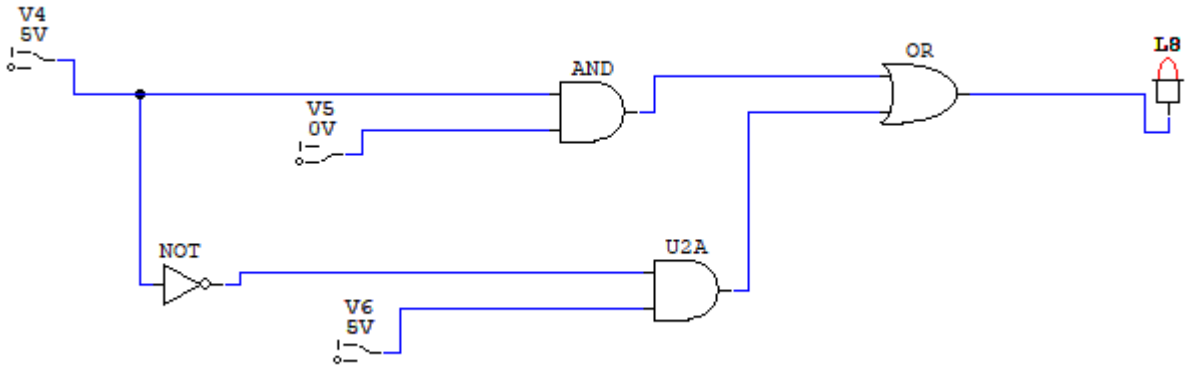
For input 0 1 1



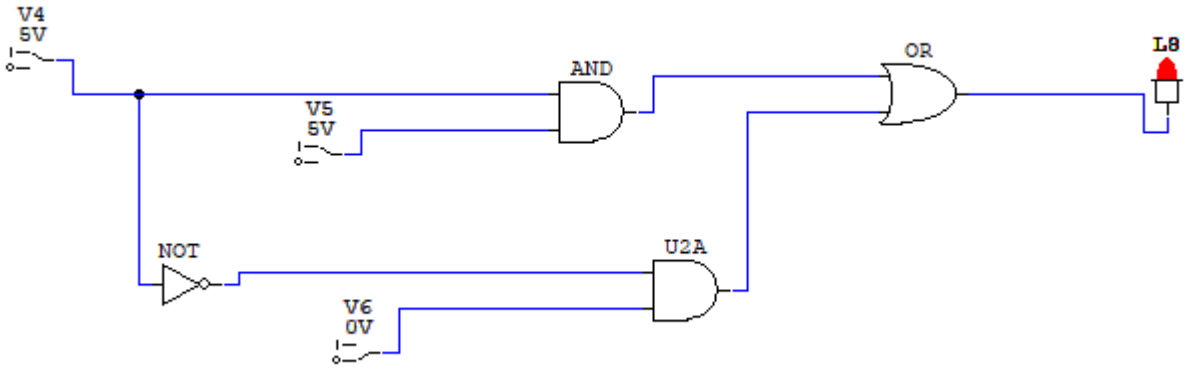
For input 1 0 0



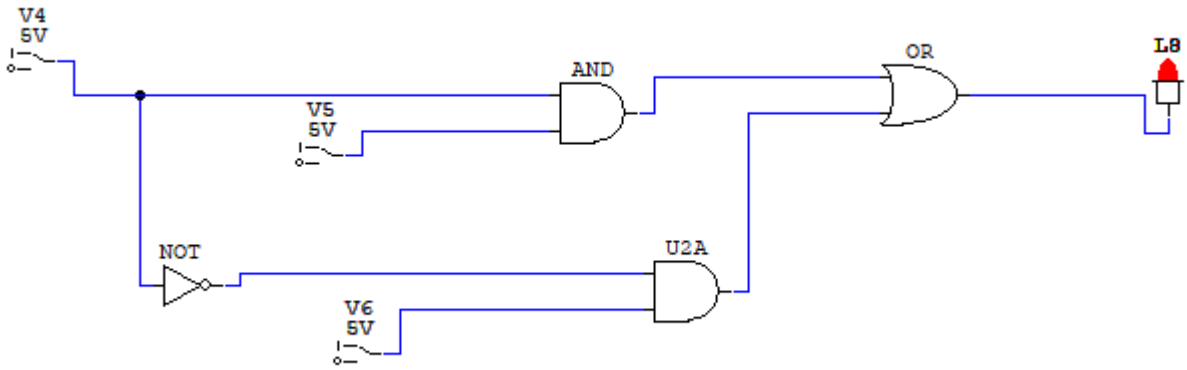
For input 1 0 1



For input 1 1 0



For input 1 1 1



Discussion: In this experiment, we simplified different equations in different ways. But in all cases, we saw that we need few logic gates to get the outputs. We found equation by simplifying the main equation using Boolean algebra or K-map. We drew the truth table and notified that circuit diagram has been matched.