UNIVERSITY OF ASIA PACIFIC

Department of Computer Science & Engineering

Course Title : Digital Logic & System Design Lab

Course Code : CSE 210

Experiment No. : 05

Experiment Name : **Implement and verify SR Latch with NAND and NOR gate.**

Date of Performance : 15-02-2022

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Submitted by:

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Problem Statement: Implement and verify SR Latch with NAND and NOR gate.

Instruments (Used in This Experiment):

i. IC-7400 (NAND GATE)
ii. IC-7402 (NOR GATE)
iii. Wires
iv. Trainer board

Truth Table:

SR Latch with NAND gate:

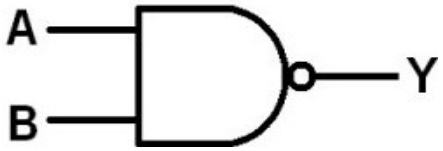
Input		Output	State
S	**R**		
0	0	Q=Q'=1	Invalid
0	1	1	Set
1	0	0	Reset
1	1	Q_0	No Change

SR Latch with NOR gate:

Input		Output	State
S	**R**		
0	0	Q_0	No Change
0	1	0	Reset
1	0	1	Set
1	1	Q=Q'=0	Invalid

Logic Diagram:

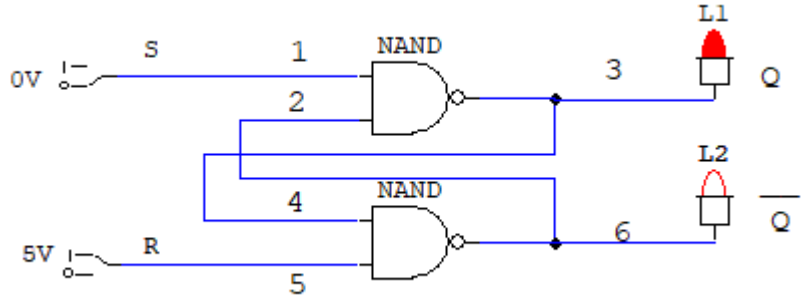
NAND Gate:



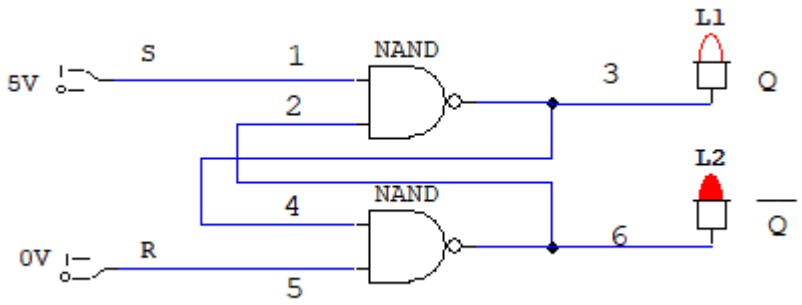
NOR Gate:

Circuit diagram of SR Latch with NAND gate:

When S=0, R=1 (SET)

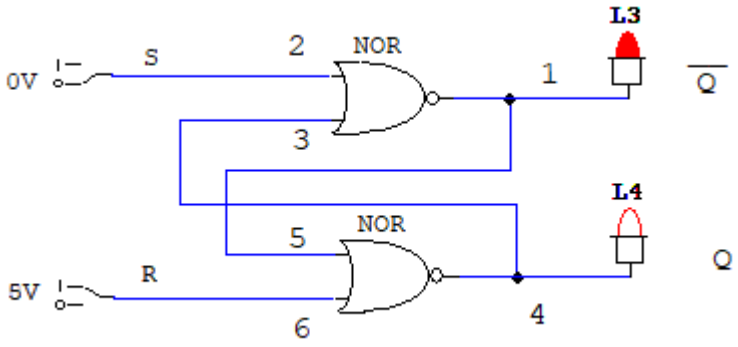


When S=1, R=0 (RESET)

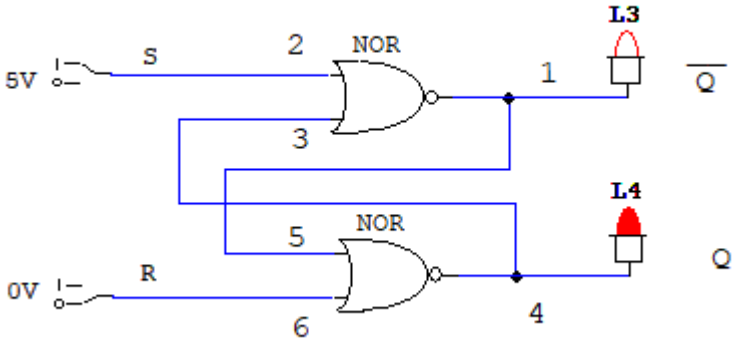


Circuit diagram of SR Latch with NOR gate:

When S=0, R=1 (RESET)



When S=1, R=0 (SET)



Discussion: In this experiment, we implemented and verified SR Latch with NAND and NOR gate. Security protocols were strictly maintained during the experiment. We verified our circuits by uses of truth table.