UNIVERSITY OF ASIA PACIFIC

Department of Computer Science & Engineering

Course Title : Digital Logic & System Design Lab

Course Code : CSE 210

Experiment No. : 04

Experiment Name :

a) Design 1 bit Half Adder and Full Adder

b) Test and verify the 4-bit parallel Adder(IC # 7483)

c) Design Subtractor using IC # 7483

d) Adder + Subtractor

e) Design a 4 bit adder-subtractor with full adders.

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Submitted by:

Name : Sheikh Nafez Sadnan

Reg. No. : 20101106

Roll No. : 106

Section : B (2)

Submitted To:

Shammi Akhtar

Assistant Professor

Department of CSE

University of Asia Pacific

Problem Statement:

a) **Design 1 bit Half Adder and Full Adder**

b) **Test and verify the 4-bit parallel Adder(IC # 7483)**

c) **Design Subtractor using IC # 7483**

d) **Adder + Subtractor**

e) **Design a 4 bit adder-subtractor with full adders.**

Instruments (Used in This Experiment):

i. XOR GATE (IC-7486)
ii. AND GATE (IC-7408)
iii. OR GATE (IC-7432)
iv. NOT GATE (IC-7404)
v. IC-7483
vi. Logic Switch
vii. Logic Display

a) Design 1 bit Half Adder and Full Adder

HALF ADDER :

Truth Table:

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

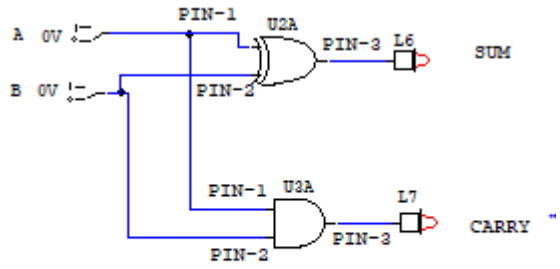
Logic Expression:

Sum= A'B+ AB' = A $\oplus$ B

Carry = AB

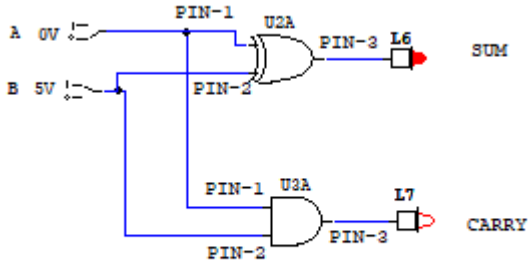
Circuit Diagram:

For A=0, B=0



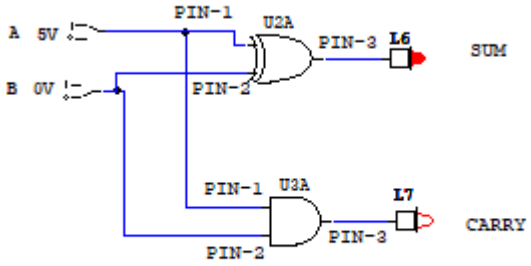
HALF ADDER

For A=0, B=1



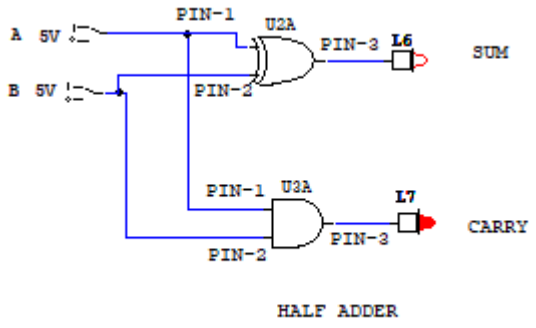
HALF ADDER

For A=1, B=0



HALF ADDER

For A=1, B=1



HALF ADDER

FULL ADDER :

Truth Table:

A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

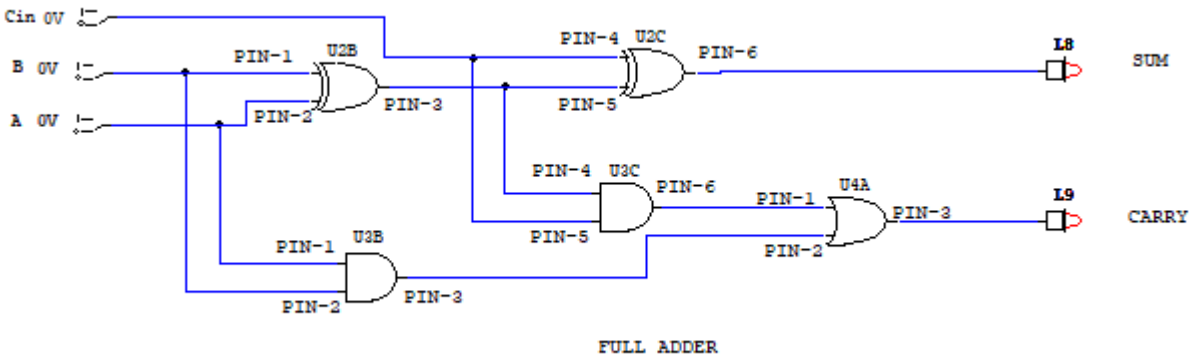
Logic Expression:

Sum = A' B' Cin + A' B Cin' +A B' Cin'+ A B Cin
= A' B Cin' + A B' Cin' + A B Cin + A' B' Cin
=Cin' (A' B + A B') + Cin (A⊕B)'
= Cin' X +Cin X' [Let A⊕B = X]
= Cin ⊕ X
= Cin ⊕ A ⊕ B
= A ⊕ B ⊕ Cin

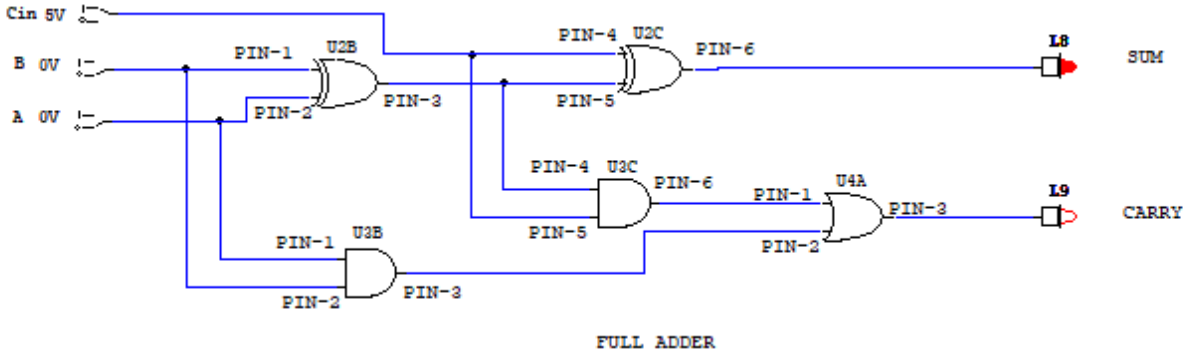
Cout = A' B Cin + A B' Cin + AB Cin' + A B Cin
=Cin (A' B + A B') + AB (Cin' + Cin)
= Cin (A⊕B) + AB. 1
= Cin (A⊕B) + AB

Circuit Diagram:

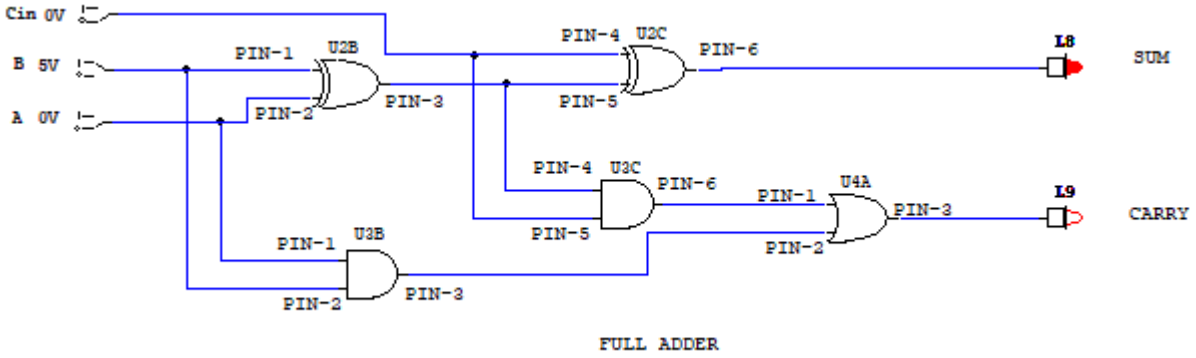
For A=0, B=0, Cin=0



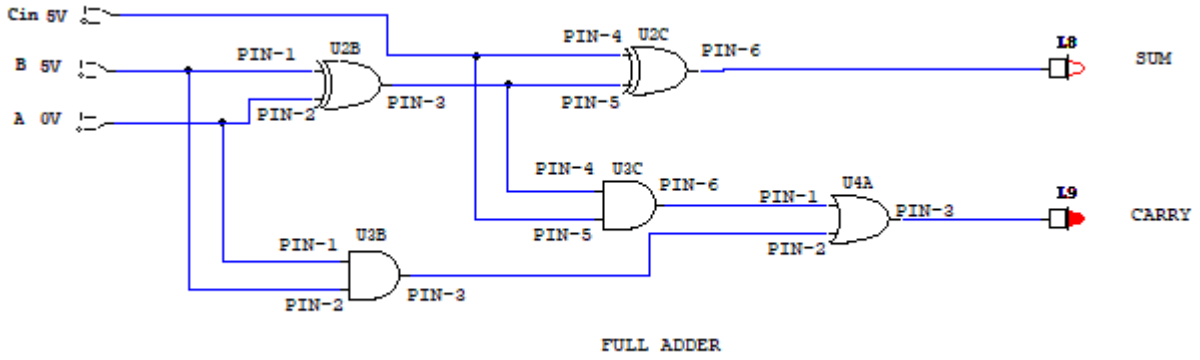
For A=0, B=0, Cin=1



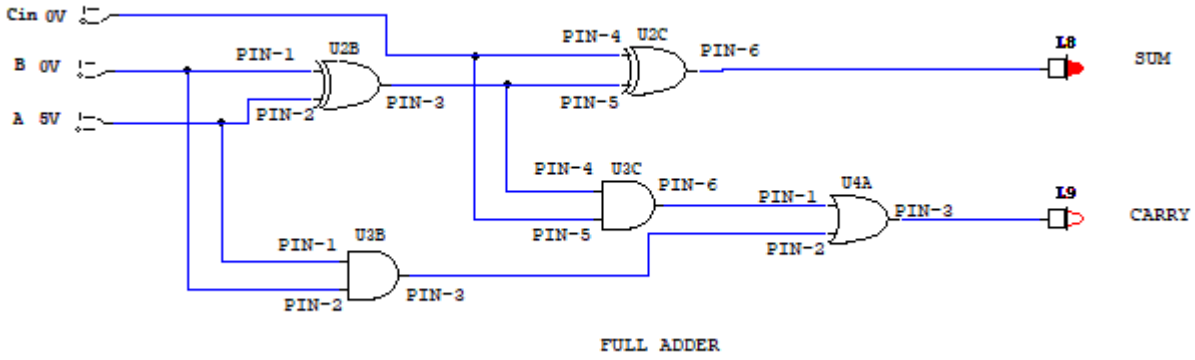
For A=0, B=1, Cin=0



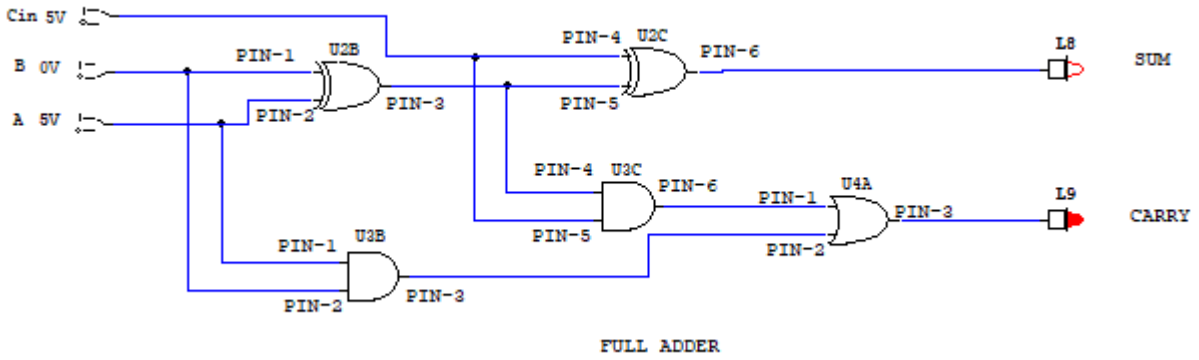
For A=0, B=1, Cin=1



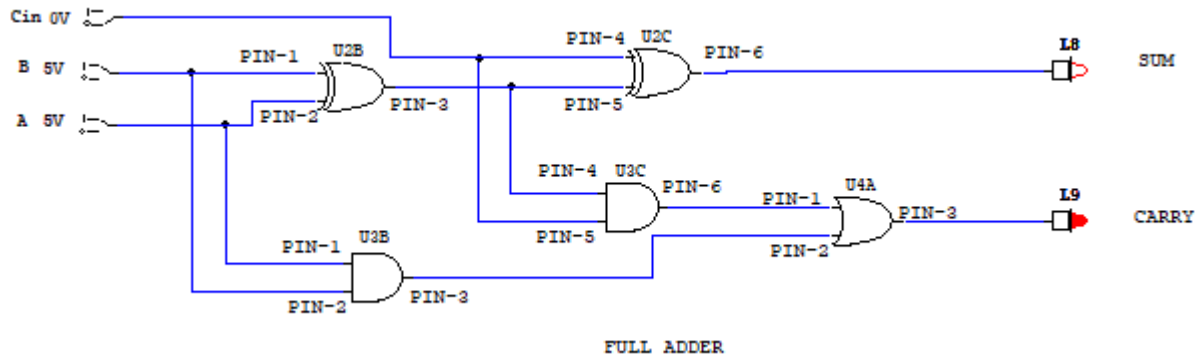
For A=1, B=0, Cin=0



For A=1, B=0, Cin=1

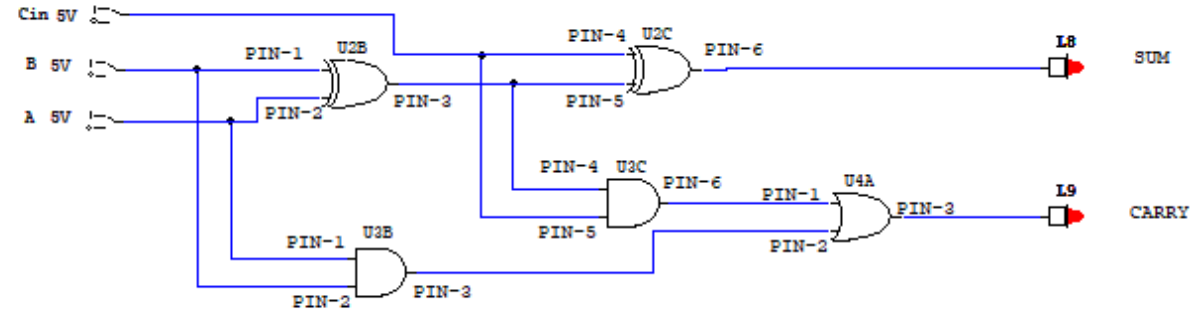


For A=1, B=1, Cin=0



FULL ADDER

For A=1, B=1, Cin=1



FULL ADDER

b) Test and verify the 4-bit parallel Adder(IC # 7483)

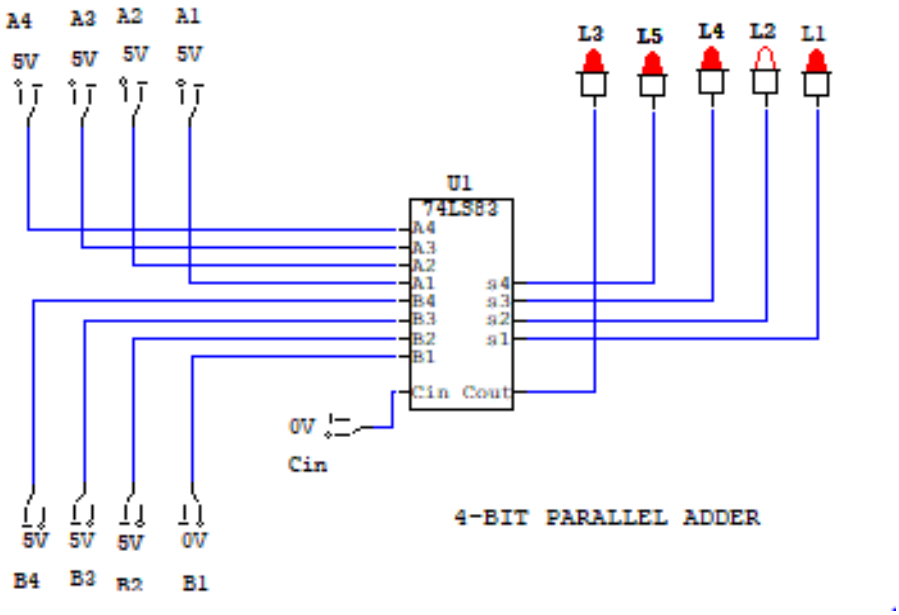
Adder Calculation:

A = 15 = 1111 (A4 A3 A2 A1)
B = 14 = 1110 (B4 B3 B2 B1)

Sum = 29= 11101 (Cout S4 S3 S2 S1)

Circuit Diagram:

A = 15 = 1111
B = 14 = 1110
Sum = 29 = 11101



c) Design Subtractor using IC # 7483

Subtractor Calculation:

A = 15 = 1111 (A4 A3 A2 A1)
B = 14 = 1110 (B4 B3 B2 B1)
So, -B = -14 = 0010 (B4 B3 B2 B1)
In Subtraction we use negative value's 2's compliment. Here we add +15 that's mean 1111 and -14 that's mean 0010.
So,

A = 15 = 1111 (A4 A3 A2 A1)
-B = -14 = 0010 (B4 B3 B2 B1)

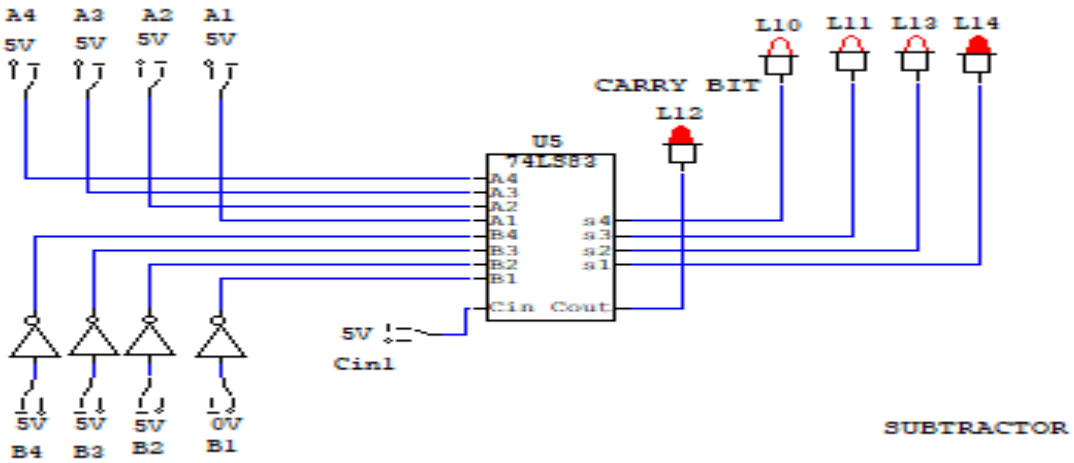
Subtraction = 1 = 10001 (Cout S4 S3 S2 S1)

But when we input value in Subtractor we put A= 1111 and B = 1110.

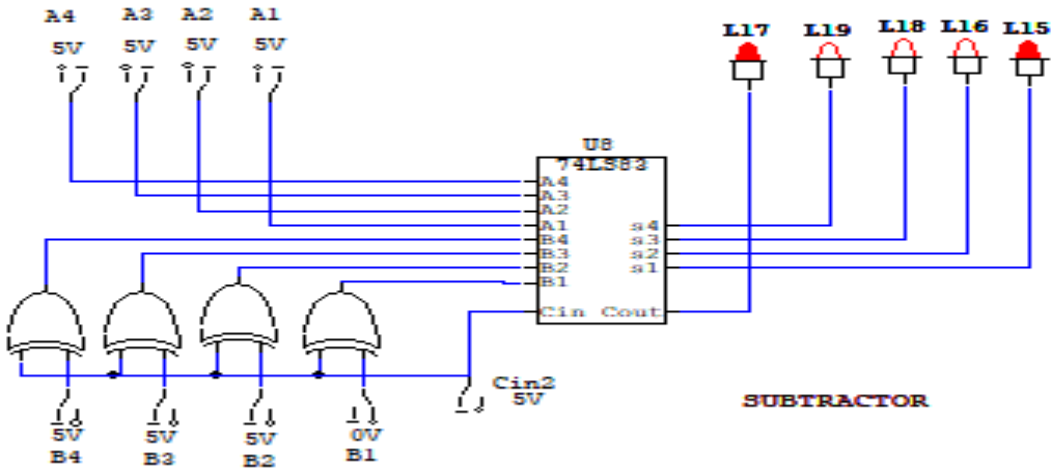
Circuit Diagram:

Here consider that,
A = 15 = 1111
B = 14 = 1110
Subtraction = 1 = 10001

(using NOT gate)



(using XOR gate)



d) Adder + Subtractor

Calculation :

For Adder,

A = 15 = 1111

B = 14 = 1110

Sum = 29 = 11101

For Subtractor,

A = 15 = 1111

B = 14 = 1110

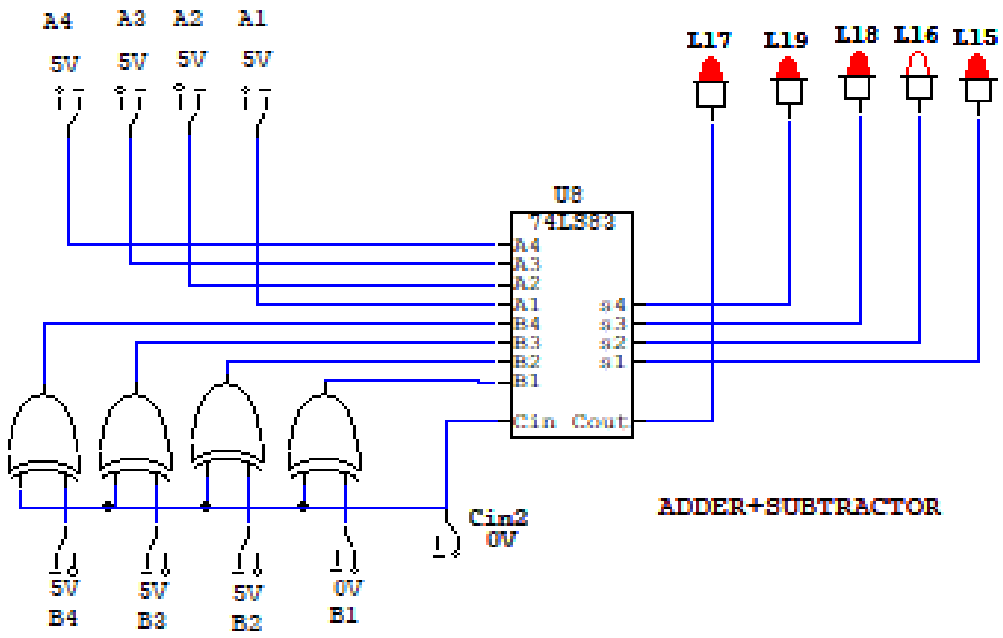
= 0001 [1's complement of B]

+1

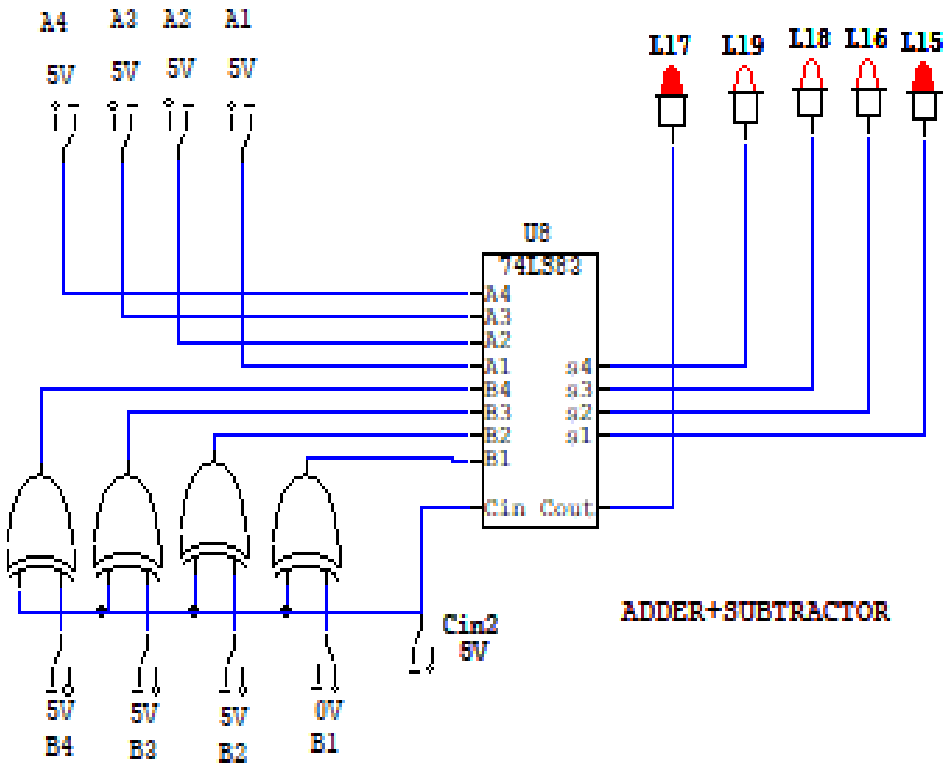
= 0010 [2's complement of B]

So, Subtraction = 10001

Circuit Diagram: (FOR ADDER)



(FOR SUBTRACTOR)



e) Design a 4 bit adder-subtractor with full adders

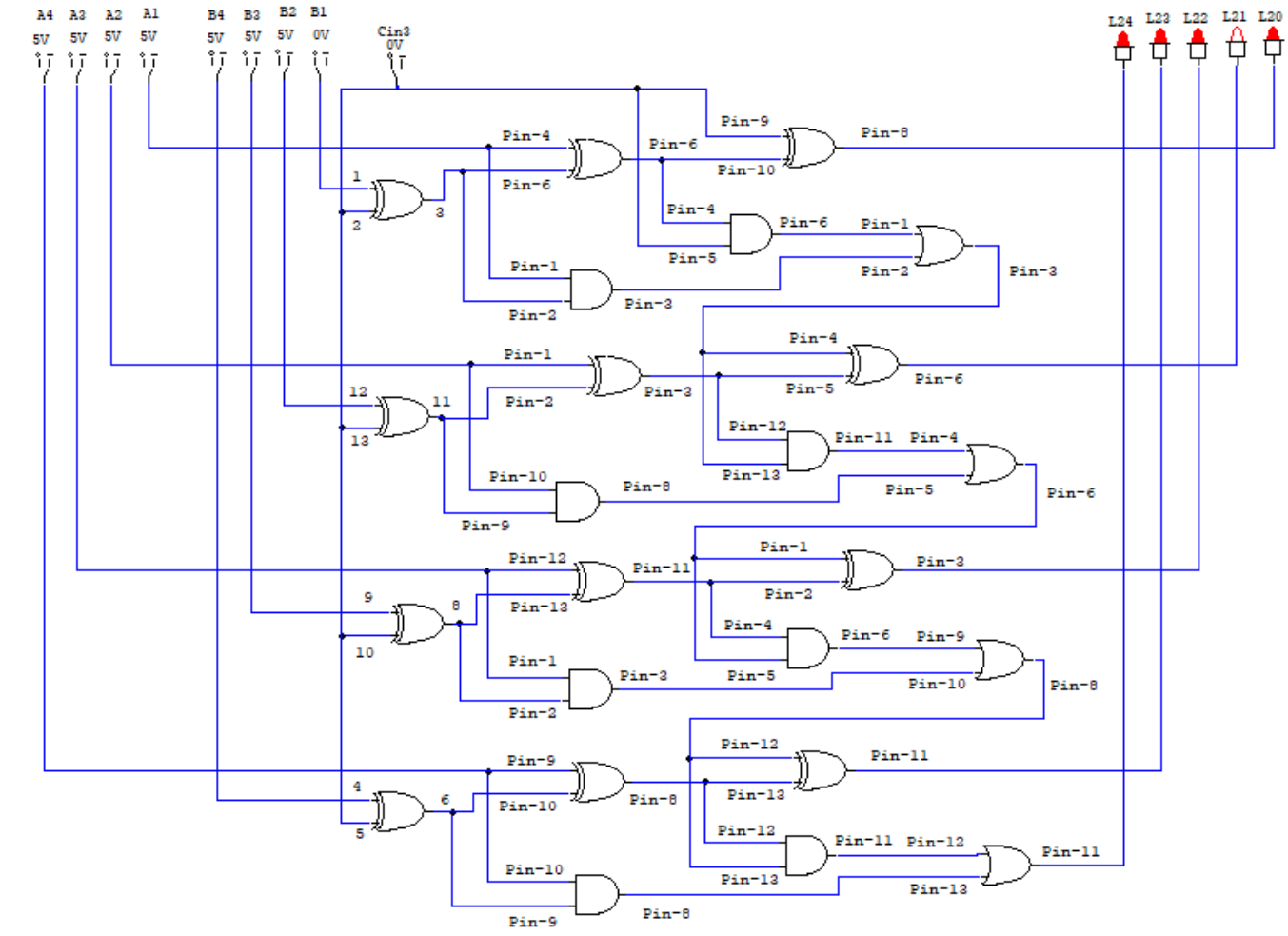
FOR ADDITION OPERATION:

A = 15 = 1111 (A4 A3 A2 A1)

B = 14 = 1110 (B4 B3 B2 B1)

Sum = 29 = 11101 (Cout S4 S3 S2 S1)

Circuit Diagram:



4 – bit example of Adder and Subtractor:

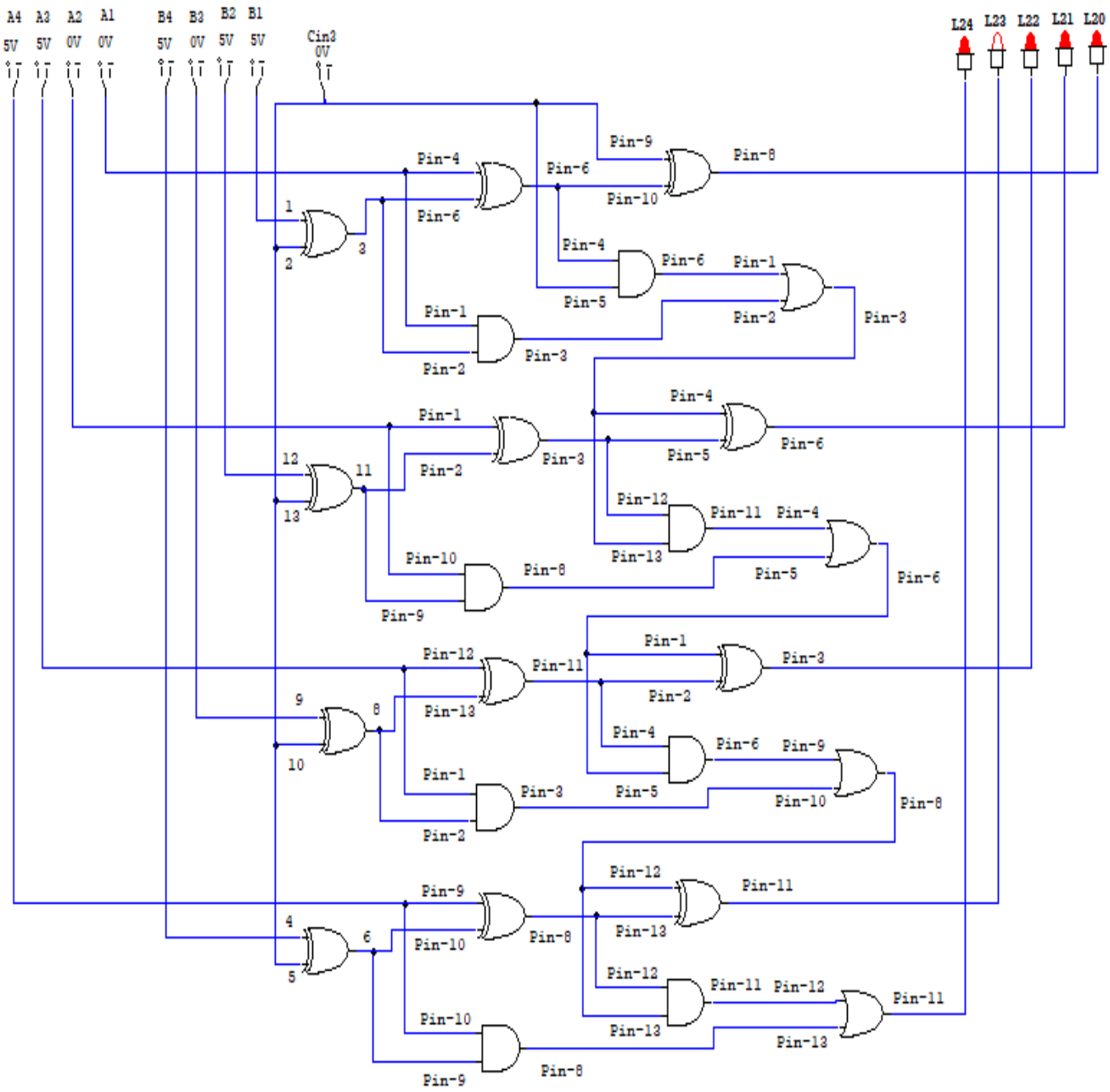
For addition operation:

A = 12 = 1100 (A4 A3 A2 A1)

B = 11 = 1011 (B4 B3 B2 B1)

Sum = 23 = 10111 (Cout S4 S3 S2 S1)

Circuit Diagram:

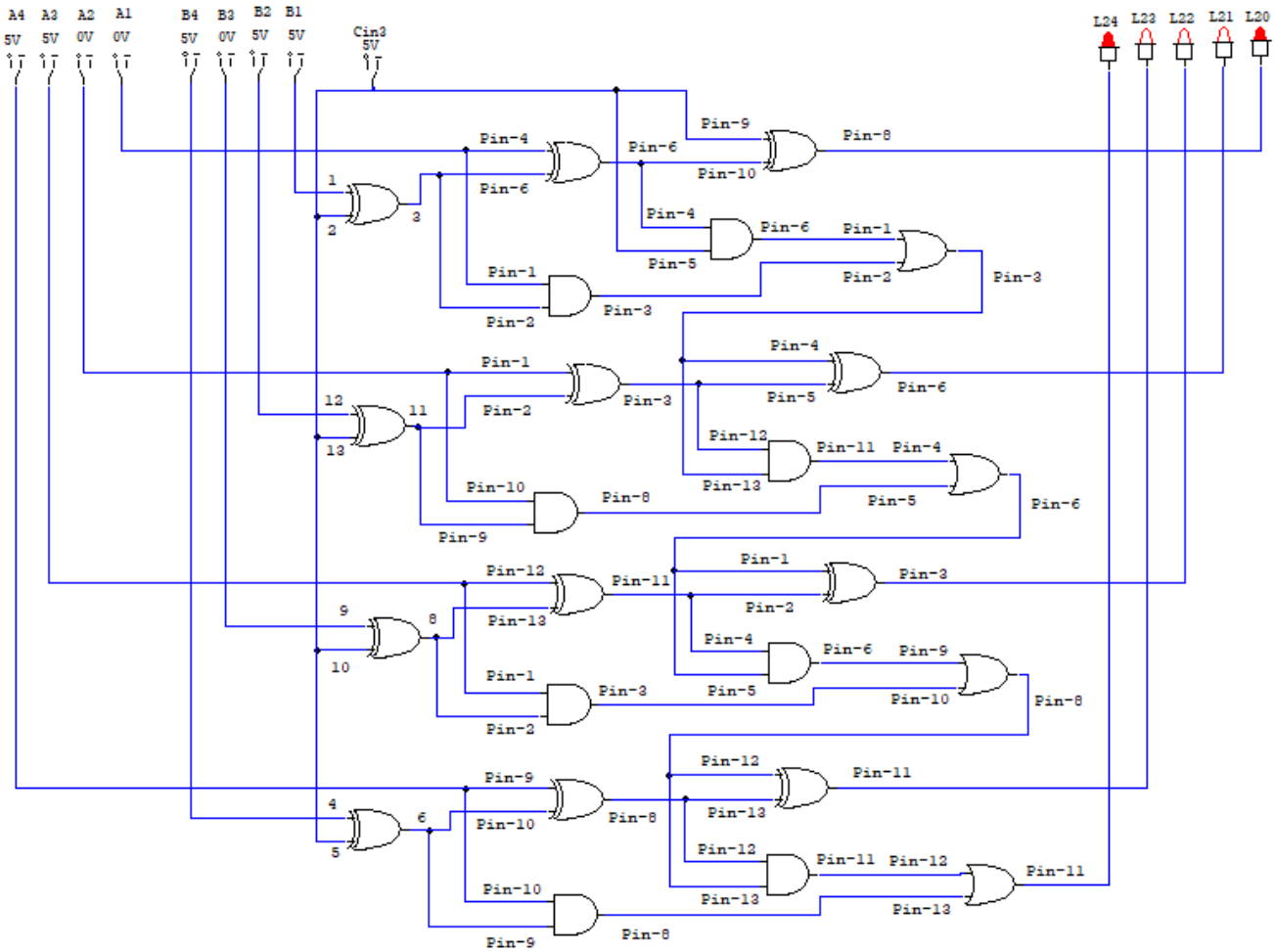


For subtraction operation:

A = 12 = 1100
B = 11 = 1011
= 0100 [1's complement of B]
+1
= 0101 [2's complement of B]

So, Subtraction = 10001

Circuit Diagram:



Discussion : In this experiment we learned about half adder & full adder. We also discussed about 4 bit parallel adder. We have verified 4-bit parallel adder using IC#7483. We also designed subtractor using IC#7483 and verified it. We designed adder+subtractor and a 4-bit example of adder and subtractor using full adder. Security issues were strictly maintained during the experiment.