

MICROPROCESSORS AND DESIGN

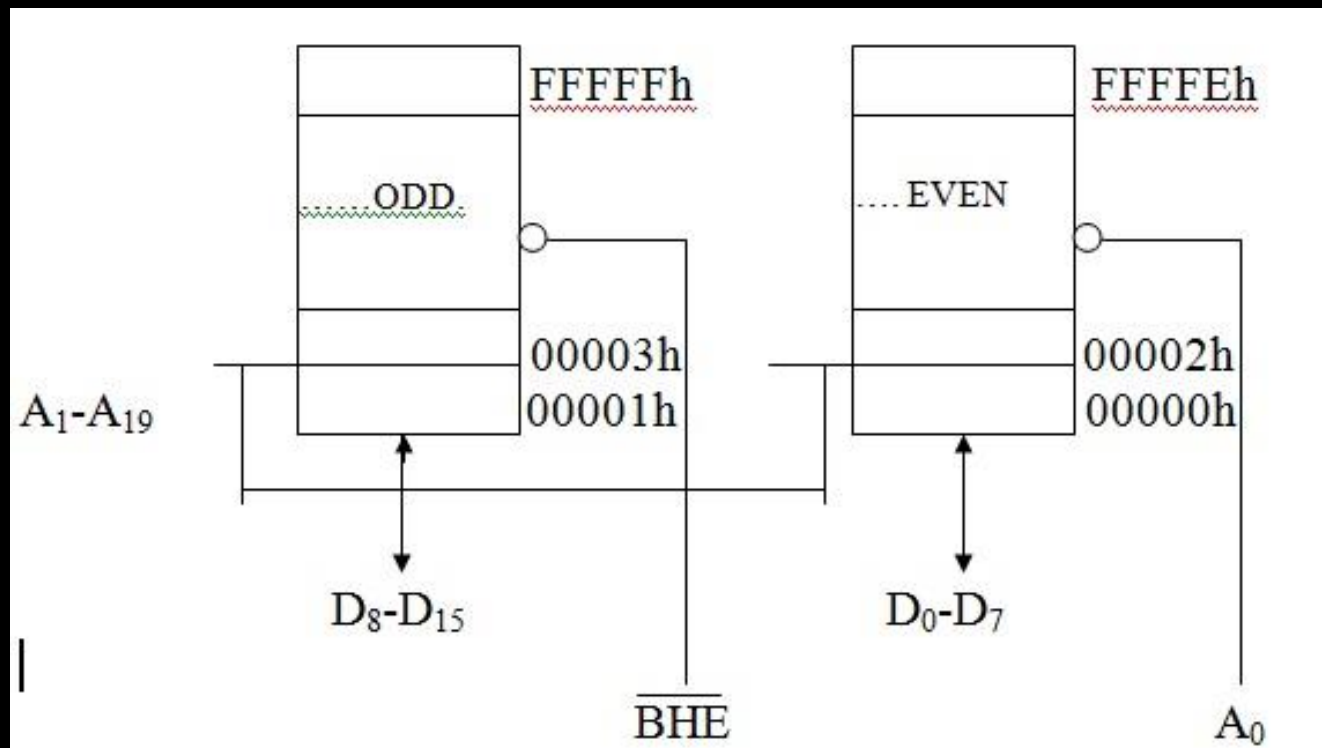
CSE 311

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8086 MEMORY BANK CONCEPT

8086 memory is organized as an array of one million bytes i.e. 1MB. The total memory is organized in two separate banks of locations. One is even and the other is odd. Each bank of size 512KB. Therefore the address space is physically implemented on 16-bit data bus.

MEMORY BANK DIAGRAM (ODD AND EVEN SPACES)



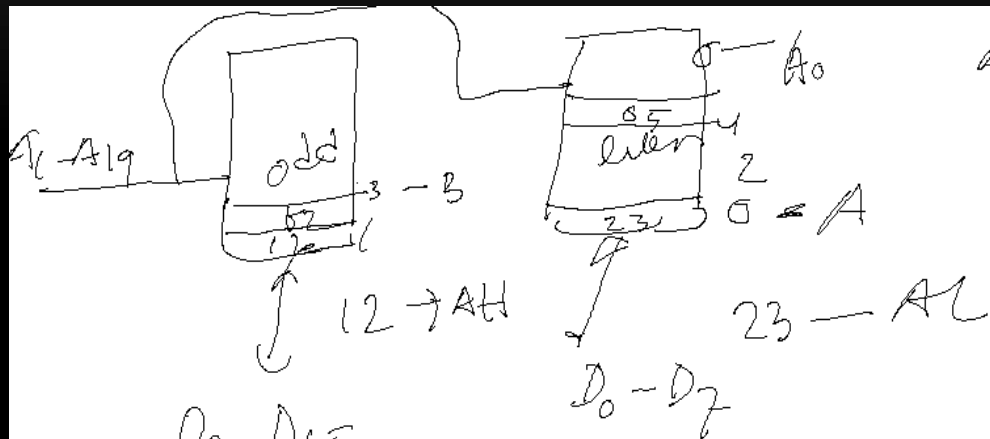
ANALYSIS

Even bank contains even address spaces ($A_0=0$) and connected to D_0 - D_7 data bus and the odd bank contains odd address spaces ($A_0=1$) and connected to D_8 - D_{15} data bus. A particular byte is addressed by A_1 - A_{19} address bus with A_0 as selector for even bank. BHE is the selector for odd address space.

FUNCTION TABLE

<u>BHE</u>	A_0	Byte Transferred
0	0	Both bytes using D0-D15
0	1	Byte from odd bank D8-D15
1	0	Byte from even bank D0-D7
1	1	No operation

EXPLANATION



D8-D15

higher byte

lower byte
DB

2nd Bus DB

1st bus D0-D7 - loc 2

D0-D7 - loc 4 - BH D8-D15 - loc 3 - BL

D8-D15 - loc 5 discard

A → 00000H

MOV AX, A

one bus cycle read

MOV BX, B

B = 00003H

BL = 00003H

BH = 00004H

WARM-UP QUESTION

8086 requires one bus cycle to fetch 16-bit data if it starts to read from even space.

8086 requires two bus cycles to fetch odd addressed 16-bit data-
Why?