University of Asia Pacific (UAP)

Department of Computer Science and Engineering (CSE)

Course Outline

Program:	Computer Science and Engineering (CSE)
Course Title:	Microprocessors & Assembly Language
Course Code:	CSE 311
Semester:	Spring-2022
Level:	3-1 (5th Semester), Section: A, B
Credit Hour:	3.0
Name & Designation of Teacher:	Shaila Rahman Assistant Professor
Office/Room:	7th Floor, teacher's compound
Class Hours:	**Tuesday 2:00PM-3:20PM (Sec B)** **Wednesday 8:00AM- 9:20AM (Sec B)** **Wednesday 11:00AM- 12:20PM (Sec A)** **Thursday 9:30AM- 10:50AM (Sec A)**
Consultation Hours:	Tuesday 11:00AM -12:20PM (Section A) Thursday 11:00AM- 12:20PM (Section B)
E-mail:	shaila@uap-bd.edu,
Mobile:	01819818234
Rationale:	.
Pre-requisite (if any)**:**	**No**

Course Synopsis: Introduction to Intel microprocessor family. 8086 architecture, pipelining concept, addressing modes, Instruction format, Instruction set, Bus cycle, 8086 system design, Interrupt system, Interfacing, Serial and parallel interface, Assembly language programming using 8086 instruction set for arithmetic logic and decision making looping string and DOS interrupts.

Course Objectives: The objectives of this course are to:

1.	P**rovide** knowledge on microprocessors, internal architecture of a general purpose Microprocessor and its operation, Internal Architecture, Functional Units and Operation of Intel 8086 Microprocessor, Register Architecture, Memory Management, Instruction Set Architecture of Intel 8086 Microprocessor
2.	**Explain** Instruction set, addressing modes and Instructions (Data Transfer, Arithmetic, Logical, String, Stack I/O etc.) of 8086 Microprocessor
3.	S**olve** Program Development and problem solving using Assembly Language Programming.
4.	**Demonstrate** System Design using 8086 Microprocessor in different modes including hardware details, functions & operations of Pins of Intel 8086 and associated interfacing components, advanced Intel processor: internal architecture, memory management, programming and interfacing design.
5	**Analyze** the different categories of microprocessors

Course Outcomes (CO) and their mapping with Program outcomes (PO) and Teaching-Learning Assessment methods:

CO No.	CO Statements: Upon successful completion of the course, students should be able to:	Corresponding POs (Appendix-1)	Bloom's taxonomy domain/level (Appendix-2)	Delivery methods and activities	Assessment Tools
CO1	**Provide** knowledge on microprocessors, architecture, functional units, registers, memory Management, Stack.	1	Remember	Lecture, multimedia,	Class Test, Written exam, Class performance, Assignment, Viva
CO2	**Explain** Instruction set, addressing modes and Instructions (Data Transfer, Arithmetic, Logical, String, Stack I/O etc.) of 8086.	2	Understand	Lecture, Multimedia	Quiz, Written exam

	Microprocessor				
CO3	**Solve** Program Development and problem solving using Assembly Language Programming.	3	Apply	Lecture, Problem Solving, Group discussion	Written exam
CO4	**Demonstrate** System Design 8086 in different modes including hardware details, functions & operations of Pins and associated interfacing components.	2	Understand	Lecture, multimedia,	Quiz, Written exam
CO5	Recognize the need and have the preparation and ability to engage in independent and life-long learning in the broadest context of Microprocessor evaluation.	12	Analyze	Overall Course	Viva

Weighting COs with Assessment methods:

Assessment Type	% weight	CO1	CO2	CO3	CO4	CO5
Final Exam (Written Exam)	**40%**	10	10	10	10	
Final Exam(Viva)	**10%**	5				5
Mid Term (Written Exam)	**20%**	15	5			
Class Test, Quiz	**20%**	5	10		5	
Class performance, Assignment	**10%**	10				

Total	**100%**	45	25	10	15	5

Instruction: 70% attendance is mandatory for final exam

Grading Policy: As per the approved grading policy of UAP (Appendix-3)

Course Content Outline and mapping with COs

Weeks	Topics / Content	Course Outcome	Delivery methods and activities	Reading Materials
1.	Introduction to Microprocessors, 8086 Microprocessors its Features. 8086 Architecture, Functional units, Pipelining and 8086 registers.	CO1	Books, class lectures and slides provided.	Douglas V. Hall, Microprocessors and interfacing: programming and hardware, McGraw-Hill.
2.	8086 Flag Register, Memory Segmentation, Physical Address Calculation, and Instruction set.	CO1	Books, class lectures and slides provided.	Douglas V. Hall, Microprocessors and interfacing: programming and hardware, McGraw-Hill.
Class Test #1				
3.	Addressing Modes- Finding the addressing mode of an operand in instruction Introduction to IBM PC assembly language, Flow control instructions, Logic, shift and rotate instructions,	CO2	Books, class lectures and slides provided.	Douglas V. Hall, Microprocessors and interfacing: programming and hardware, McGraw-Hill.
4.	The stack and introduction to procedures, Multiplication and division instructions,	CO2	Books, class lectures and slides provided.	Assembly Language Programming and Organization of the IBM PC by Ytha Yu and Charles Marut.

Class Test #2				
5.	8086 hardware details, functions & operations of pins & signals of Intel 8086, Minimum versus Maximum mode operation,	CO4	Books, class lectures and slides provided.	Douglas V. Hall, Microprocessors and interfacing: programming and hardware, McGraw-Hill.
6.	System design in Minimum and Maximum modes and associated interfacing components,	CO4	Books, class lectures and slides provided.	Douglas V. Hall, Microprocessors and interfacing: programming and hardware, McGraw-Hill.
7.	Bus Operation, Processor Read & Write bus cycles,	CO4	Books, class lectures and slides provided.	Douglas V. Hall, Microprocessors and interfacing: programming and hardware, McGraw-Hill.
Mid-Term Examination				
8.	Interrupts and Interrupt Handing system design using 8086, Basic I/O Interfacing: Parallel I/O, Programmed I/O	CO4	Books, class lectures and slides provided.	Douglas V. Hall, Microprocessors and interfacing: programming and hardware, McGraw-Hill.
9.	The 8255A Programmable Peripheral Interface (PPI), programming 8255, Operation modes with examples	CO4	Books, class lectures and slides provided.	Barry B. Brey, The Intel Microprocessors, Processor Architecture, Programming, and Interfacing, Eighth Edition, 2009, Prentice

				Hall
10.	Architectural overview of advanced Intel Processors- 80186/80286/80386/80486	CO4	Books, class lectures and slides provided.	Barry B. Brey, The Intel Microprocessors, Processor Architecture, Programming, and Interfacing, Eighth Edition, 2009, Prentice Hall
10.	Pentium Processor, Cache memory, TLB segment register formats, Paged memory operation, page Directory and page table address translation. Linear to physical address translation, Protected Mode Memory Management; segmentation and virtual addressing, segment selectors segment descriptor tables, segment descriptor, Cache Memory, TLB	CO4	Books, class lectures and slides provided.	Barry B. Brey, The Intel Microprocessors, Processor Architecture, Programming, and Interfacing, Eighth Edition, 2009, Prentice Hall
Class Test #3				
11.	Handling Arrays and solving addressing modes,	CO3	Books, class lectures and slides provided.	Assembly Language Programming and Organization of the IBM PC by Ytha Yu and Charles Marut.
12.	Memory management, DOS interrupts, and advanced arithmetic	CO3	Books, class lectures and slides provided.	Assembly Language Programming and Organization of the IBM PC by Ytha Yu and Charles Marut.

Class Test #4				
13.	The string instructions, Subroutines and solving related problems.	CO3	Books, class lectures and slides provided.	Assembly Language Programming and Organization of the IBM PC by Ytha Yu and Charles Marut.
14.	Review	CO5	Books, class lectures and slides provided.	

Required Reference(s):

1. Barry B. Brey, The Intel Microprocessors, Processor Architecture, Programming, and Interfacing, Eighth Edition, 2009, Prentice Hall
2. Douglas V. Hall, Microprocessors and Microcomputer Based System Design, McGraw-Hill.
3. M. Rafiquzzaman., Microprocessors Theory and Applications: Intel and Motorola, 2003, Prentice Hall of India. *Pvt. Ltd., New Delhi, 6.*
4. Assembly Language Programming and Organization of the IBM PC by Ytha Yu and Charles Marut.

Recommended Reference(s):

5. Intel 64 and IA-32 Architectures Software Developer's Manual, http://www.intel.com/design/literature.htm

Special Instructions:

•Minimum Required Attendance: 70% class attendance is mandatory for a student in order to attend the final examination.

•Late presence: Consecutive two days late presence in the class will be counted as one day absent

•Assignment submission rules: Have to submit assignment by the last date of submission.

Prepared by	Checked by	Approved by

 Shaila Rahman Assistant Professor		

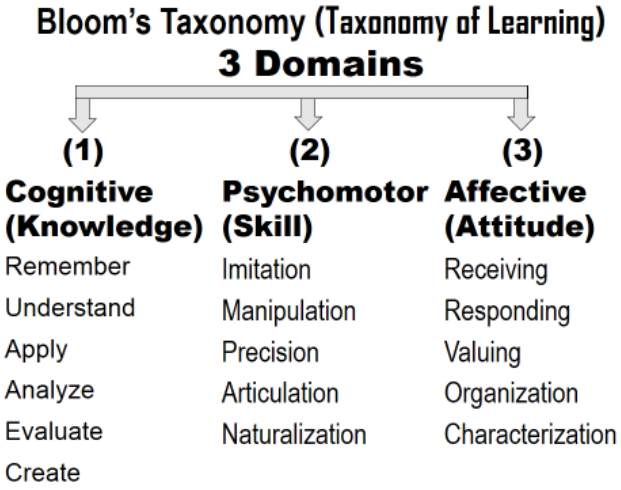
Appendix-1:

Washington Accord Program Outcomes (PO) for engineering programs:

No.	POs	Differentiating Characteristic
1	Engineering Knowledge	Breadth and depth of education and type of knowledge, both theoretical and practical
2	Problem Analysis	Complexity of analysis
3	Design/ development of solutions	Breadth and uniqueness of engineering problems i.e. the extent to which problems are original and to which solutions have previously been identified or codified
4	Investigation	Breadth and depth of investigation and experimentation
5	Modern Tool Usage	Level of understanding of the appropriateness of the tool
6	The Engineer and Society	Level of knowledge and responsibility
7	Environment and Sustainability	Type of solutions.
8	Ethics	Understanding and level of practice
9	Individual and Team work	Role in and diversity of team
10	Communication	Level of communication according to type of activities performed
11	Project Management and Finance	Level of management required

		for differing types of activity
12	Lifelong learning	Preparation for and depth of Continuing learning.

Appendix-2



Appendix-3

UAP Grading Policy:

Numeric Grade	Letter Grade	Grade Point
80% and above	A+	4.00
75% to less than 80%	A	3.75
70% to less than 75%	A-	3.50
65% to less than 70%	B+	3.25
60% to less than 65%	B	3.00
55% to less than 60%	B-	2.75
50% to less than 55%	C+	2.50
45% to less than 50%	C	2.25
40% to less than 45%	D	2.00
Less than 40%	F	0.00