Department of Computer Science & Engineering
University of Asia Pacific (UAP)

Final Examination **Fall 2021** **3rd Year 2nd Semester**

Course Code: CSE317 **Course Title: Computer Architecture** **Credits: 3**

Full Marks: 150 **Duration: 3 Hours**

Instructions:

1. There are **Six (6)** Questions. Answer all of them. All questions are of equal value. Part marks are shown in the margins.
2. Non-programmable calculators are allowed.

1. Design and Implement the single cycle data path for the following instructions and write down the procedure of data path for following MIPS instructions: (consider all the functional units of Data path according to MIPS architecture) **[13+12]**

i) A [22] =Y + A [15];

ii) Add $to , $s1 , $s2;

2 a. Draw and Explain all the instruction format for the MIPS instruction set architecture. **[10]**

b. Draw and explain the basic components of computer and Layer of a computer. Show the relationship among Instruction Set, Software and Hardware that define computer architecture. **[15]**

OR

a. What is the objective of memory hierarchy? According to cost, size, distance and speed compare among the levels of memory. **[10]**

b. What are the four questions about cache design? Show and explain the hardware implementation of block identification. (data may be Hit OR miss). **[15]**

3. a. This question considers the basic MIPS, 5-stage pipeline (IF, ID, EXE, MEM, WB). **[15]**

Assume that you have the following sequence of instructions:

lw $s2, 0($s1)

add $s3, $s4, $s2

Sub $s6, $s2, $s3.

Show the implementation through 5 stages and explain the implementation for both pipelined and non-pipelined design.

b. 'Pipelining does not reduce latency of a single task' proves this statement. **[10]**

OR

$5+1+(3-1)\times 1$

a. Instruction and Opcode/Function: lw 100011, sw 101011, sub 100010, add 100000 [15]

i) Analysis the following high level statement according to MIPS instruction format and write the MIPS machine Code.

X[4] = Z + X[3] ;

ii) Analysis the following MIPS machine Code to identify the instruction and write the high level statement.

00198820(hex)

b. Suppose we have two implementation of same instruction set architecture. Computer A has a clock cycle time of 300 PS and a CPI of 1.8 for some program, and computer B has a clock cycle time of 550 PS and a CPI of 1.4 for the same program. Which computer is faster and how much? [10]

4. a. Consider a non-pipelined machine with 6 execution stages of lengths 20 ns, 25 ns, 30 ns, 35ns, 20 ns, and 25 ns. [10]

- Find the instruction latency on this machine.
- How much time does it take to execute 68 instructions?

Suppose we introduce pipelining on this machine. Assume that when introducing pipelining, the clock skew adds 3ns of overhead to each execution stage.

- What is the instruction latency on the pipelined machine?
- How much time does it take to execute 68 instructions?

Also calculate the speedup for this implementation.

b. Suppose there are 9 instructions in a program. Draw the page table and compute the following: [15]
(consider there are 4 stages and each takes one clock cycle)

- Total time for pipeline and non-pipeline.
- CPI
- Speedup
- Efficiency or utilization

5. Solve the following using 3rd version of division algorithm. [25]

7 by 2.

Also draw the algorithm flowchart and hardware design of 3rd version of division algorithm.

6. CPU request the following Block addresses 20, 16, 25, 16 and 25. [5+20]
There are 16 blocks in cache. Design and Show the memory mapping for the following cache configurations.

I. Direct mapped
II. 2- Way, 4-way 8-way and 16 way set associative mapped.