Department of Computer Science & Engineering

University of Asia Pacific (UAP)

Program: B.Sc. in Computer Science and Engineering

Final Examination **Spring 2021** **3rd Year 2nd Semester**

Course Code: CSE 317 **Course Title: Computer Architecture** **Credits: 3**

Full Marks: 120* (Written) **Duration: 2 Hours**

* Total Marks of Final Examination: 150 (Written: 120 + Viva: 30)

Instructions:

1. There are **Four (4)** Questions. Answer all of them. All questions are of equal value. Part marks are shown in the margins.
2. Non-programmable calculators are allowed.

1. Design and Implement the single cycle data path for the following instructions and write down the procedure of data path (consider all the functional units of Data path according to MIPS architecture)

* Where X= last two digits of your ID.

A [x+10] =Y + A [x+15]; **30**

2. **a)** CPU request the following Block addresses (x+11), (x+21) and (x+17). **20**
There are 16 one-word blocks in cache. Design and Show the memory mapping for the following cache configurations.

I. Direct mapped.

II. 4-way ,8-way and 16- way set associative mapped. (use LRU replacement policy) * Where X= last two digits of your ID.

b) **10**

For the following configuration Determine the number of bits required for physical address, tag, index and block offset.

i) Consider 32 words cache and 512 words main memory. Block size 4 words. Determine the number of memory blocks and cache lines.
ii) Consider 16 words cache and 64 words main memory. Block size 4 words.
iii) Consider 16 words cache and 128 words main memory. Block size 4 words.
iv) Consider 32 words cache and 1024 words main memory. Block size 4 words.
v) Consider 8 words cache and 16 words main memory. Block size 4 words
Also draw the required block for direct mapping cache.

3. **a)** Compare between pipeline machine and non-pipeline machine. suppose there are (X+9) instructions in a program. Draw the page table and compute the following: (where X is the last digit of you ID **10**

number) * consider there are 5 stages and each takes one clock cycle.

- Total time for pipeline and non-pipeline.
- CPI
- Speedup
- Efficiency or utilization

b) Consider a non-pipelined machine with 5 execution stages of lengths 35 ns,40 ns, 45ns, 30 ns, and 20 ns. **10**

- Find the instruction latency on this machine.
- How much time does it take to execute (**i**+1010) instructions?

Suppose we introduce pipelining on this machine. Assume that when introducing pipelining.

- What is the instruction latency on the pipelined machine?
- How much time does it take to execute (**i**+1010) instructions?

Also calculate the speedup.

(where **i** is the last two digits of you ID number)

c) This question considers the basic MIPS, 5-stage pipeline (IF, ID, EXE, MEM, WB). **10**

Assume that you have the following sequence of instructions:

lw $s2, 0($s1) (instr1)
add $s3, $s4, $s2 (instr2)
Sub $s6, $s2, $s3. (instr3)

Show the implementation through 5 stages and explain the implementation for both pipelined and non-pipelined design. (explain if there is any pipeline hazards)

4. **a)** Draw the basic components of computer and Layer of a computer. Show the relationship among Instruction Set, Software and Hardware that define computer architecture. **5**

b) Compiler designer is trying to decide between two code sequences for a particular machine. Based on the hardware implementation, there are three different classes of instructions: Class A, Class B, and Class C, and they require three, two, and four cycles (respectively). **20**
The first code sequence has **(i+ 9)** instructions: 4 of A, 2 of B, and 3 of C.
The second sequence has **(i+11**)instructions: 6 of A, 3 of B, and 2 of C.
Where i= last two digits of your ID.
Which sequence will be faster? How much?

c) How many instruction classes are in MIPS architecture? Why R-type class instructions are faster than I- type instruction class. **5**

OR

a) What are the four questions about cache design? Show and explain the hardware implementation of block identification. (data may be Hit OR miss). **5**

b) For the following high-level statement write the MIPS machine Code. **20**

A[**i**] = B+ A[**i**+11] - C; Where **i** = last two digits of your registration number.

Instruction	Opcode/Function
lw	100011
sw	101011
sub	100010
add	100000

c) What is the objective of memory hierarchy? According to cost, size, distance and speed compare among the levels of memory. **5**