AFTER MID

Carry Select Adden

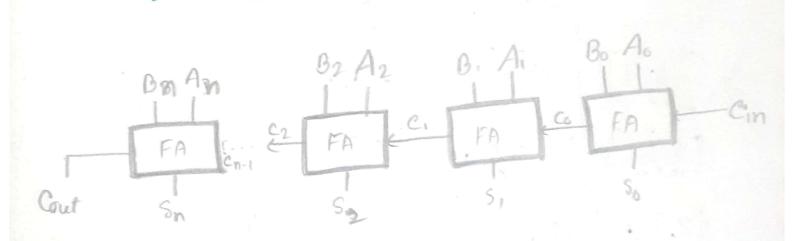
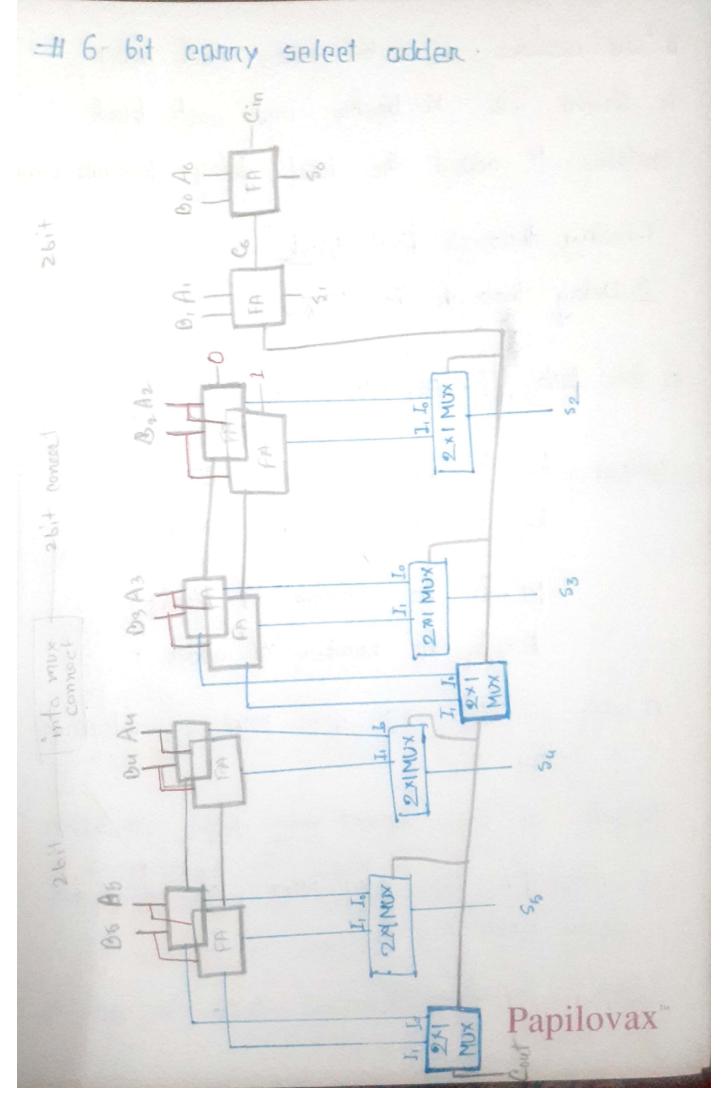


figure : n bit rupple carry adden

if we conside a n-bit ripple carmy adders and k, is the delay for a FA.

Total delay, $T = \frac{nk_1}{\alpha p} - 0$



If we consider a n-bit carry select adder is divided into M blocks and each block contains P added the total delay depends on-H 1. Delay through first block 2. Delay through the MUX so, total Delay, T = Pk, + (M-1) k2 - 2 Where, K1 = is the delay for FA kz: is the delay for MDX M = is the number of blocks P = is the number of adder 1 12 abs FA delay 214, 2001 Mux 29 selection

Delay 2001

Delay

Ams: 5 gate met

1 Hlu sobi sobi FA delay = 1 see 221 K, = 1 &C, n= 20 bit. () + total delay, T= nk1 = 20x1 = 20 delay (I) T= 20 == 2 x pk, + (M-1) k2 = 2 x 1 .+ (10-1) · 1 · = 2+9 &c. 2 Il S.C. 20 MAR, 2024 1 # Programm Logie Annay (PLA) 1 AND:OR PLA 1 I $F_1 = xy + xyz + zx = P_1 + P_2 + P_3$ I F2 = xyz + xyz + xzy = P2+P4+P5 1 of 161 PLAG 361 input, 261 output, 5 to Product I 1 a v= number of imput 1 P = number of product I Z = number of output 11 size of PLA = VXPXZ Papilovax* - 3×5×2

I

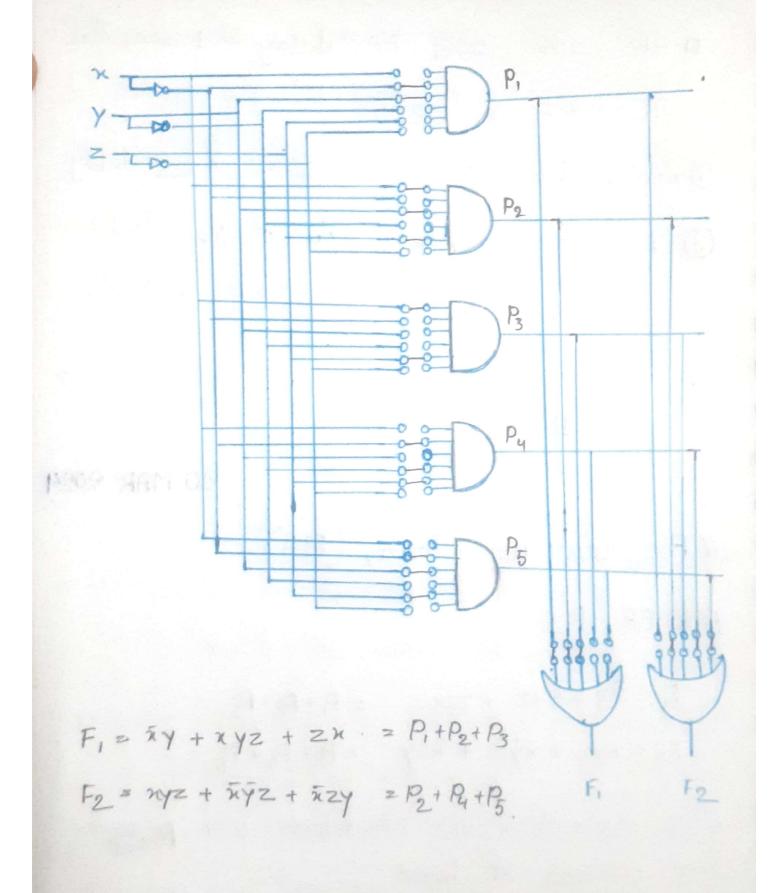
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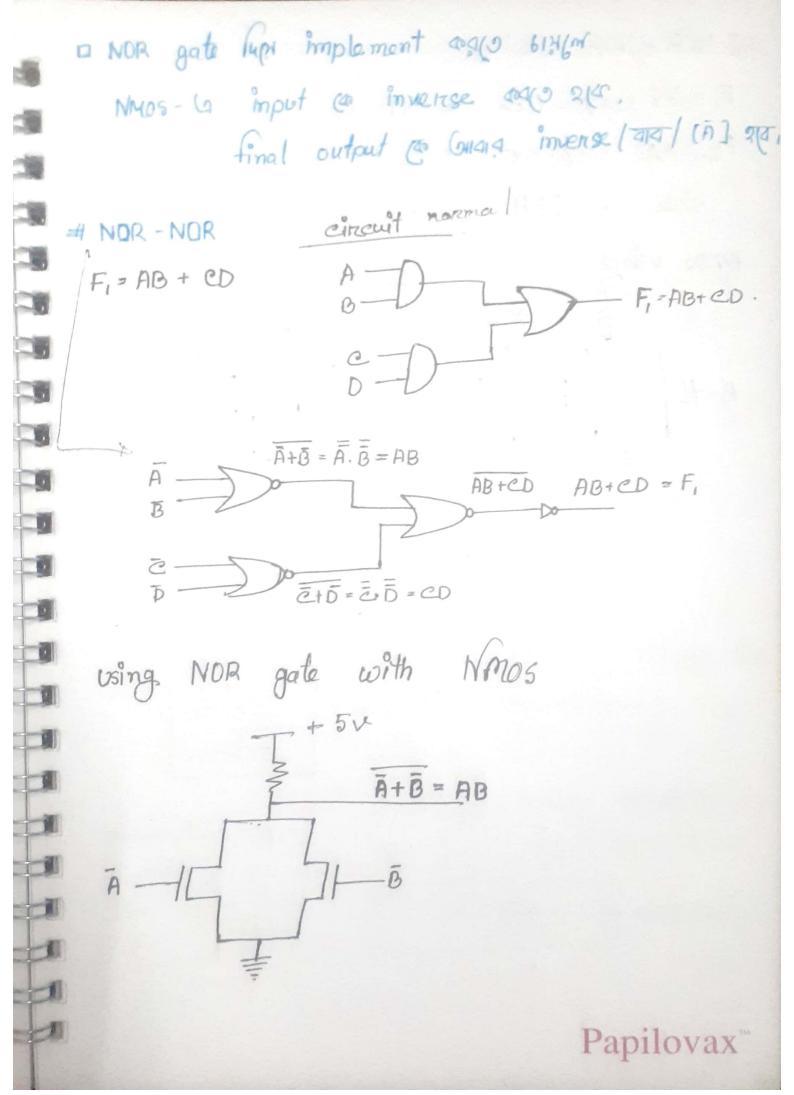
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T

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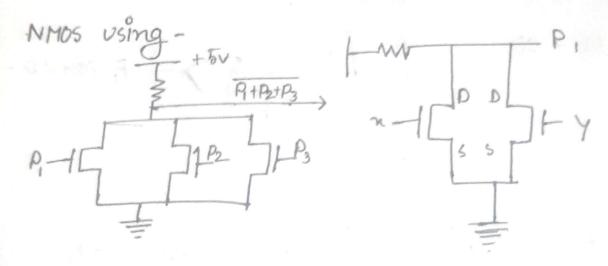


H NOR - NOR PLA

$$F_1 = \overline{x}\overline{y} + x\overline{y}z + zx = P_1 + P_2 + P_3$$

$$F_2 = x\overline{y}z + \overline{x}y + x\overline{y}\overline{z} = P_2 + P_4 + P_5$$

$$\text{size of PLA} = (3x5x2)$$



Threshold voltage: threshold voltage is the minimum gate voltage that is needed to create a conducting path between Drain and Source. Drain & Source 1 gate 29 21(8) (4 missier voltage supply lugar THE CH MESTIGE CONDUCTING PATH COLO 274 PILO CHAISI threshold voltage alm 1 - gate 2 (4 supply als Drain & source 20 अदि channel रेगिन कित -> metal charge, Qg ++++ >oxide change, Qss oxide -> inversion channel charge , Qe channel -> Depletion. Negion charge, Qd. 900 substate. D = voltage supply.

D = channel capacitons, Cq

A

- 6

1

1

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we can write , Qg + Qss = Qc + Qd :. Qg - Qc + Qd - Qss Three-shold voltage, V+ = Qg = Qe+Qd + - Qss where , og is the gate capacitance # Body effect a body tearminal stastant source 20 mily sout ago. sort / क्लीट काव भावाव कावत कीव voltage अवसम्भ zeno à marga, sulca Body effect alm. if we consider vo is the threshold voltage when , Vin = 0 if Vso = 0, then V+ = V+ + 8 VVso when 8 = is a constant. FOR MOSFET, 8 = 0.3 ~ 0.7 8 = ton JagEsi NA

where, tox = thickness of O2

Eon = Oxide Permitivite

q = charge of an electron

Es = Permitivity of silicon

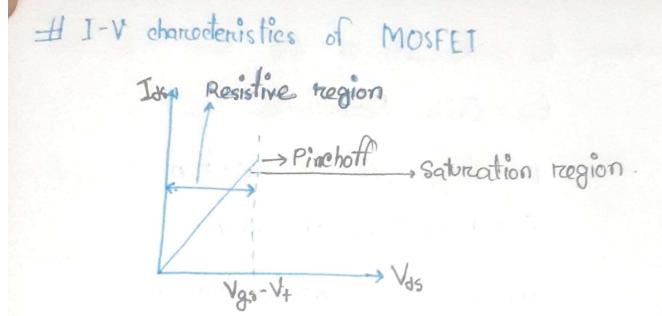
NA = Dopoing Contradocentration

VSB = 0 24 the shold (yet (yet about equation and)

VSB = 0 24 GRM gara body effect GATE,

GRAT Gota equation ANG.

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MOSFET & 1 card mode (Resistive | Saturation region)

for NMOS

Isaturation mode

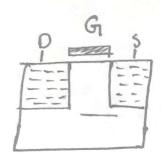
trasistine Made

For PMOS toesistine Mode if Vsd < Vsj - V4 Isd = EMP Wo 1 (Veg-V4) Vsd - Vsd - 5 saturation Mode if Vsd > Vsg - 14 Isd = EMP Wp of (Vsg - 4)2 } Wheres, D -> Depth of 02 Mn -> Mobility of Electron Mp > Mobility of Hole E > Permitivity Wp/Wn -> channel width Lp/Ln -> channel length Vgs = Vg - Vs Vg = gate roltage Vo = source voltage Papilovax"

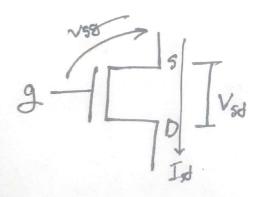
pinchoff = (point la longe voltage alumno Ids ally M

Council with Compressors

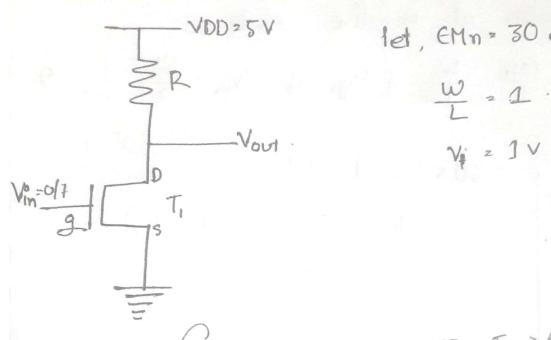
MOSFET - 2006 electronic switch.



9 - I Vos > 25 Me current flow 42 Ids.



I NMOS inventor with Resisting load



Solne - if Vin = O, Ti > OFF To > Always on.

a COFF 2110pm not need.

CZ, Vin 20 21 conrent flow 2 coals of

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Ti operates at resistive mode.

$$T_1 = I_{ds} = \frac{f_{Mn}}{D} \cdot \frac{W_n}{L_n} \left\{ (v_{gs} - V_+) V_{ds} - \frac{V_{ds}^*}{2} \right\} = ?$$

$$\frac{W_n}{L_n} = 1$$
.

$$=30\times1\left\{ \left(5-1\right) \times0.33-\frac{\left(0.33\right) ^{2}}{2}\right\}$$

$$=30$$
 ($9\times0.33-0.05445.$)

$$= \frac{5 - 0.33}{37.96 \times 10^{-6}}$$

Example: VDD = 3v, EMm = 50 MA/v2, T = 4 R=? V+ = 0.75 v, Vds = 0.2 v, Vin = 3.5 v Some: if Yin-0, Ids OFF If 49 = 5V, Ids ON Vin = 3.5 V = V8 Vgs = Vg - Vs = 3.5 - 0 v= 3.5 v. :. Vgs-V+ = (3.5 - 0.75) V = 2.75 V see, Vds < Vgs-V+; 0.2V < 2.75 V Ids operates at resistive Mode. Ids = EMm W & (Vgs - 4,) Vds - Vds - Vds - b = 50 × 4 {(3.5 - 0.75) 0.2 - (0.2) } = 200 (2.75 x0.2 - 0.02) = 200 x 0.53 = 106

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Problem: A NMOS inventer with Enhancement type load is biased at VDD = 3v,

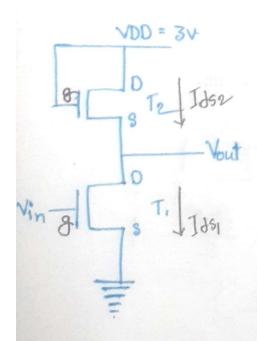
The MOSEET Promotore are VIVL = 0.4V

The MOSFET Parameters are $V_4 = V_{12} = 0.4 \text{ V}$. $\frac{\text{EMm}}{D} = 60 \text{ MAI} \text{ V}^2$. $\frac{\omega_1}{L_1} = 16$. $\frac{\omega_2}{L_2} = 2$.

Find the output voltage when (1) Vin = Ov.

1 Vin= 2.6 4

Also calculate the Power dissipated in the inverter when Vin = 2.6 v.





minput, output voltage ag aggo angol connection conoli cond mode only

Solve = (1) Vin = Or 2(m, Vout = Voo - Vt2

Ti = off

Ti = always on = 3 - 0.4 = 2.6 V

(i) Vin= 2.6 v alm, Vds = Vd-Vs = Vout - Vs Vout = Vds = Vout - 0.

Power dissipated -

T

Vds = 0

Vgs = 2.6 V

V+1=0.41

Vas-V+1=2.2V

Vds = COLO = NOS O

Vgs = VBD- Vout.

= 3 - Vout

V+2=0.4V.

Vgs-V+2=3-0-4=2.6

Vds < Vgs - V+, ; Vds < Vgs - V+2

> <2.2 > 3 < 500.9.6.

> 3 > 2.6.

saturation Mode.

resistine mode, Ti.

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now, Idsi = Idsz output Yout = Vds. => EMM W. L. d (Vgs-V+1) Vds-Vds - Vds - J = EM/n . W2 . (Vgs - V+2)2 => 16 \((2.6-0.4) \Vds - \frac{Vds}{2} \] = \frac{1}{2} \((3-\text{Vout} - 0.4)^2 \) => 16 x {2.2 Vds - Vds } = (Vds - 2.6)2 =D 16 x (4.4 vds - Vds2) = Vds2 - 5.2 Vds + 6.76. =D 8 (4.4 Vds - Vds") = Vds" - 5.2 Vds + 6.76 軒 = 35.2 Vds - 8 Vds 2 - Vds + 5.2 Vds - 6.76 = 0 町 → -9 Vds + 40.4 Vds - 6.76 = 0 → Vds2 - 4.489 Vds + 0.75 = 0 → Vds - 2×2.2445× Vds + (2.2445) - 4.288 = 0 → (Vds - 2.2445) - 4.288 = 0 = (Vds - 2.2445) = 14.288 D Vds = 2.07 + 2.2495 ° . Vds = 4.315. V

$$I_{dS2} = \frac{fMn}{2D} \cdot \frac{W_2}{V_2} \left(v_{gs} - V_{f_2} \right)^2$$

$$= \frac{60}{2} \times 2 \left(3 - 0.174 - 0.4 \right)^2$$

$$= 353 \text{ MA}$$

Problem: VDD = 5v, V+1 = V+2 = 0.8 v. FMn = 35 MA | V2 V0 = 0.1 V , Vin = 4.2 V W1/L1 = ? P2) Solve: if Vo= 0 0 V., T, = off, T2 > always on Vto = IV. Vout = VDO - V+2 8=0.5 = VDD - (V+6 + 8 TV50) * Vout = 5 - (1+0.5 Vout) → Vout = 4 + 0.5 \ Vout + 2 Vout = 8 + 0.5 ×2 √ Vout 1 2 Vout = 8 1-1 Vout 4 Nout = 8 - 2 Vout + Vout = 64 - 32 Vout + 4 Vout - 4 4 Vout 2 - 33 Vout + 64 20. -> Vout 2 - 8.25 Vout + 16 = 0. + Vout 2 - 2 x Vout x 4.125 + (4.125) - 1.015625=0 - (Voat - 4.125) = 1.015625 00. - Voul = 1 - 05 625 + 4125 + Vout = 5.140625. : Vout = 5.13 v or 3.12 v.