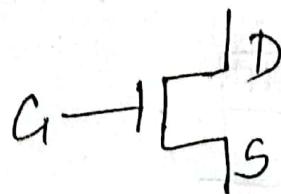


PMOS  $G = \begin{cases} 1, OFF \\ 0, ON \end{cases}$

କୁଣ୍ଡଳ PMOS ଫିଲ୍ଡ୍ ଦେଣ୍ଡାଲ୍ ପରିପାତ  
ନୀର୍ବାହୀ ହାତ ଅବ୍ୟାହୀ  
ଆଶକତାକୁଟ୍ ଗୋଚର.



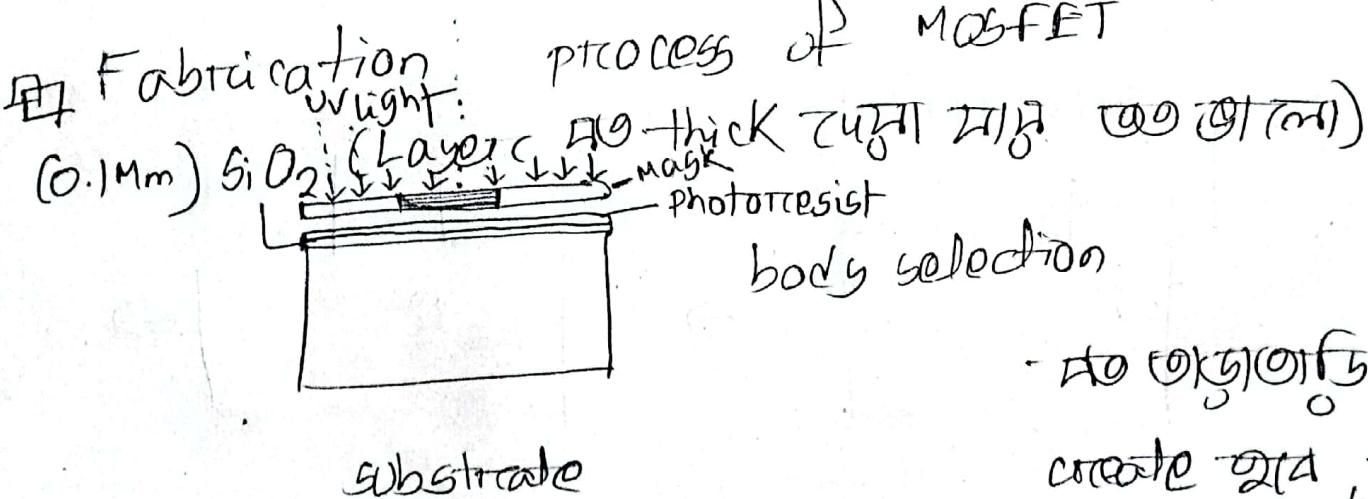
NMOS  $G \gg \begin{cases} 1-ON \\ 0-OFF \end{cases}$

କୁଣ୍ଡଳ NMOS ଫିଲ୍ଡ୍ ଦେଣ୍ଡାଲ୍ ଲୋଜିକ୍ 1  
ଦେଣ୍ଡାଲ୍ ପରିପାତ ଲୋଜିକ୍ 0

$PMOS + NMOS = CMOS$

କୁଣ୍ଡଳ କେଂପିଙ୍ଗ  $SiO_2$  ଫିଲ୍ଡ୍ ପିଲ୍ଟ ଏବଂ  
ବାଲ୍ ମସ୍କ

process of MOSFET

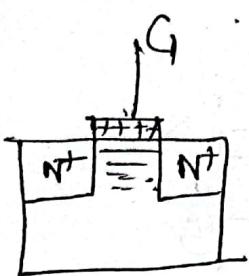


- ଏବଂ କୁଣ୍ଡଳ ଚାନ୍କ୍ଯ ତୋରିବା  
କୁଣ୍ଡଳ ତୋରିବା
- ଏବଂ କୁଣ୍ଡଳ ଚାନ୍କ୍ଯ ତୋରିବା  
କୁଣ୍ଡଳ ତୋରିବା

$H_2SO_4$

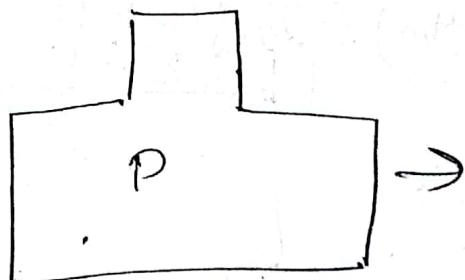
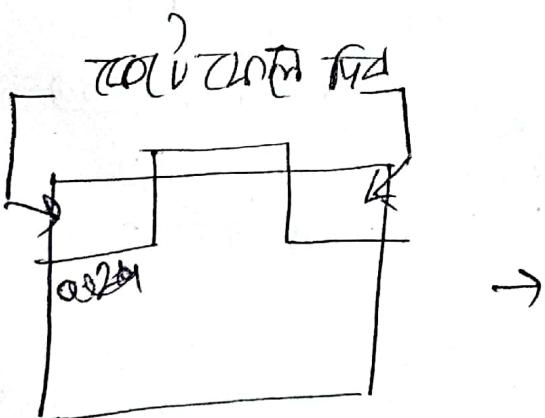
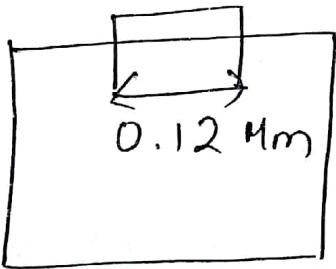
G - Gate  
S - Source  
D - Drain

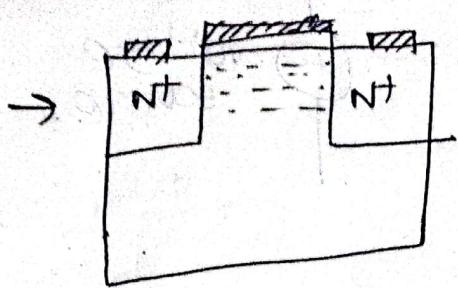
Capacitor value මෙම තාක්ෂණ නමුව යොමු කළ ලාභ,



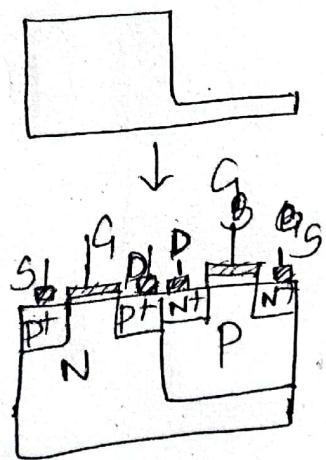
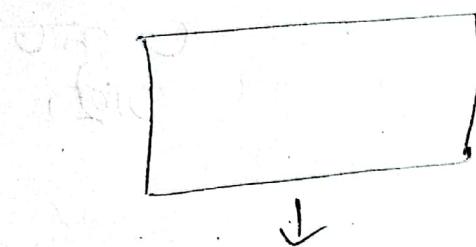
තාක්ෂණ ප්‍රමාණ නමුව ලාභ, Discharge තුළ  
ජ්‍යෙන් පෙනු ලාභ!

Mm → micrometer

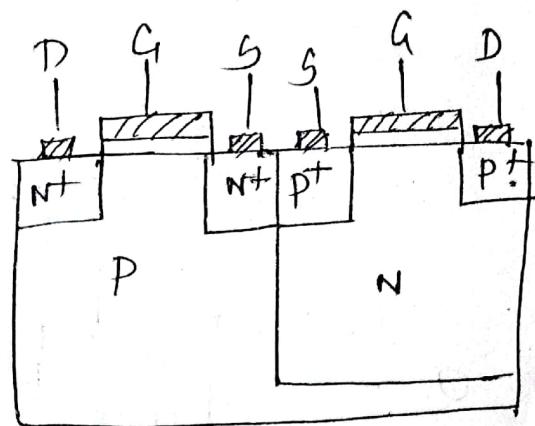




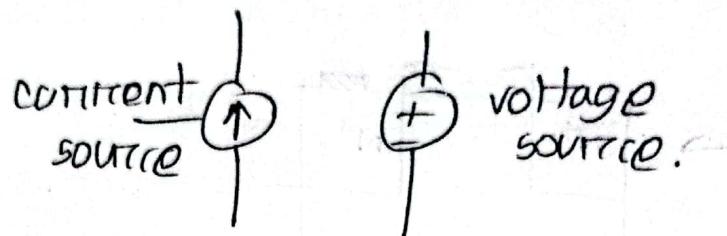
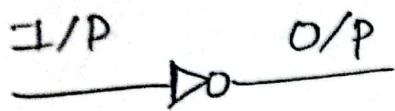
P-well  
technology



N-well  
technology

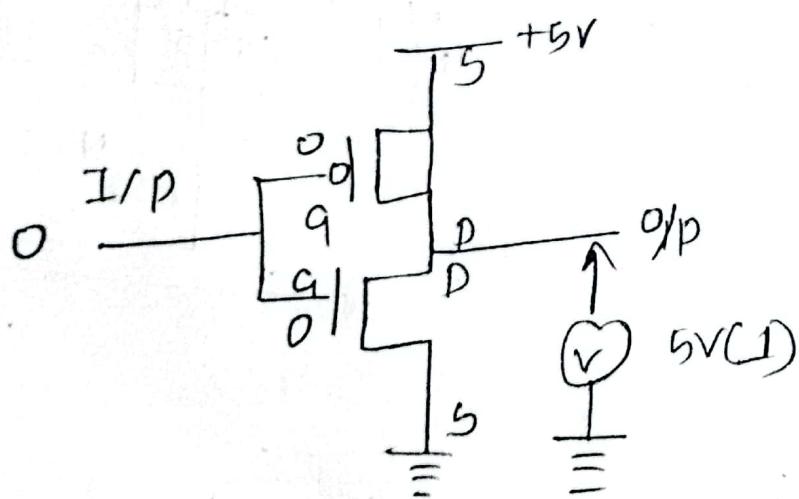
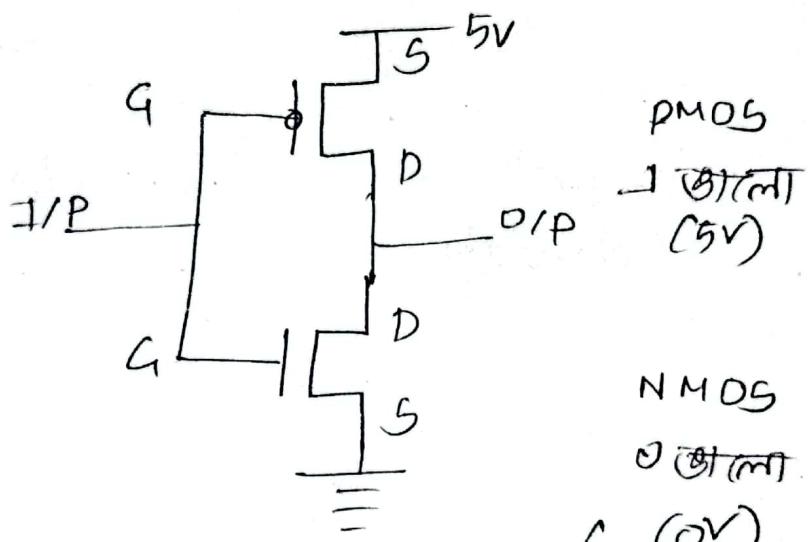


NOT Gate



Truth Table

I/P	O/P
0	1
1	0

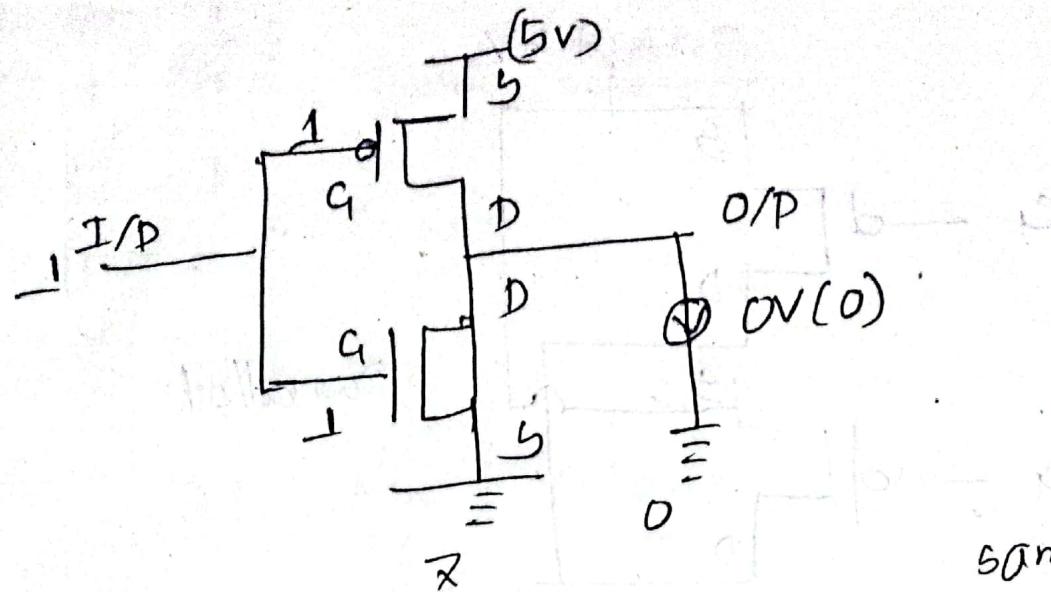


PMOS  
 1 (0) (1)  
 (5V)

NMOS  
 0 (1) (0)  
 (0V)

Ground  
 0 (0) 1





same terminal connect

—parallel

opposite terminal connect

—series

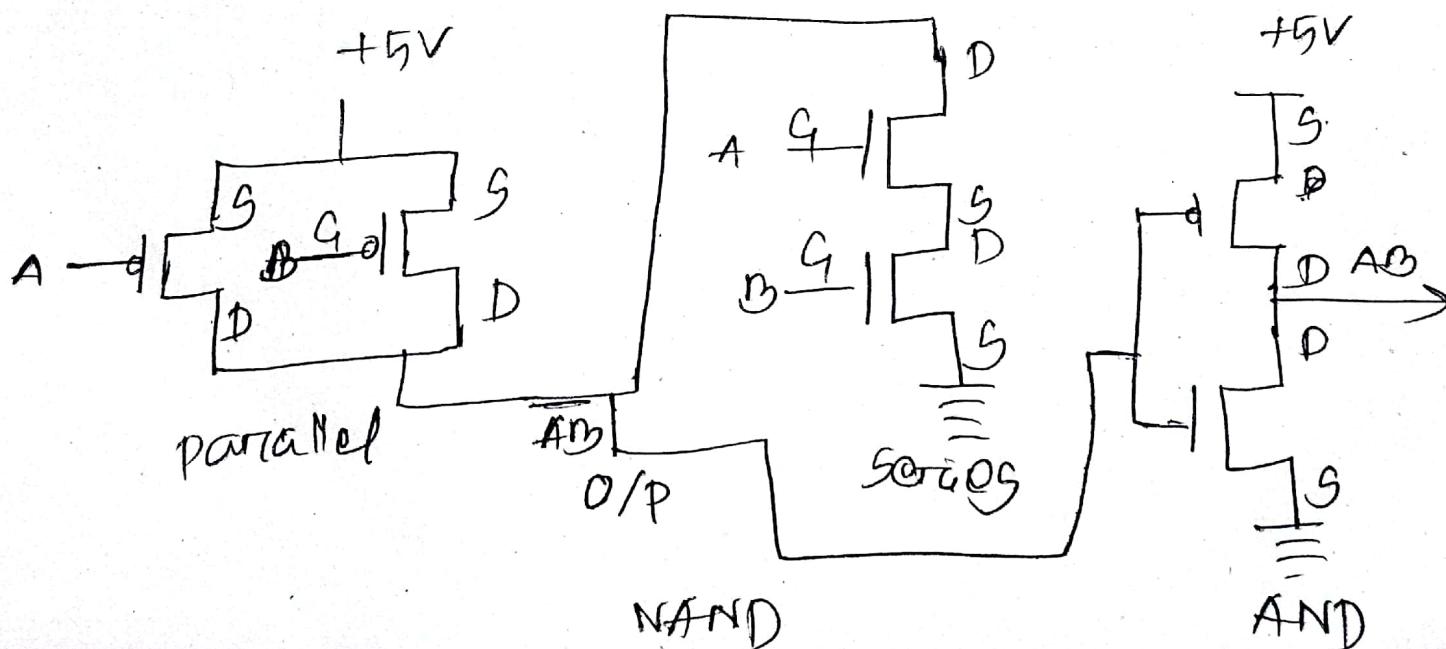
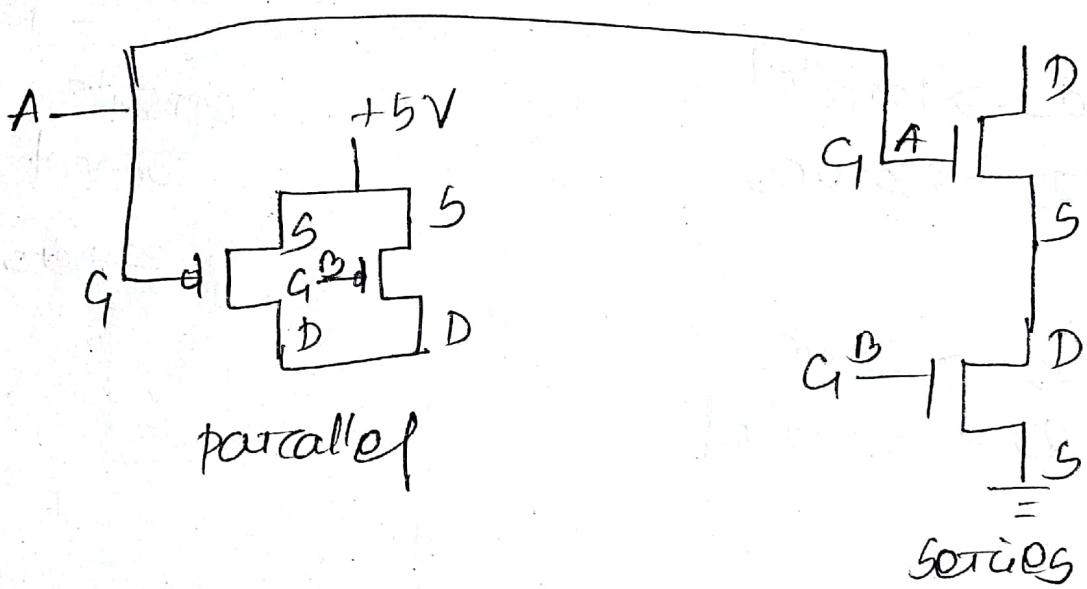
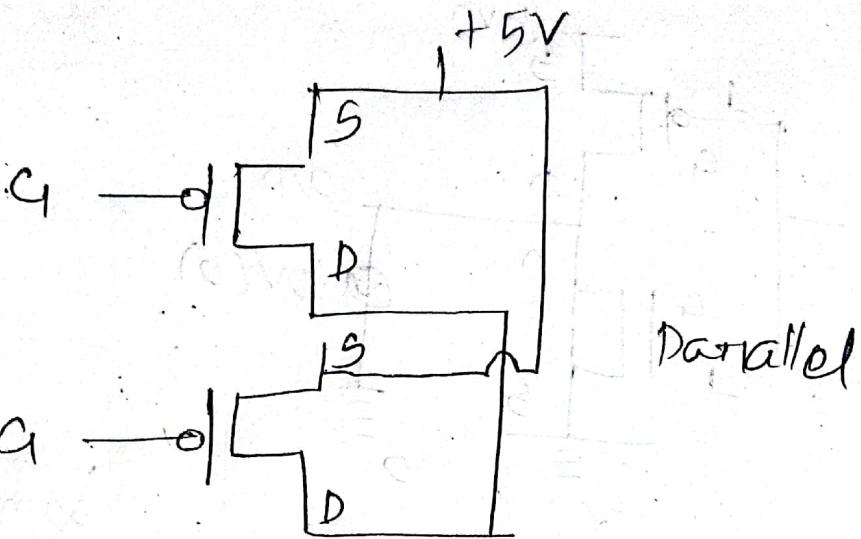
PMOS → parallel

product → NMOS → series

sum → PMOS → series

NMOS → parallel





Q1

A B O/P

0 0 1

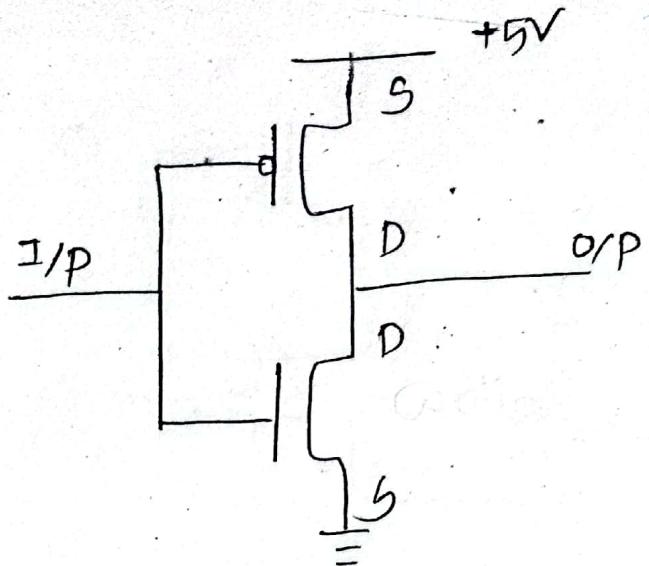
0 1 1

1 0 1

1 1 0

← NAND

Red Green Blue Yellow



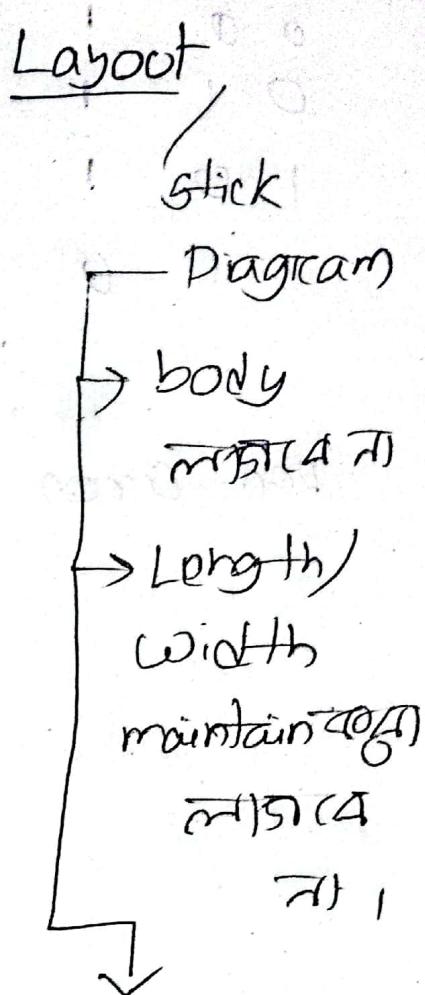
CMOS ckt

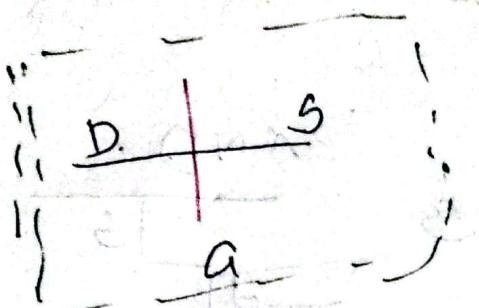
Red  $\rightarrow$  Polysilicon ( $SiO_2$ )

Green  $\rightarrow$  N-type material

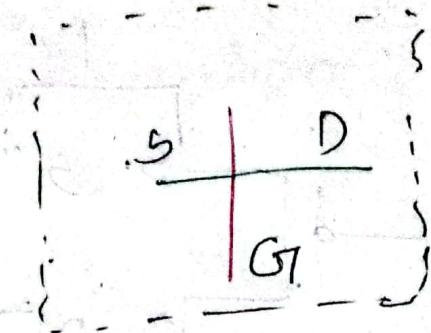
Blue  $\rightarrow$  Metal

Yellow  $\rightarrow$  P-type material





PMOS



NMOS

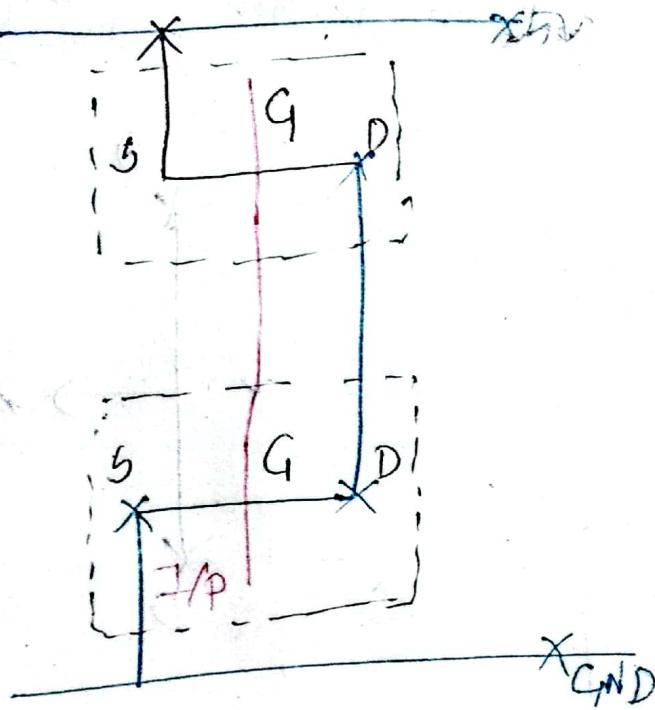


Different material connect

contact

via  $\rightarrow X$

বেজ টু সেক্ষেন ফিল্ড এলেক্ট্রো



connect টু গেট স্ট্রাইপ

(N<sub>A</sub>) মার্কেট মার্কেট

connect টু গেট স্ট্রাইপ

বেজ টু সেক্ষেন ফিল্ড এলেক্ট্রো

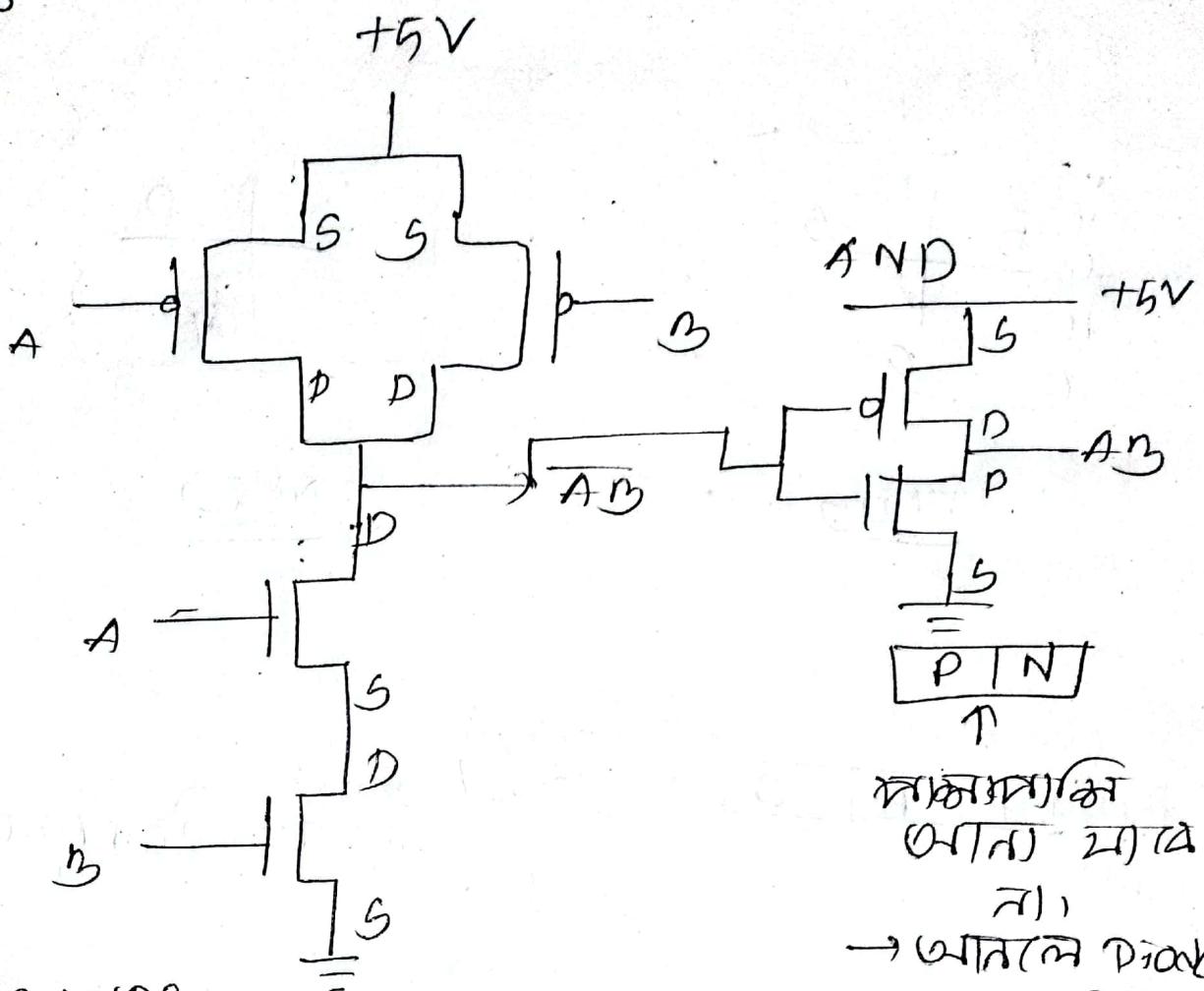
এলেক্ট্রো

(N<sub>A</sub>) point টু ডাফ

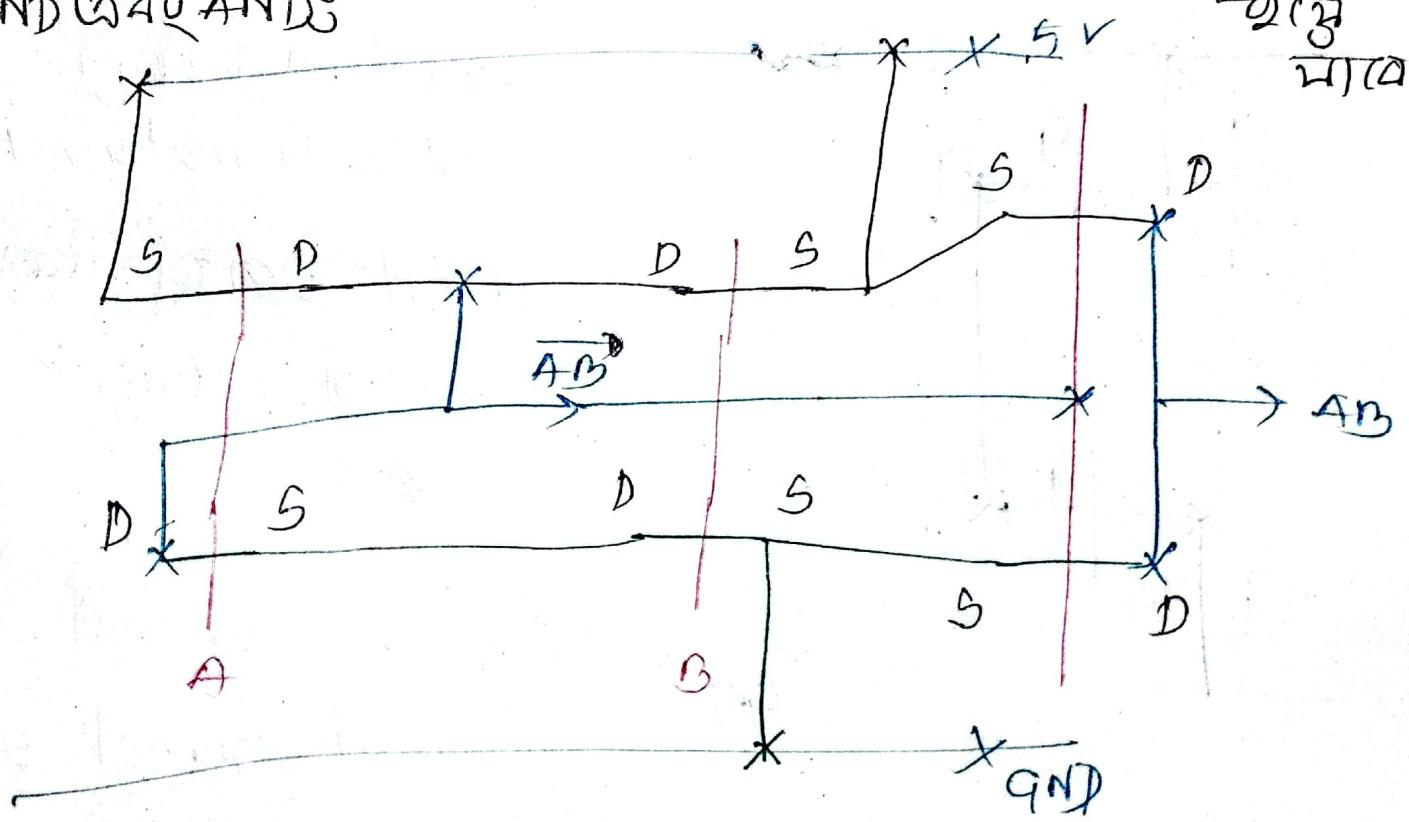
মার্কেট মার্কেট টু গে

বেজ টু এলেক্ট্রো

NAND<sup>o</sup>



NAND<sup>o</sup>  $\Rightarrow$  AND<sup>o</sup>



प्राक्तिक गेट  
OR<sup>o</sup> 20 mA

→ घटक गेट  
Diode  
20 mA

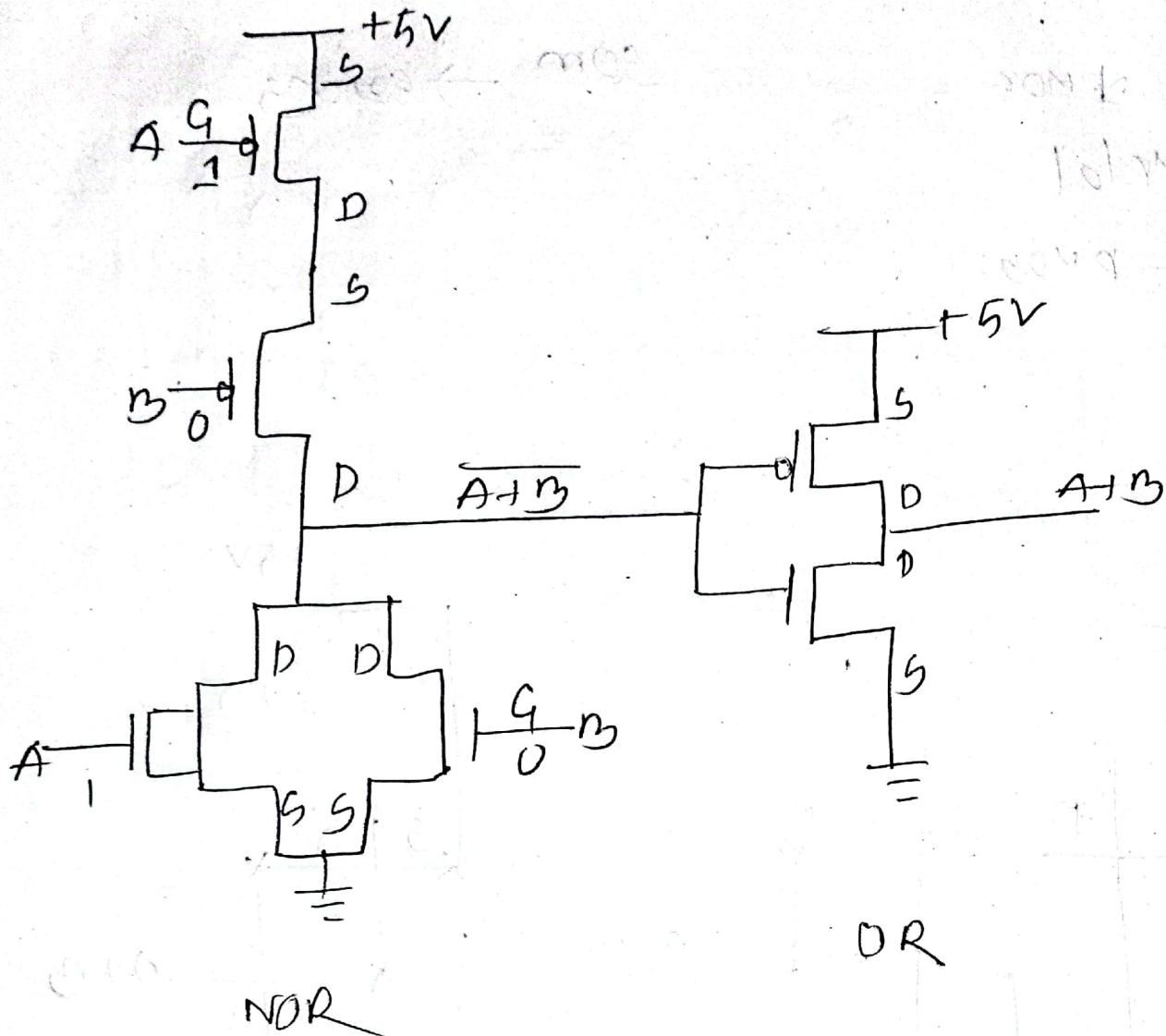
X 5 V  
X GND

CS  
CamScanner

VLSI || 24-Jan-2024

Topic -

Inverter & Buffer



## Layout

red - S, D

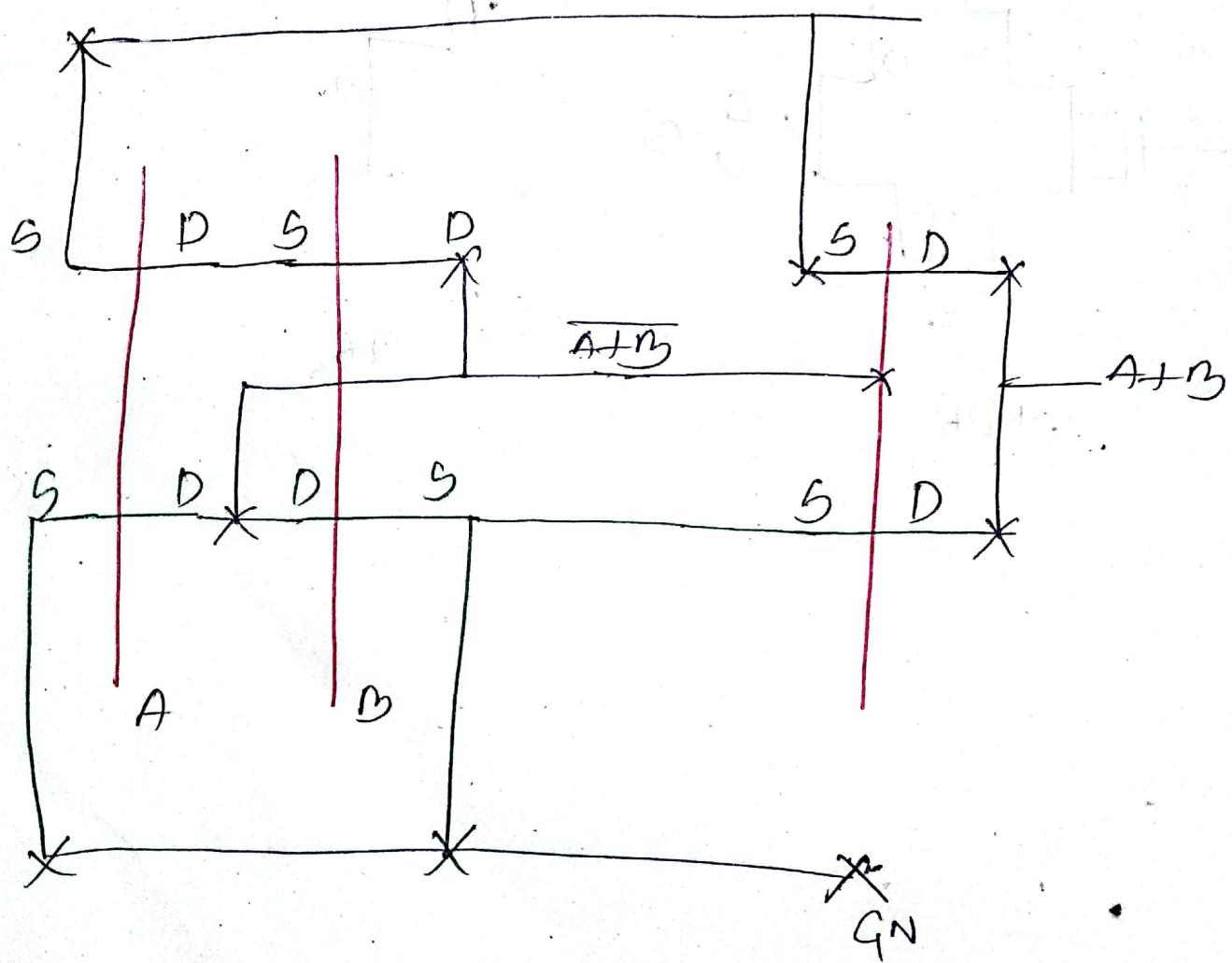
Green - n MOS

Blue - metal

black - p MOS

product  $\rightarrow$  parallel

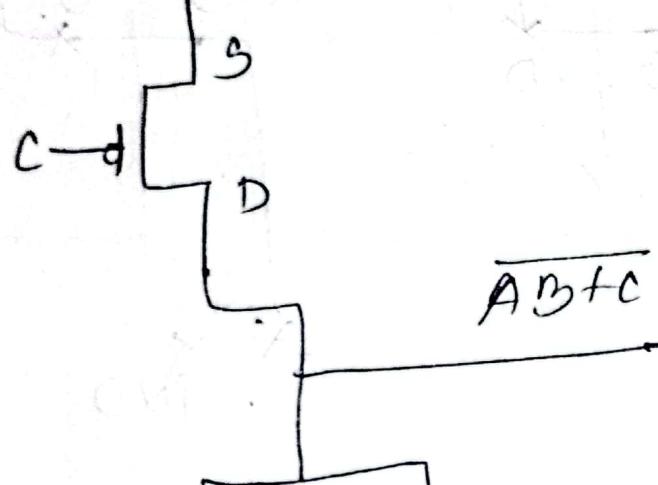
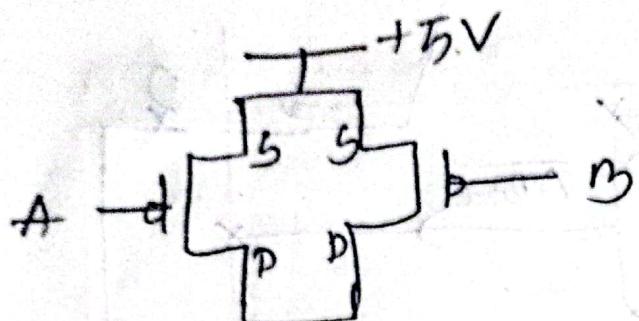
S, D  $\rightarrow$  series



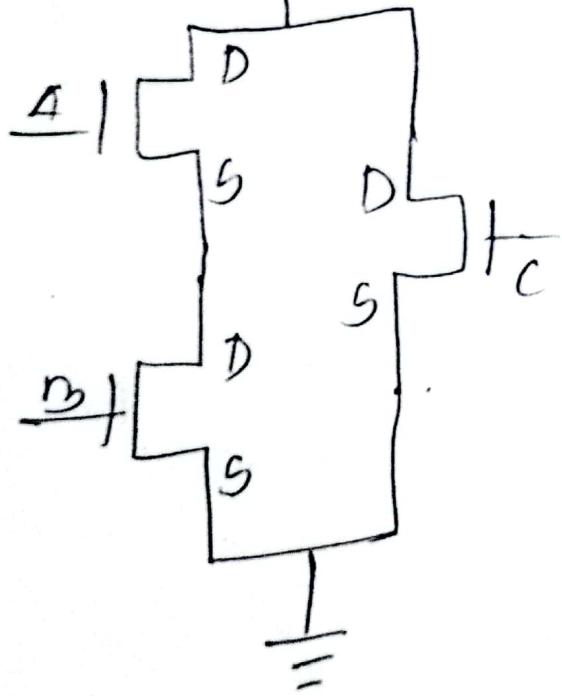
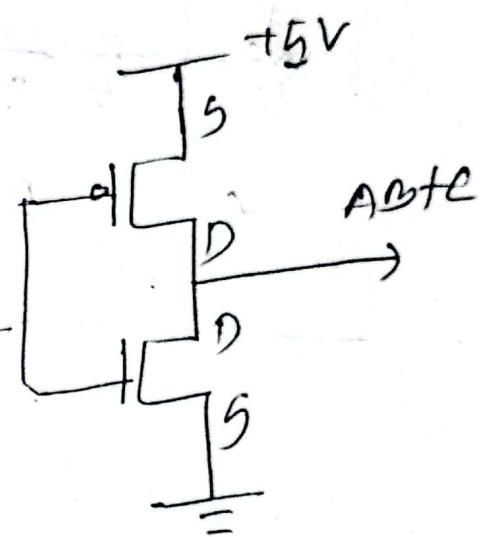
$$Y = (AB + C)$$

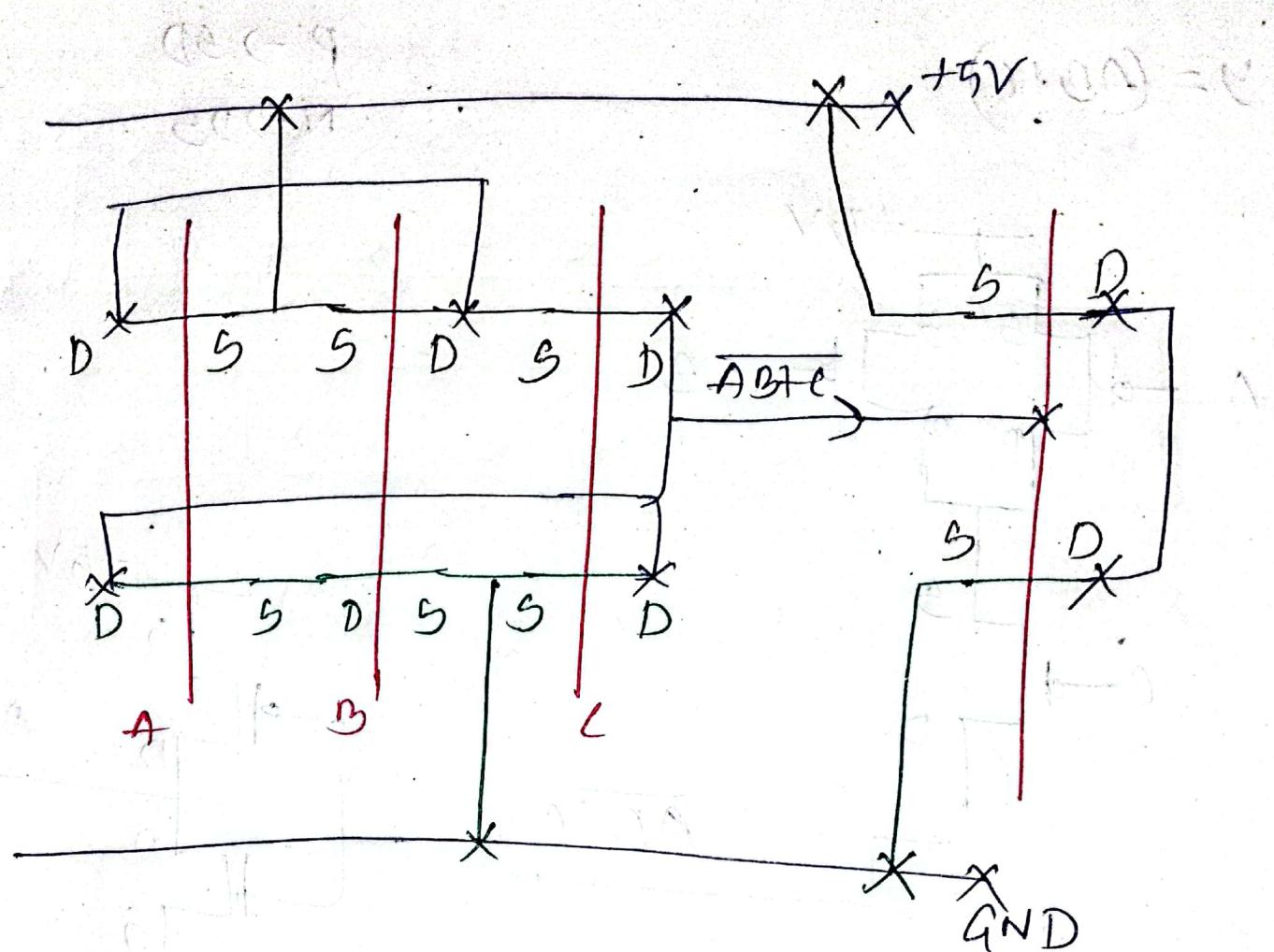
$$P \rightarrow SD$$

$$N \rightarrow DS$$

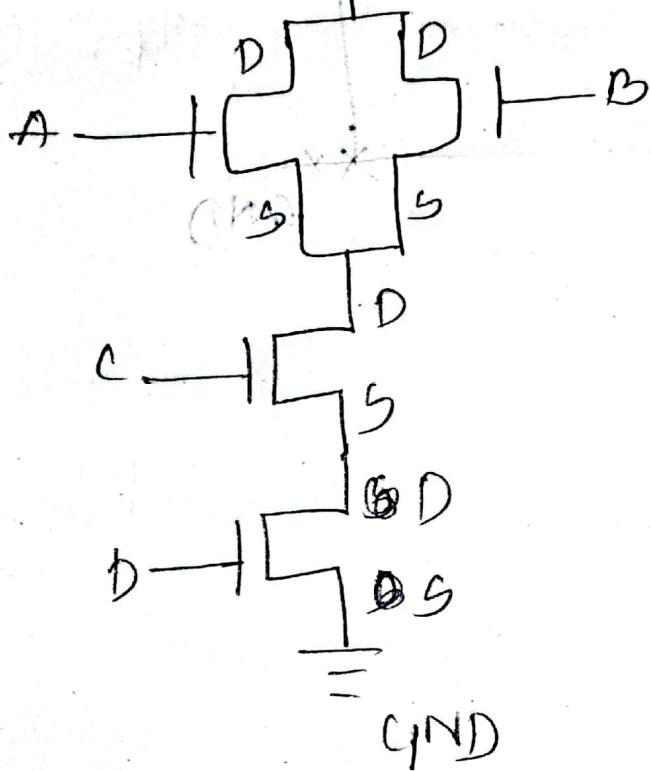
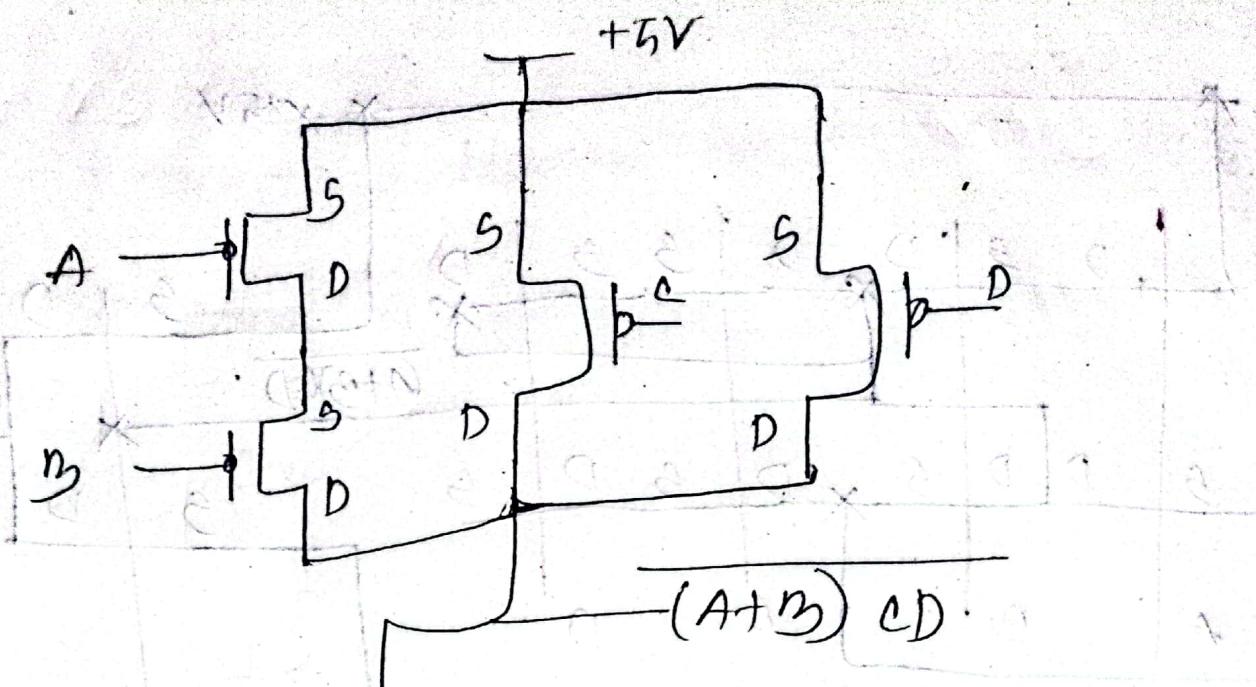


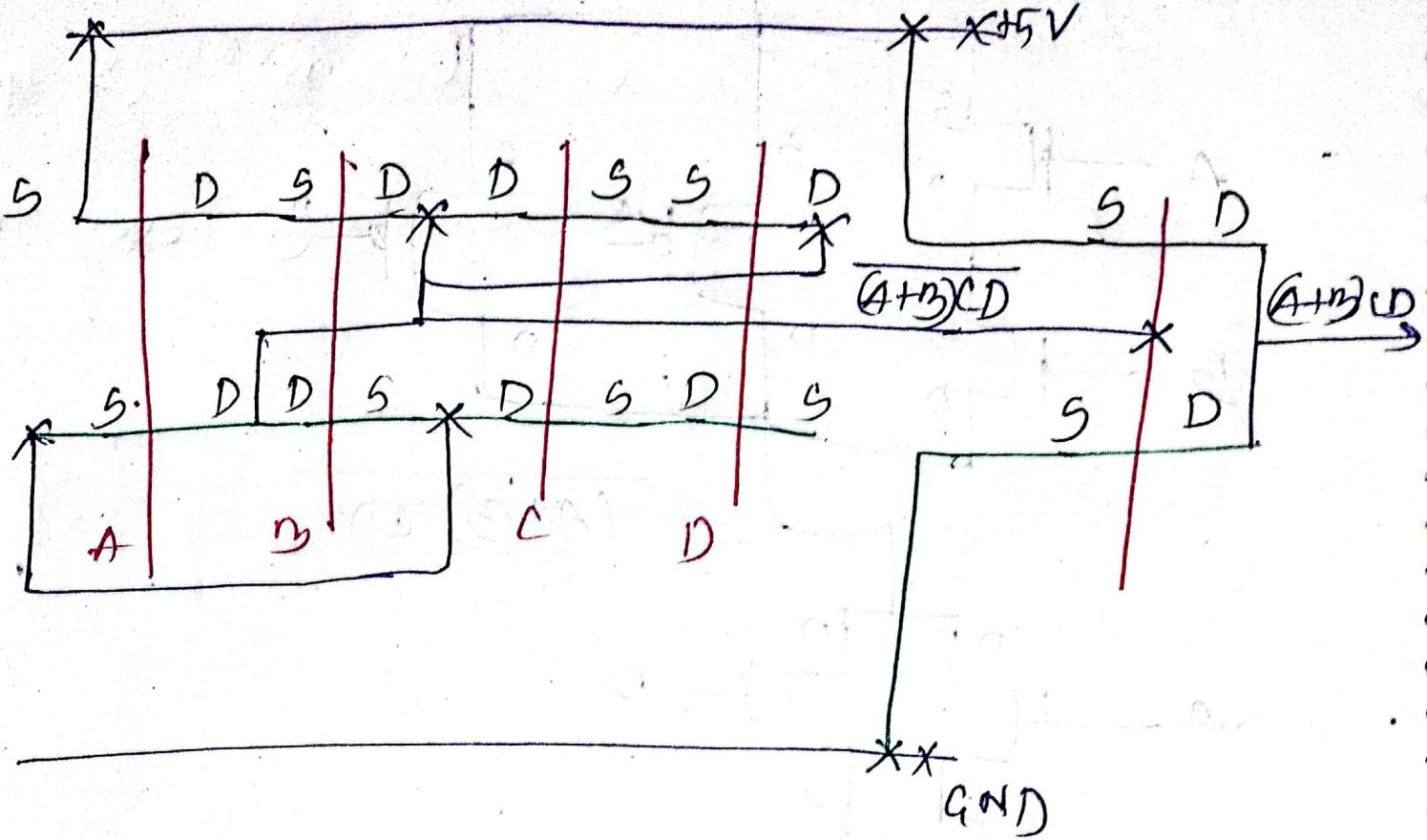
$$\overline{AB+C}$$



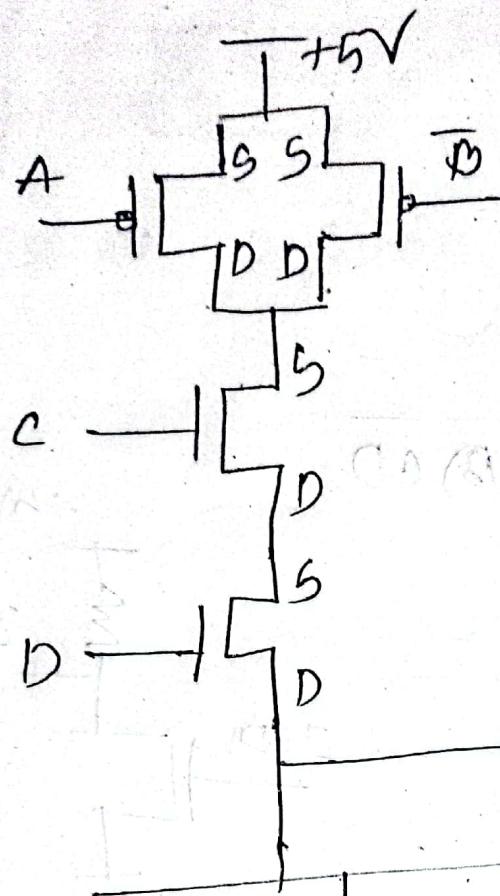


$$\gg Y = (A+B)CD$$



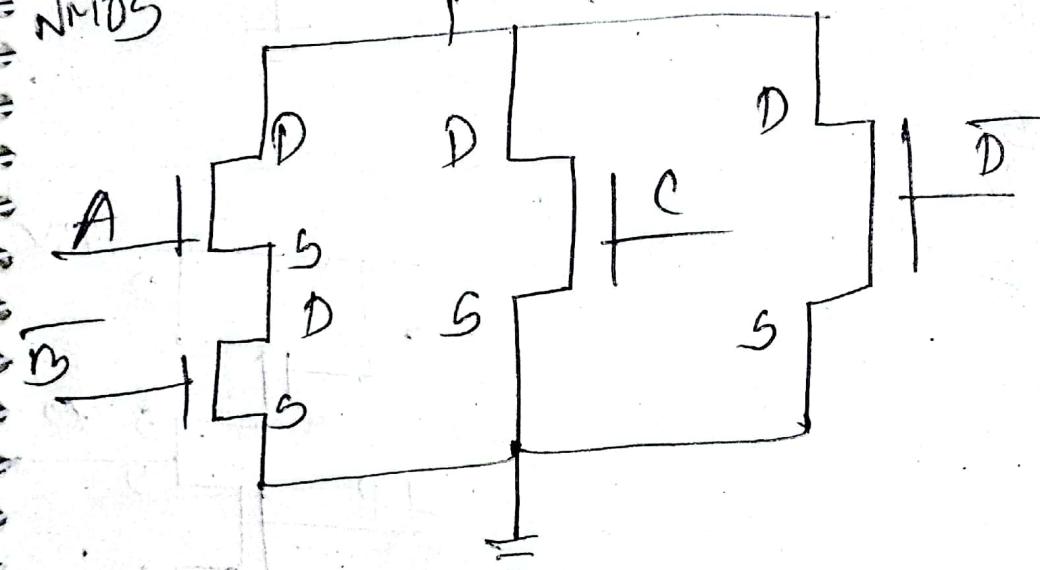


PMOS



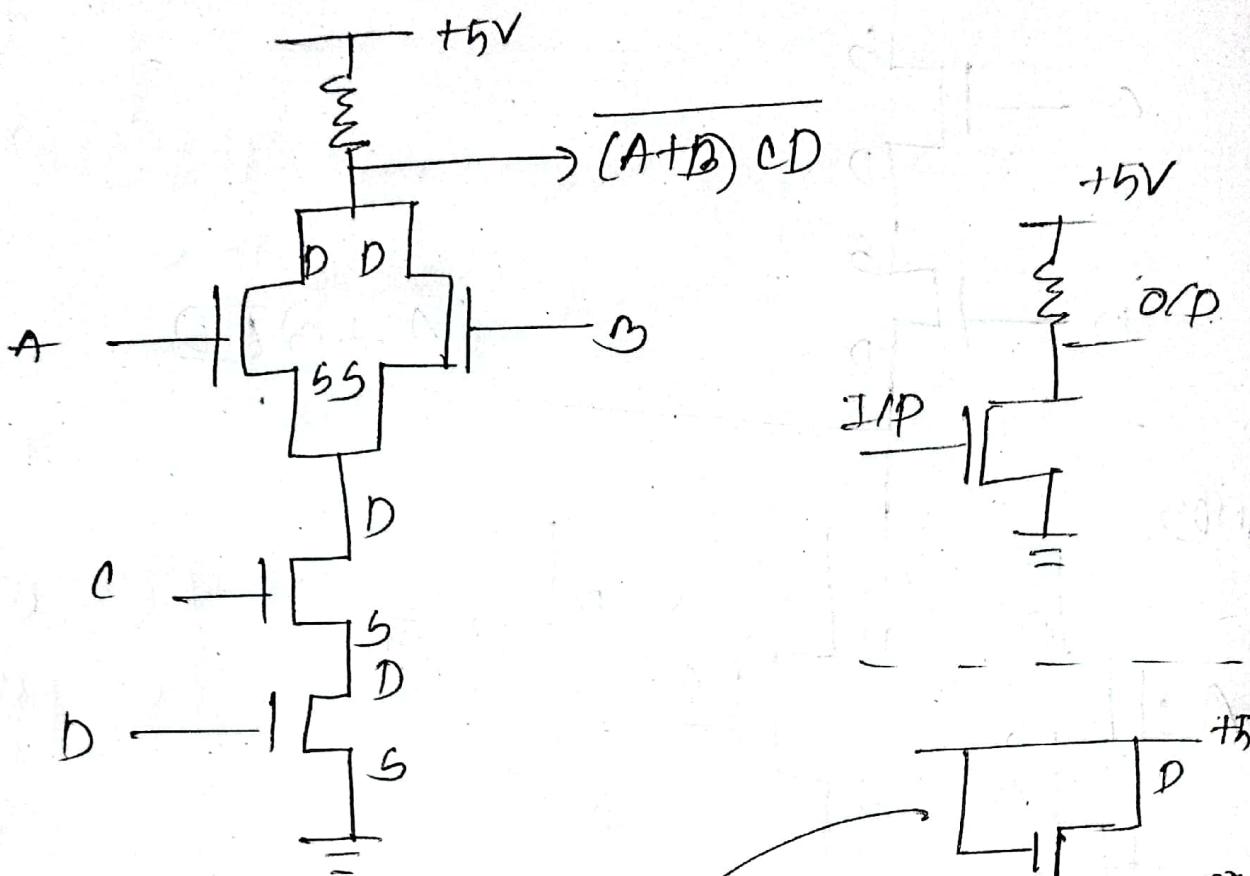
$$(\bar{A} + B)\bar{D}$$

NMOS



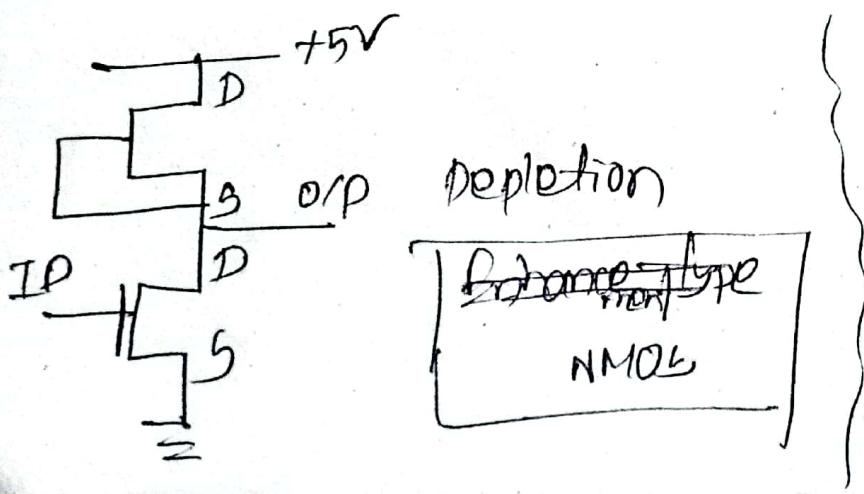
NMOS CKT

$$y = (A+B) \overline{CD}$$

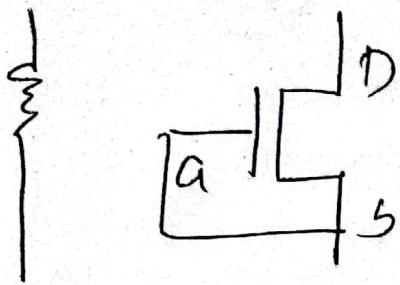


Enhancement  
~~Depletion~~ type  
 NMOS

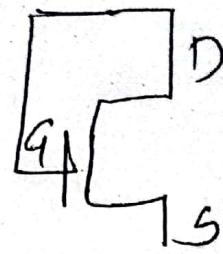
↑  
 depletion circuit  
 ഡോംഗ് മാ  
 on സ്റ്റോർജ്ജേറ്റ  
 നാലു തൃപ്പി നാലു  
 Head issue CO,



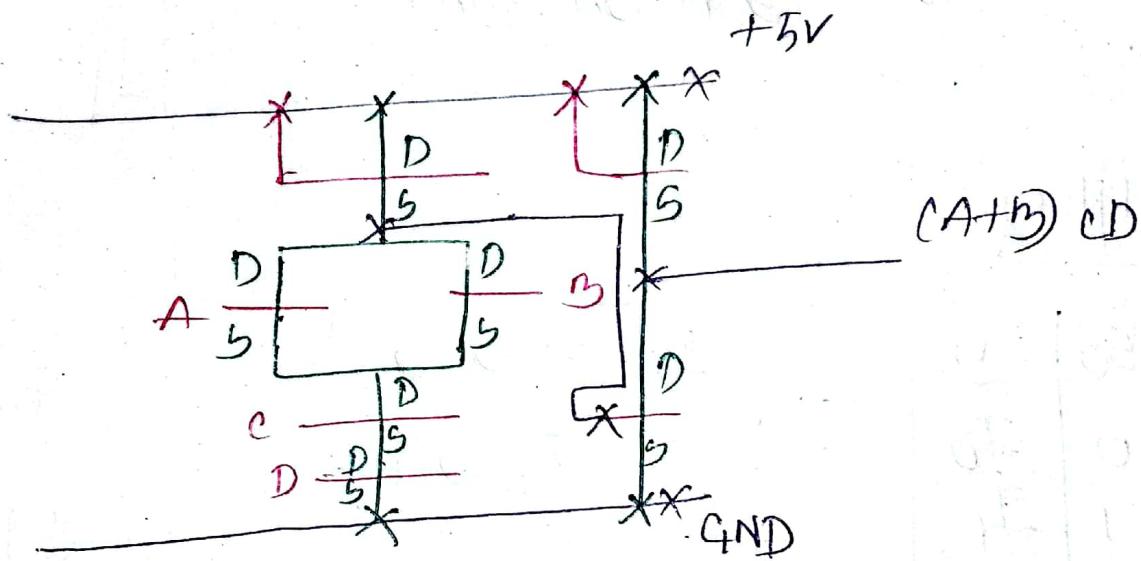
Depletion  
 Enhancement type  
 NMOS



Resistive Depletion

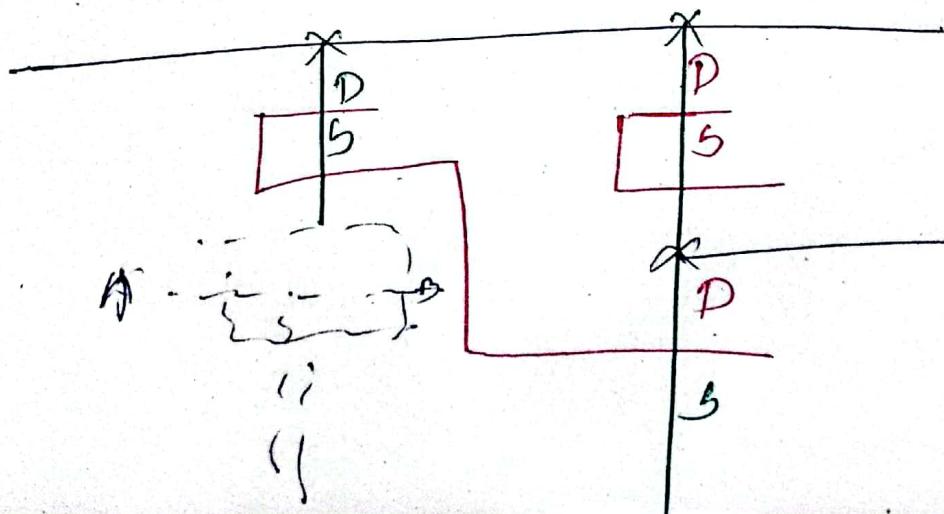


Enhancement

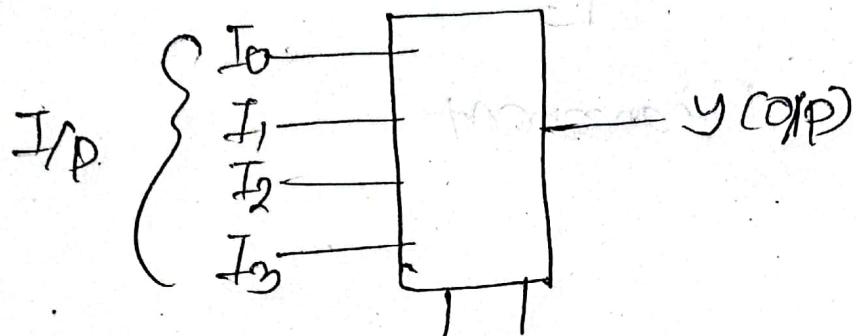


Enhancement

for Depletion



# Multiplexer



S<sub>0</sub>, S<sub>1</sub> (Selection pin)

Truth table

S <sub>1</sub>	S <sub>0</sub>	y
0	0	I <sub>0</sub>
0	1	I <sub>1</sub>
1	0	I <sub>2</sub>
1	1	I <sub>3</sub>

$$y_1 = \bar{s}_1 s_0 I_0 +$$

$$\bar{s}_1 s_0 I_1 +$$

$$s_1 \bar{s}_0 I_2 +$$

$$s_1 s_0 I_3$$

25 Feb, 2024

$S_1 \ S_0 \ \bar{S}$

4x1 MUX

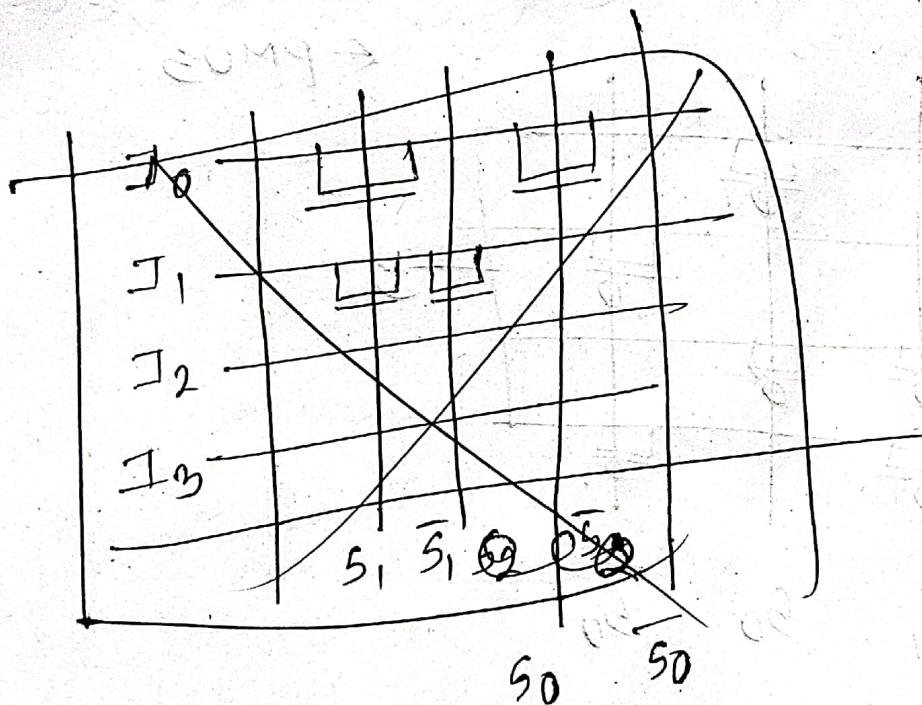
0 0  $I_0$

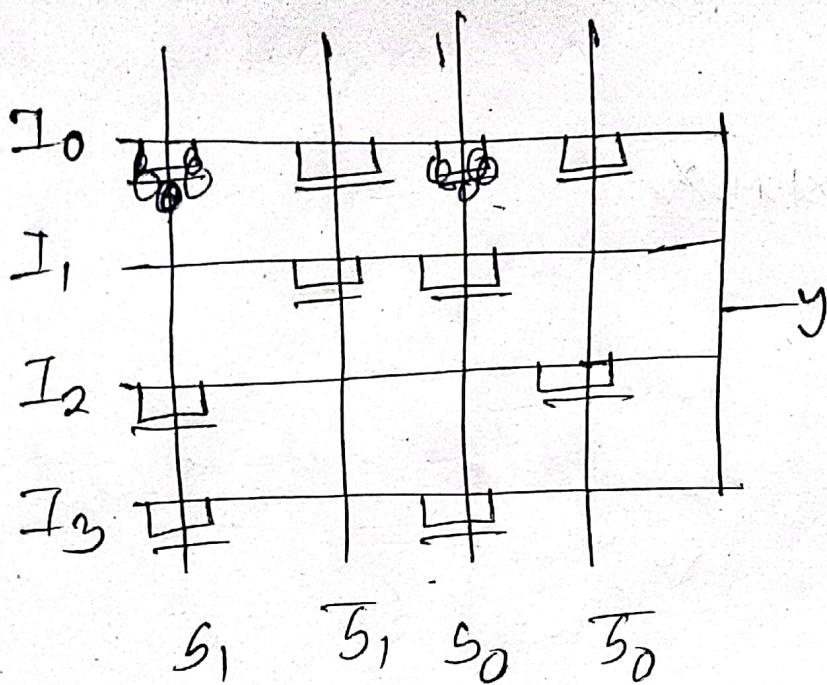
0 1  $I_1$

1 0  $I_2$

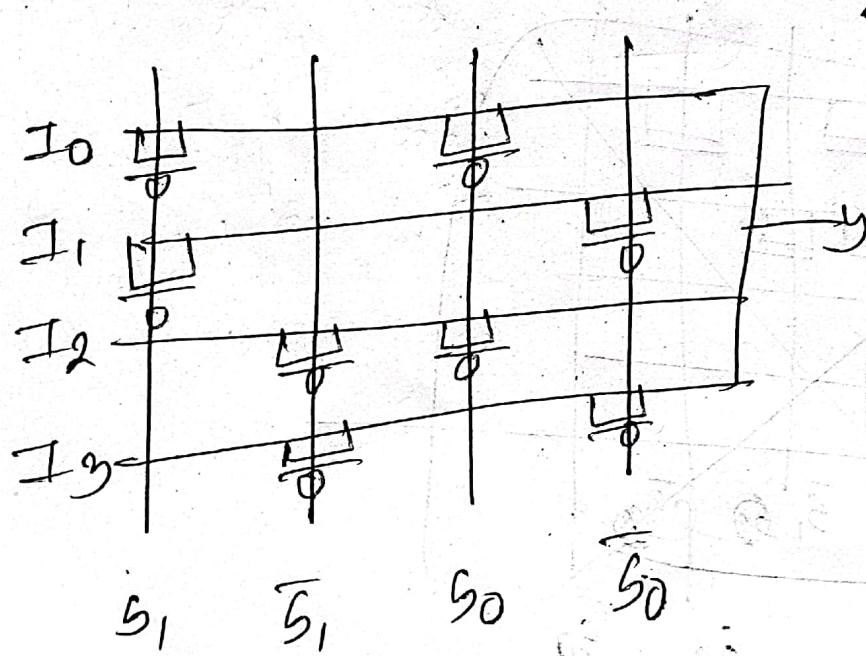
1 1  $I_3$

$$y = \overline{S_1} \overline{S_0} I_0 + \overline{S_1} S_0 I_1 + S_1 \overline{S_0} I_2 + S_1 S_0 I_3$$

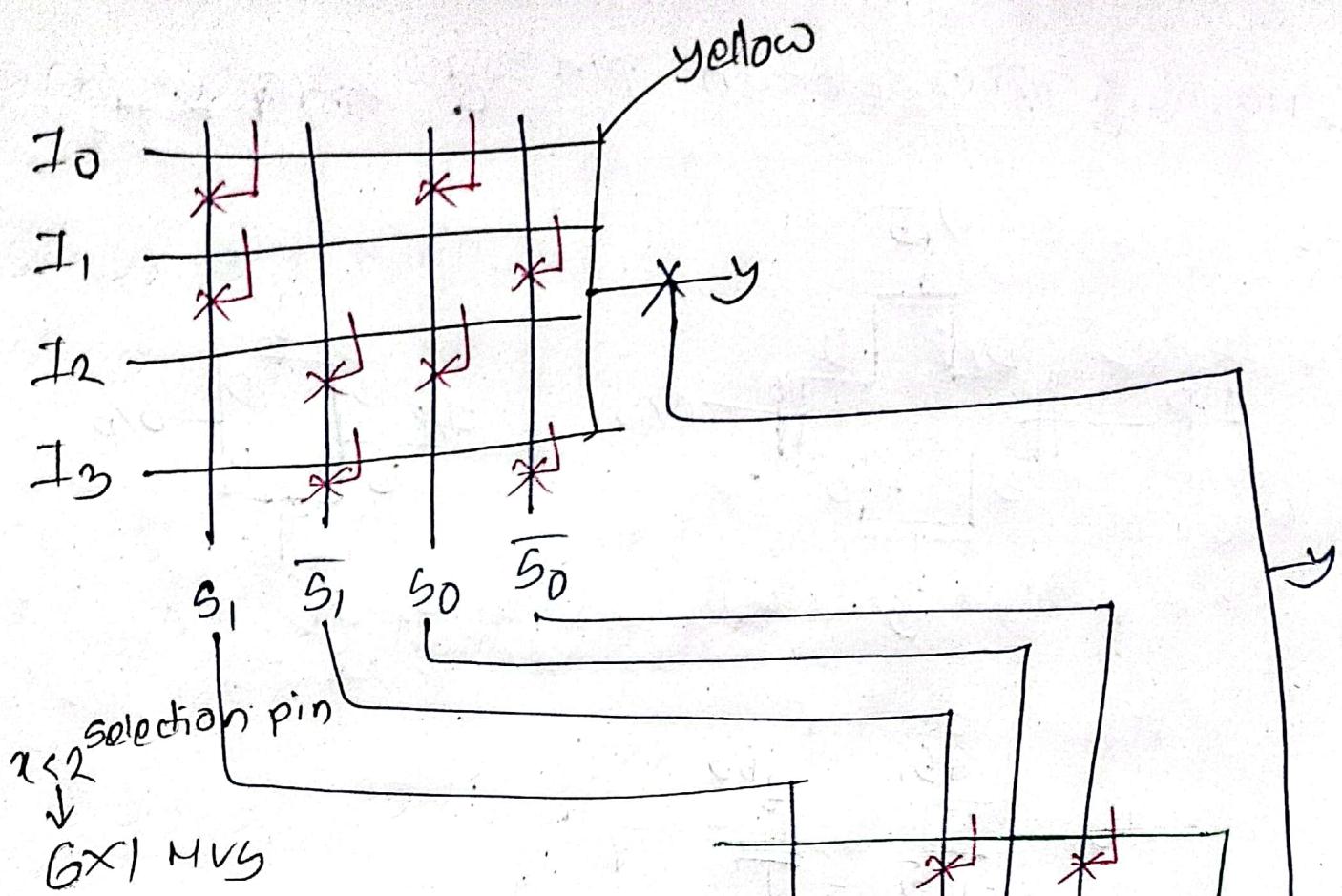




$\leftarrow$  NMOS



$\leftarrow$  PMOS



$S_2 \quad S_1 \quad S_0$

$I_0 \quad 0 \quad 0 \quad 0$

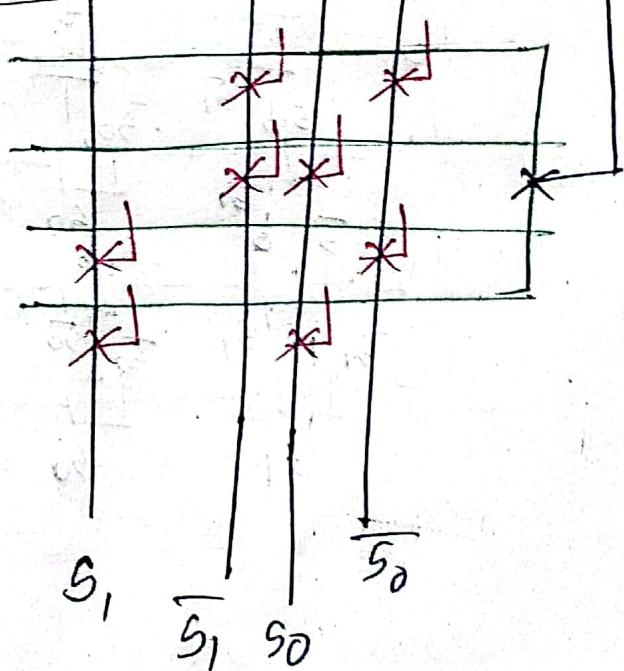
$I_1 \quad 0 \quad 0 \quad 1$

$I_2 \quad 0 \quad 1 \quad 0$

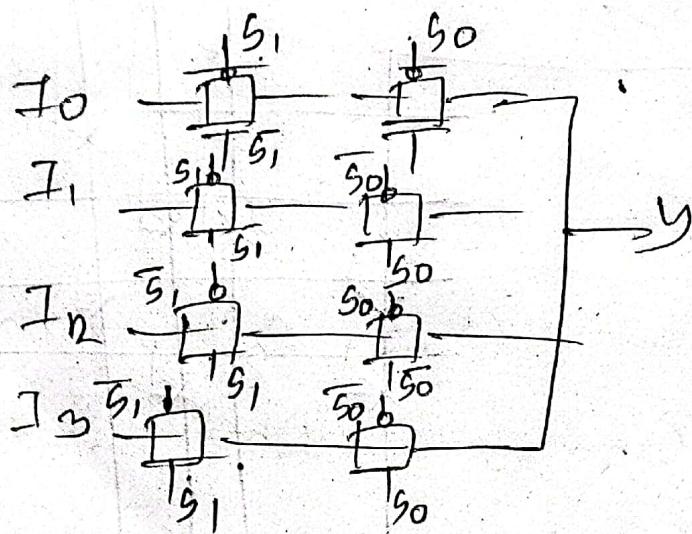
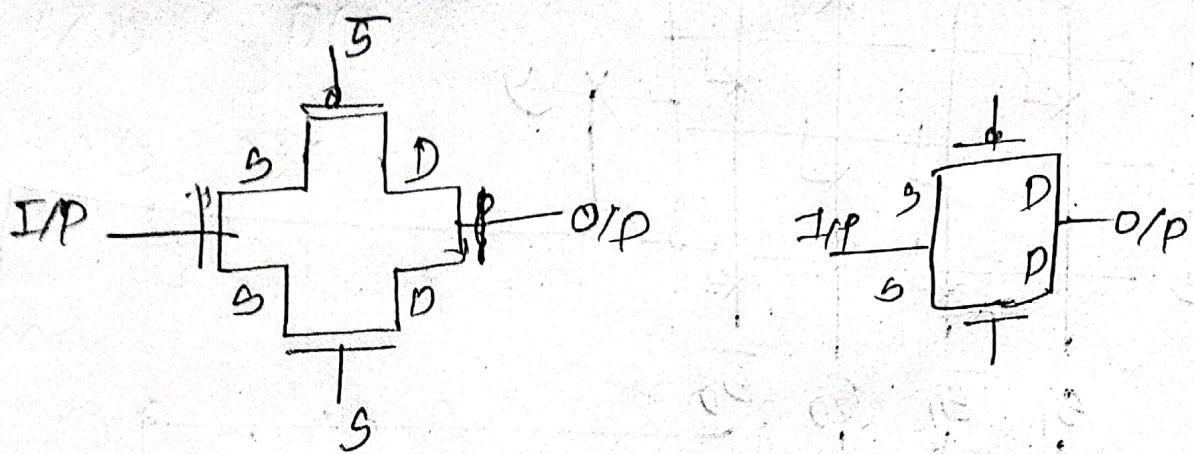
$I_3 \quad 0 \quad 1 \quad 1$

$I_4 \quad 1 \quad 0 \quad 0$

$I_5 \quad 1 \quad 0 \quad 1$



Cmos logic gate selection pin diagram



## Verilog Code

```

module space Name;
    input space ---;
    output space ---;
    and space Name(O/P,I/P);
endmodule

```

[ endmodule এস্ট  
 সেমি সেমি  
 অব না, যা কি  
 স্বল্প নেও  
 নেও হো ]

$$y = (A \bar{B} + C) D \bar{E}$$

```

module FunctionY(A,B,C,D,E,y);
    input A,B,C,D,E;
    output y;
    not notA(N1,A);
    and and1(N2,w1,B);
    or  or1(w3,w2,C);
    not notE(w4,E);
    and and2(y,w3,w4,D);
endmodule

```

$$y_1 = (A+B)\bar{C}D+E$$

$$y_2 = (\bar{A}\bar{B}+C)DE$$

$$y_3 = (AB+CD)\bar{E}$$

~~name of~~

module function (A, B, C, D, E; y<sub>1</sub>, y<sub>2</sub>, y<sub>3</sub>);

input A, B, C, D, E;

output y<sub>1</sub>, y<sub>2</sub>, y<sub>3</sub>;

or or1(w<sub>1</sub>, A, B);

not not1(w<sub>2</sub>, C);

and and1(w<sub>3</sub>, w<sub>1</sub>, w<sub>2</sub>, D);

or or2(y<sub>1</sub>, w<sub>3</sub>, E);

namd namd1(w<sub>4</sub>, A, B);

or or3(w<sub>5</sub>, w<sub>4</sub>, C);

not not E (w<sub>6</sub>, E);

and and2(y<sub>2</sub>, w<sub>5</sub>, w<sub>6</sub>, D);

and and3(w<sub>7</sub>, A, B);

and AND4 ( $\omega_8, \omega_1, D$ );

Full Adder

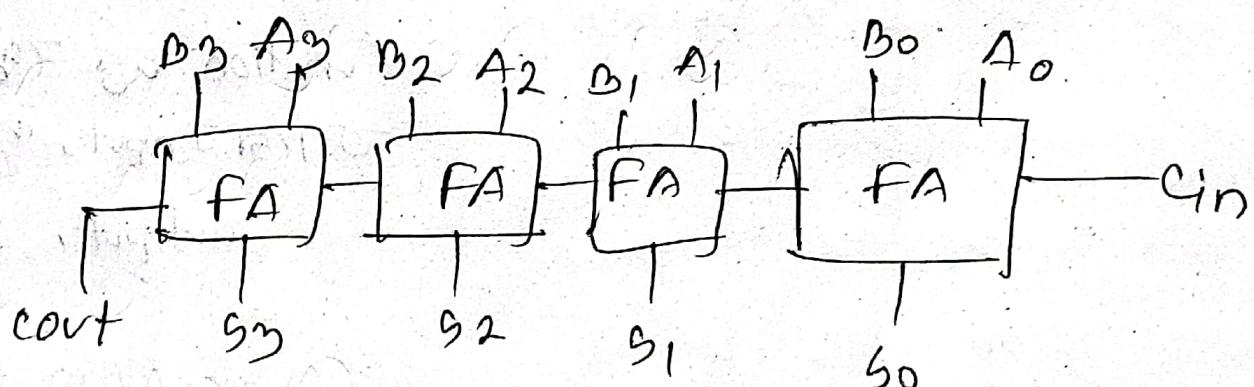
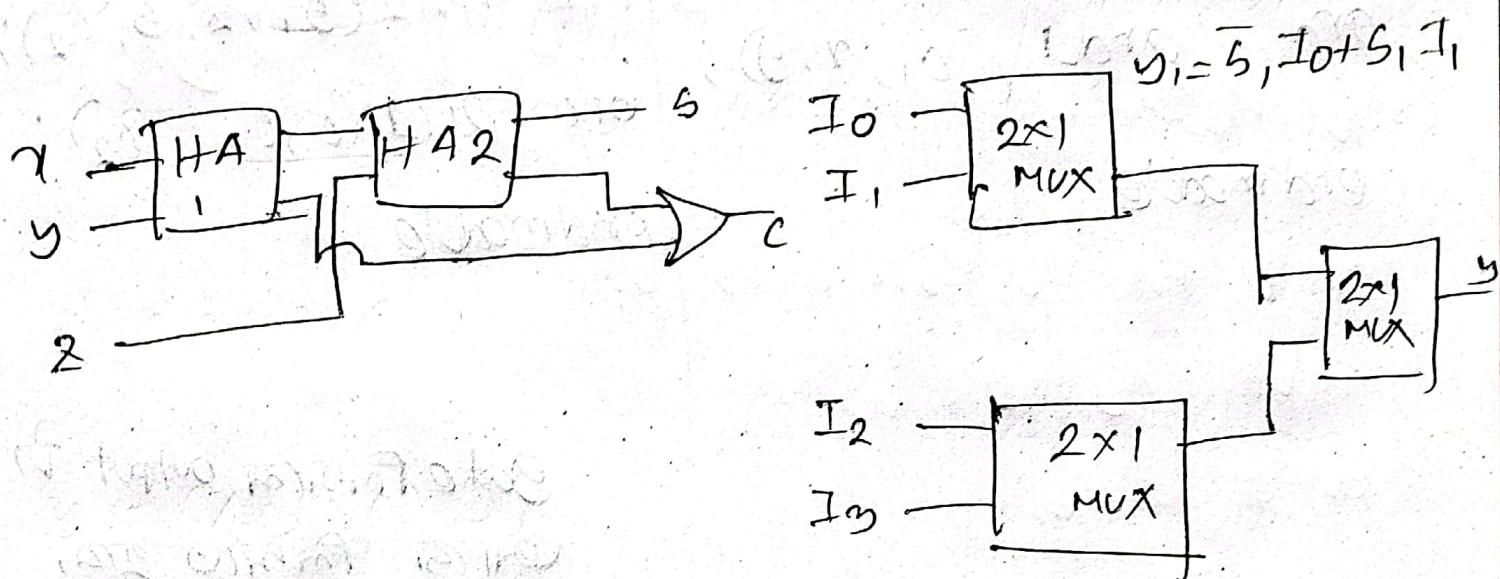
Subtractor

OR, OR4 ( $\omega_9, \omega_2, \omega_8$ );

Half Subtractor

and AND5 ( $y_3, \omega_9, \omega_6$ );

and module



```

module HA(x,y,s,c);
    input x,y;
    output s,c;
    xor . XOR1(s,x,y);
    and . AND1(c,x,y);
end module

```

```

module FA(x,y,z,s,c);
    input x,y,z;
    output s,c;
    HA HA1(x,y,s,c1);
    HA HA2(s1,z,s,c2);
    ORC ORC1(c,c1,c2);
endmodule

```

gate লিপিতে output

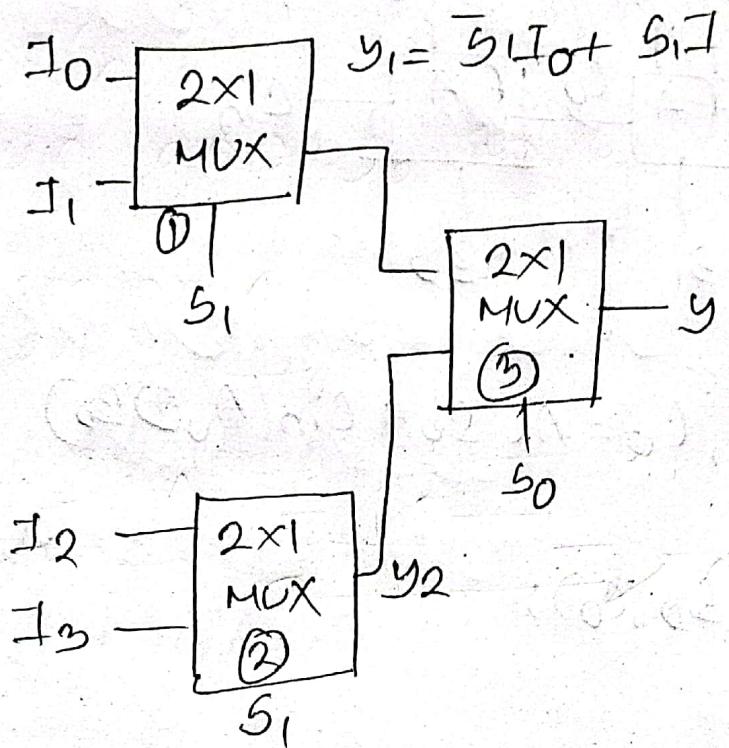
আজ লিপিতে

function র ক্ষেত্রে

আজ Input, এবং

Output,

28 Feb, 2024



Module 2x1 MUX ( $I_0, I_1, S_1, y_1$ );

Input  $I_0, I_1, S_1$ ;

Output  $y_1$ ;

not not  $S_1 (\omega_1, S_1)$ ;

and and1 ( $\omega_2, \omega_1, I_0$ );

any and2 ( $\omega_3, S_1, I_1$ );

or or1 ( $y_1, \omega_2, \omega_3$ );

end module

| module 4x1 MUX ( $I_0, I_1, I_2,$

$I_3, I_4, I_5, S_1, S_0, y$ );

| input  $I_0, I_1, I_2, I_3, S_1, S_0$ ;

| output  $y$ ;

| 2x1 MUX MUX1 ( $I_0, I_1, S_1, y_1$ );

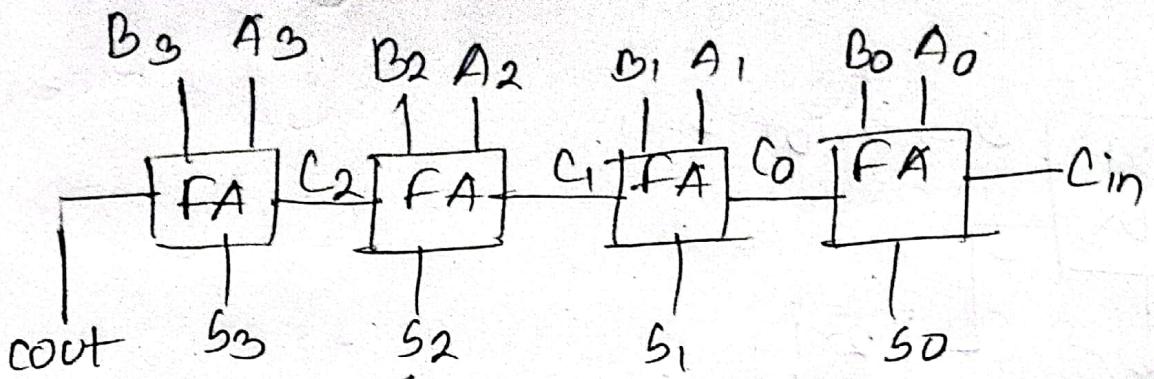
| 2x1 MUX MUX2 ( $I_2, I_3, S_1, y_2$ );

| 2x1 MUX MUX3 ( $y_1, y_2, S_0, y$ );

| end mod

| end module

# 4bit parallel adder



$$S_0 = A_0 \oplus B_0 \oplus C_{in}, \quad C_0 = A_0 B_0 + C_{in}(A_0 \oplus B_0)$$

module FA( $A_0, B_0, C_{in}, S_0, C_0$ );

input  $A_0, B_0, C_{in}$ ;

output  $S_0, C_0$ ;

not  $xor1(S_0, A_0, B_0, C_{in})$ ;

and  $and1(C_0, A_0, B_0)$ ;

$xorc$   $xorc2(C_0, A_0, B_0)$ ;

and  $and2(C_0, C_0, C_{in})$ ;

or  $or1(C_0, A_0, B_0)$ ;

end module

modulo PFA( A<sub>0</sub>, B<sub>0</sub>, A<sub>1</sub>, B<sub>1</sub>, A<sub>2</sub>, B<sub>2</sub>, A<sub>3</sub>, B<sub>3</sub>, Cin, Cout,  
S<sub>0</sub>, S<sub>1</sub>, S<sub>2</sub>, S<sub>3</sub>);

input A<sub>0</sub>, B<sub>0</sub>, A<sub>1</sub>, B<sub>1</sub>, A<sub>2</sub>, B<sub>2</sub>, A<sub>3</sub>, B<sub>3</sub>, Cin;  
output S<sub>0</sub>, S<sub>1</sub>, S<sub>2</sub>, S<sub>3</sub>, Cout;

FA FA1(A<sub>0</sub>, B<sub>0</sub>, Cin, C<sub>0</sub>, S<sub>0</sub>);

FA FA2(A<sub>1</sub>, B<sub>1</sub>, C<sub>0</sub>, C<sub>1</sub>, S<sub>1</sub>);

FA FA2(A<sub>2</sub>, B<sub>2</sub>, C<sub>1</sub>, C<sub>2</sub>, S<sub>2</sub>);

FA FA4(A<sub>3</sub>, B<sub>3</sub>, C<sub>2</sub>, Cout, S<sub>3</sub>);

endmodule

### Full Adder

#### Truth Table

x	y	z	Carry	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

$$\text{Sum} = \bar{x}\bar{y}z + \bar{x}y\bar{z} + x\bar{y}z + xy\bar{z}$$

$$= x \oplus y \oplus z$$

$$\text{Carry} = \bar{x}yz + x\bar{y}z + xy\bar{z} + xyz$$

$$+xyz$$

$$= xy + z(x \oplus y)$$

Let,  $H = x \oplus y$

Sum =  $H \oplus z$

Carry =  $xy + z + 1$

$x = y$	$0 \oplus 0 \rightarrow 0$
$Sum = H \oplus z$	$1 \oplus 0 \rightarrow 1$
$= 0 \oplus z$	
$= z$	

Carry =  $xy + z \cdot 0 = xy - 1 \cdot x = x$

$x \neq y, H = 0 \oplus 1 = 1$

$= 1 \oplus 0 = 1$

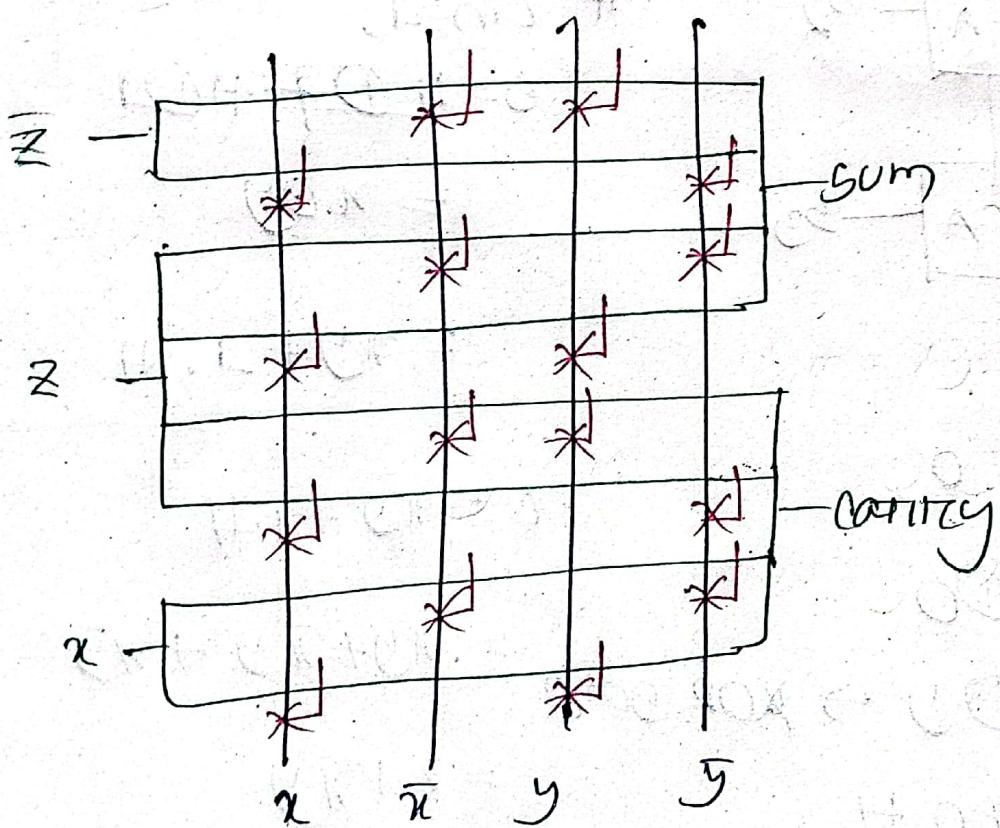
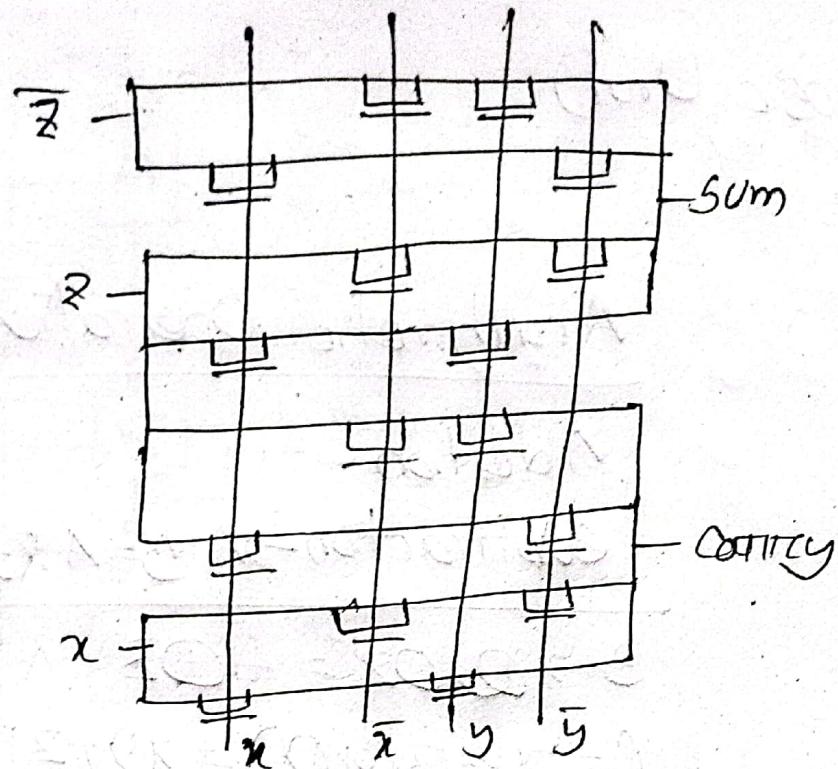
Sum =  $H \oplus z = 1 \oplus z = z$

Carry =  $xy + z \cdot 1$

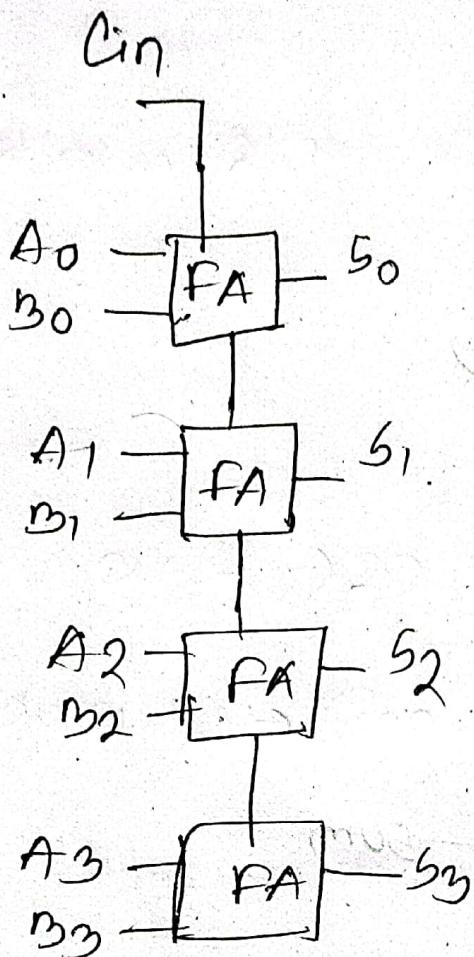
$= xy + z = z$

Modified Table

$x$	$y$	Carry	Sum
0	0	$x$	$z$
0	1	$z$	$z$
1	0	$z$	$z$
1	1	$x$	$z$



# ALU (Arithmetic Logic Unit)



## Arithmetic Operation

Addition -

$$\text{Subtraction} \rightarrow A - B = A + \overline{B} + 1$$

$$S = x \oplus y \oplus z = x \oplus z$$

$$C = xy + z(x \oplus y) = xy + z \cdot H$$

If Cin = 1,

$$S = \cancel{x \oplus z} + x \oplus 1$$

$$= x \oplus y$$

$$= xy + 1 \cdot H$$

If Cin = 0,

$$C = xy + 0 \cdot H$$

$$S = H \oplus 0$$

$$= x \oplus y + \overline{x}y + xy$$

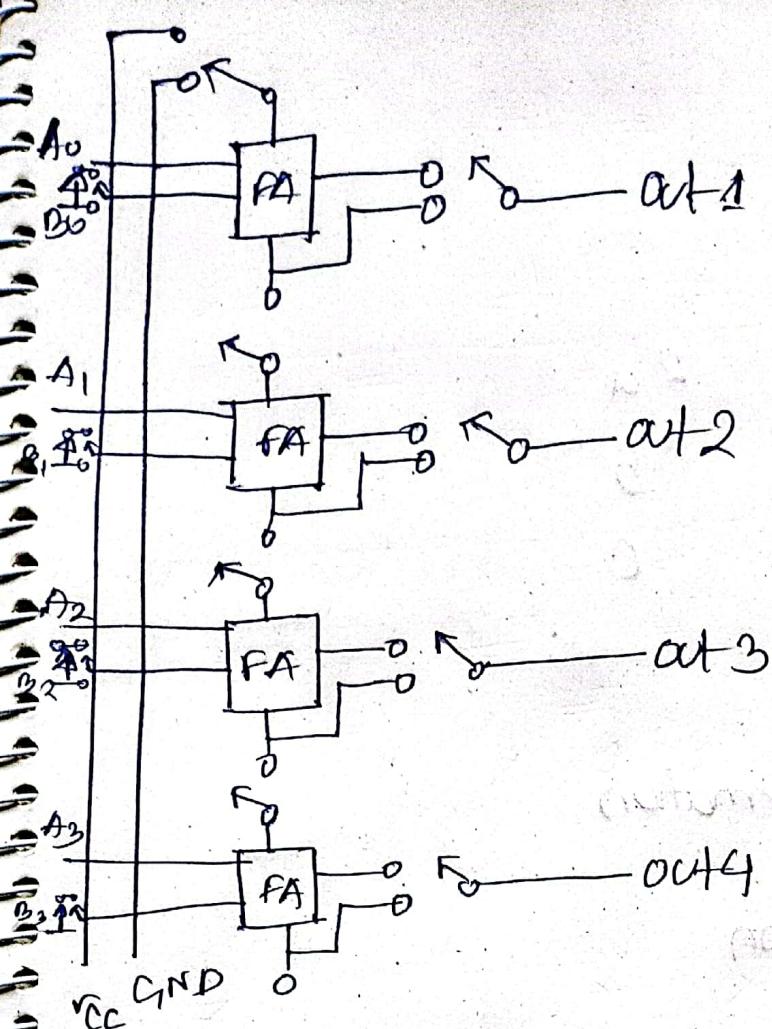
$$= x \oplus y \rightarrow \text{XOR gate}$$

$$= x + \overline{x}y$$

$$C = xy + 0 \cdot H$$

$$= xy \rightarrow \text{AND gate}$$

$$= x \cdot y \rightarrow \text{OR gate}$$



4-bit ALU