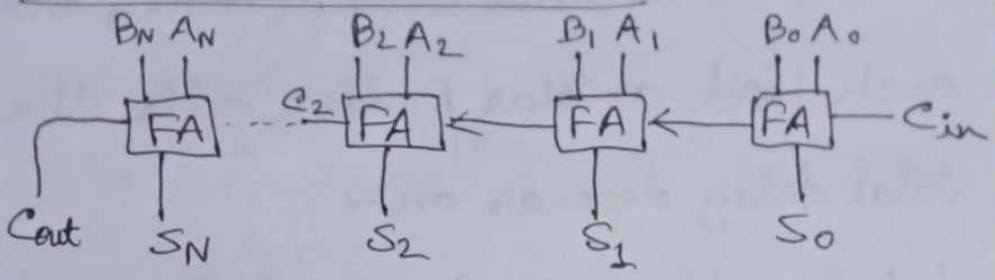
VLSI

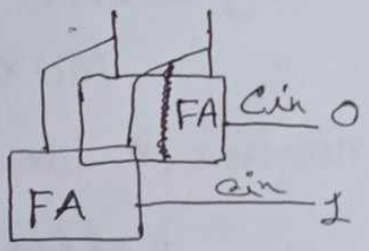
Carry Select Adder:



n-bit ripple carry adder

If we consider a n-bit ripple carry adder and K_1 is the delay for a FA.

Total delay, $T = nK_1$



If we consider a n-bit carry select adder is divided into M blocks and each block contains P adder cells the total delay depends on—

1. Delay through first block.
2. Delay through the MUX.

So, total delay,

$$T = Pk_1 + (M-1)k_2 \quad \ldots (2)$$

Where, k_1 is the delay for FA

k_2 " " " " MUX

M " " number of blocks

P " " " " adder cells in a block.

$n = 20, k_1 = 1$ sec, $P = 2$

∴ Paraller adder $= nk_1 = 20 \times 1 = 20$ sec

20-bit carry select adder -

$m = (20/2) = 10$

$\therefore T = Pk_1 + (m-1)k_2$

$= 2 \times 1 + (10-1)1$

$= 2 + 9$

$= 11$ sec.

VLSI

Programmable Logic Array (PLA)

AND-OR PLA

NOR-NOR PLA

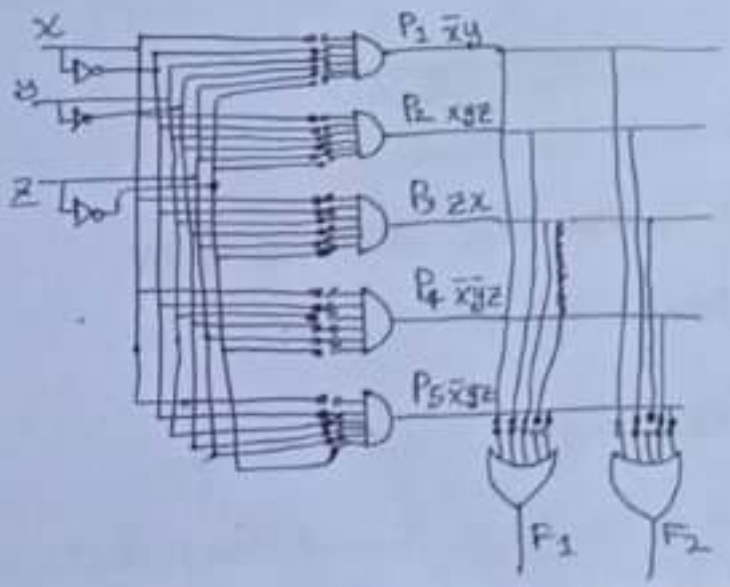
AND-OR PLA

$F_1 = \bar{x}y + xyz + z\bar{x} = P_1 + P_2 + P_3$

$F_2 = xyz + \bar{x}\bar{y}z + \bar{x}\bar{z}y = P_2 + P_4 + P_5$

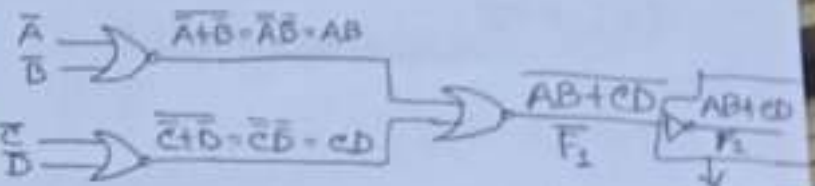
Size of PLA := $V \times P \times Z$ → number of output; P → number of product

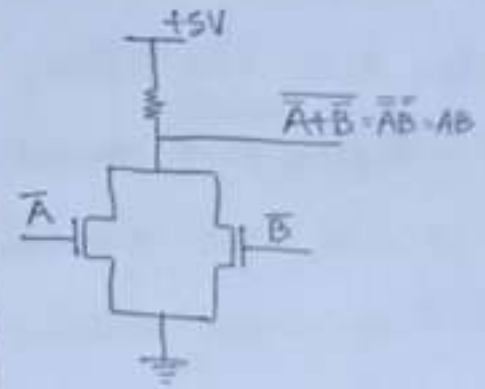
$3 \times 5 \times 2$



NOR-NOR:

$AB + \bar{C}\bar{D}$





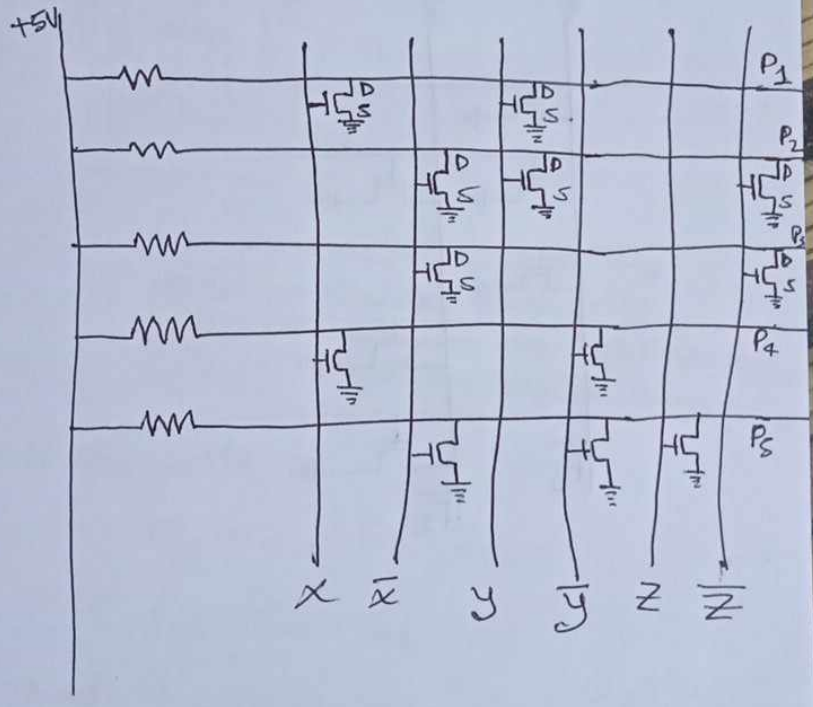
VLSI

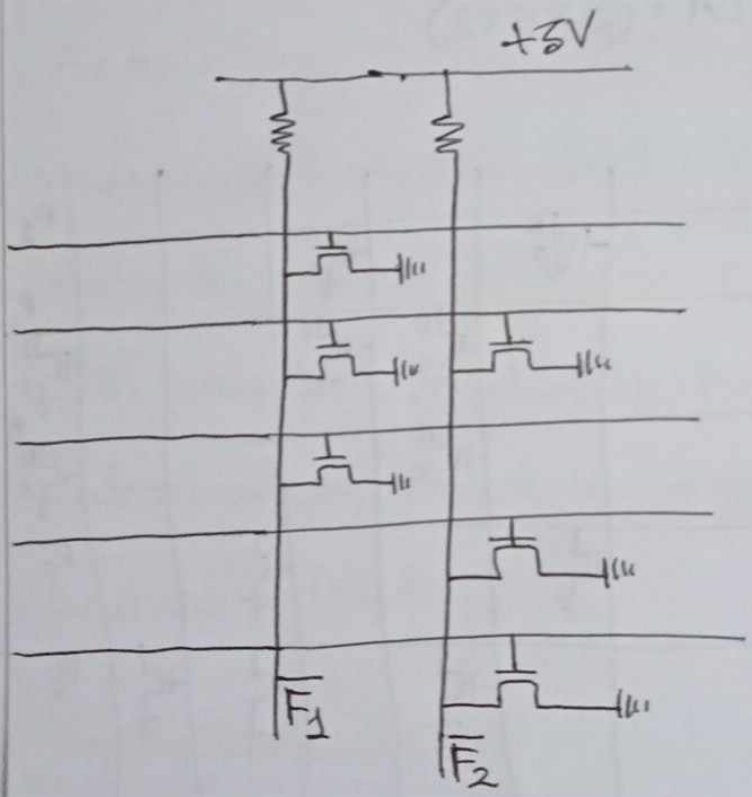
NOR-NOR PLA

$F_1 = \bar{x}\bar{y} + x\bar{y}z + zx = P_1 + P_2 + P_3$

$F_2 = x\bar{y}z + \bar{x}y + xy\bar{z} = P_2 + P_4 + P_5$

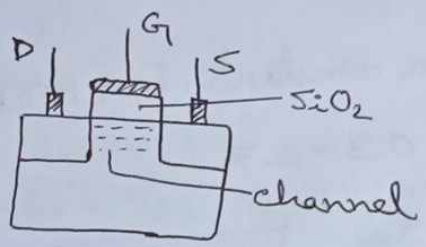
size of PLA = (3x5x2)

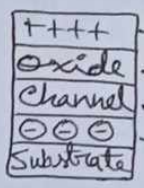



+5V
F1
F2

Threshold Voltage

Threshold voltage is the minimum gate voltage that is needed to create a conducting path between drain and source.





→ metal charge Q_g
→ Oxide charge Q_{ss}
→ Inversion channel charge Q_c
→ Depletion region charge Q_d

We can write,

$$Q_g + Q_{ss} = Q_c + Q_d$$

$$Q_g = Q_c + Q_d - Q_{ss}$$

Threshold voltage, $V_t = \frac{Q_g}{C_g} = \frac{Q_c + Q_d - Q_{ss}}{C_g}$

Where, C_g is the gate capacitance

Body Effect:

If we consider V_{to} is the threshold voltage when $V_{SB}=0$, then $V_{to}=\frac{Q_c+Q_d-Q_{ss}}{C_g}$

If $V_{SB}\neq 0$ then,

$$V_t = V_{to} + \gamma\sqrt{V_{SB}}$$

Where γ is a constant. For MOSFET,

$$\gamma = 0.3 \sim 0.7$$

$$\gamma = \frac{t_{ox}}{\epsilon_{ox}}\sqrt{2q\epsilon_{si}N_A}$$

t_{ox} = thickness of O_2

q = charge of an electron

ϵ_{ox} = Oxide premitivity

ϵ_{si} = Premitivity of Silicon

N_A = Doping concentration

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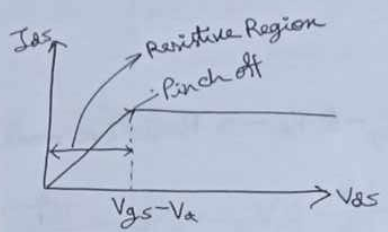
I-V characteristics of MOSFET:



For NMOS

If $V_{ds} < V_{gs} - V_t$ → Resistive mode

$$I_{ds} = \frac{\epsilon M_n}{D}\frac{W_n}{L_n}\left\{(V_{gs}-V_t)V_{ds} - \frac{V_{ds}^2}{2}\right\}$$

If $V_{ds} \geq V_{gs} - V_t$ → Saturation mode

$$I_{ds} = \frac{\epsilon M_n}{2D}\frac{W_n}{L_n}\left\{(V_{gs}-V_t)^2\right\}$$

Where,

D → Depth of O_2

M_n → Mobility of Electron

M_p → Mobility of hole

ϵ → Permittivity

$W_p/W_n \rightarrow$ channel width

$L_p/L_n \rightarrow$ channel length

For PMOS:

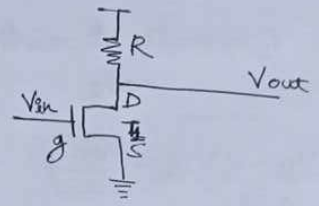
If $V_{sd} < V_{sg} - V_t \rightarrow$ Resistive mode

$$I_{sd} = \frac{\in M_p}{D} \frac{W_p}{L_p} \left\{ (V_{sg} - V_t) V_{sd} - \frac{V_{sd}^2}{2} \right\}$$

If, $V_{sd} \geq V_{sg} - V_t \rightarrow$ Saturation mode

$$I_{sd} = \frac{\in M_p}{2D} \frac{W_p}{L_p} \left\{ (V_{sg} - V_t)^2 \right\}$$

NMOS inverter with resistive load



Let, $\frac{\in M_n}{D} = 30 \mu A/V^2$

$\frac{W}{L} = 1$

$V_t = 1V$

If $V_{in} = 0V$, $T_1 \rightarrow$ OFF

$V_{out} = V_{DD} - V_R$

If $V_{in} = 5V$, $T_1 \rightarrow$ ON

$V_{out} = \frac{1}{3} V_t = 0.33V$

$V_{ds} = V_d - V_s = 0.33 - 0 = 0.33V$

$V_{gs} = V_g - V_s = 5 - 0 = 5V$

$V_t = 1V$

$V_{gs} - V_t = 5 - 1 = 4V$

$\therefore V_{DS} < V_{gs} - V_t$, T_1 operates at resistive mode

$$I_{ds} = \frac{\epsilon M_n}{D} \frac{W_n}{L_n} \left\{ (V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right\}$$

$$= 30 \times 1 \left((4) \times 0.33 - \frac{0.33^2}{2} \right)$$

$$= 37.96 \mu A$$

$$\therefore R = \frac{V_{DD} - V_{out}}{I_{ds}} = \frac{5 - 0.33}{37.96 \times 10^{-6}} = 123024 \Omega$$

$$= 123 k\Omega$$

Ex:

$VDD = 3V$

$\frac{\epsilon M_n}{D} = 50 \mu A/V^2$

$\frac{W}{L} = 4$

$V_t = 0.75V$

$V_{ds} = 0.2V$

$V_{in} = 3.5V$

$R = ?$

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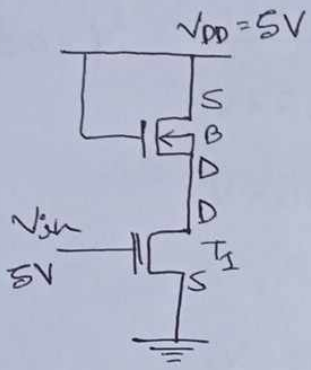
NMOS inverter with Enhancement type Load:



$V_{in}=0$, $T_1 \rightarrow$ OFF

$T_2 \rightarrow$ Always on

$V_{out} = V_{DD} - V_{t2}$

$V_{out} = V_{DD} - (V_{t0} + \gamma\sqrt{V_{SB}})$

এই টার্মটি → Voltage ↓ 0

$= 5 - (1 + 0.5\sqrt{V_{out}})$

$= 5 - 1 - 0.5\sqrt{V_{out}}$

$= 4 - 0.5\sqrt{V_{out}}$

$2V_{out} = 8 - \sqrt{V_{out}}$

$\Rightarrow \sqrt{V_{out}} = 8 - 2V_{out}$

$\Rightarrow V_{out} = 64 - 32V_{out} + 4V_{out}$

$\Rightarrow 4V_{out} - 33V_{out} + 64 = 0$

$\Rightarrow V_{out} = 3.1V_{out}$ or $3.12V$

$\therefore V_{out} = 3.12V$

$V_{in} = 5V$, T_1 and T_2 both are on

$$V_{out} = \frac{1}{3} V_t = 0.33V$$

$V_{t_0} = 1V$

$\gamma = 0.5$

For T_1

$V_{DS} = 0.33V$

$V_{gs} = 5V$

$V_{t_1} = 1V$ } 4V

$V_{DS} \leq V_{gs} - V_{t_1}$ → T_1 operates at Resistive Mode

For T_2

$V_{DS} = 4.67V$

$V_{gs} = 4.67V$

$V_{t_2} =$

$V_{DS} > V_{gs} - V_{t_2}$

T_2 operates at Saturation mode

For both,

$$\frac{E\mu_n}{D} = 30\mu A/V^2$$

$V_{t_0} = 1V$

For T_1

$$V_{out} = V_{DD} - V_{t_1}$$

$$I_{ds_1} = \frac{E M_n}{D} \frac{W_1}{L_1} \left\{ (V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right\}$$

$$= 30 \frac{W_1}{L_1} \left\{ (4) 0.33 - \frac{0.33^2}{2} \right\}$$

$$= 30 \frac{W_1}{L_1} (1.26) = 37.96 \left(\frac{W_1}{L_1}\right) \mu A$$

$$I_{ds_2} = \frac{E M_n}{2D} \frac{W_2}{L_2} \left\{ (V_{gs} - V_{t_2})^2 \right\}$$

$$= \frac{E M_n}{2D} \frac{W_2}{L_2} \left\{ V_{gs} - (V_{t_0} + \gamma \sqrt{V_{SB}}) \right\}^2$$

$$= \frac{1}{2} \times 30 \frac{W_2}{L_2} \left\{ 4.67 - (1 + 0.5 \sqrt{\frac{37.96 \frac{W_1}{L_1}}{3.12}}) \right\}^2$$

$$= 15 \frac{W_2}{L_2} \left\{ 0.34 \frac{W_1}{L_1} \right\}$$

$$= 15 \frac{W_2}{L_2} (4.65)$$

$$= 116.49 \left(\frac{W_2}{L_2}\right) \mu A$$

$\frac{W}{L}$ এর value control করে আমরা current control করতে পারি।

$$\frac{W_1/L_1}{W_2/L_2} = \frac{116.49}{37.96} = 3.068 \cong 3$$

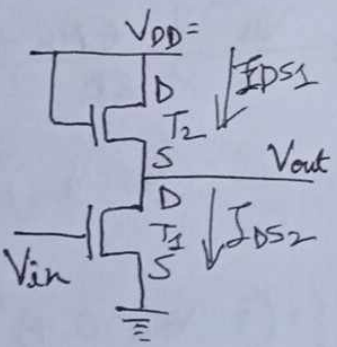
VLSI XM-25

A NMOS inverter with Enhancement type load is biased at $V_{DD}=3V$, The MOSFET parameter are $V_{t1}=V_{t2}=0.4V$

$\frac{EM_n}{D}=60\mu A/V^2$, $\frac{W_1}{L_1}=16$, $\frac{W_2}{L_2}=2$.

Find the output voltage when,

i) $V_{in}=0V$, ii) 2.6V, also calculate the power dissipated in the inverter when $V_{in}=2.6V$



i) $V_{in}=0V$

$V_{out}=V_{DD}-V_{t2}$

$=3-0.4$

≈ 2.6

ii) $V_{in}=2.6V$

T_1	T_2
$V_{ds} =$	$V_{ds} = V_{gs}$
$V_{gs} = 2.6V$	$V_{gs} =$
$V_{t_1} = 0.4V$	V_{t_2}
$V_{gs} - V_{t_1} = 2.6 - 0.4 = 2.2V$	$\therefore$ Ars $V_{ds} = V_{gs}$ $\therefore V_{ds} > V_{gs} - V_{t_2}$

* V_{ds} = Output এর voltage
V_{gs} = Input " " "

$\therefore T_2$ is saturation mode

$V_{ds} < V_{gs} - V_t$

$\therefore T_1$ in resistive mode

$I_{ds_1} = I_{ds_2}$

$$\Rightarrow \frac{\epsilon \mu_n}{D} \frac{W_1}{L_1} \left\{ (V_{gs} - V_{t_1}) V_{ds} - \frac{V_{ds}^2}{2} \right\} = \frac{\epsilon \mu_n}{2D} \frac{W_2}{L_2} (V_{gs} - V_{t_2})^2$$

$$\Rightarrow 16 \left\{ (2.6 - 0.4) V_{ds} - \frac{V_{ds}^2}{2} \right\} = (3 - V_{out} - 0.4)^2$$

$$\Rightarrow 16 \left\{ \{2.2\} V_{out} - \frac{V_{out}^2}{2} \right\} = (3 - V_{out} - 0.4)^2$$

~~$\Rightarrow 35.2 V_{out}$ ⟹~~

$$\Rightarrow 16 \left(2.2 V_{out} - \frac{V_{out}^2}{2} \right) = (2.6 - V_{out})^2$$

$$\Rightarrow 16 (4.4 V_{out} - V_{out}^2) = 6.76 - 5.2 V_{out} + V_{out}^2$$

$$\Rightarrow 70.4 V_{out} - 16 V_{out}^2 - 6.76 + 5.2 V_{out} - V_{out}^2 = 0$$

$$\Rightarrow 75.6 V_{out} - 17 V_{out}^2 - 6.76 = 0$$

$\Rightarrow V_{out} = 4.31 V$ or $0.174 V$

$\therefore V_{out} = 0.174V$ [0র কাছাকাছি]

Power

$$I_{ds_2} = \frac{\epsilon \mu_n}{2D} \frac{W_2}{L_2} (V_{gs} - V_{t_2})^2$$

$$= \frac{60}{2} \times 2 (3 - 0.174 - 0.4)^2$$

$$= 353.13 \mu A$$

$P = VI = 3 \times 353 \times 10^{-6} A$

$= ~~1059~~ 0.001059 ~~A~~ W$