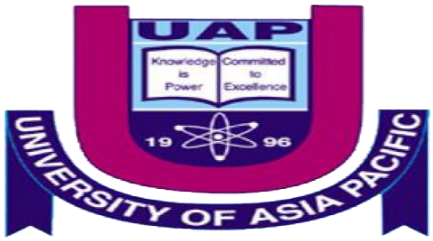

UNIVERSITY OF ASIA PACIFIC

- Transient Analysis of NAND and NOR Gates

- LAB1 Pending task (Inverter Symbol)

Course Code : CSE 458

Course Title : Design & Testing of VLSI Lab

Submitted by:

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Section : B (2)

Submitted To:

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Lecturer

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Introduction

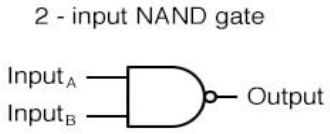
NAND and NOR gates are essential components in the field of digital electronics that are used to create a wide range of intricate circuits. The foundation of logical operations in almost all digital systems, from basic flip-flops to sophisticated microprocessors, is made up of these fundamental gates. It is essential to comprehend their behavior in order to develop and optimize digital circuits.

An important method in electrical engineering is called transient analysis, which looks at how circuits behave over time. It captures the dynamic features that steady-state analysis could miss and sheds light on how a circuit reacts to variations in input signals over time. Transient analysis is necessary for NAND and NOR gates in order to assess how well they work in real-world applications where switching durations, transient effects, and delays in signal propagation all play important roles.

Engineers may anticipate and reduce problems like timing mistakes, undesired oscillations, and signal degradation by doing transient analysis on NAND and NOR gates. By ensuring that the gates switch appropriately and quickly in response to changes in input, this analysis serves to preserve the integrity of the logical processes the gates carry out.

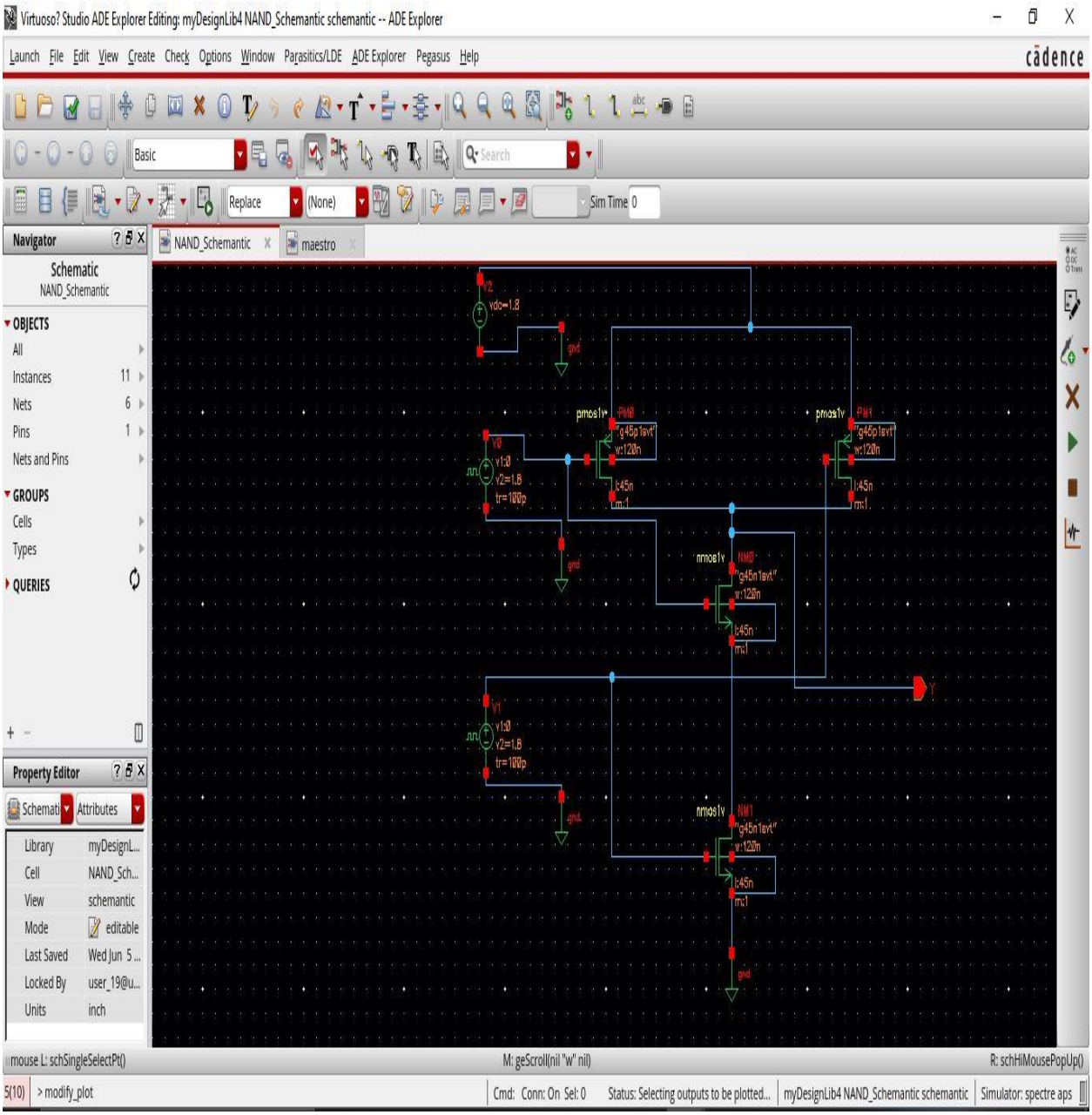
NAND Gate

NAND gates are essential to the development of many digital devices and logical processes. Because of its universality, NAND gates may be used to build any other logic gate (AND, OR, NOT, NOR, XOR, or XNOR), making them a fundamental component of digital circuit design. Because of its universality, integrated circuits require fewer different kinds of gates throughout the manufacturing process.



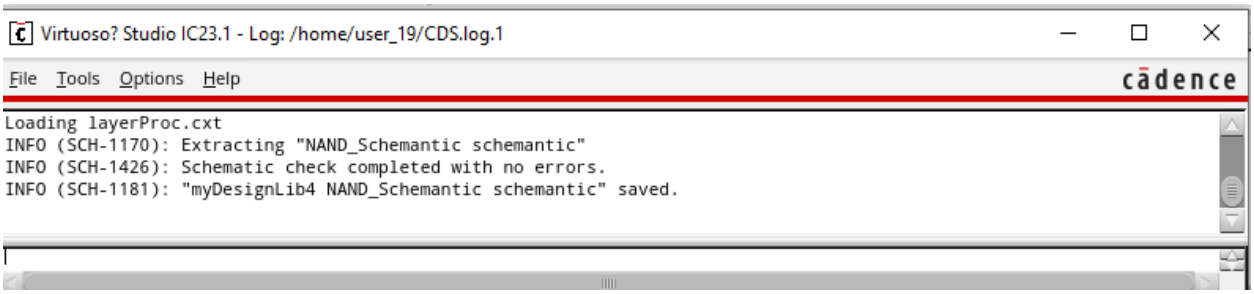
A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

Circuit Diagram of NAND Schematic:

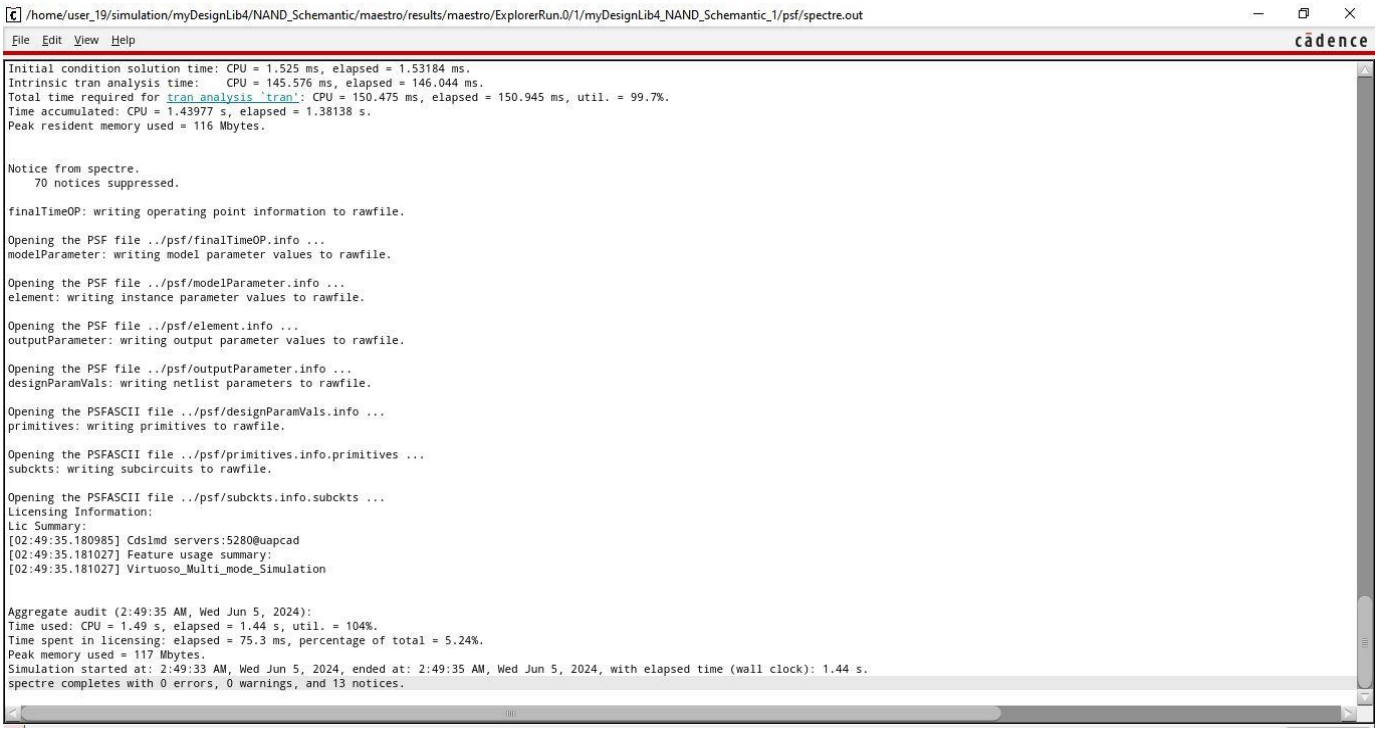


Here, I have constructed the circuit using 2 pmos in parallel, 2 nmos in series, also 2 vpulse, a vdc, single output Y, wires and 4 grounds.

Output in cadence of NAND Schematic (no error):



Simulation Report of NAND Schematic in maestro (no error):



My simulation report confirms that my NAND schematic has **no errors and no warnings.**

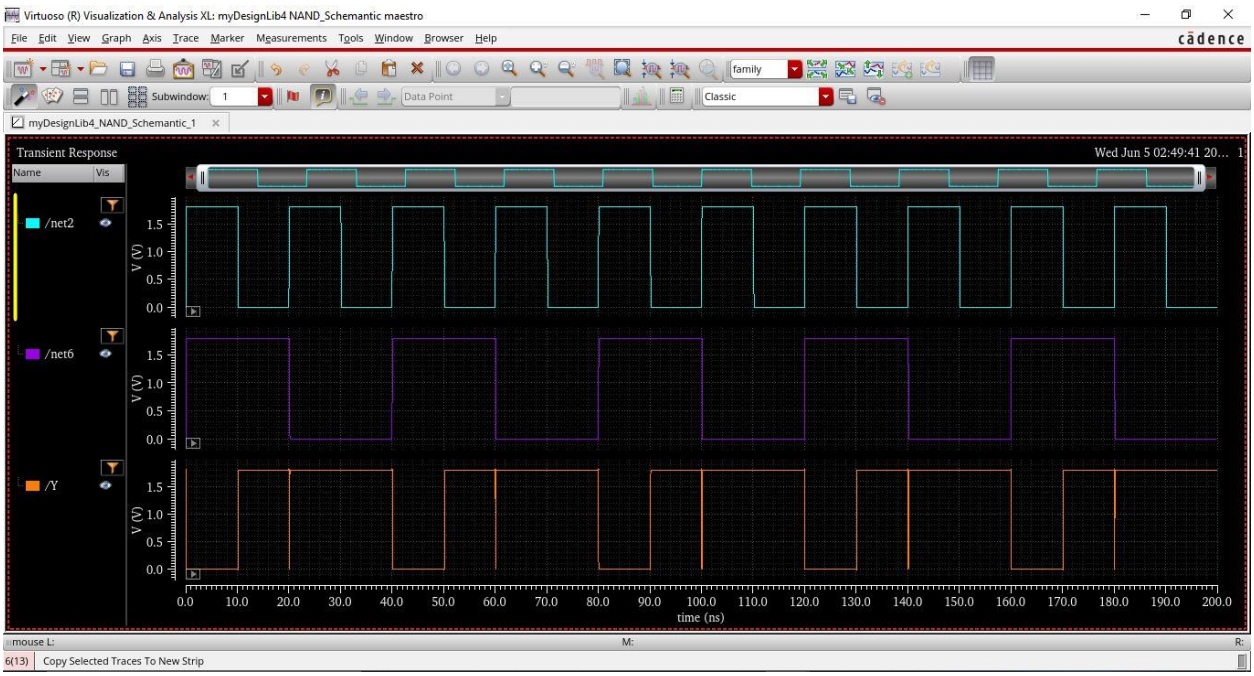
Better view:

```
/home/user_19/simulation/myDesignLib4/NAND_Schematic/maestro/results/maestro/ExplorerRun.0/1/myDesignLib4_NAND_Schematic_1/psf/spectre.out
File  Edit  View  Help
Initial condition solution time: CPU = 1.525 ms, elapsed = 1.53184 ms.
Intrinsic tran analysis time:    CPU = 145.576 ms, elapsed = 146.044 ms.
Total time required for tran analysis `tran': CPU = 150.475 ms, elapsed = 150.945 ms, util. = 99.7%.
Time accumulated: CPU = 1.43977 s, elapsed = 1.38138 s.
Peak resident memory used = 116 Mbytes.
```

Here, User 19 is my id (20101106)

```
Aggregate audit (2:49:35 AM, Wed Jun 5, 2024):
Time used: CPU = 1.49 s, elapsed = 1.44 s, util. = 104%.
Time spent in licensing: elapsed = 75.3 ms, percentage of total = 5.24%.
Peak memory used = 117 Mbytes.
Simulation started at: 2:49:33 AM, Wed Jun 5, 2024, ended at: 2:49:35 AM, Wed Jun 5, 2024, with elapsed time (wall clock): 1.44 s.
spectre completes with 0 errors, 0 warnings, and 13 notices.
```

Transient Response Plot of NAND Schematic:

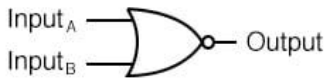


Here is my graph plotting, when both inputs are high, the output is low, as expected from the NAND gate truth table. When at least one of the inputs is low, the output remains high. These results confirm the correct functionality of the designed NAND gate.

NOR Gate

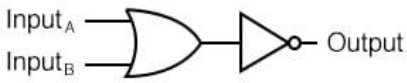
The NOR gate is distinguished by its universality, which allows it to be configured in a way that makes it possible to generate any other logic gate, including AND, OR, NOT, NAND, XOR, and XNOR. Because of these qualities, it is a crucial component for creating digital circuits as it facilitates quicker design procedures and effective resource utilization in integrated circuits.

2 - input NOR gate

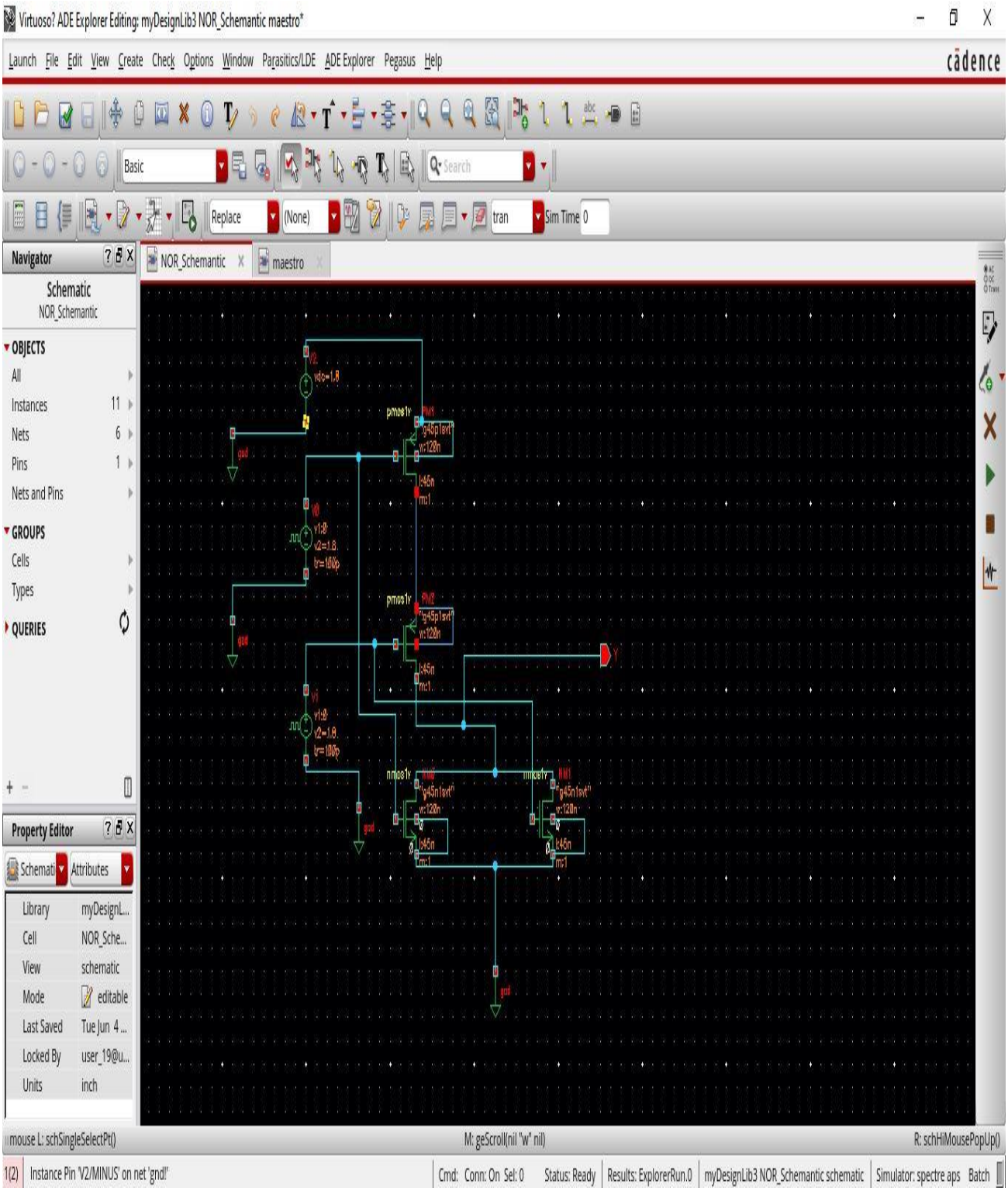


A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

Equivalent Gate Circuit

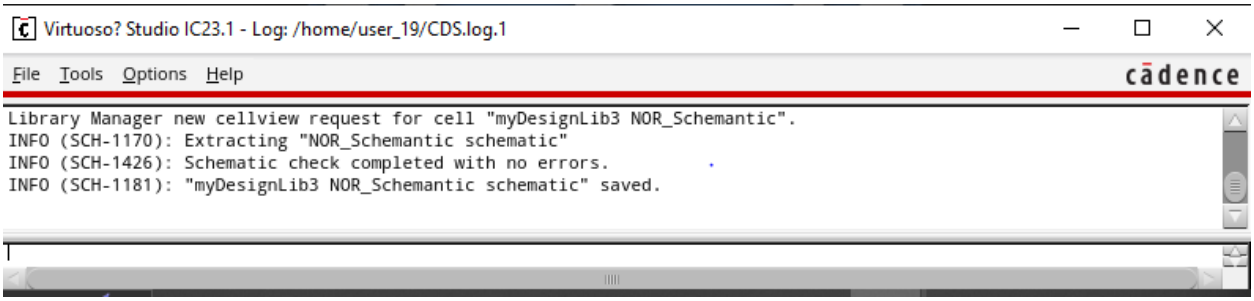


Circuit Diagram of NOR Schematic:

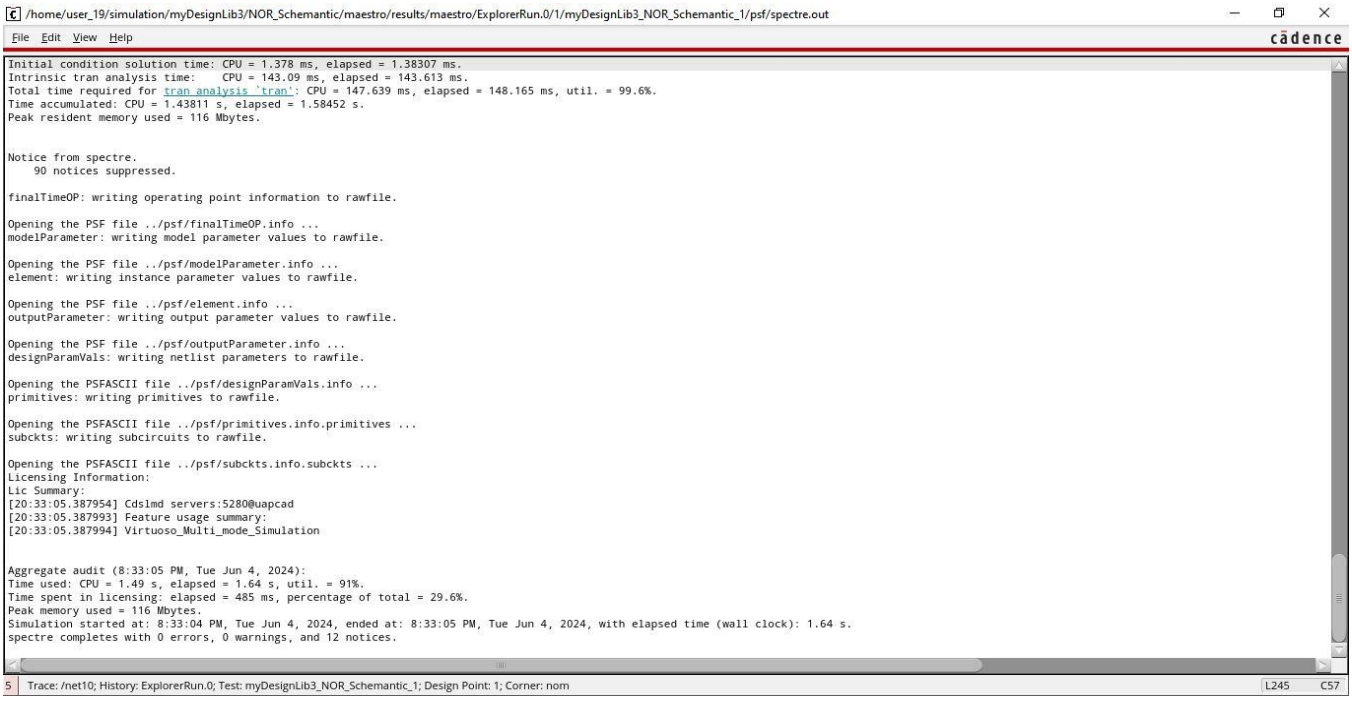


Here, I have constructed the circuit using 2 pmos in series, 2 nmos in parallel, also 2 vpulse, a vdc, single output Y, wires and 4 grounds.

Output in cadence of NOR Schematic (no error):

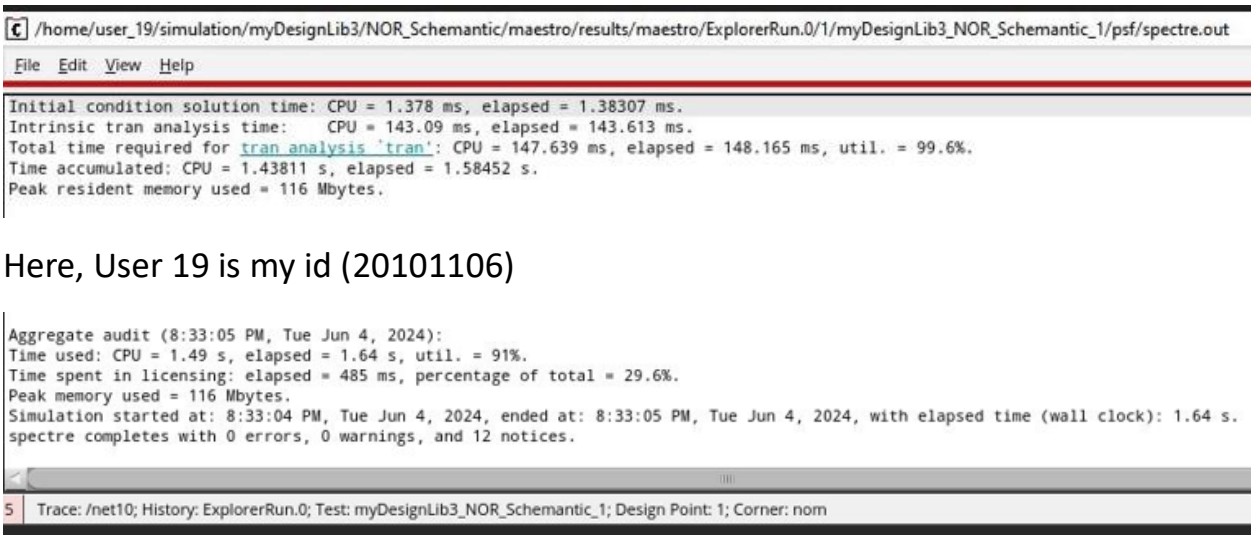


Simulation Report of NOR Schematic in maestro (no error):



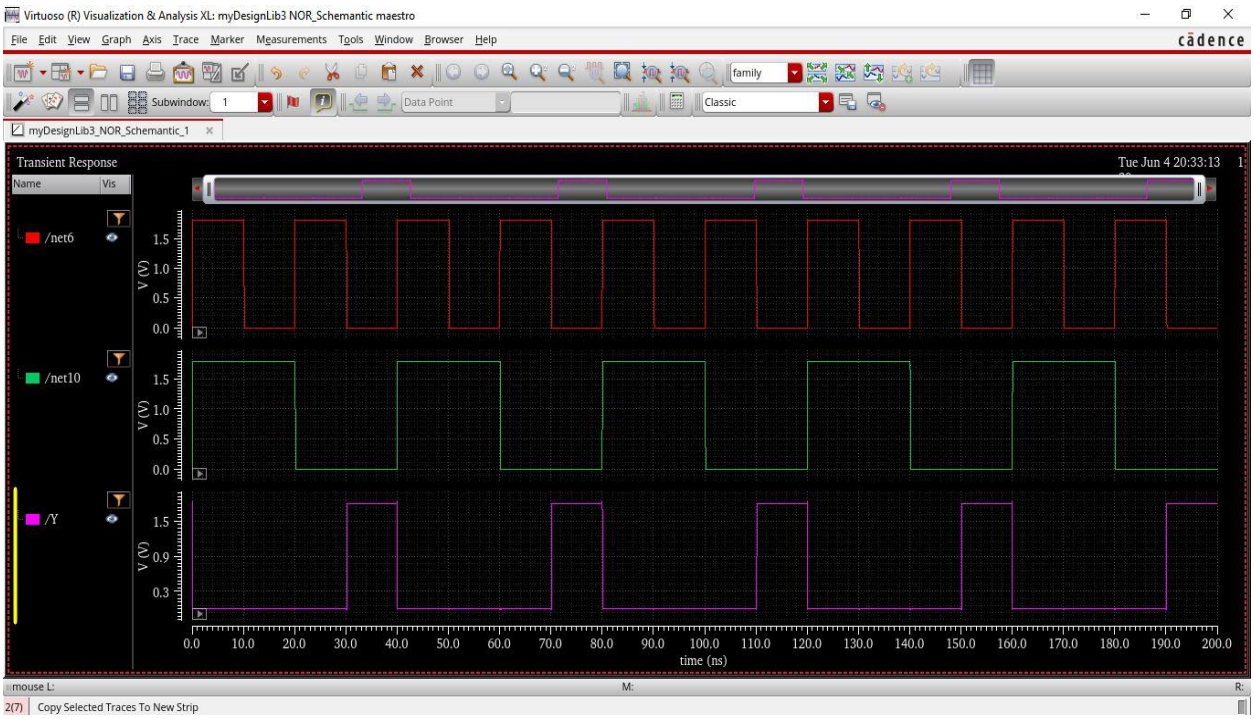
My simulation report confirms that my NOR schematic has **no errors and no warnings.**

Better view:



Here, User 19 is my id (20101106)

Transient Response Plot of NOR Schematic:



Here, is my graph plotting, when both inputs are low, the output is high, as expected from the NOR gate truth table. When at least one of the inputs is high,

the output is low. These results confirm the correct functionality of the designed NOR gate.

Conclusion:

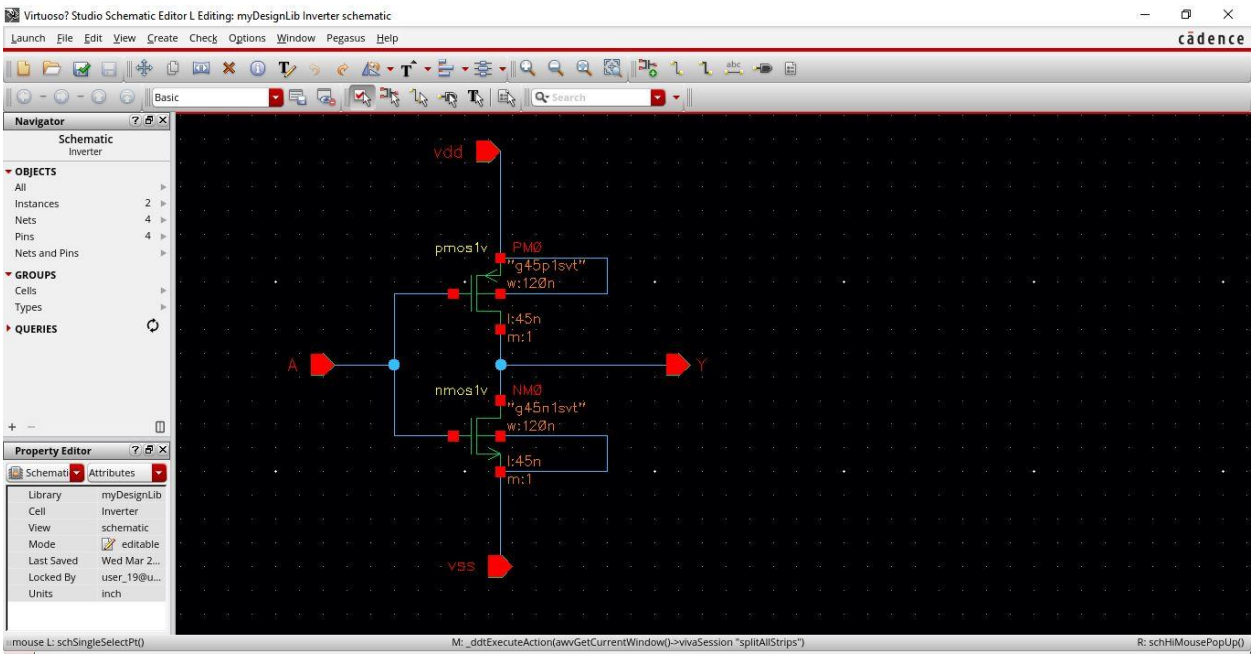
Using Cadence techniques for transient analysis of NAND and NOR gates, we get important insights into the performance and dynamic behavior of these basic digital components. Through the simulation of these gates, I've learned that the simulation results aligned perfectly with the expected theoretical behavior, confirming the correct design and implementation of the NAND & NOR gates.

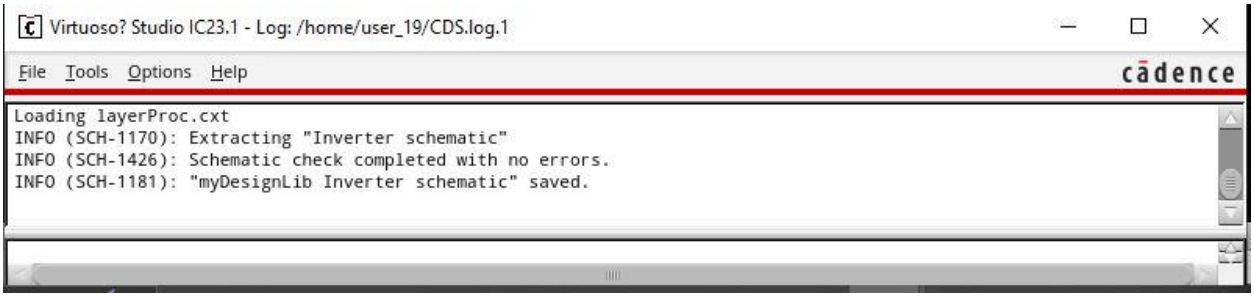
Pending tab task:

LAB-1:

Inverter Schematic **(Already shown in the lab)**

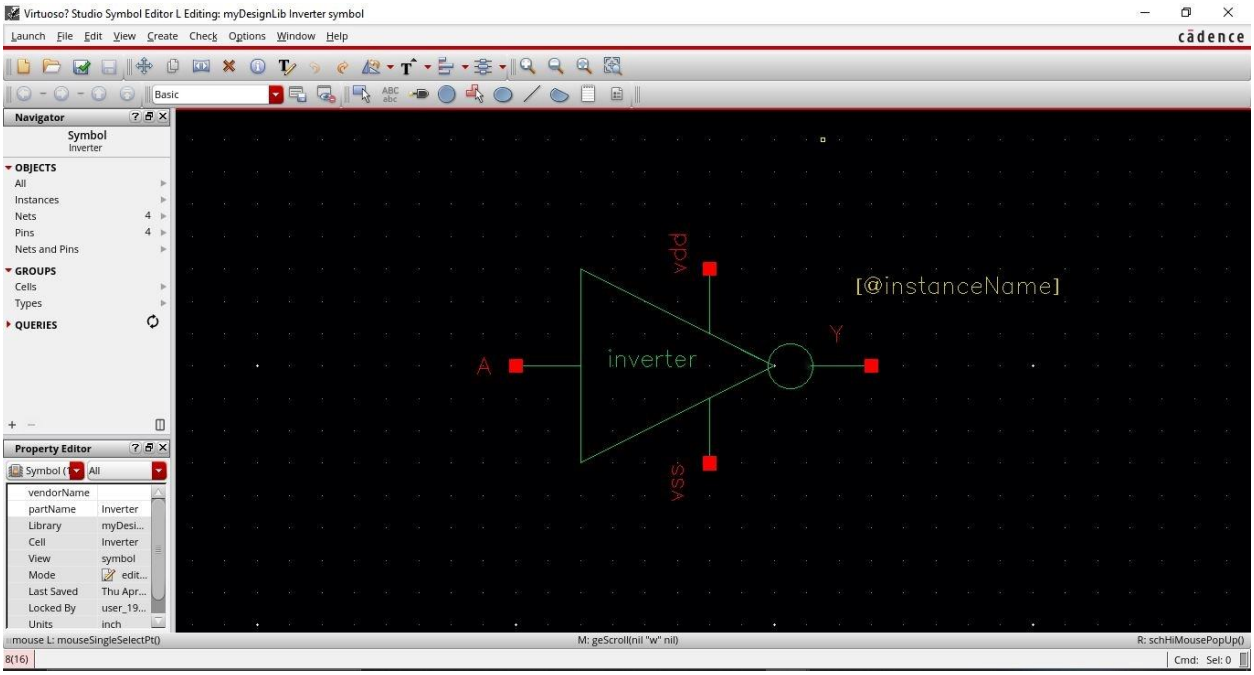
Inverter Symbol is pending due to accessibility issues in lab **(please go to next page for screen shot)**

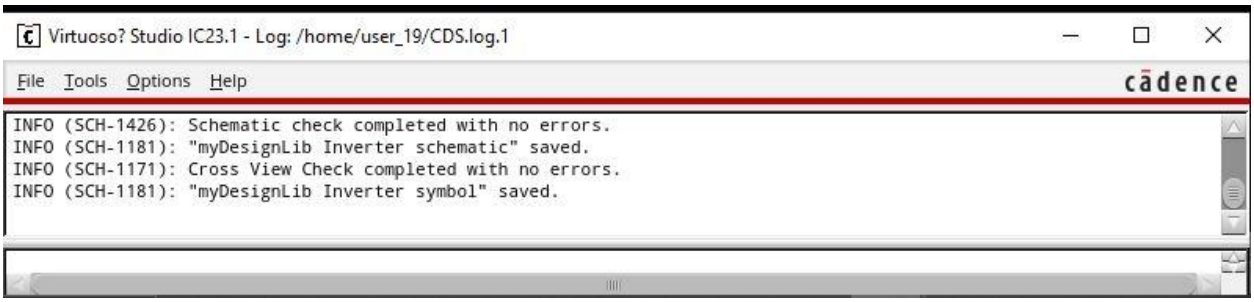




It is inverter schematic with **no error.**

Inverter symbol:





Here is inverter symbol with **no error.**