Product → PMOS → Parallel

(গুণ) NMOS → Series

(NAND, AND, XOR, XNOR)

এগুলোয় আছে

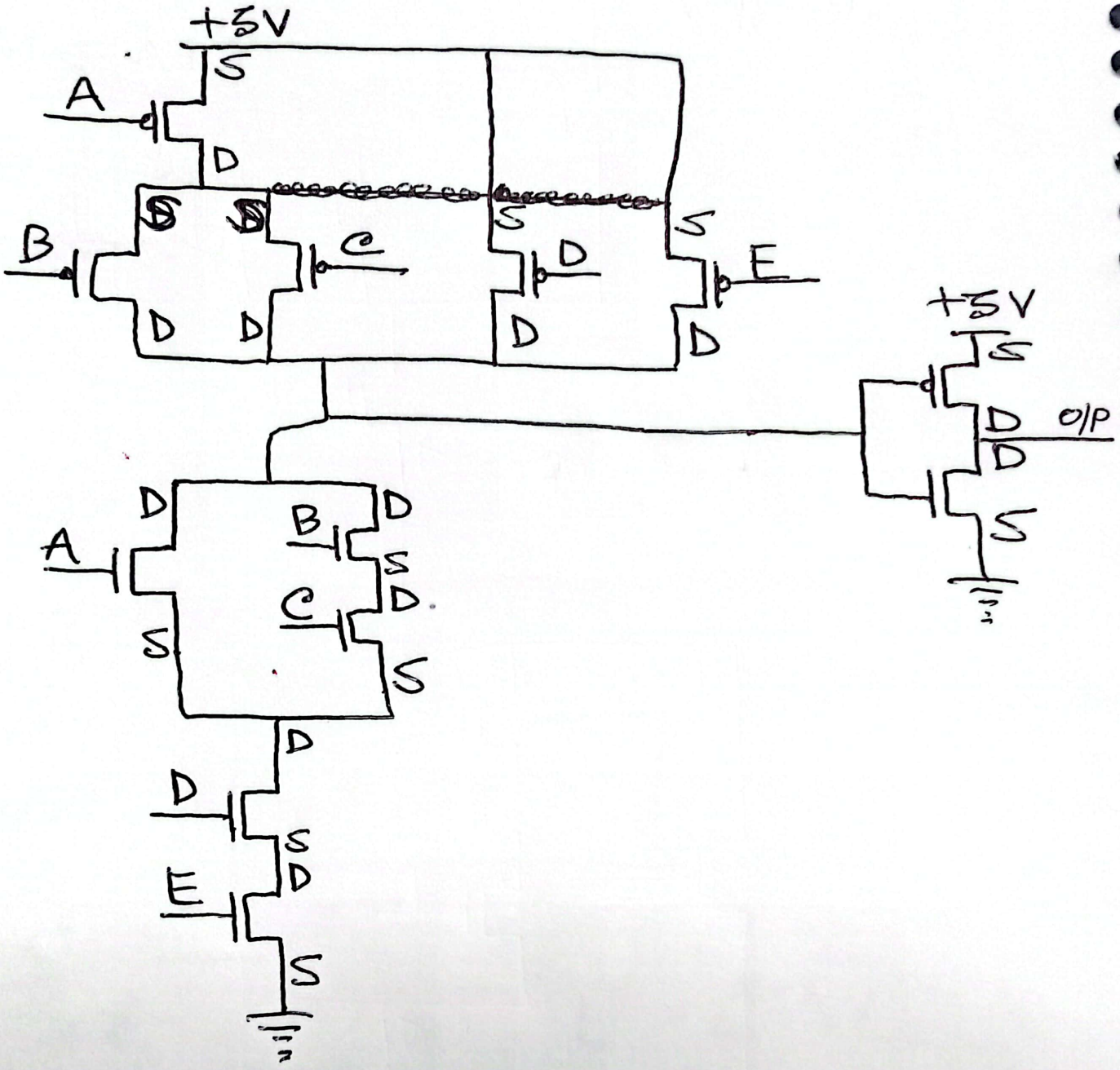
Sum → PMOS → ~~Parallel~~ Series

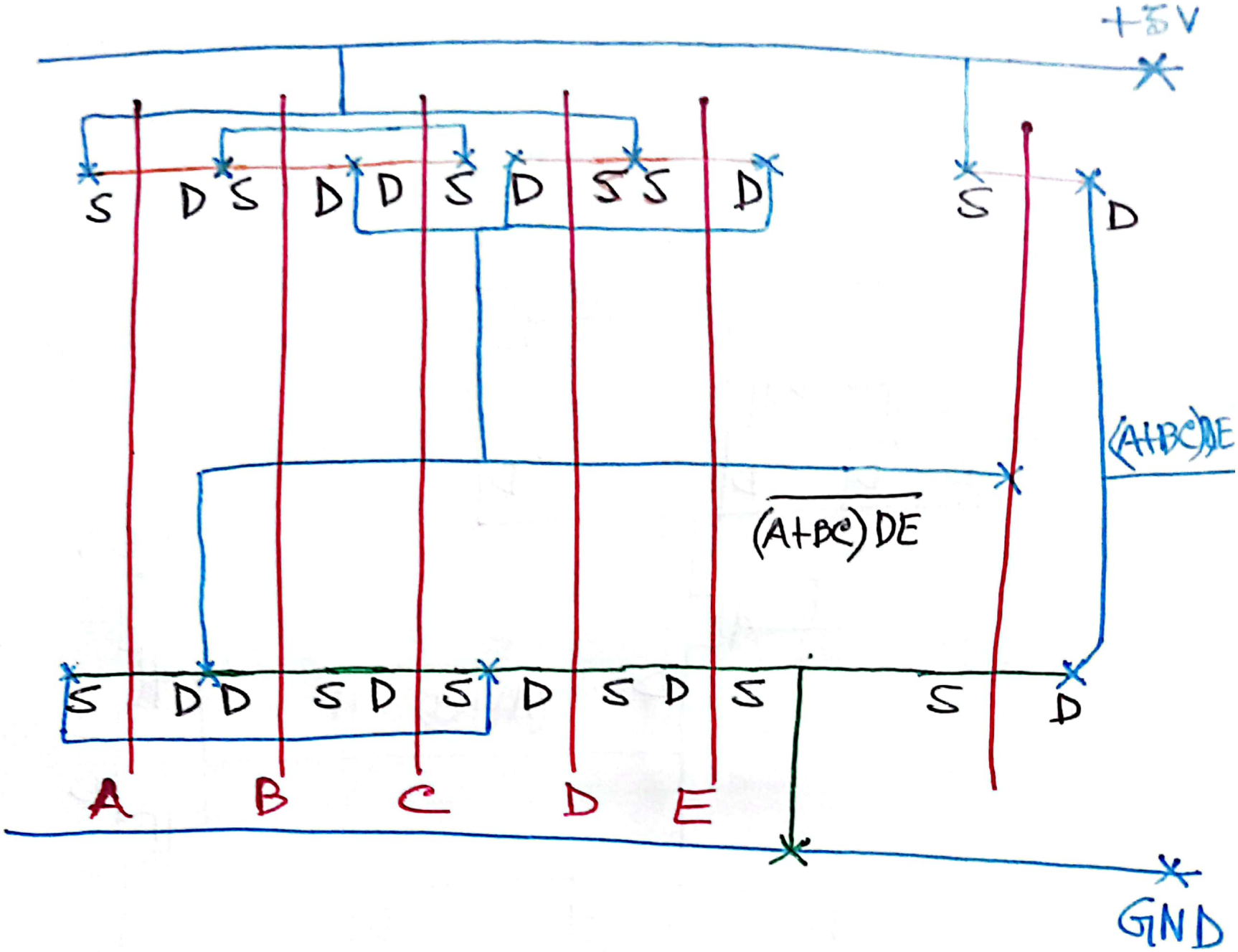
↙

(OR, XOR, NOR) NMOS → Parallel

এগুলোয় আছে

$y = (A + BC)DE$

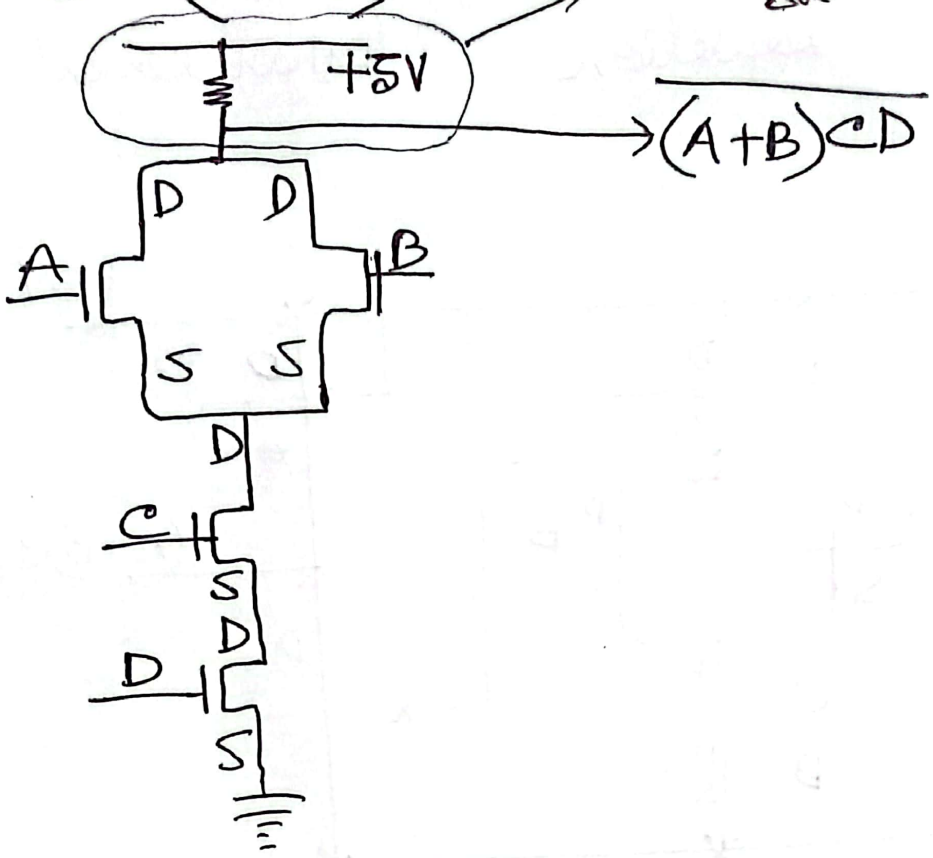



+5V
S D S D D S D S S D
S D
(A+BC)DE
$\overline{(A+BC)DE}$
S D D S D S D S D S S D
A B C D E
GND

NMOS CKT:

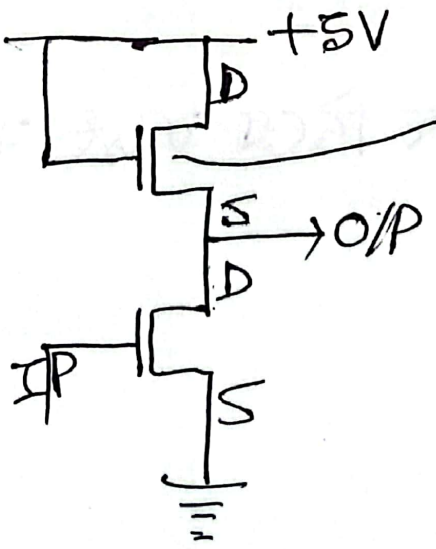
$Y = (A+B) \cdot D$

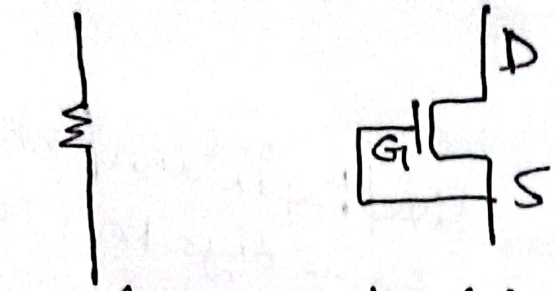
Resistive/Depletion/Enhancement Same diye NOT বানাবে



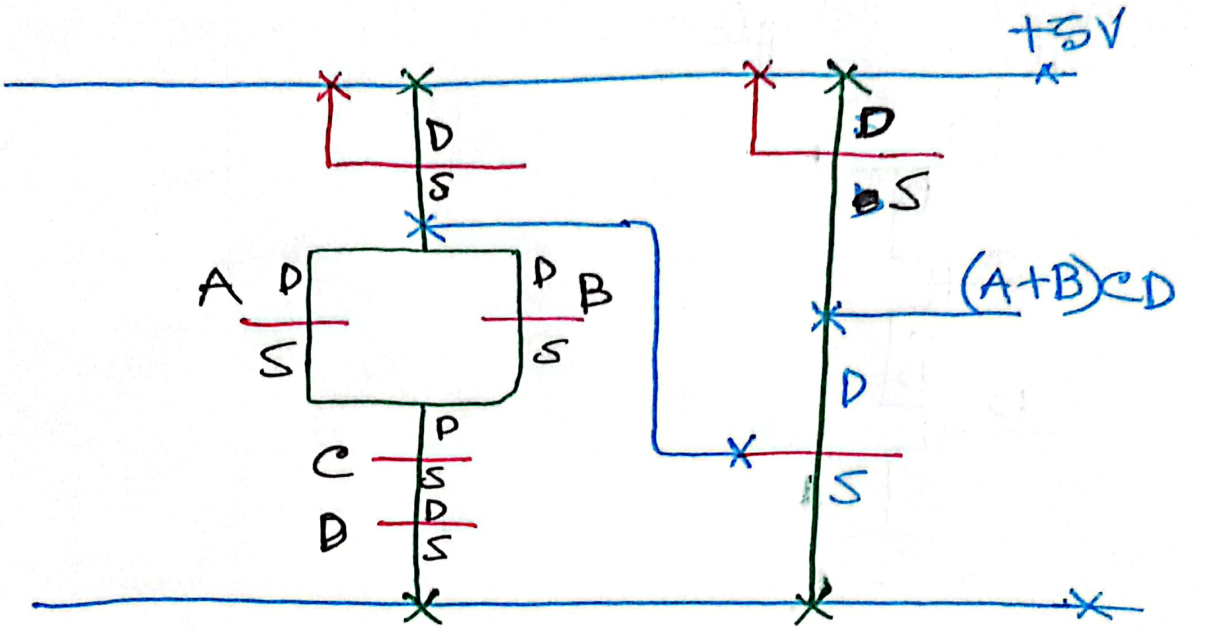
NOT Gate using NMOS only:

1. Enhancement type
2. Depletion type NMOS ↓ Resistance হিসেবে ব্যবহৃত





Resistive Depletion Enhancement

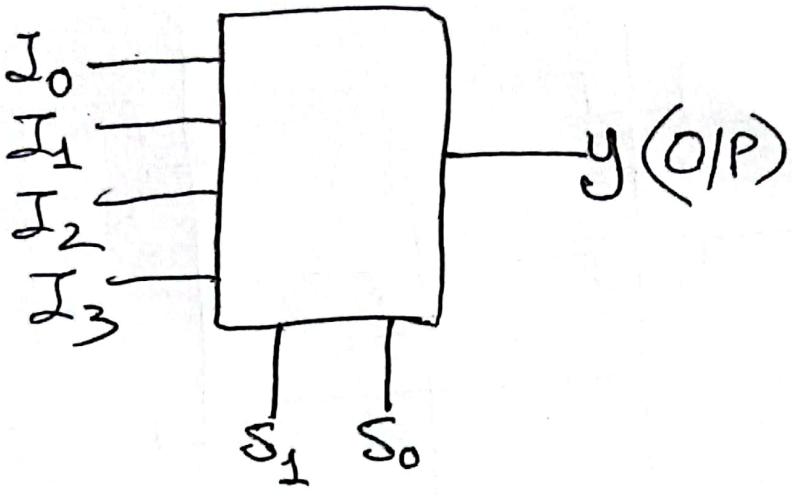


এটা Enhancement টাইপ

Resistive হলে,

এটার ন্যাক দিয়ে Just কানেক্ট করব

Multiplexers (MUX)



$0 \rightarrow \bar{x}$

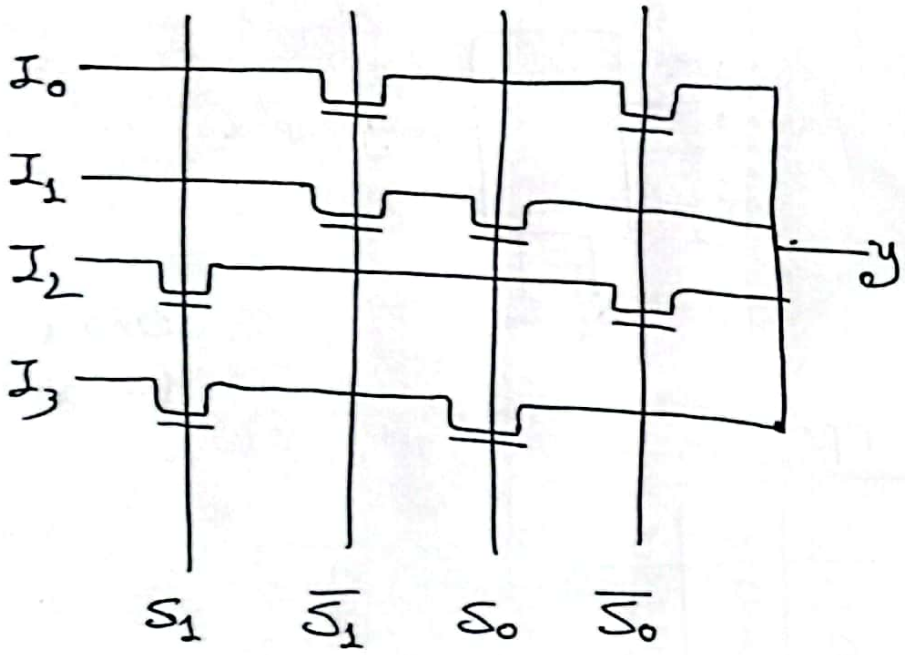
$1 \rightarrow x$

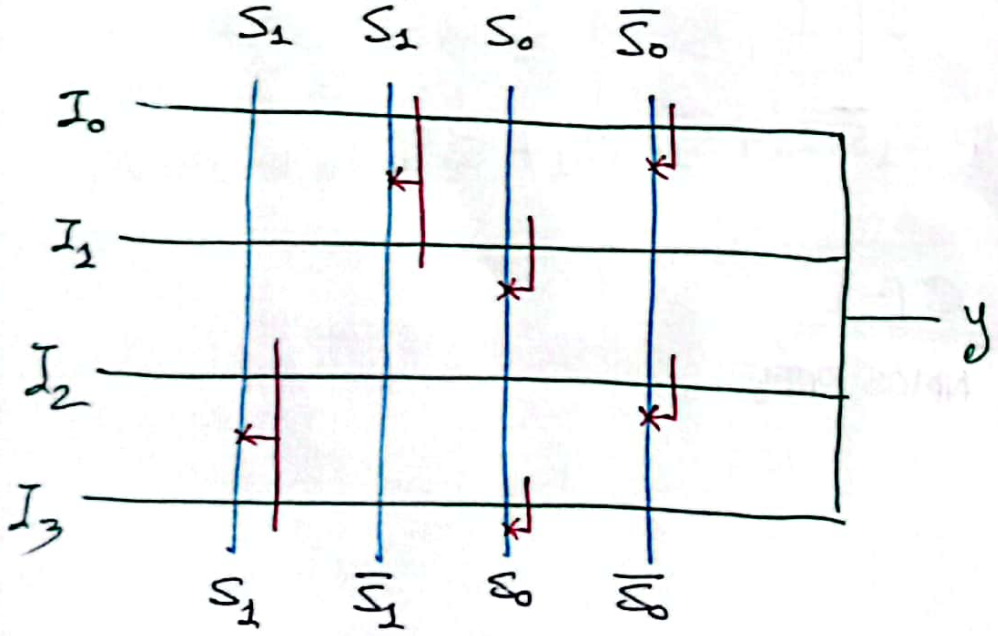
TT:

S_1	S_0	y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

$$y_1 = \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3$$

NMOS দিয়ে MUX



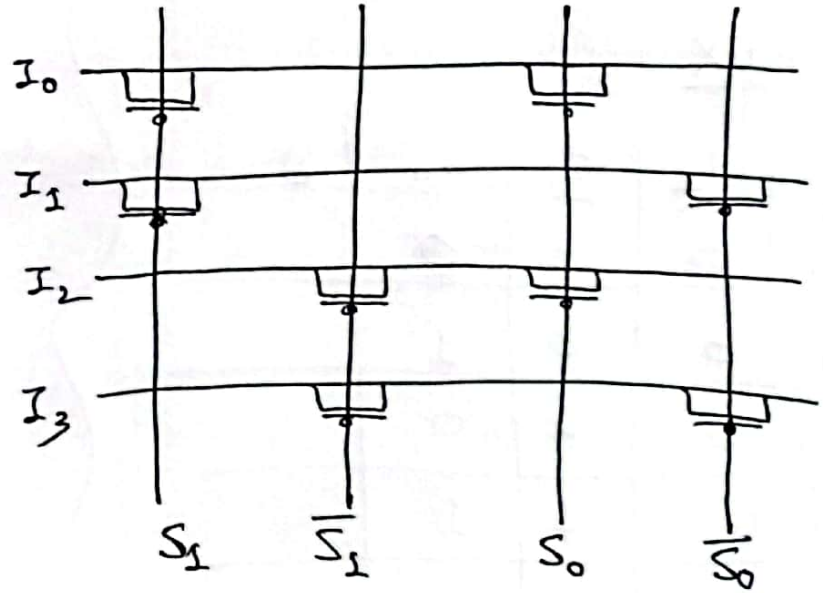


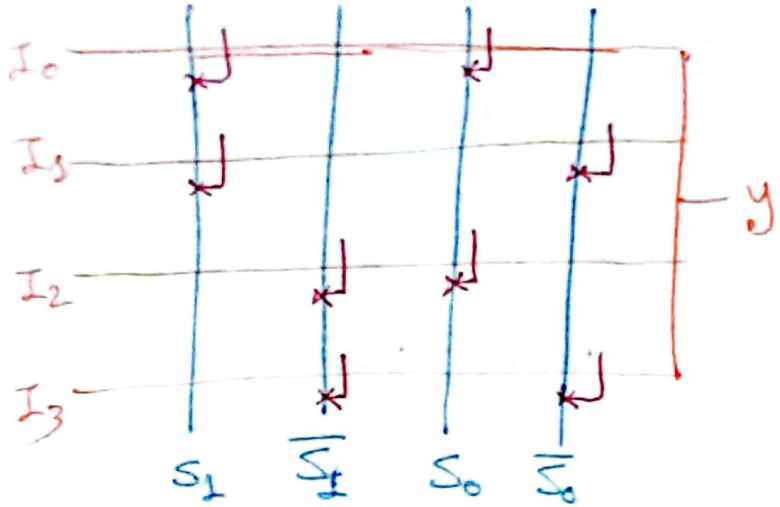
VLSI

MUX

S_1	S_0	y	NMOS	PMOS
0	0	I_0	$\bar{S}_1\bar{S}_0$	S_1S_0
0	1	I_1	$\bar{S}_1S_0$	$S_1\bar{S}_0$
1	0	I_2	$S_1\bar{S}_0$	$\bar{S}_1S_0$
1	1	I_3	S_1S_0	$\bar{S}_1\bar{S}_0$

PMOS দিয়ে MUX :



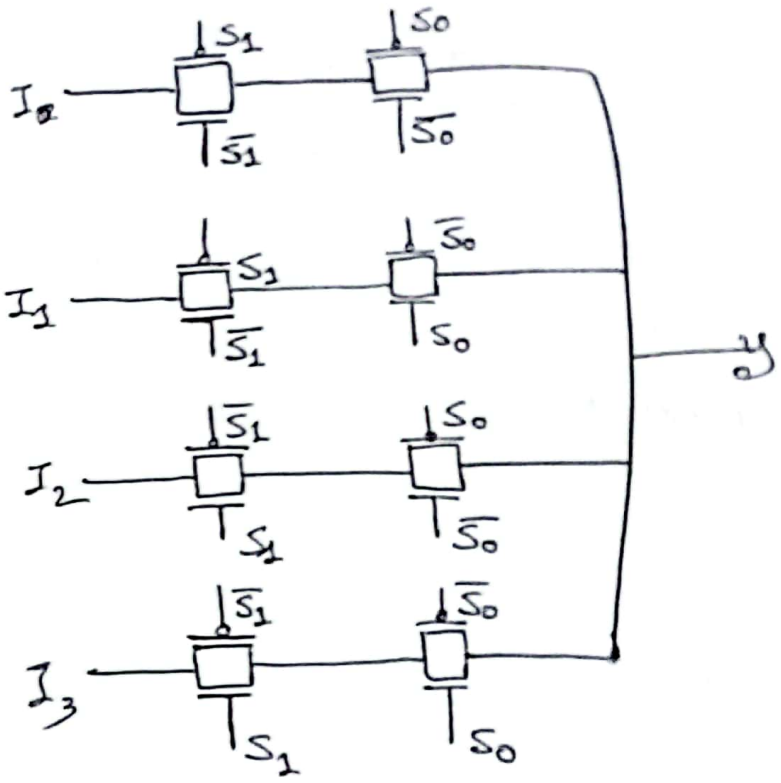


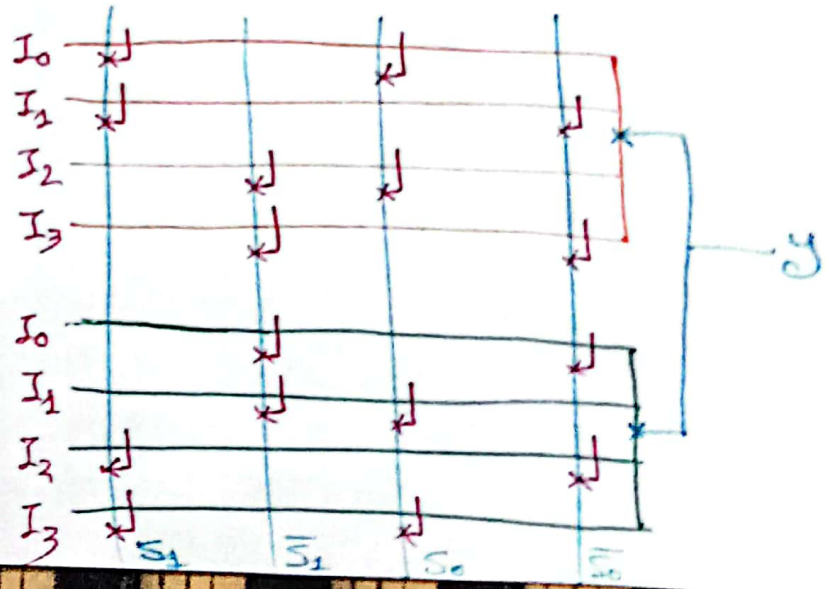
6X1 MUX

y	S_2	S_1	S_0
I_0	0	0	0
I_1	0	0	1
I_2	0	1	0
I_3	0	1	1
I_4	1	0	0
I_5	1	0	1

Extra

CMOS দিয়ে MUX

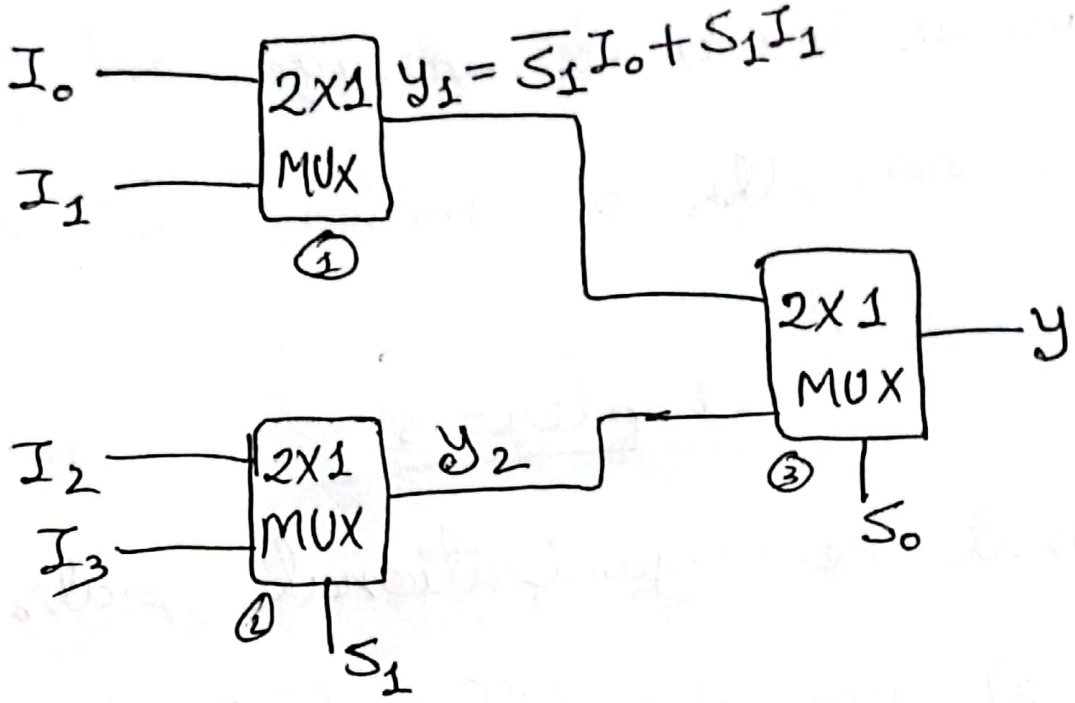




Verilog Code:

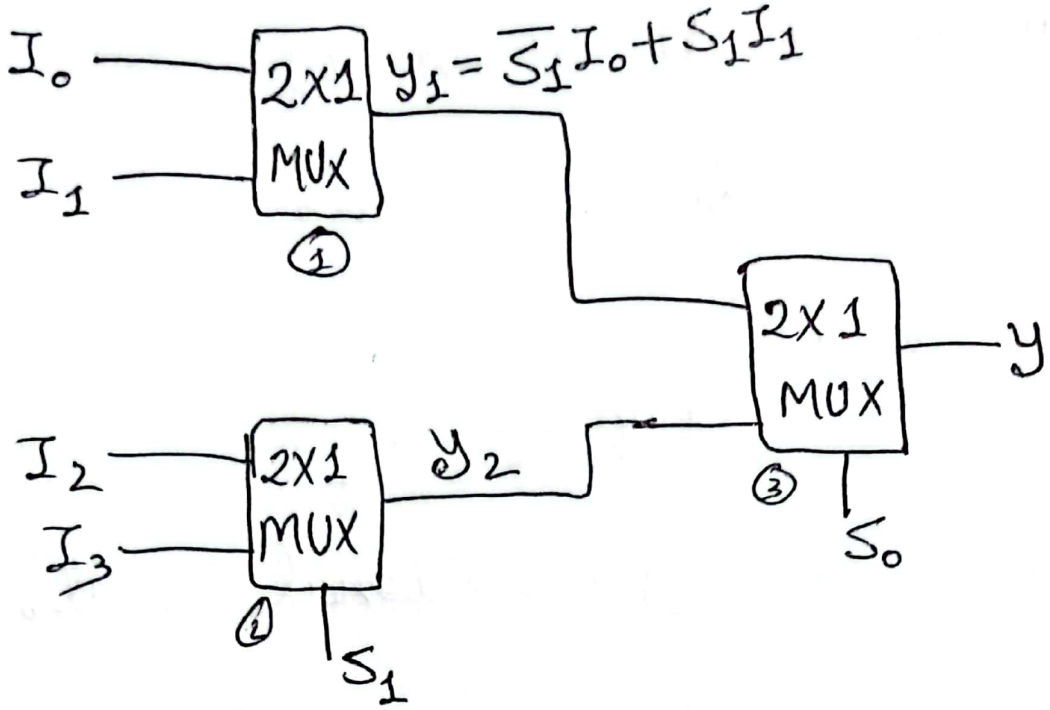
```
module space Name.(I/Ps, O/Ps);
input space ....;
output ____ ....;
and/or/xor/.... ____ Name(O/P, I/Ps);
endmodule
```

VLSI




```
Module 2X1MUX(I0, I1, S1, y1);
input I0, I1, S1;
output y1;
not not S1(W1, S1);
and and 1(W2, W1, I0);
and and2(W3, S1, I1);
or or1(y1, W2, W3);
endmodule
```

VLSI




```
Module 2X1MUX(I0, I1, S1, y1);
input I0, I1, S1;
output y1;
not not S1(W1, S1);
and and1(W2, W1, I0);
and and2(W3, S1, I1);
or or1(y1, W2, W3);
endmodule
```