Course Code: CSE 210

Course Title: Digital Logic & System Design Lab

Name of the Experiment: Design and implement 4 bits ALU (Arithmetic Logic Unit

Function table:

S2	S1	S0	Cin	ALU Functions	
0	0	0	0	**A**	**AU Operations**
0	0	0	1	**A + 1**	
0	0	1	0	**A + B**	
0	0	1	1	**A + B + 1**	
0	1	0	0	**A + B'**	
0	1	0	1	**A - B**	
0	1	1	0	**A - 1** **(Output carry effect)**	
0	1	1	1	**A**	
1	0	0	x	**OR**	**LU Operations**
1	0	1	x	**XOR**	
1	1	0	x	**AND**	
1	1	1	x	**NOT**	

Inputs and outputs:

There are 2 inputs A, B, and select function input S0, S1, S2, and Cin.
Outputs: A=1110 = 14, B =1010 =10; B'=0101=5

S2	S1	S0	Cin	ALU Functions	
0	0	0	0	A = 1110	**AU Operation**
0	0	0	1	A+1 = 1111	
0	0	1	0	A+B = 11000	
0	0	1	1	A+B+1 = 11001	
0	1	0	0	A+B' = 10011	
0	1	0	1	A-B = 0100	
0	1	1	0	A-1 = 1101	
0	1	1	1	A = 1110	
1	0	0	x	OR=1110	**LU Operation**
1	0	1	x	XOR=0100	
1	1	0	x	AND=1010	
1	1	1	x	NOT=0001	