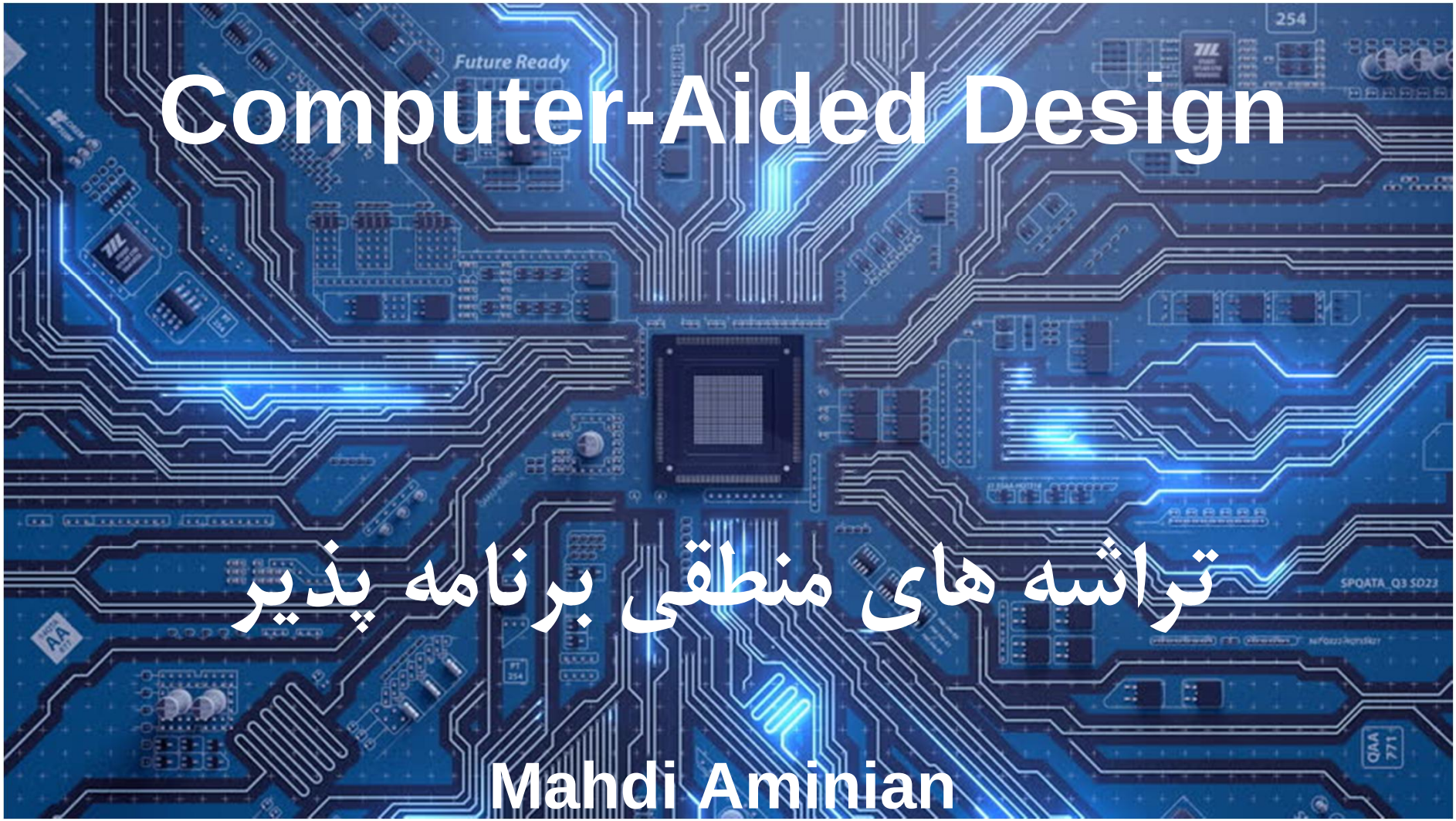


Computer-Aided Design

تراشه های منطقی برنامه پذیر

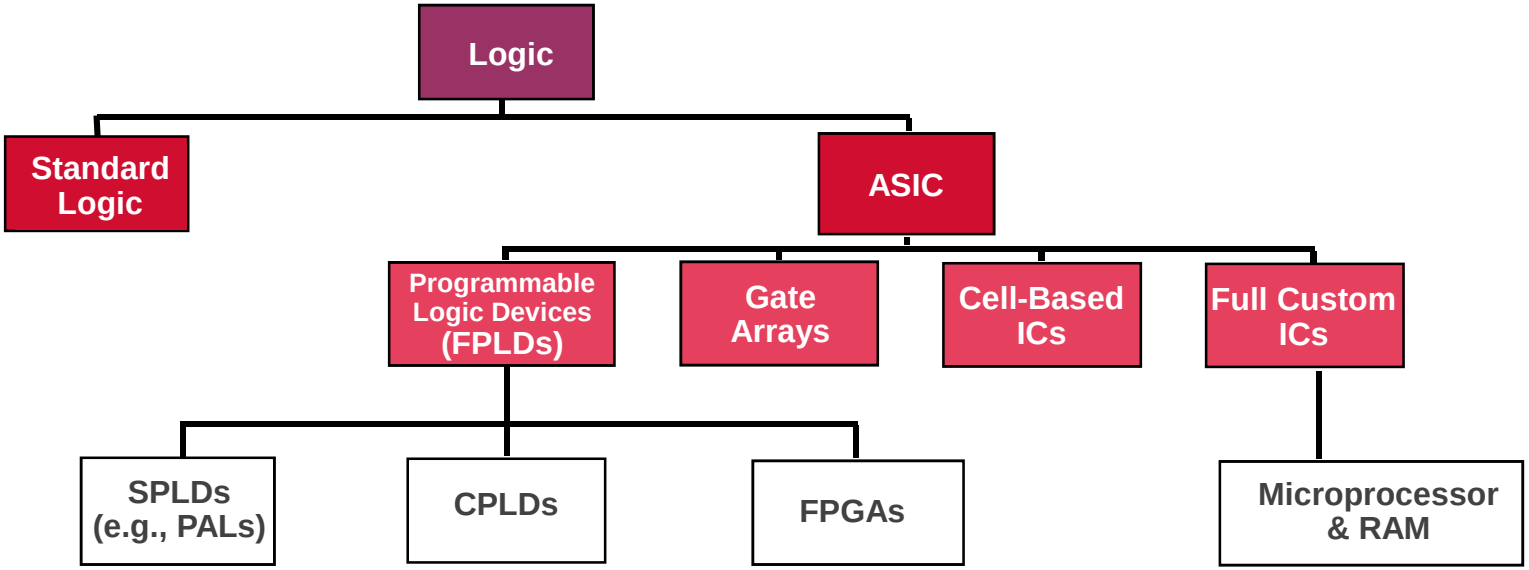
Mahdi Aminian

The University Of Guilan
Rasht - Iran

Some slides courtesy of:

- CAD slides, Dr. Saheb Zamani
- allaboutcircuits.com

Digital Circuits



Acronyms

SPLD = Simple Programmable Logic Device
PAL = Programmable Array Logic
CPLD = Complex PLD
FPGA = Field Programmable Gate Array
ASIC = Application Specific IC

Common Resources

Configurable Logic Blocks (CLB)
- Memory Look-Up Table (LUT)
- AND-OR planes
- Simple gates

Input / Output Blocks (IOB)
- Bidirectional, latches, inverters, pullup/pulldowns

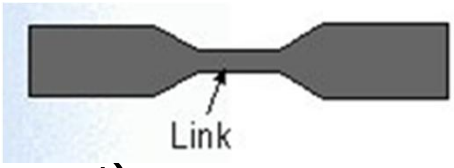
Interconnect or Routing
- Local, internal feedback, and global

“PROGRAMMABLE”

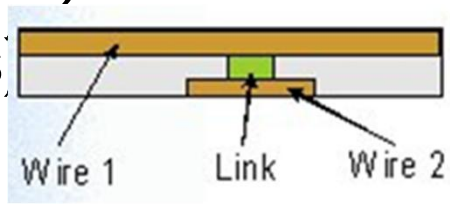
“Programmable”?

- One time programmable
  - Fuses

  (destroy internal links with current)
  - Anti-fuses (grow internal links)
  - PROM
- Reprogrammable
  - EPROM
  - EEPROM
  - Flash
  - SRAM → *volatile*



· Fuse-Technology

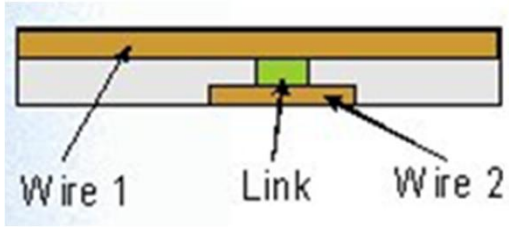


Antifuse-Technology

} *non-volatile*

Antifuse

- جریان برنامه ریزی بالا ß عایق ONO را ذوب می کند ç اتصال دایم.
- به علت کوچکی، PLDهای آنتی فیوز ظرفیت بسیار بالایی دارند.



Antifuse-Technology

Antifuse

- مزایا:
  - عدم نیاز به حافظه ی خارجی.
  - مساحت بسیارکم (تقریبا هم اندازه با viaی سیمهای فلزی).
  - قابلیت اطمینان بسیار بالا
  - (**Time-Dependent Dielectric Breakdown**:**TDDB**) حدود 40 سال.
  - مقاومت کم در حالت روشن (در طی زمان هم کم می ماند).
  - خازن پارازیتی بسیار کمتر.
  - امنیت بالای طرح در برابر سرقت.
  - توان مصرفی بسیار کمتر.
- اشکالات:
  - عدم امکان برنامه ریزی مجدد.
  - برنامه ریزی آن نیاز به مدار اضافی دارد (باید ولتاژ و جریان بالا ایجاد کند).

Programmable ROM (PROM)

- First ones had fusible links
- High voltage would blow out links
- Fast to program
- Single use

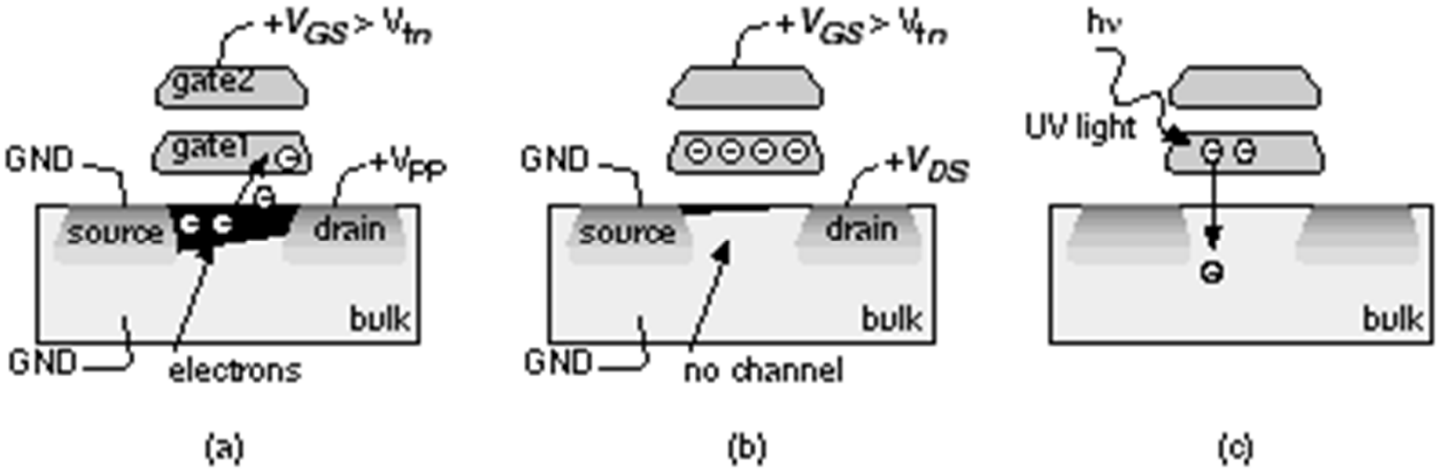
UV EPROM

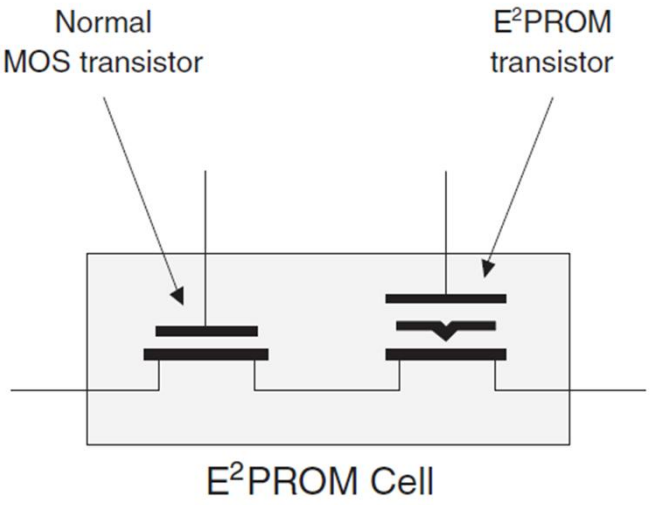
- *Erasable* PROM
- Common technologies used UV light to erase complete device
  - Took about 10 minutes
- Holds state as charge in very well insulated areas of the chip
- Nonvolatile for several (10?)

EEPROM

- *Electrically Erasable* PROM
- Similar technology to UV EPROM
- Erased in blocks by higher voltage
- Programming slower than reading
- Some called *flash memory*
  - Digital cameras, MP3 players, BIOS
  - Limited life
  - Some support individual word write, some block
  - Has a *boot block* that is carefully protected

EPROM/EEPROM/Flash



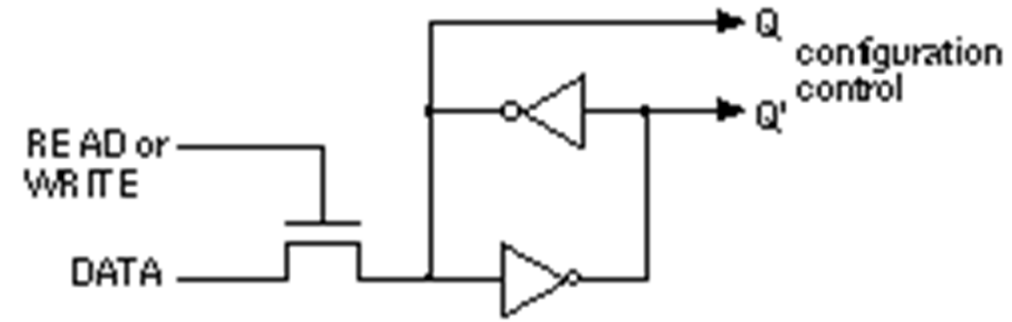


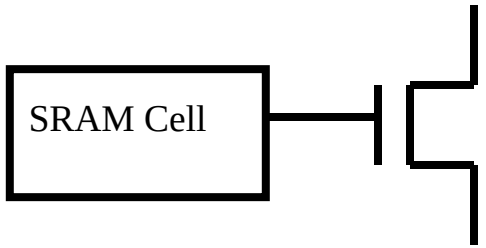
- ولتاژ برنامه ریزی بالا ß محبوس شدن الکترونها ç Vdd نمی تواند ترانزیستور را روشن کند

- **EEPROM**: باز گرداندن الکترونها با میدان الکتریکی (ظرفیت کمتر از **EPROM**).

SRAM

SRAM





SRAM

- مزایا:
  - برنامه ریزی مجدد سریع.
  - برنامه ریزی on-chip به دفعات نامحدود.
  - ç prototyping در داخل سیکل طراحی
  - کارخانه ی سازنده می تواند همه ی مسیرها را با reprogram کردن FPGA تست کند (ç کاربر، آی سی کاملا تست شده را می گیرد و نیازی به ایجاد الگوهای تست و مدارهای DFT ندارد).
- اشکالات:
  - مساحت (اشکال اصلی): 5 ترانزیستور برای هر سلول SRAM + یک ترانزیستور برای سوییچ.
  - نیاز به حافظه ی خارجی non-volatile (دارای مدار حسگر power-on است برای initialization).
  - امنیت کم طرح در برابر سرقت (intellectual property)
  - توان مصرفی بالای سلول های SRAM (حتی وقتی که برنامهٔ آن تغییر نمی کند).

PROGRAMMABLE LOGIC DEVICE (PLD)

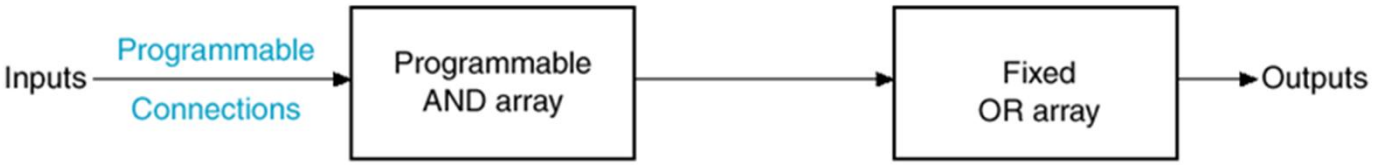
Three FPLD Types

- Simple Programmable Logic Device (SPLD)
  - LSI device (Less than 1000 logic gates)
  - PLA or PAL
  - Fixed internal routing, deterministic propagation delays
- Complex Programmable Logic Device (CPLD)
  - VLSI device (Higher logic capacity than SPLDs)
  - Multiple SPLDs onto a single chip
  - Programmable interconnect
- Field Programmable Gate Array (FPGA)
  - VLSI device (Higher logic capacity than CPLDs)
  - An array of logic blocks
  - Large number of gates, user selectable interconnection, delays depending on design and routing
  - A high ratio of flip-flops to logic resources

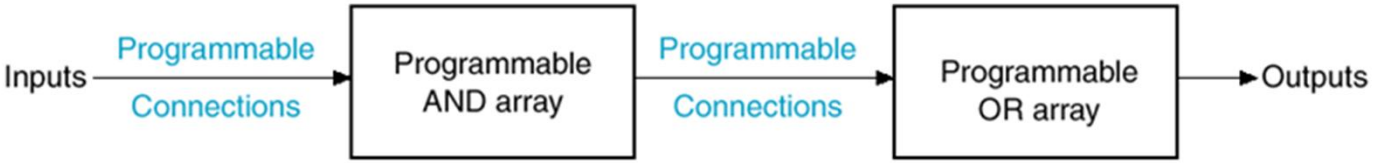
SPLD

Simple PLD (SPLD)

- Popular SPLD Architecture Types
  - Programmable Logic Array, PLA
  - Programmable Array Logic, PAL
  - General Array Logic, GAL
  - others
- Architecture Differences
  - AND versus OR implementation
  - Programmability (e.g., EE)
  - Fundamental logic block



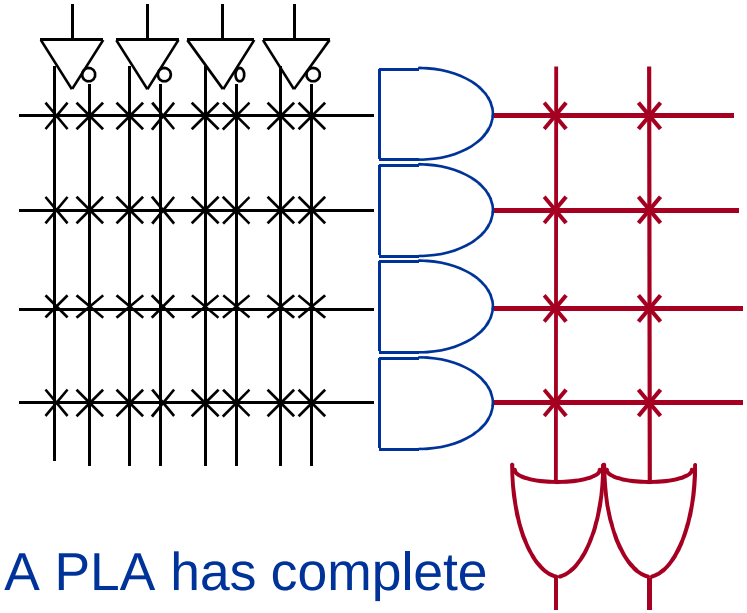
(a) Programmable array logic (PAL) device



(b) Programmable logic array (PLA) device

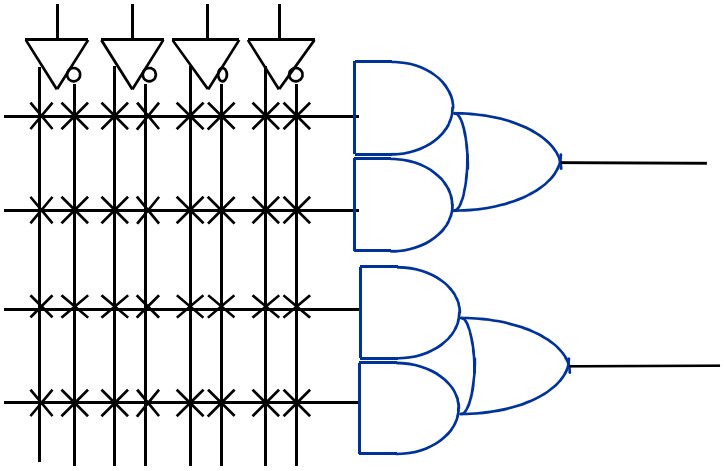
PLA & PAL

Programmable Logic Array



A PLA has complete flexibility of its sum-of-products groupings.

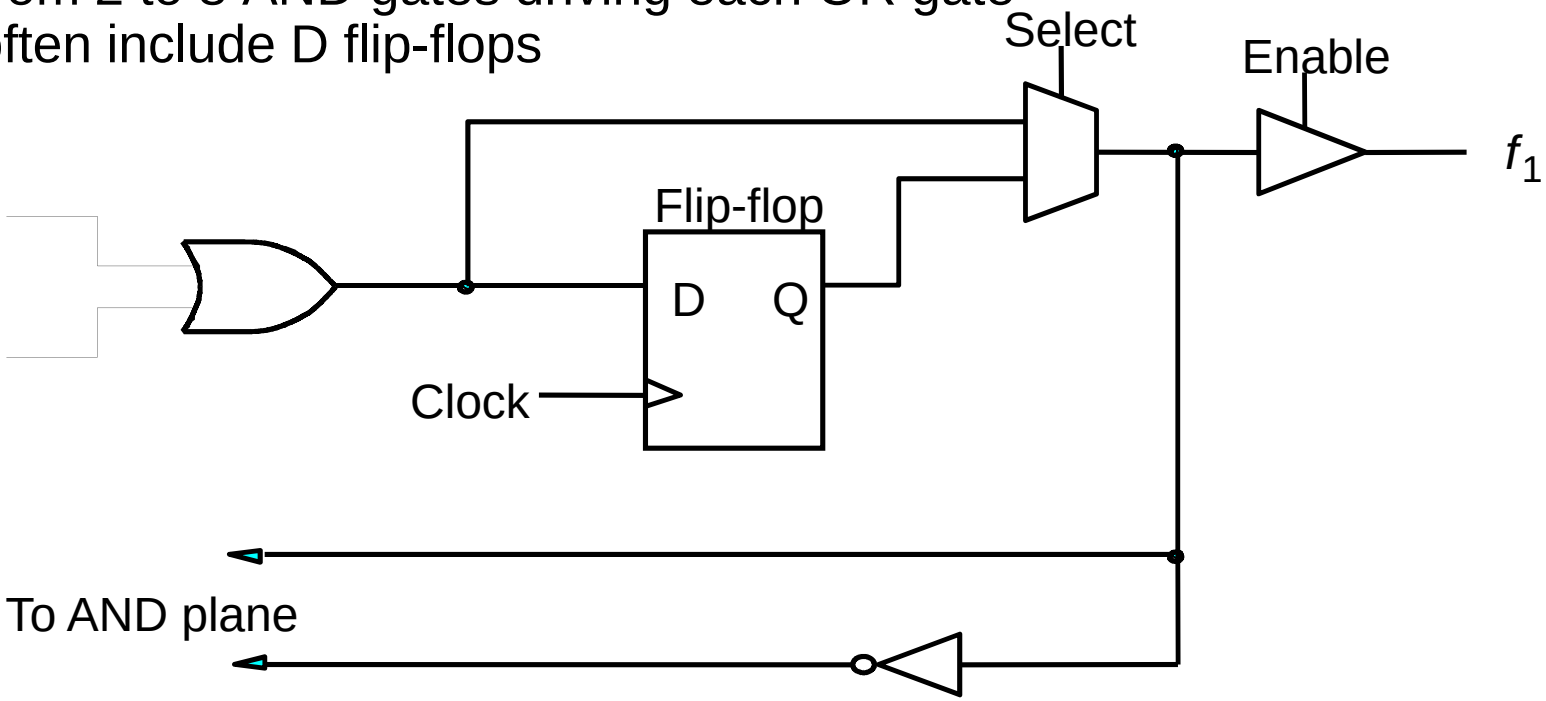
Programmable Array Logic



A PAL has limits on the arrangement of its sum-of-products groupings.

PAL Outputs

- Typical PALs have:
  - from 10 to 20 inputs
  - from 2 to 10 outputs
  - from 2 to 8 AND gates driving each OR gate
  - often include D flip-flops



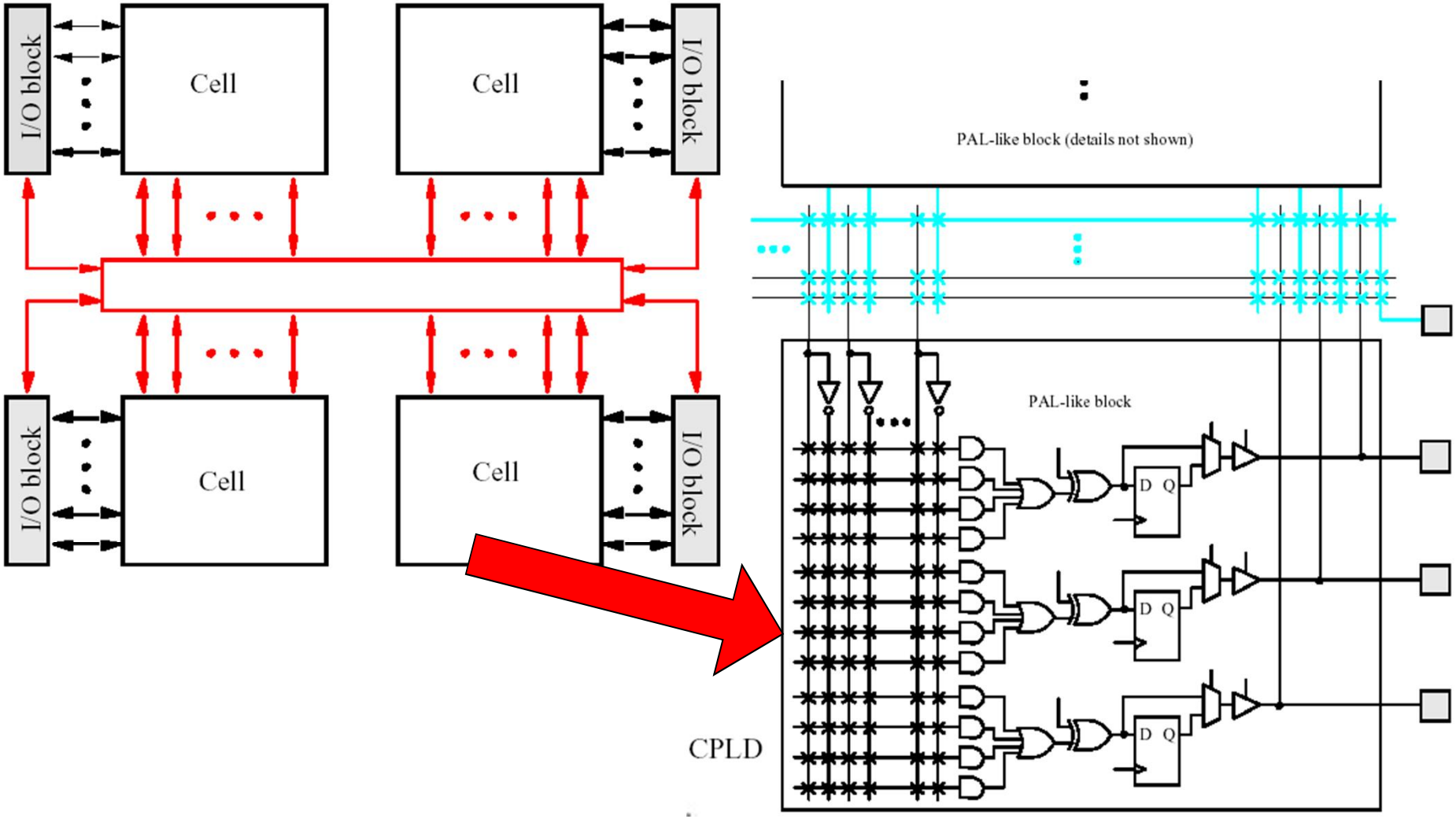
MUX output is “fed back” to the AND plane.

CPLD

CPLD

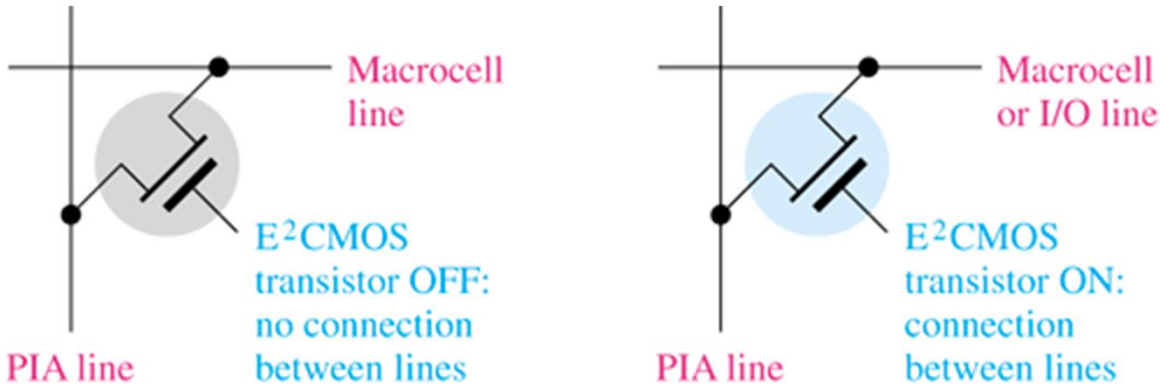
- PALs and GALs are available only in small sizes
  - equivalent to a few hundred logic gates
- For bigger logic circuits, complex PLDs or CPLDs can be used.
- CPLDs contain the equivalent of several PALs/GALs
  - linked by programmable interconnections
  - all in one integrated circuit (IC)
- CPLDs can replace thousands, or even hundreds of thousands, of individual logic gates
  - increased integration density

CPLD


I/O block
Cell
Cell
I/O block
I/O block
Cell
Cell
I/O block
PAL-like block (details not shown)
PAL-like block
D Q
D Q
D Q
CPLD

Programmable Interconnect Array

- Consists of connectors that run throughout the CPLD to connect the macrocells in each LAB
- The PIA also connects the AND gate and other elements of the macrocells

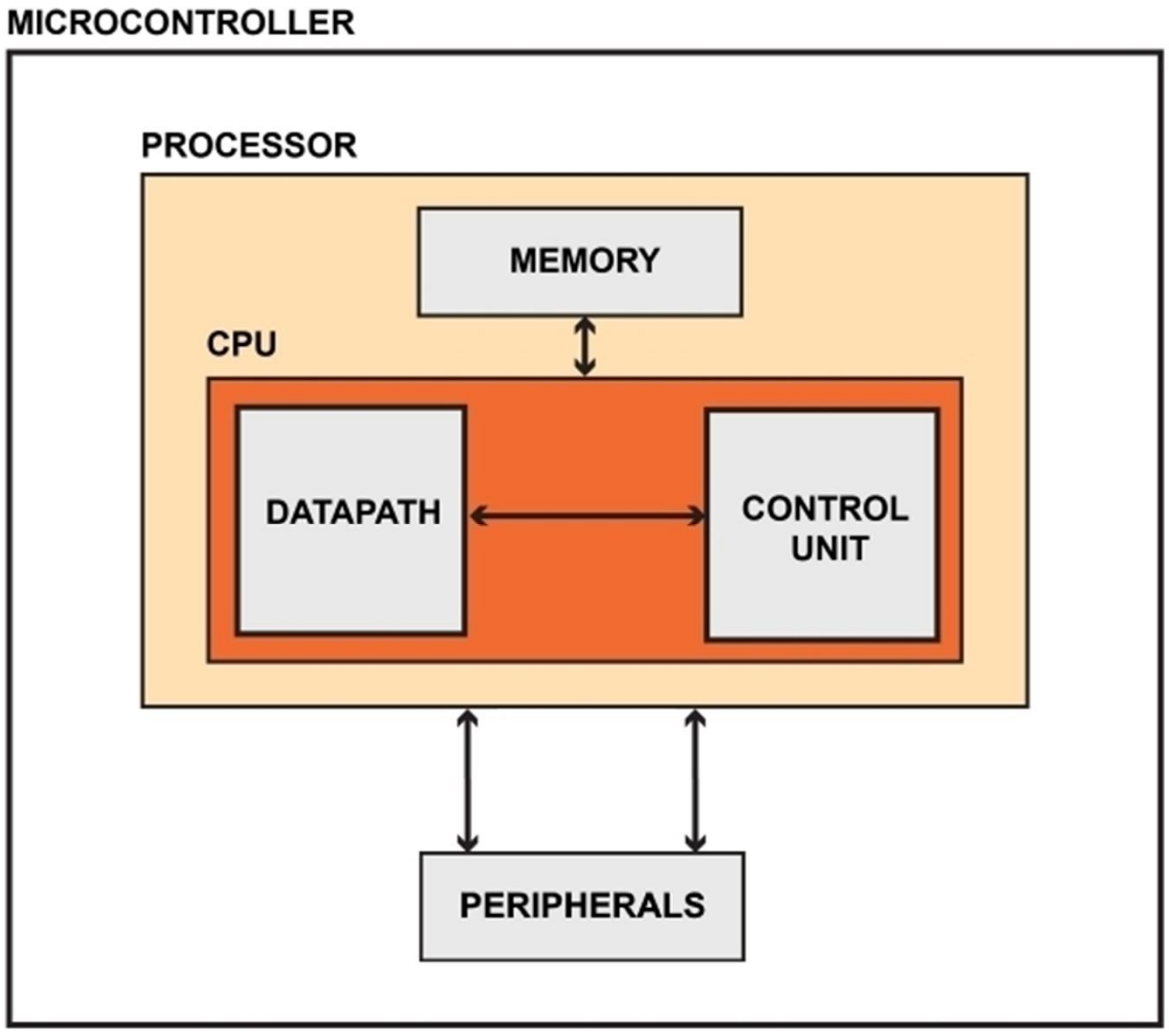


FPGA

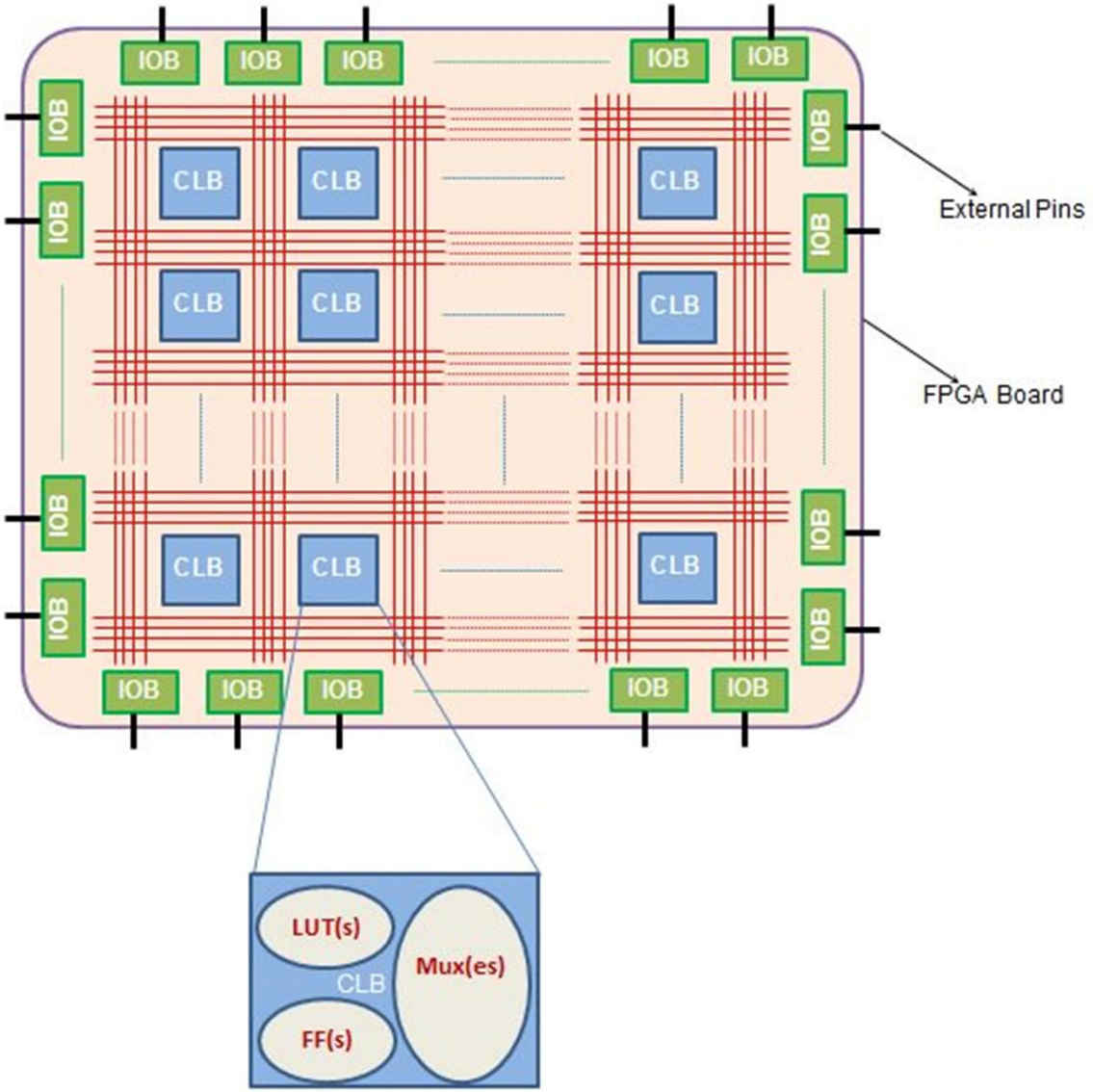
Field Programmable Logic Array (FPGA)

- 2-D array of logic blocks and flip-flops with programmable interconnections
- User can configure
  - Intersections between the logic blocks
  - The function of each block
- FPGAs are usually programmed after being soldered down to the circuit board, in the same way as larger CPLDs
- In most larger FPGAs the configuration is volatile, and must be re-loaded into the device whenever power is applied or different functionality is required

FPGA vs. MicroController



FPGA vs. MicroController

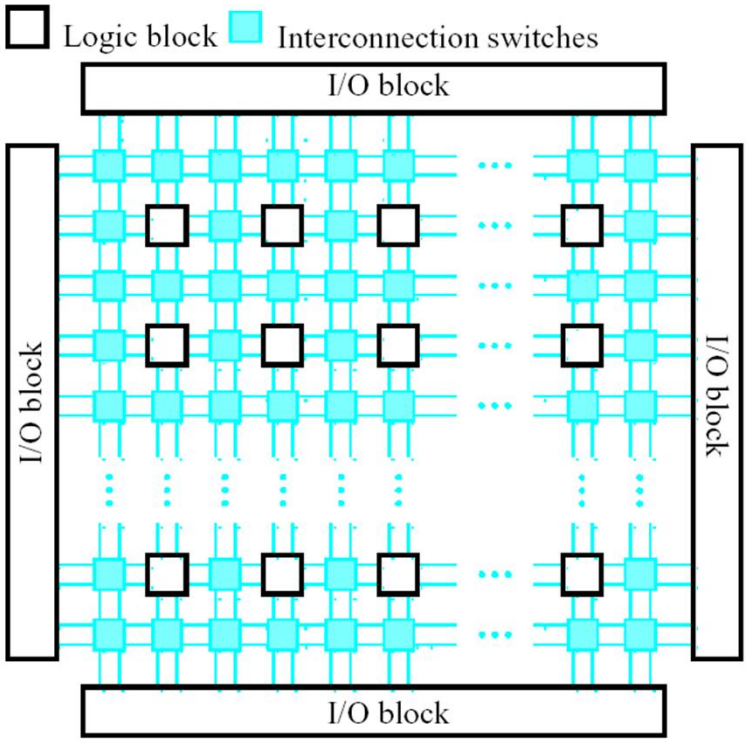


Logic Blocks (LB)

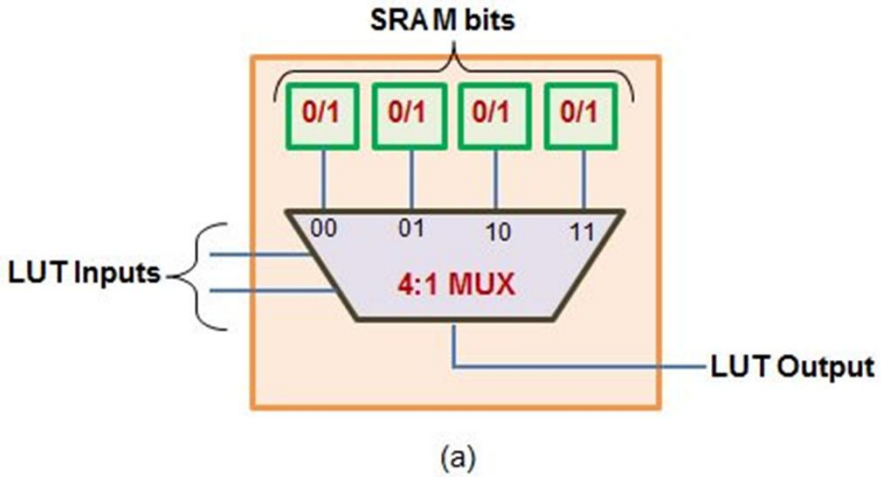
- Purpose: to implement combinational and sequential logic functions.
- Logic blocks can be implemented by:
  - Transistor pairs
  - Multiplexers
  - Look up tables(LUT)
  - Wide fan-in AND-OR structure.

Granularity: is the hardware abstraction level. According to granularity, two types of Blocks :

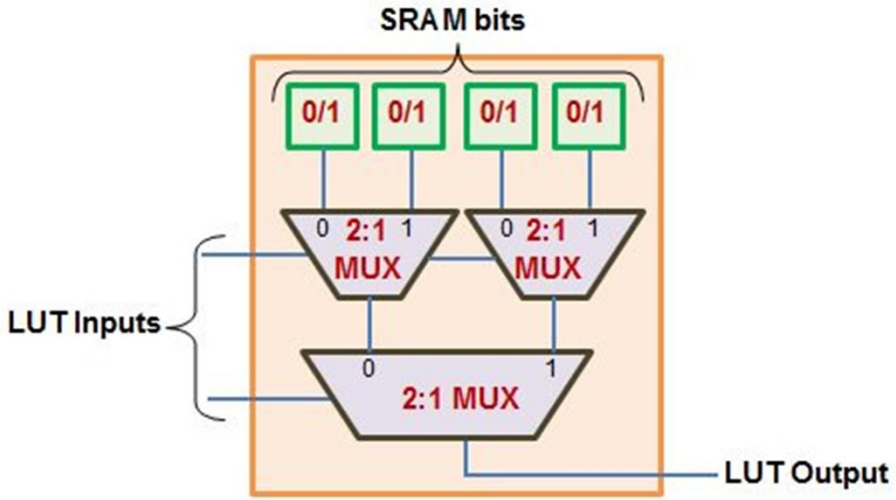
- Fine Grain Logic Blocks
- Coarse Grain Logic Blocks



Look-Up Table (LUT)



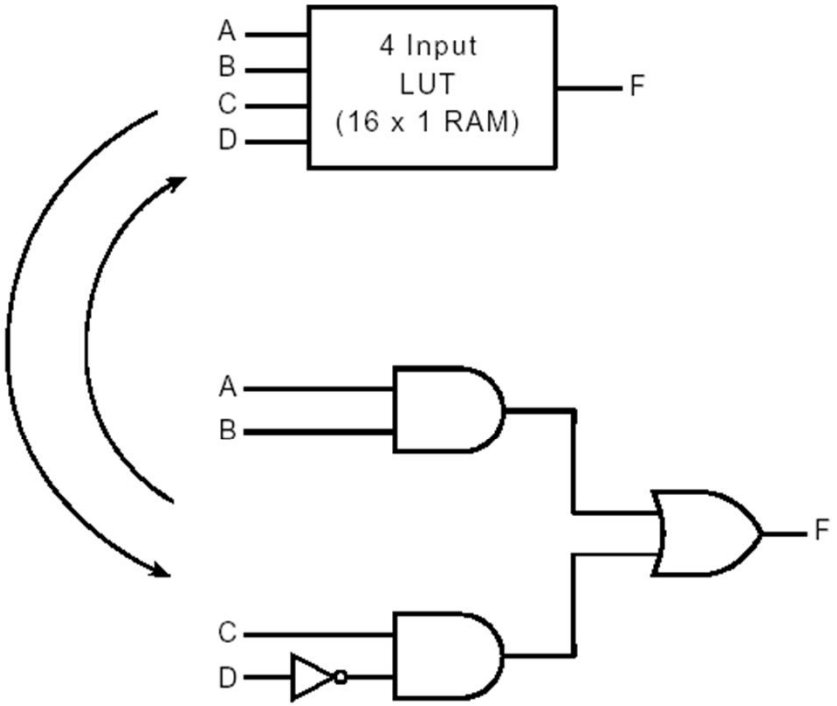
(a)



(b)

Look-Up Table (LUT)

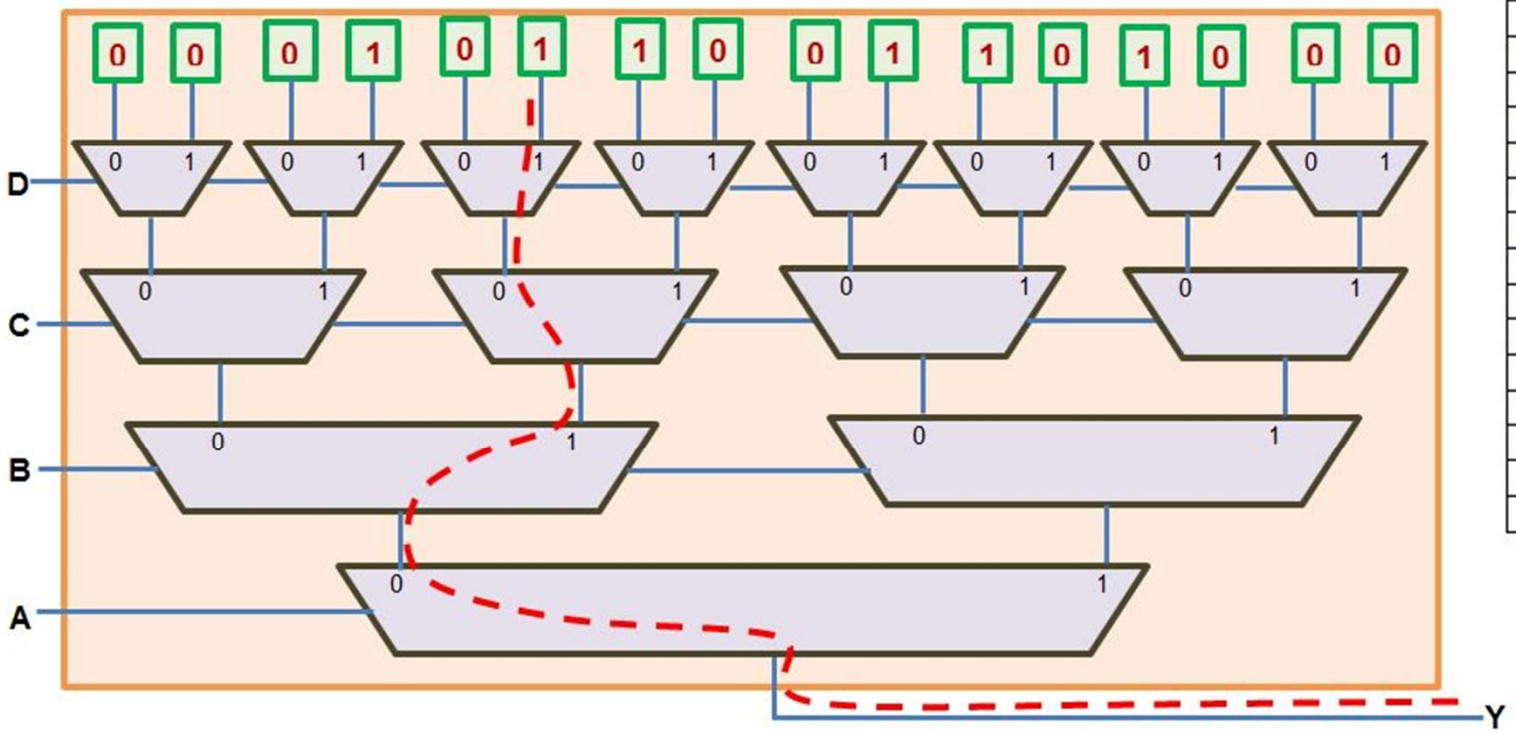
- Output of SRAM gives the logic output
- k-input logic function =2^k size SRAM
- K-input LUT gives 2^2^k logic functions



RAM Contents				
Address				Data
A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Using a lookup table (LUT) to model a gate network.

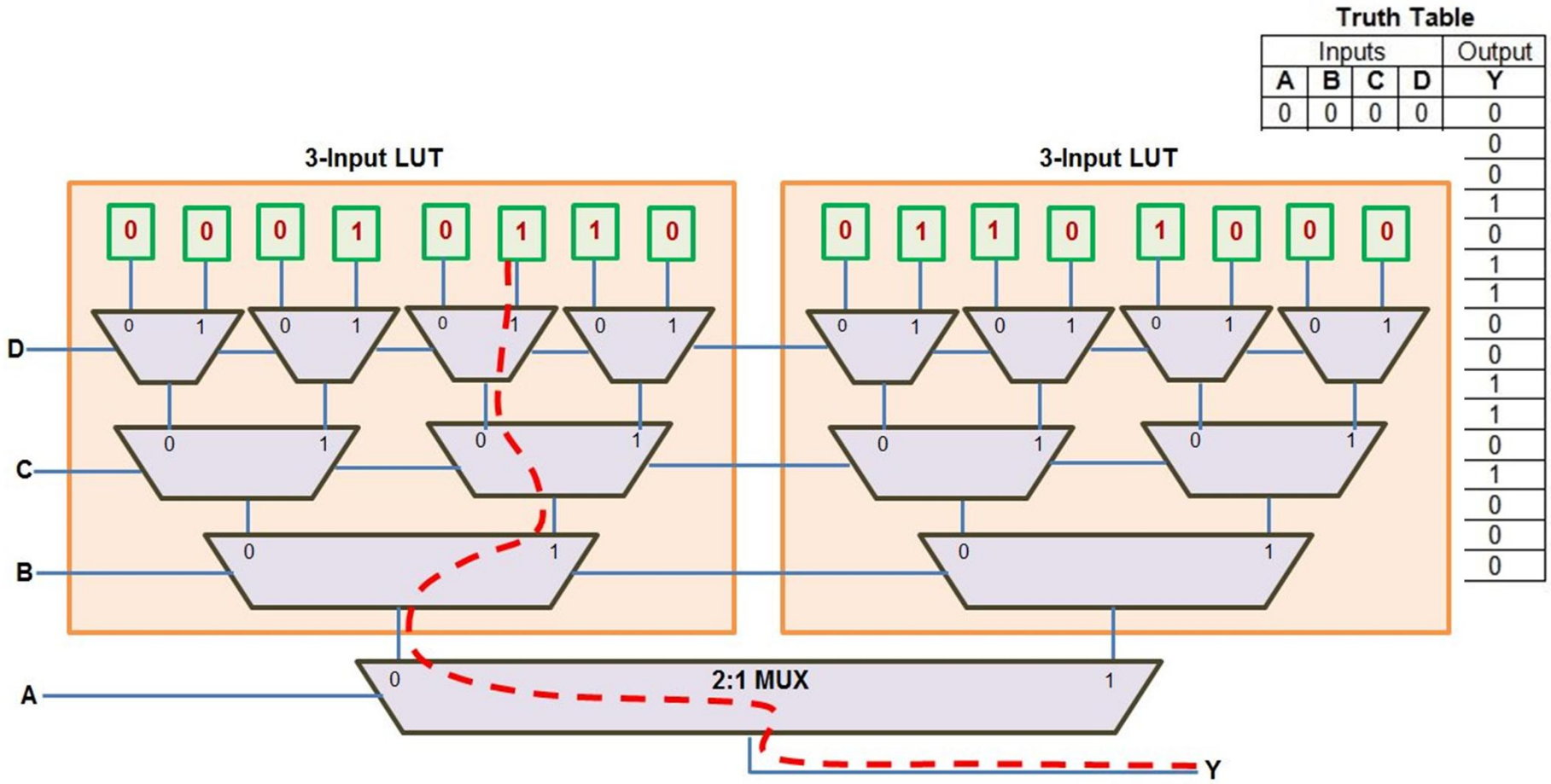
Implementation of Logic Functions using LUT



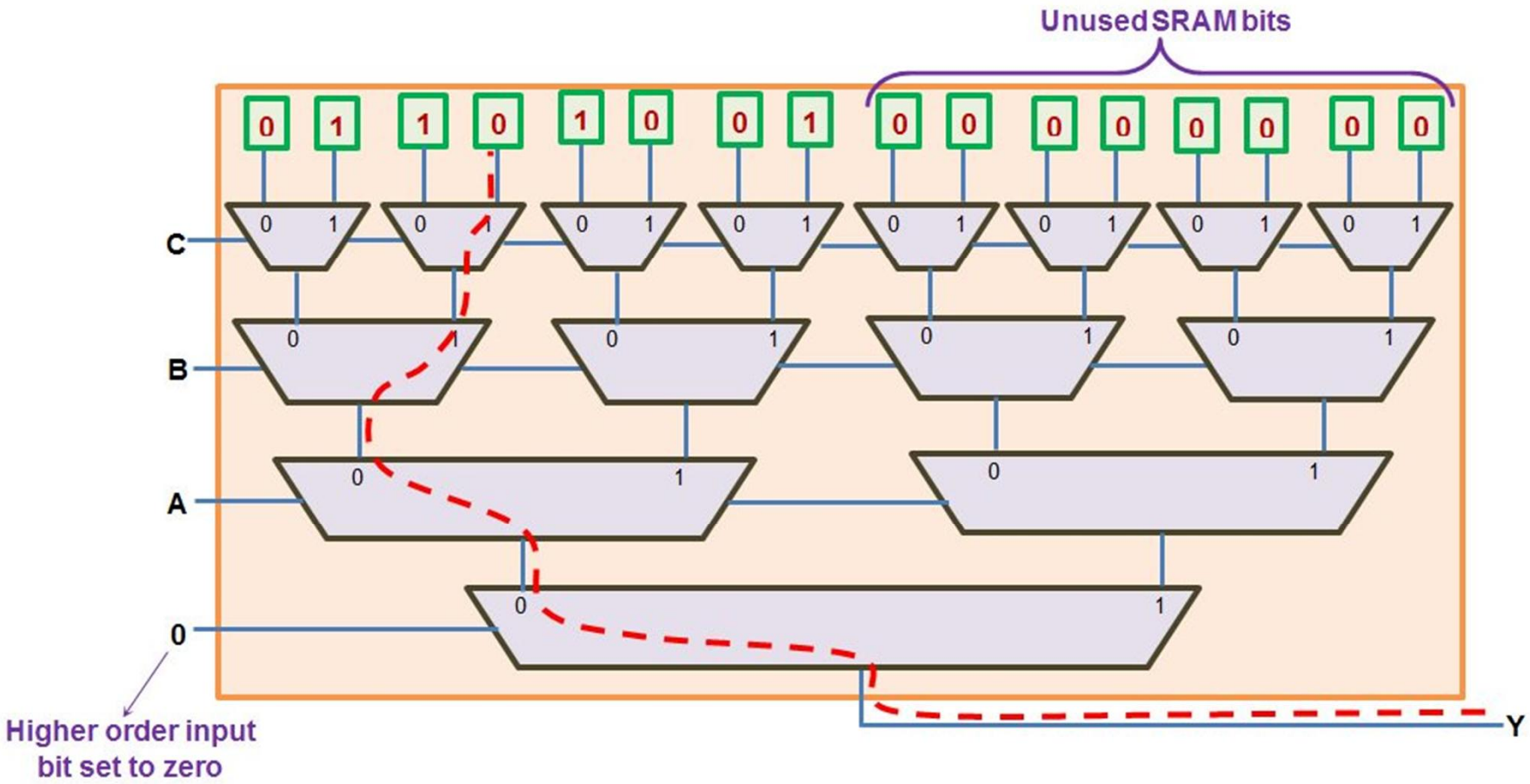
Truth Table

Inputs				Output
A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

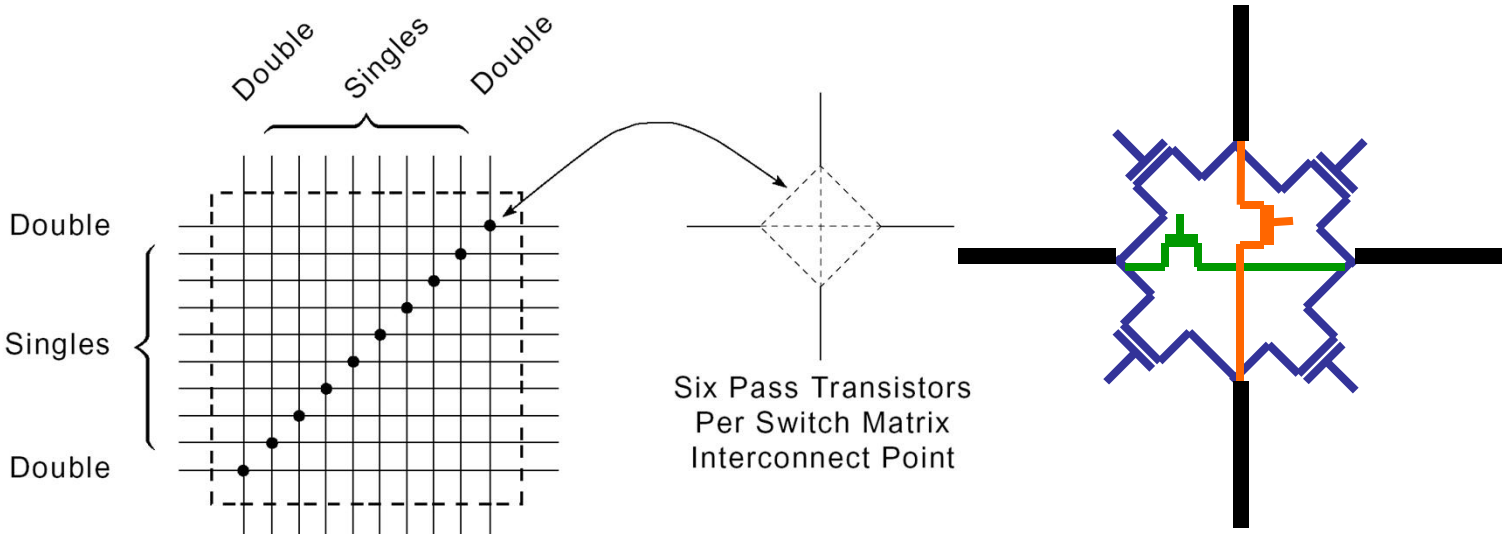
Implementation of Logic Functions using LUT-3 & MUX



Implementation of a 3-input logic function using 4-input LUT



Programmable Switch Matrix (PSM)



SRAM-Based FPGA