Computer-Aided Design

تراشه های منطقی برنامه پذیر 2

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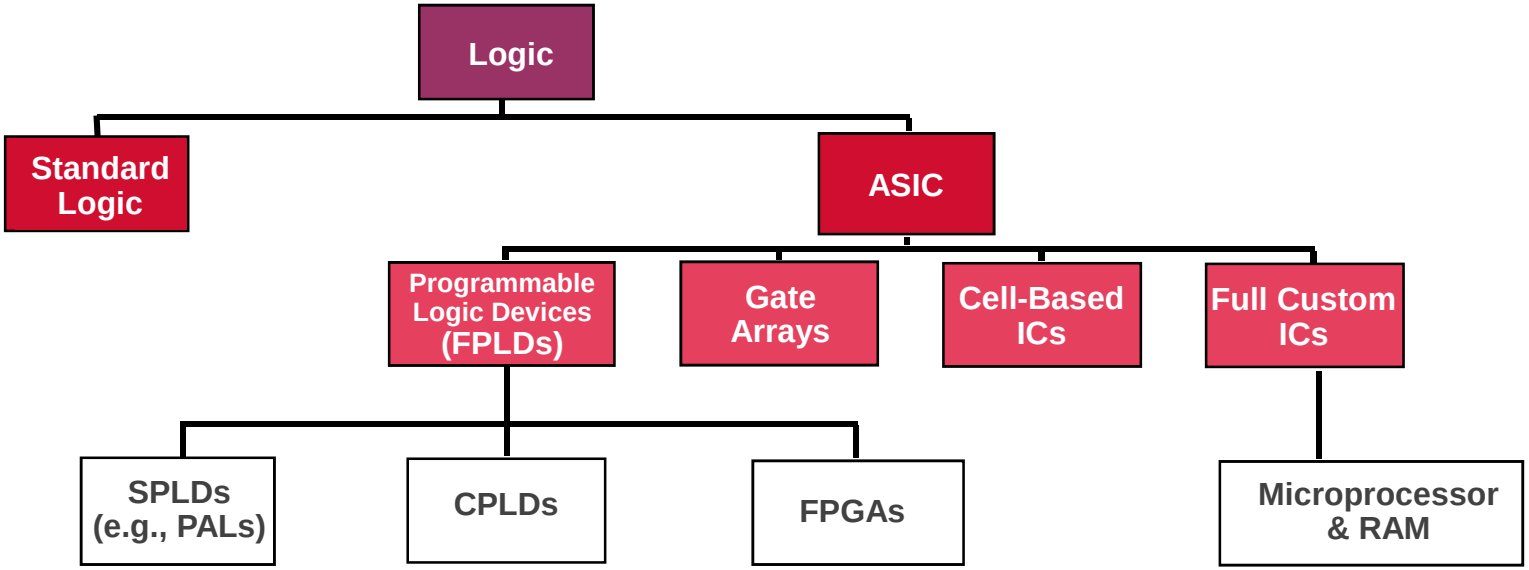
Some slides courtesy of:

- CAD slides, Dr. Saheb Zamani
- allaboutcircuits.com

Digital Circuits



Acronyms

SPLD = Simple Programmable Logic Device
PAL = Programmable Array Logic
CPLD = Complex PLD
FPGA = Field Programmable Gate Array
ASIC = Application Specific IC

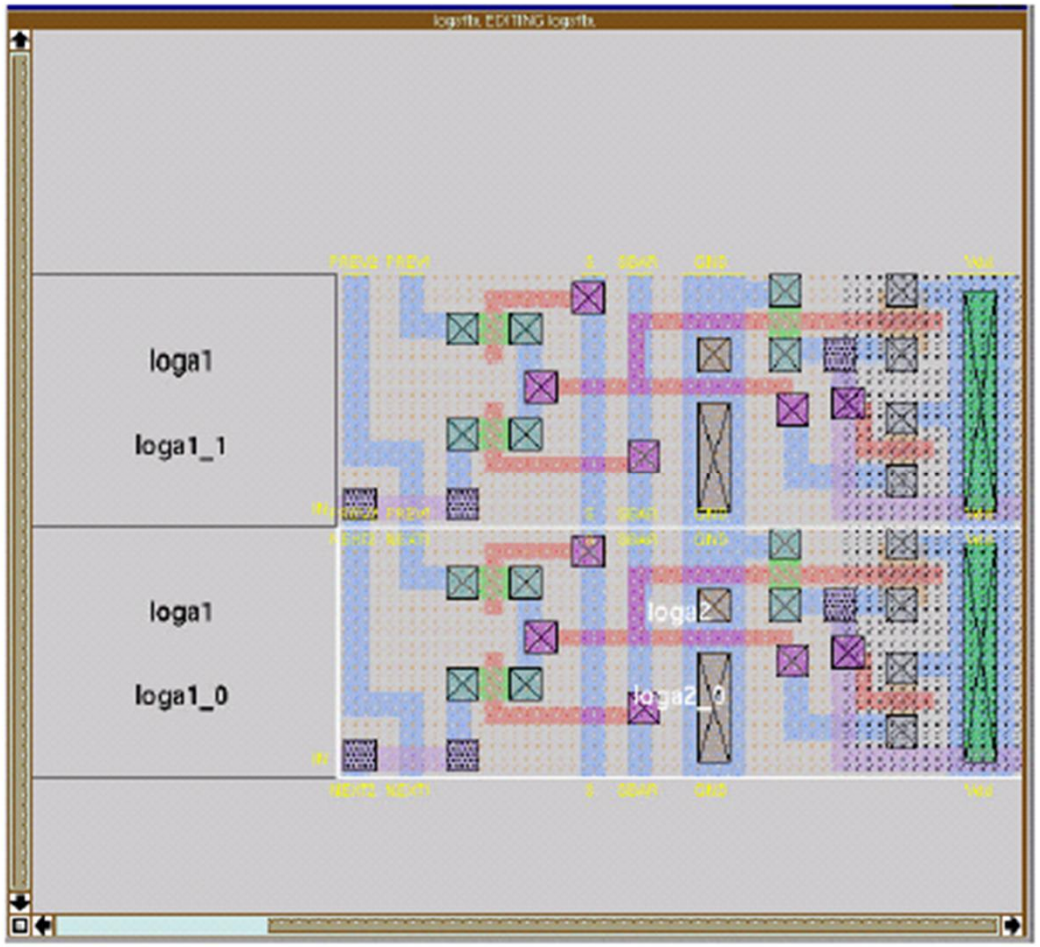
Common Resources

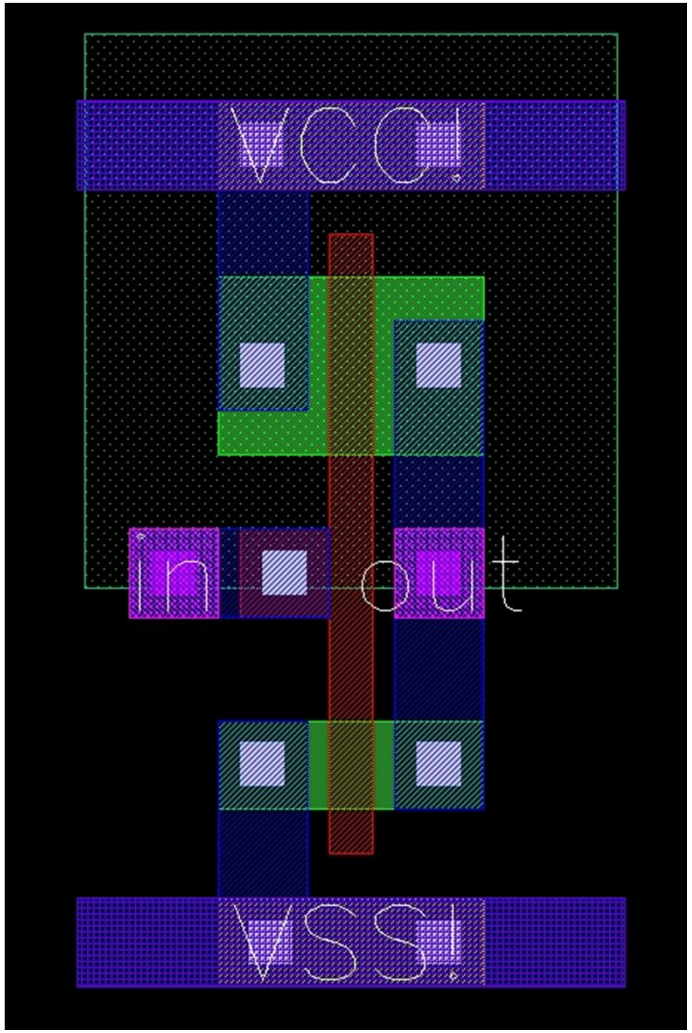
Configurable Logic Blocks (CLB)
- Memory Look-Up Table (LUT)
- AND-OR planes
- Simple gates

Input / Output Blocks (IOB)
- Bidirectional, latches, inverters, pullup/pulldowns

Interconnect or Routing
- Local, internal feedback, and global

Full Custom

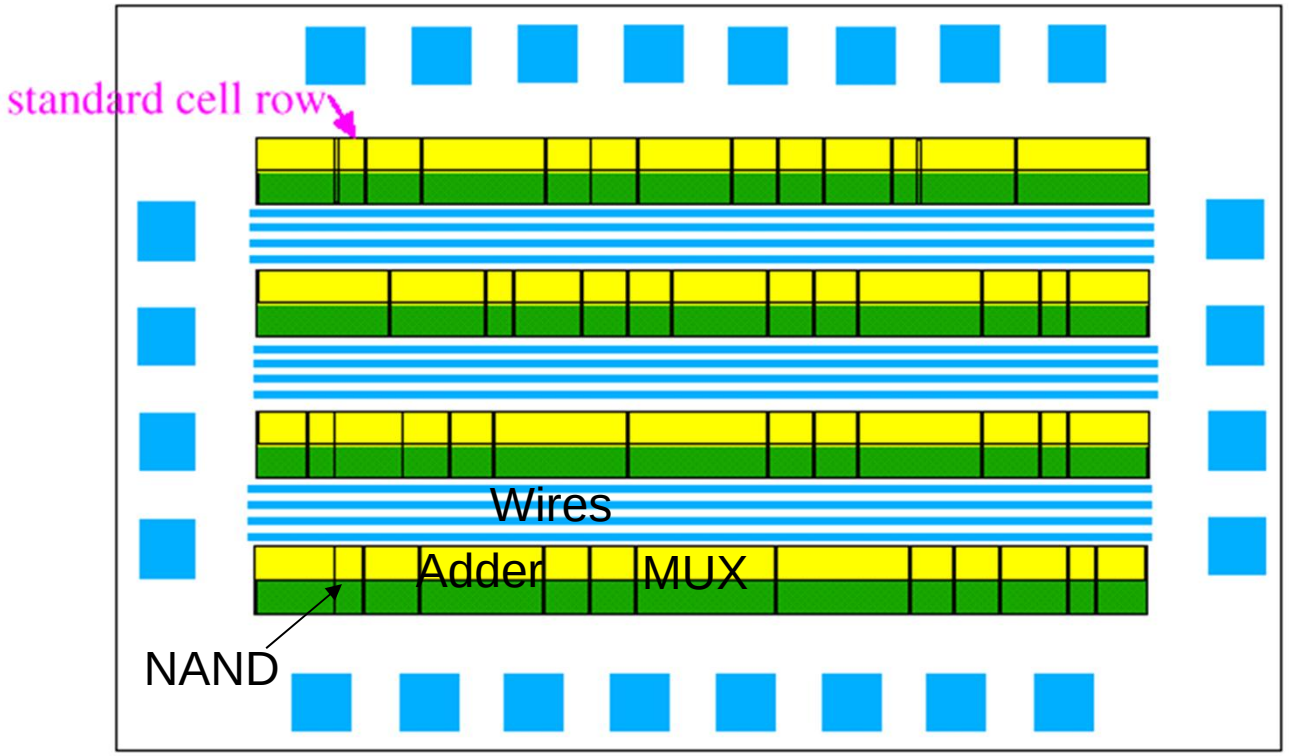




ASIC (Application Specific IC)

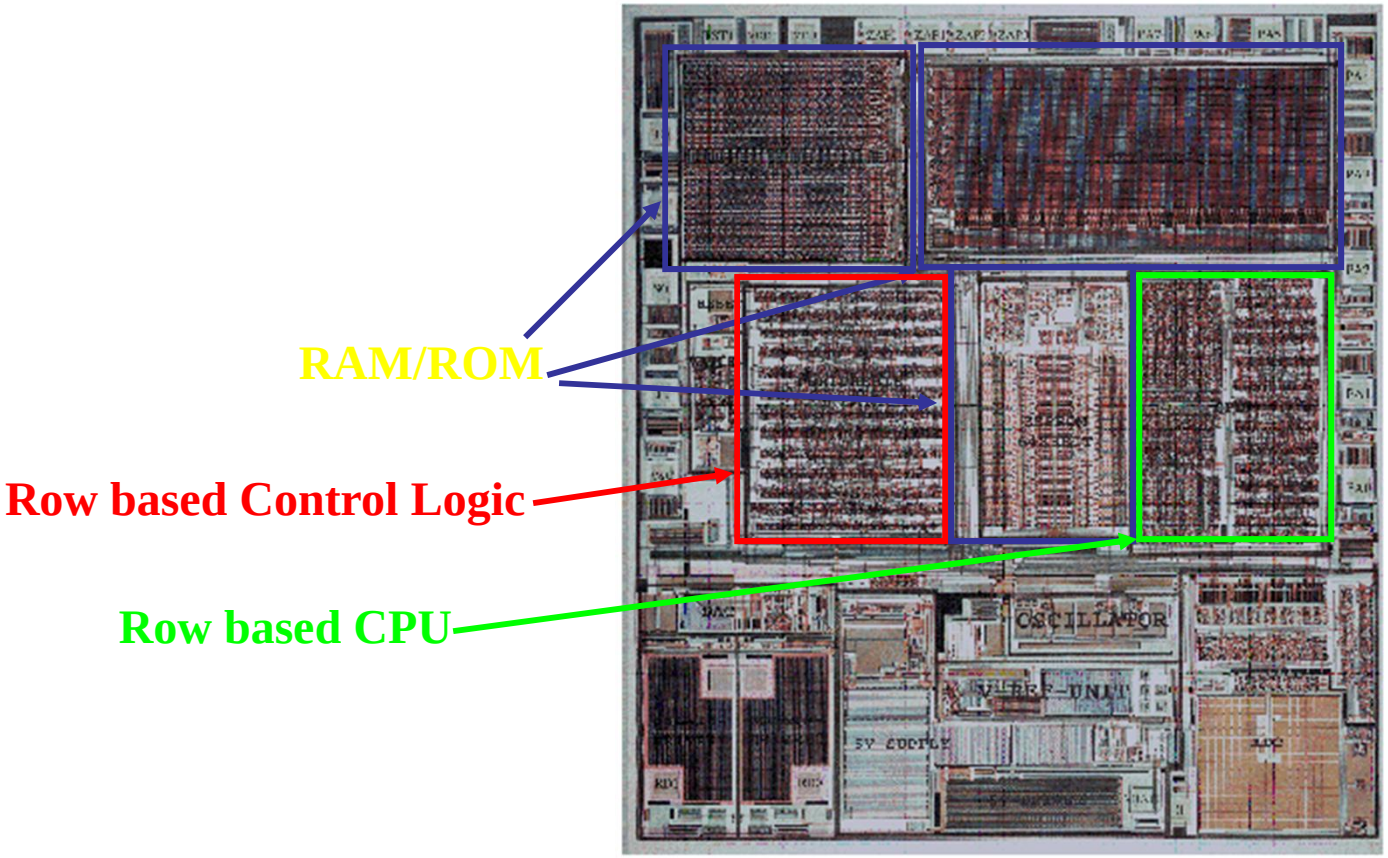
- ASIC: Application-Specific Integrated Circuits
- **Semi-Custom ASIC:**
  - Standard Cells
    - عناصر در ردیفها چیده می شوند
    - پورتها در بالا و پایین سلولها (تکنولوژی جدید: روی سلولها)
  - Gate Array
    - آرایه ای از سلولهای مشابه
  - PLD (Programmable Logic Device)

سلول های استاندارد



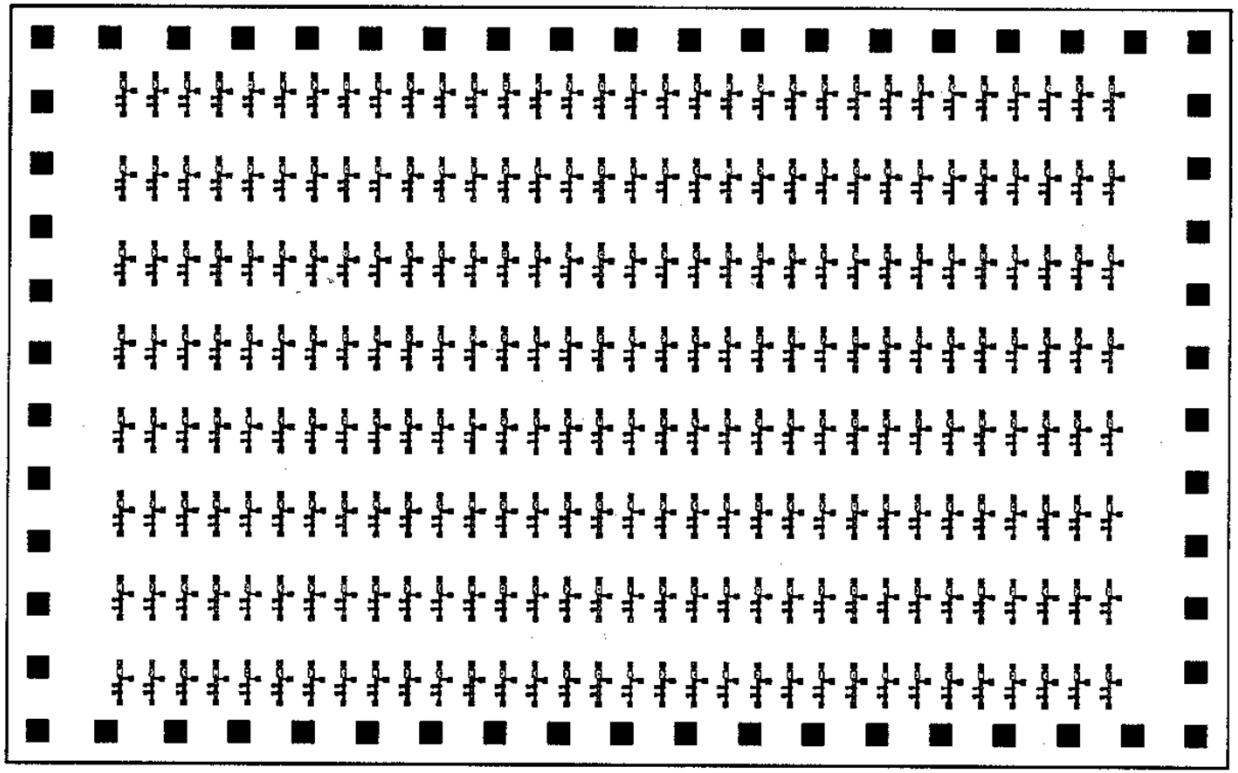
Mixed

- Full custom & Standard cells



Gate Array (Uncommitted)

- Using a prefabricated chip with active devices like NAND-gates
- Later, interconnected according to a custom order by adding metal layers in the factory environment

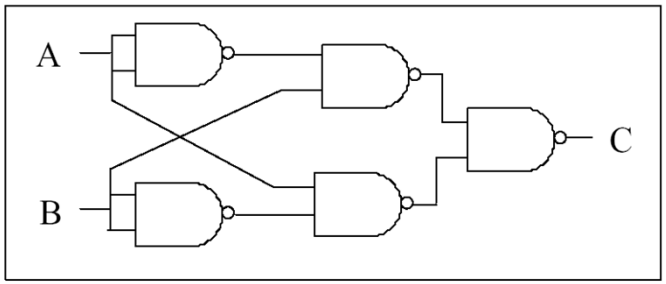


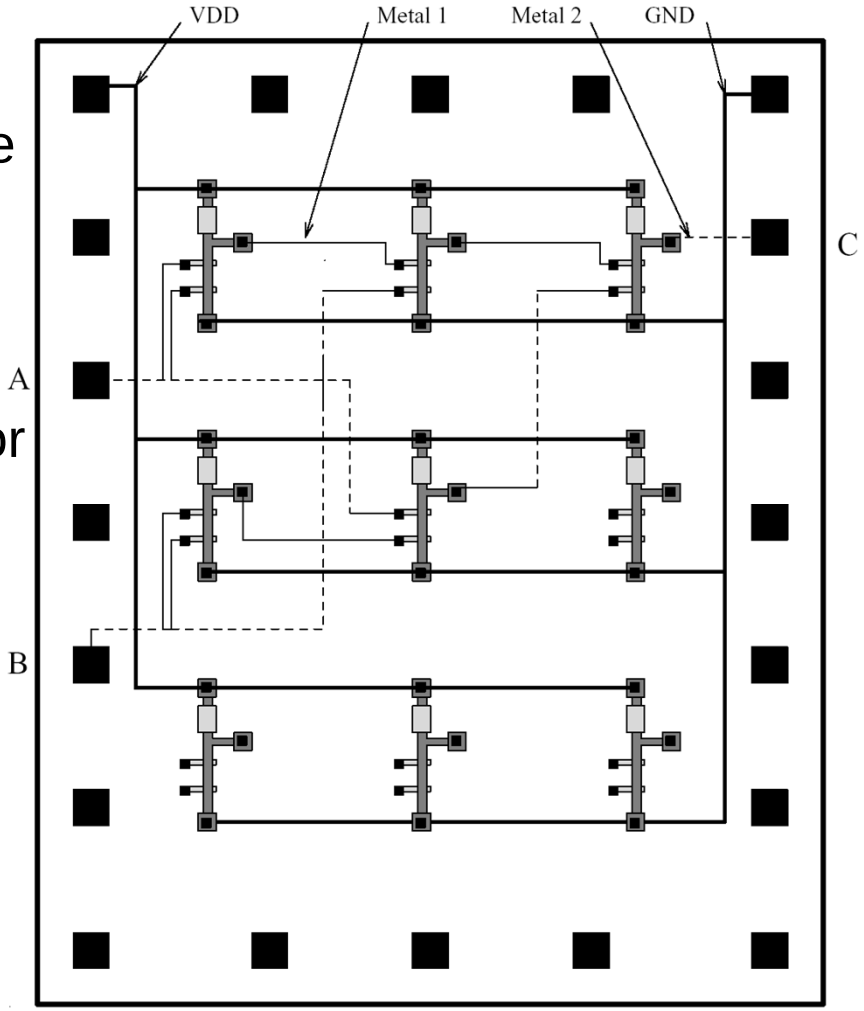
Gate Array (Committed)

- MPGA: mask-programmed gate array
- MPLD: mask-programmed logic device
- A base of pre-designed transistors
- Customized wiring during manufacturing process

→ Each design requires custom masks for wiring

- Mask-making costs

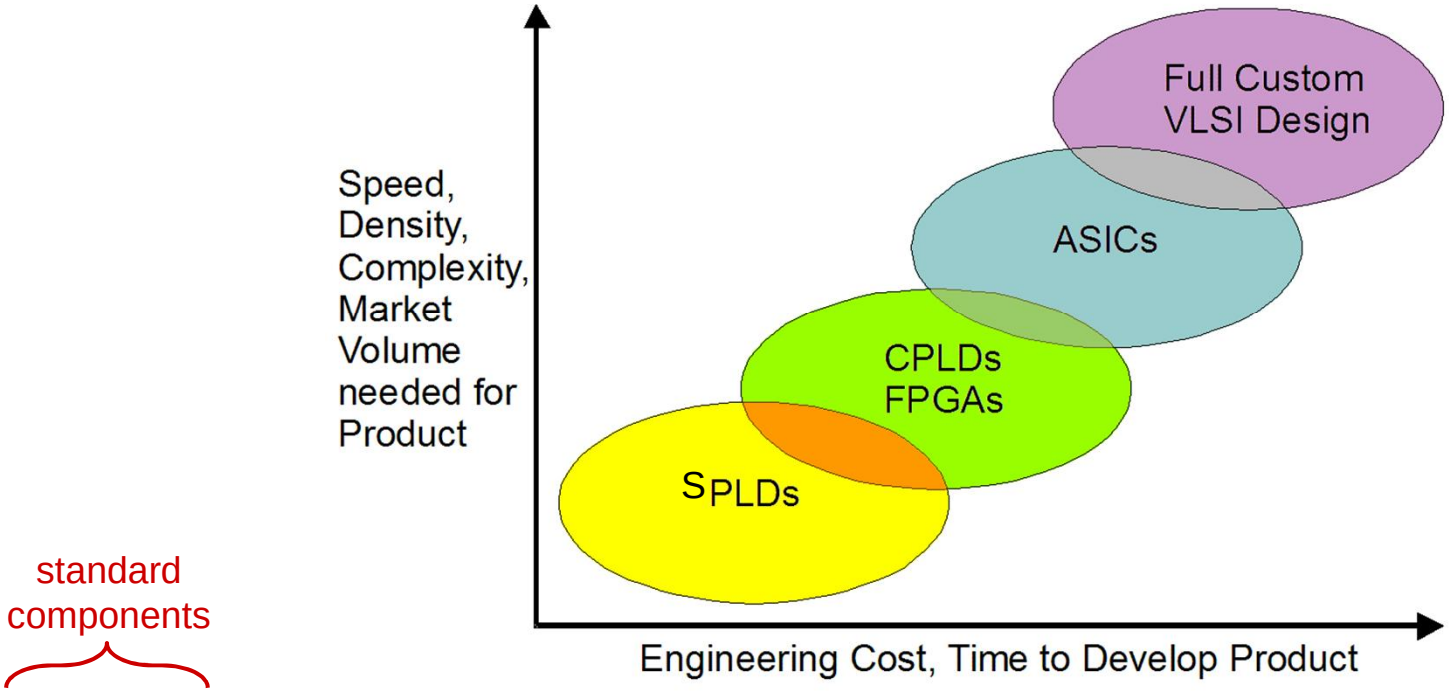


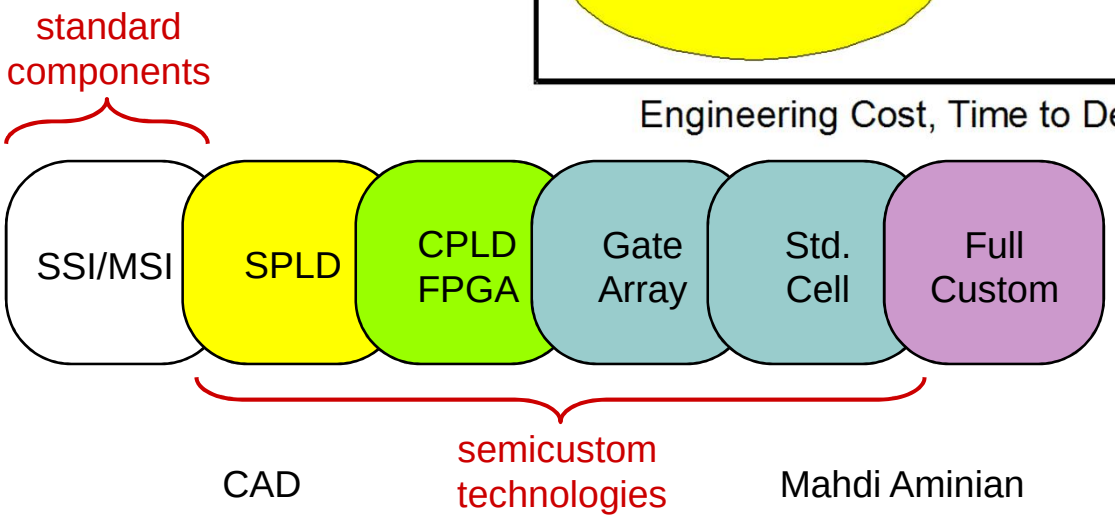


Programmable Logic Device

- A programmable logic device or PLD is an electronic component used to build digital circuits
- Unlike a logic gate, which has a fixed function, a PLD has an undefined function at the time of manufacture
- Before the PLD can perform in a circuit it must be programmed

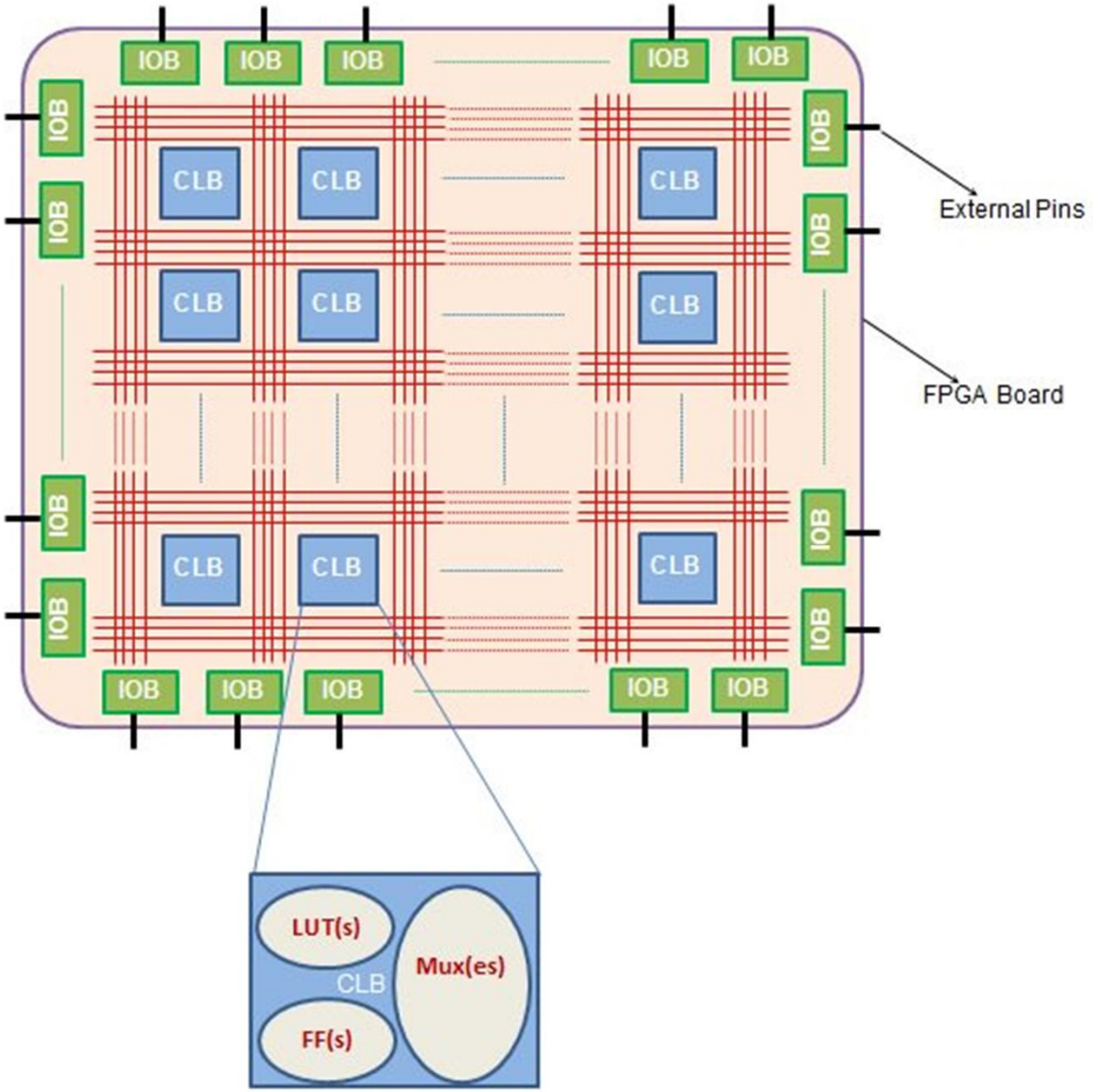
Digital Technology Tradeoffs



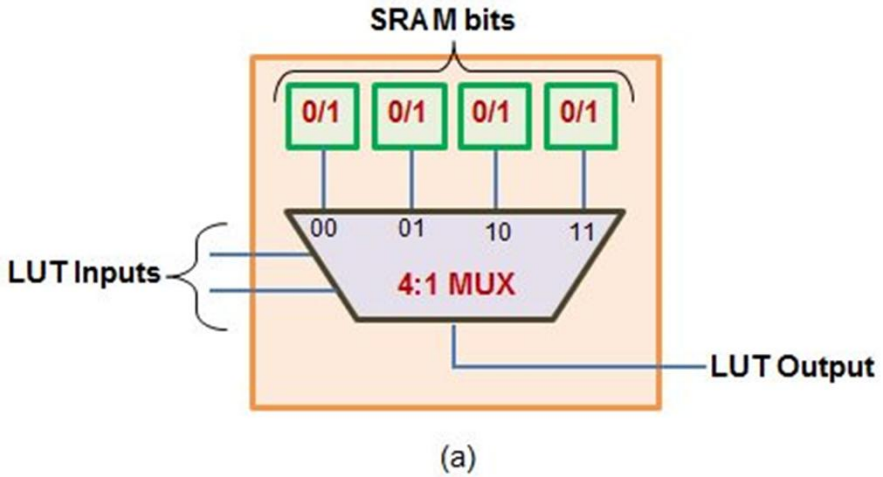


FPGA

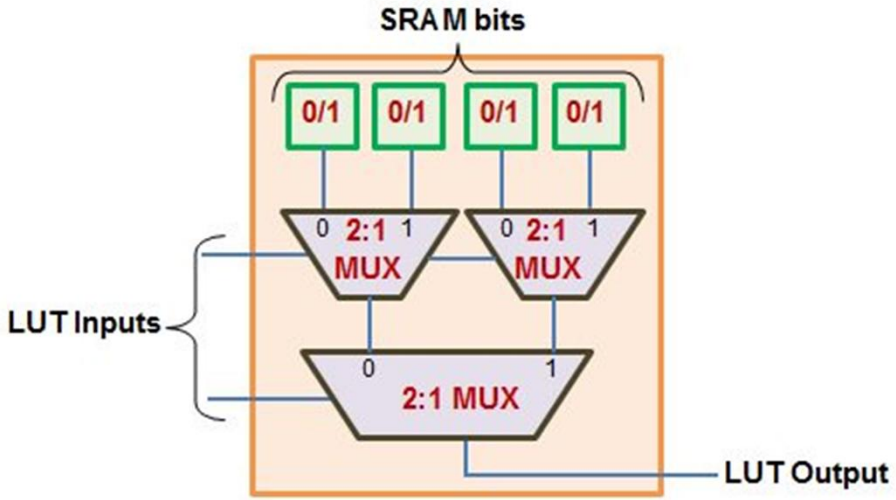
FPGA



Look-Up Table (LUT)



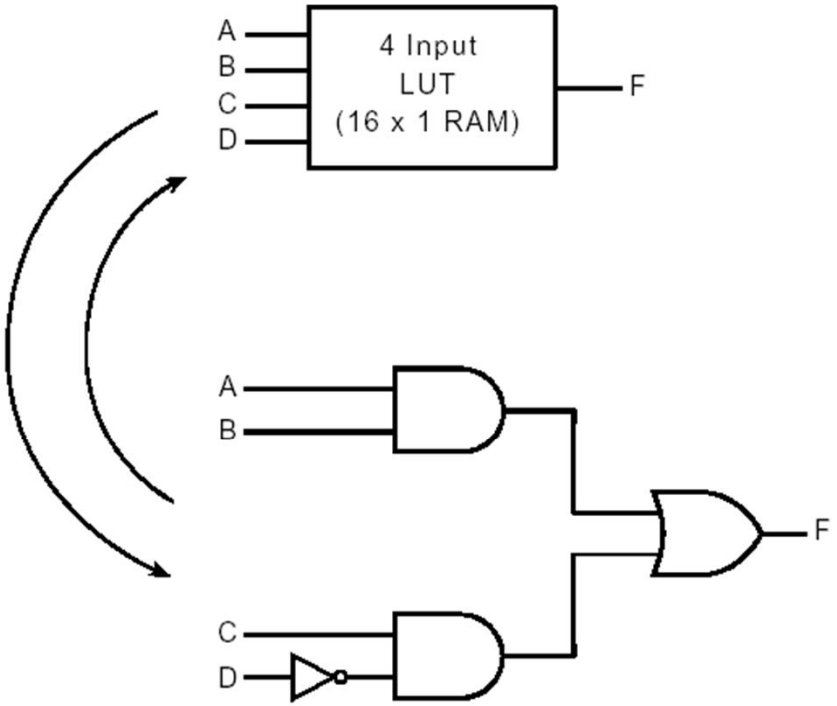
(a)



(b)

Look-Up Table (LUT)

- Output of SRAM gives the logic output
- k-input logic function =2^k size SRAM
- K-input LUT gives 2^2^k logic functions



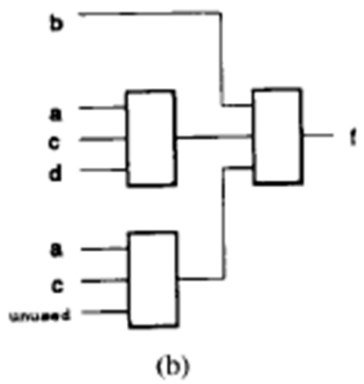
RAM Contents				
Address				Data
A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Using a lookup table (LUT) to model a gate network.

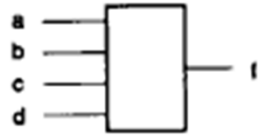
Effects of Granularity on FPGA Density and Performance

- Tradeoff
  - Granularity increase → Blocks less
  - More Functional Blocks → more area

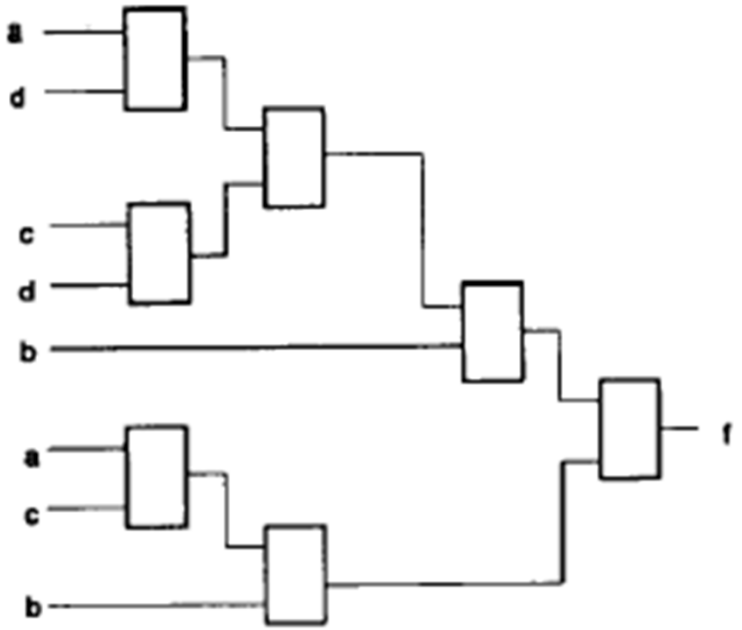
Area is normally measured by total number of bits needed to implement the design. So look the example



(b)

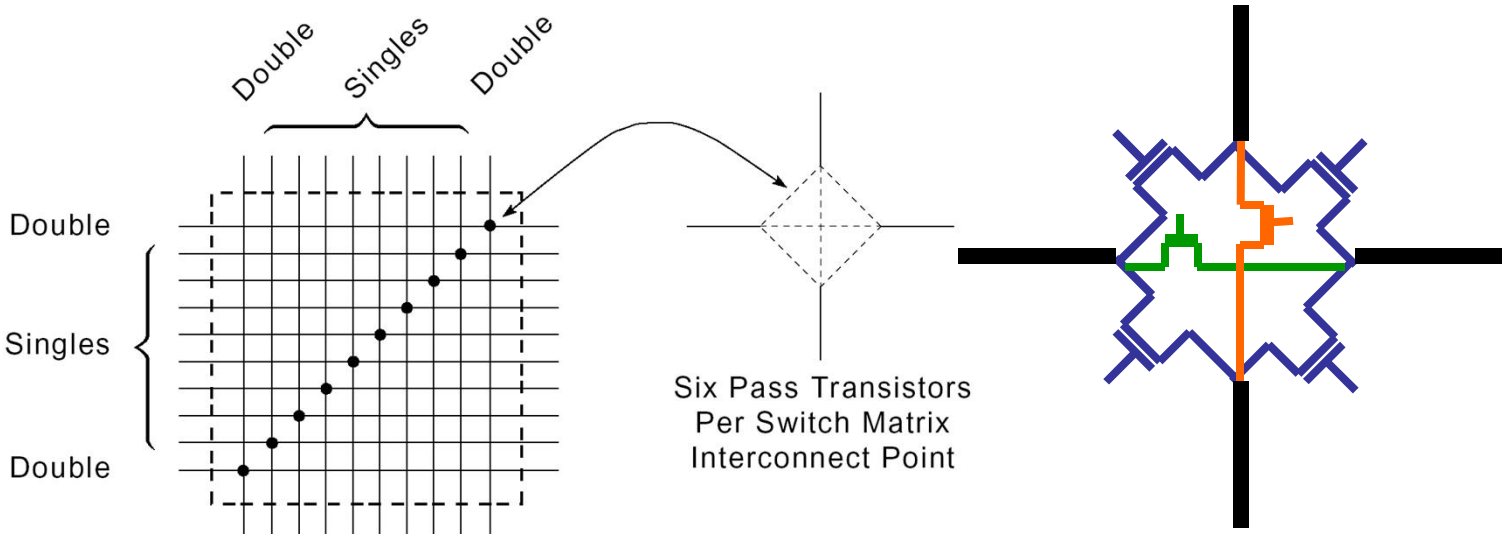


(c)

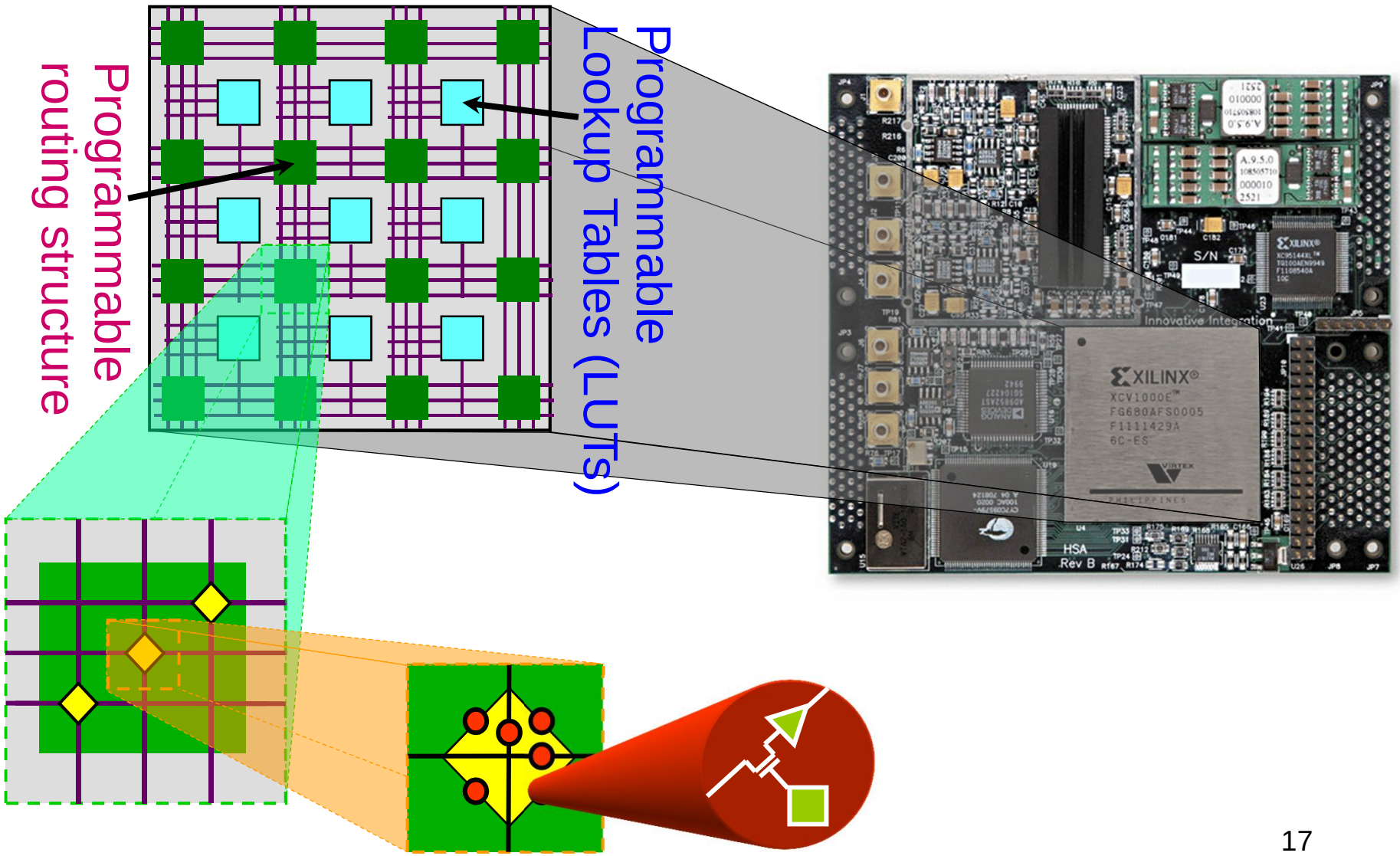


Three implementations of $f = abd + bc\bar{d} + \bar{a}\bar{b}\bar{c}$.

Programmable Switch Matrix (PSM)

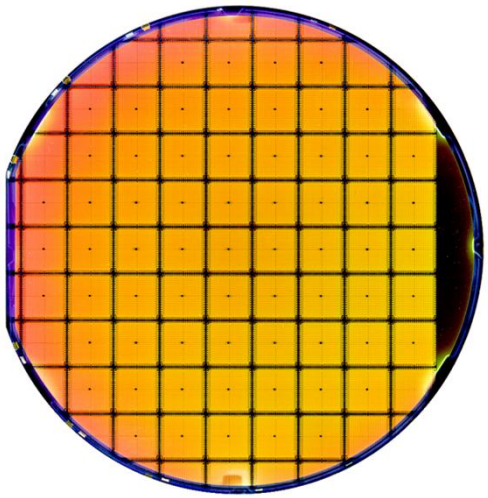


SRAM-Based FPGA

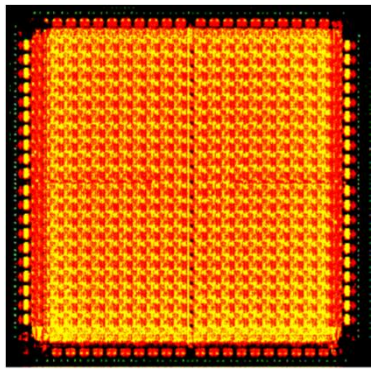


FPGA ARCHITECTURE

FPGA

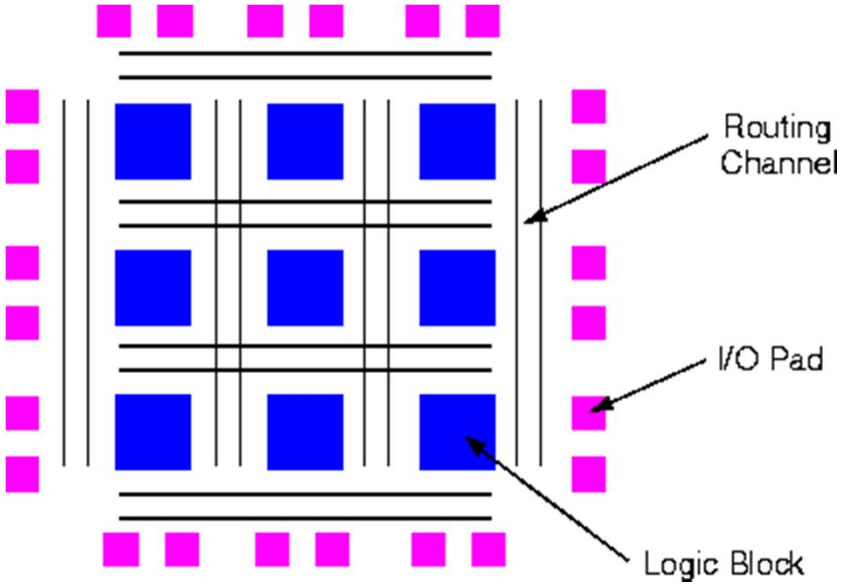


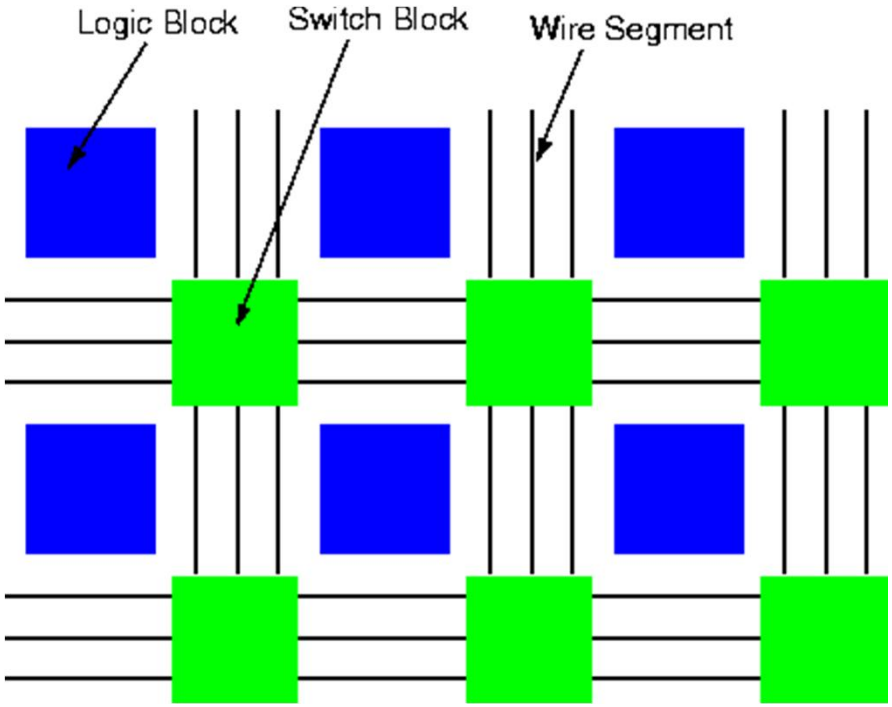
Silicon wafer containing XC4010E 10,000 gate FPGAs.



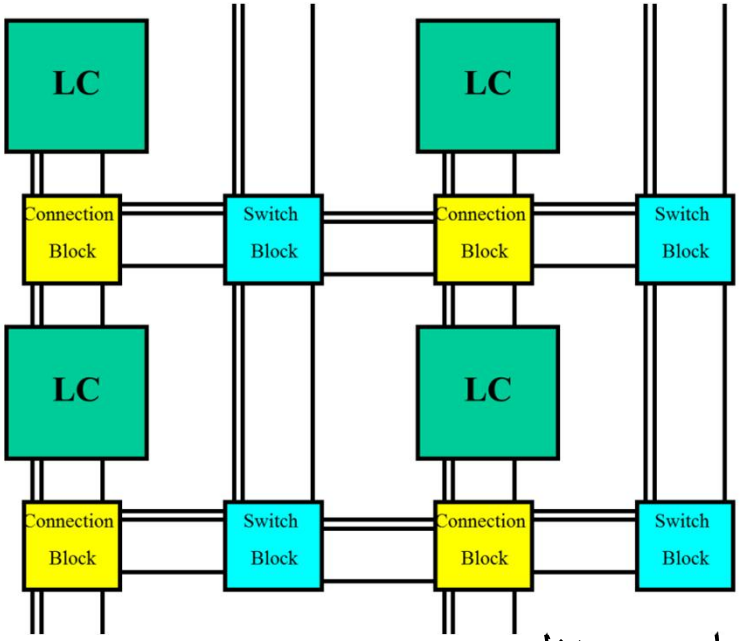
die showing 20 by 20 array of logic elements and interconnect.

FPGA Architecture





Routing Criteria



- Routability •
- سرعت: تعداد سوییچها در مسیر
- فضا.

- منابع اتصالی کم ß کاهش امکان پیاده سازی مدار مورد نظر
- منابع اتصالی زیاد ß اتلاف مساحت و کاهش بخش های منطقی

Terms Definition

- Wire Segment: قطعه سیمی که به یک سوییچ برنامه پذیر منتهی شده است.
  - یک یا چند سوییچ می تواند به یک wire segment وصل شده باشد.
- Track (شیار): دنباله ای از یک یا چند wire segment در امتداد یک خط.
- Channel: گروهی از Trackهای موازی.
- Connection Block: اتصال از ورودیها و خروجیهای یک LC به wire segmentهای کانال.
- Switch Block: اتصال بین wire segmentهای افقی و عمودی.

Routing Structure Example

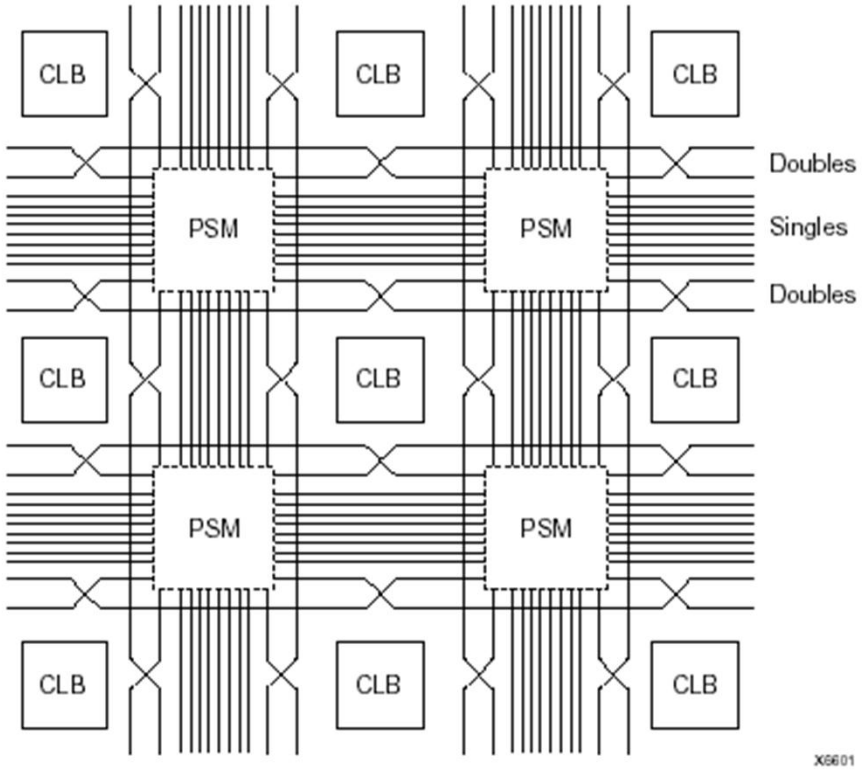


Figure 28: Single- and Double-Length Lines, with Programmable Switch Matrices (PSMs)

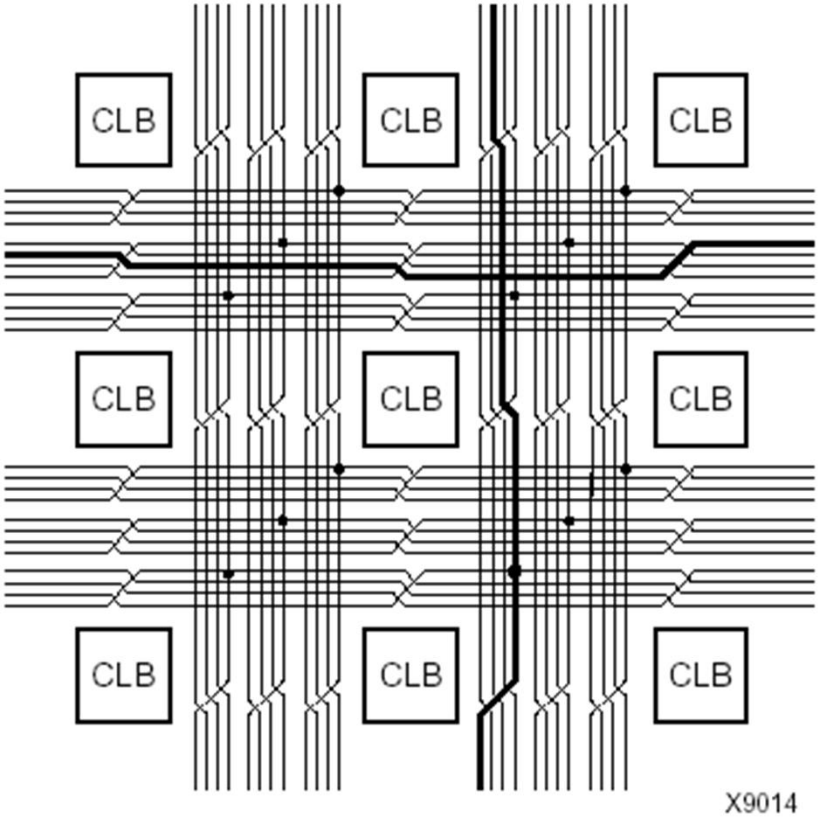
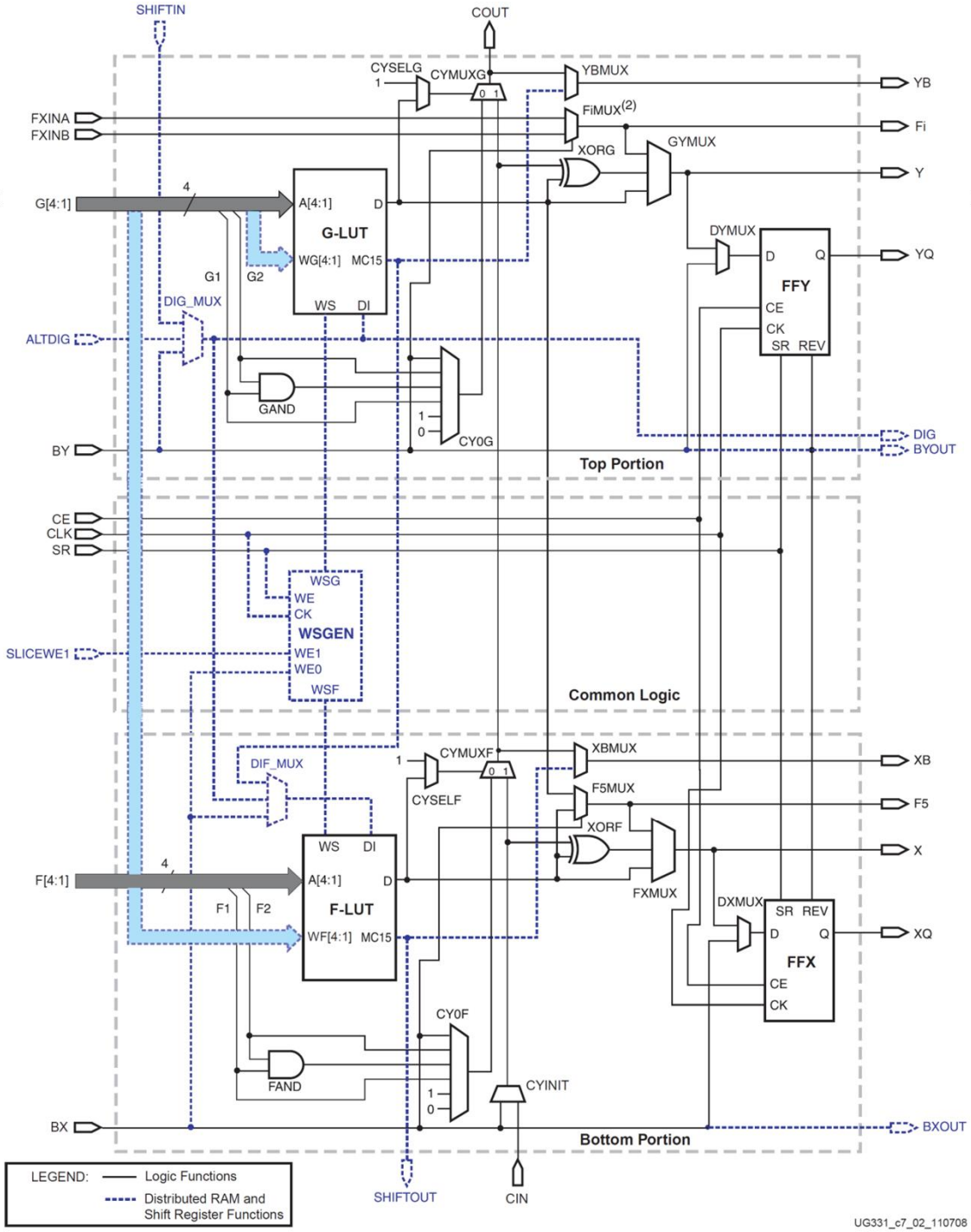


Figure 29: Quad Lines (XC4000X only)

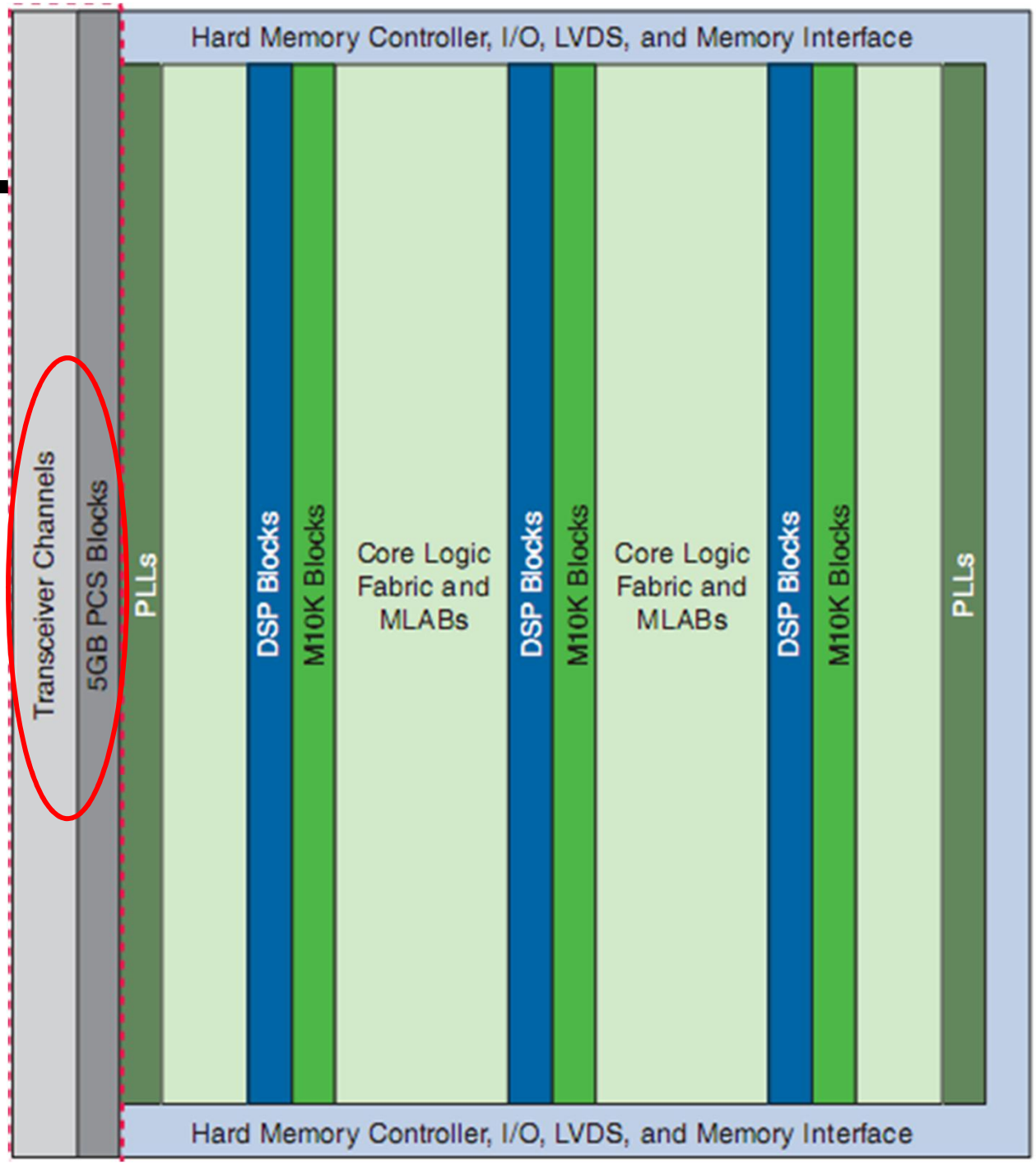
Spartan Logic Cell



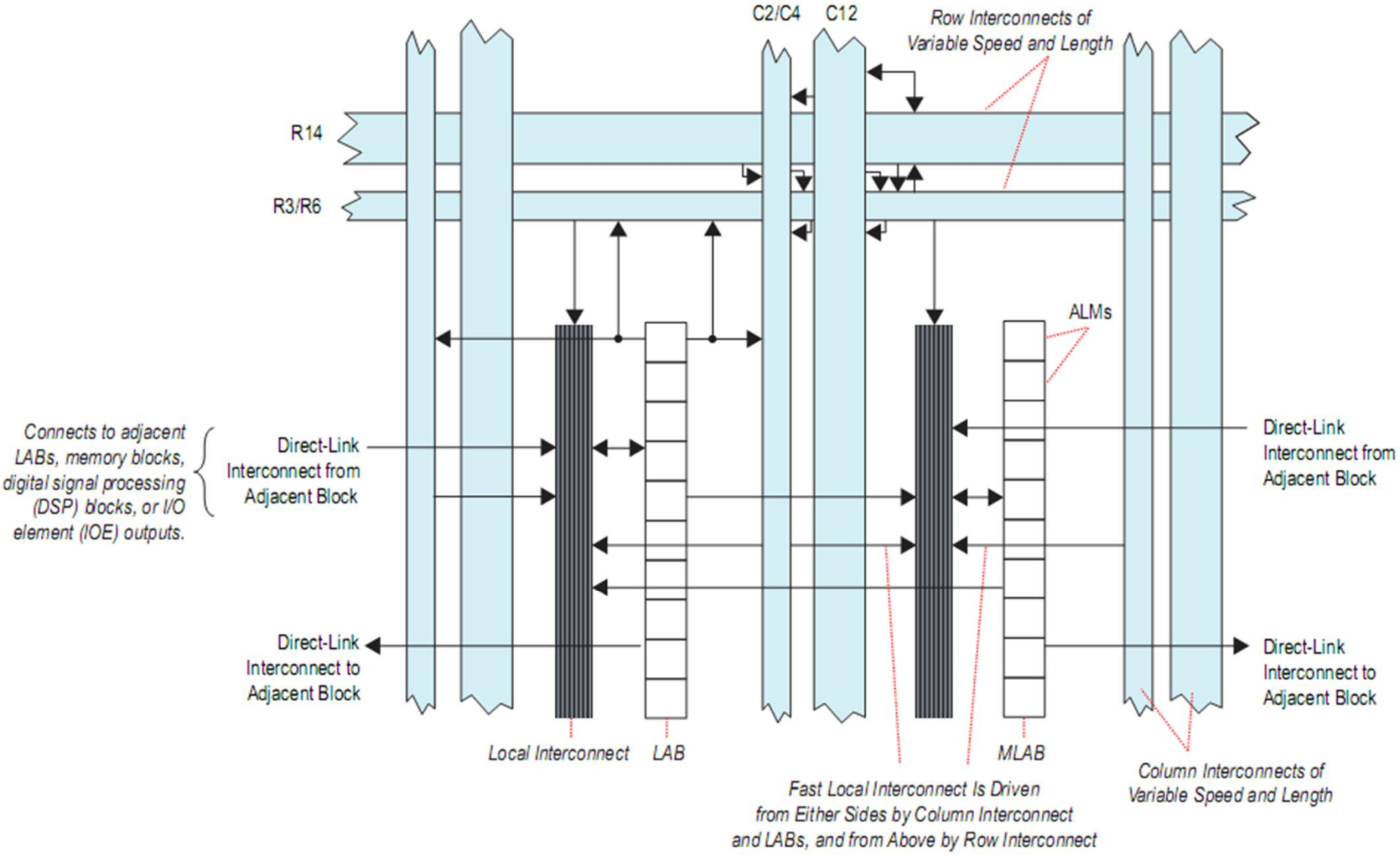
Cyclone FPGA

- SRAM-based

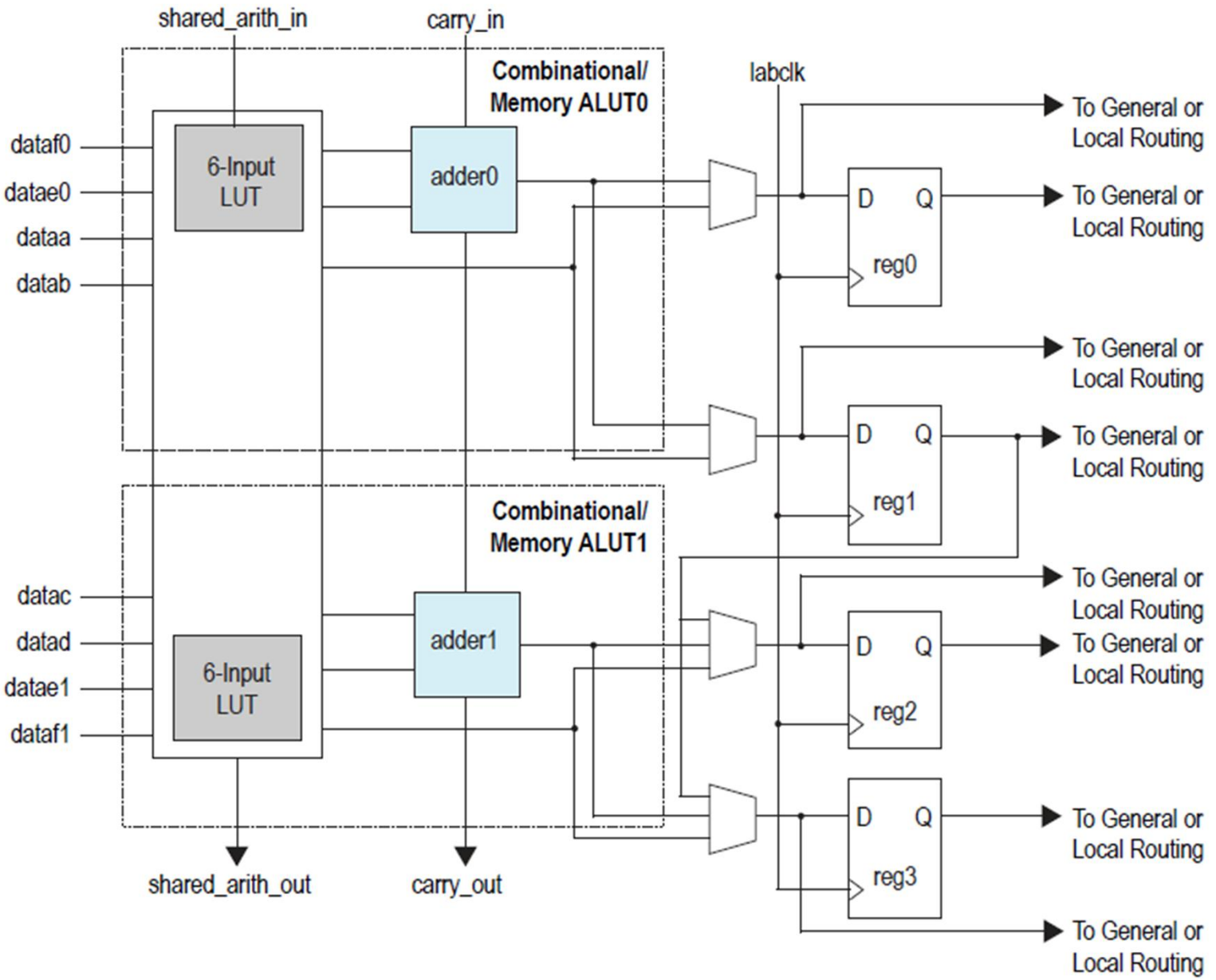
Gigabit Transceiver Blocks



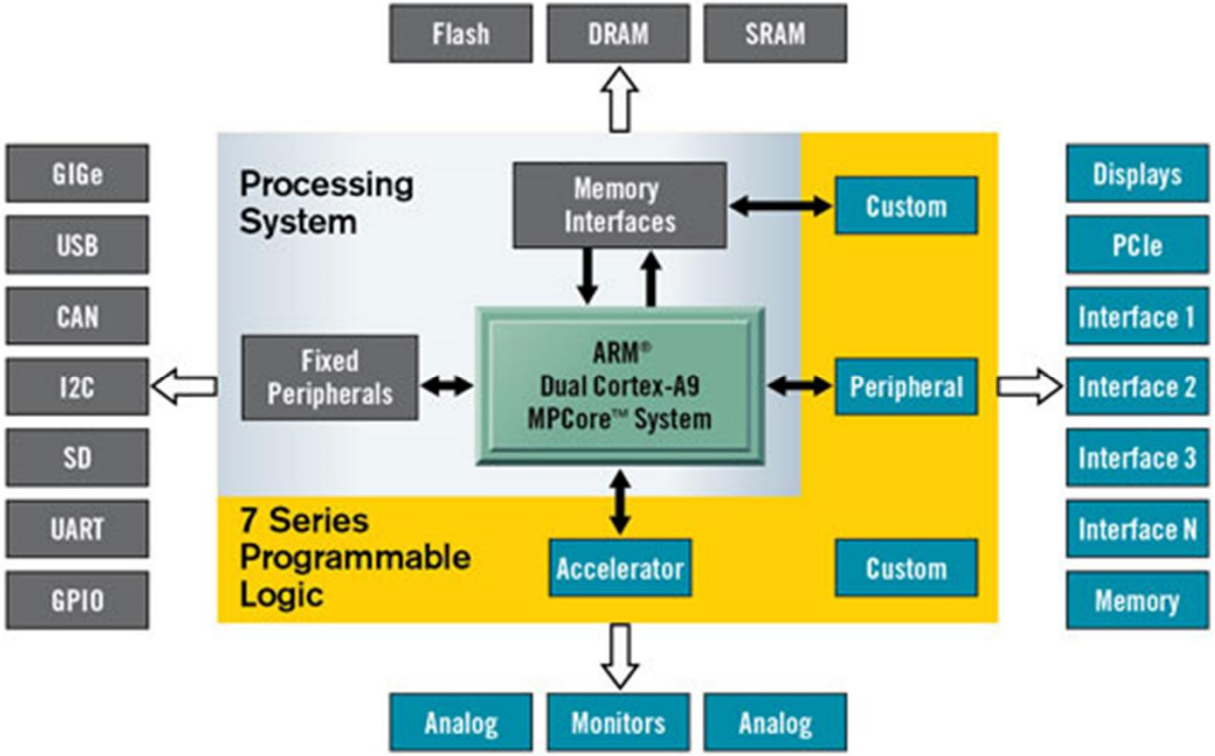
Cyclone V Architecture



ALM Structure



Advanced FPGA Architectures



The Xilinx **Zynq-7000 AP** SoC product line provides scalable performance and configuration serving a wide range of applications needs. The combination of the ARM® dual-core Cortex™-A9 MPCore™ processing system and 7 series programmable logic provides a computing platform. Zynq-7000 AP SoC is ideal for solutions requiring advanced system control combined with sophisticated signal processing.