Parameter	Value	Type
in_width	8	Signed Integer
out_width	32	Signed Integer

FP_COPROCESSOR
in1[31..0]　　fp_out[31..0]
in2[31..0]　　NaN
opcode[4..0]　　UF
clock　　OF
DIVISION_BY_ZERO

MULTIPLEXER
data1[31..0]
data0[31..0]　　result[31..0]
sel0

PC_MUX
data3a[31..0]
data2a[31..0]
data1a[31..0]　　result[31..0]
data0a[31..0]
sel0

PC_ADDER
result[31..0]
data[31..0]　　A+B

INSTRUCTION_MEMORY_2
address[7..0]　　q[31..0]
clock　　Block Type: AUTO

control_unit
clk
instruction[31..0]
clk
rst
coP_NaN_Flag
coP_UF_Flag
coP_OF_Flag
coP_Division_by_zero_flag

reg0[4..0]
reg1[4..0]
reg2[4..0]
s_r_amount[4..0]
im_data[31..0]
register_write_word_enable
register_write_byte_enable
alu_opcode[4..0]
jump_mux_signal1
write_back_on_register_mux_signal
alu_input_mux_signal
alu_or_coprocessor_mux_signal
PC_enable
memwrite_enable_a
memwrite_enable_b
memread_enable_a
memread_enable_b

register_array

Parameter	Value	Type
register_num	32	Signed Integer
register_width	32	Signed Integer
register_num_length	5	Signed Integer

clk
clk
rst
reg0_address[4..0]
reg1_address[4..0]
reg2_address[4..0]
write_reg_address[4..0]
write_word_enable
write_byte_enable
write_data[31..0]

reg0[31..0]
reg1[31..0]

ALU
opcode[4..0]
in1[31..0]
in2[31..0]　　output[31..0]
opcode[4..0]

MAIN_MEMORY_32
data_a[31..0]
address_a[15..0]
wren_a　　q_a[31..0]
data_b[7..0]
address_b[17..0]　　q_b[7..0]
wren_b
rden_a
rden_b
clock　　Block Type: AUTO

jmp_constant2
data[31..0]
distance[1..0]　　result[31..0]

MULTIPLEXER
data1[31..0]
data0[31..0]　　result[31..0]
sel0

MULTIPLEXER
data1[31..0]
data0[31..0]　　result[31..0]
sel0

MULTIPLEXER
data1[31..0]
data0[31..0]　　result[31..0]
sel0