North South University

Course	CSE-231
Gropup	5
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Our project was to show (EEE-2111) in seven segment display with the help of 555 timer. To complete this project, we have divided our work into two part.

1. Combinational Circuit Part
2. Sequential Circuit Part

Combinational Circuit Part:

We have 7 items to display. If we take 3 bit input, then we can display total 2^3=8 outputs. So, to display (EEE-211), we can use 3 bit input.

First we have to draw the truth table with 3 bit input and expected output(output in seven segment display). Then for equations, we will k-map.

Combinational Circuit Making Process:

Truth Table:

Output in 7 segment display	A	B	C	a	b	c	d	e	f	g
E	0	0	0	1	0	0	1	1	1	1
E	0	0	1	1	0	0	1	1	1	1
E	0	1	0	1	0	0	1	1	1	1
-	0	1	1	0	0	0	0	0	0	1
2	1	0	0	1	1	0	1	1	0	1
1	1	0	1	0	1	1	0	0	0	0
1	1	1	0	0	1	1	0	0	0	0
X	1	1	1	X	X	X	X	X	X	X

K-Map:(SOP)

For – a:

A \ BC	0 0	0 1	1 1	1 0
0	1	1	0	1
1	1	0	x	0

a = A'C' + A'B' + B'C'

For – b:

A \ BC	0 0	0 1	1 1	1 0
0	0	0	0	0
1	1	1	x	1

b = A

For – c:

A \ BC	0 0	0 1	1 1	1 0
0	0	0	0	0
1	0	1	x	1

c = AC + AB

For - d :

A \ BC	0 0	0 1	1 1	1 0
0	1	1	0	1
1	1	0	x	0

d = A'C' + A'B' + B'C'

For - e :

A \ BC	0 0	0 1	1 1	1 0
0	1	1	0	1
1	1	0	x	0

e = B'C' + A'C' + A'B'

For - f :

A \ BC	0 0	0 1	1 1	1 0
0	1	1	0	1
1	0	0	x	0

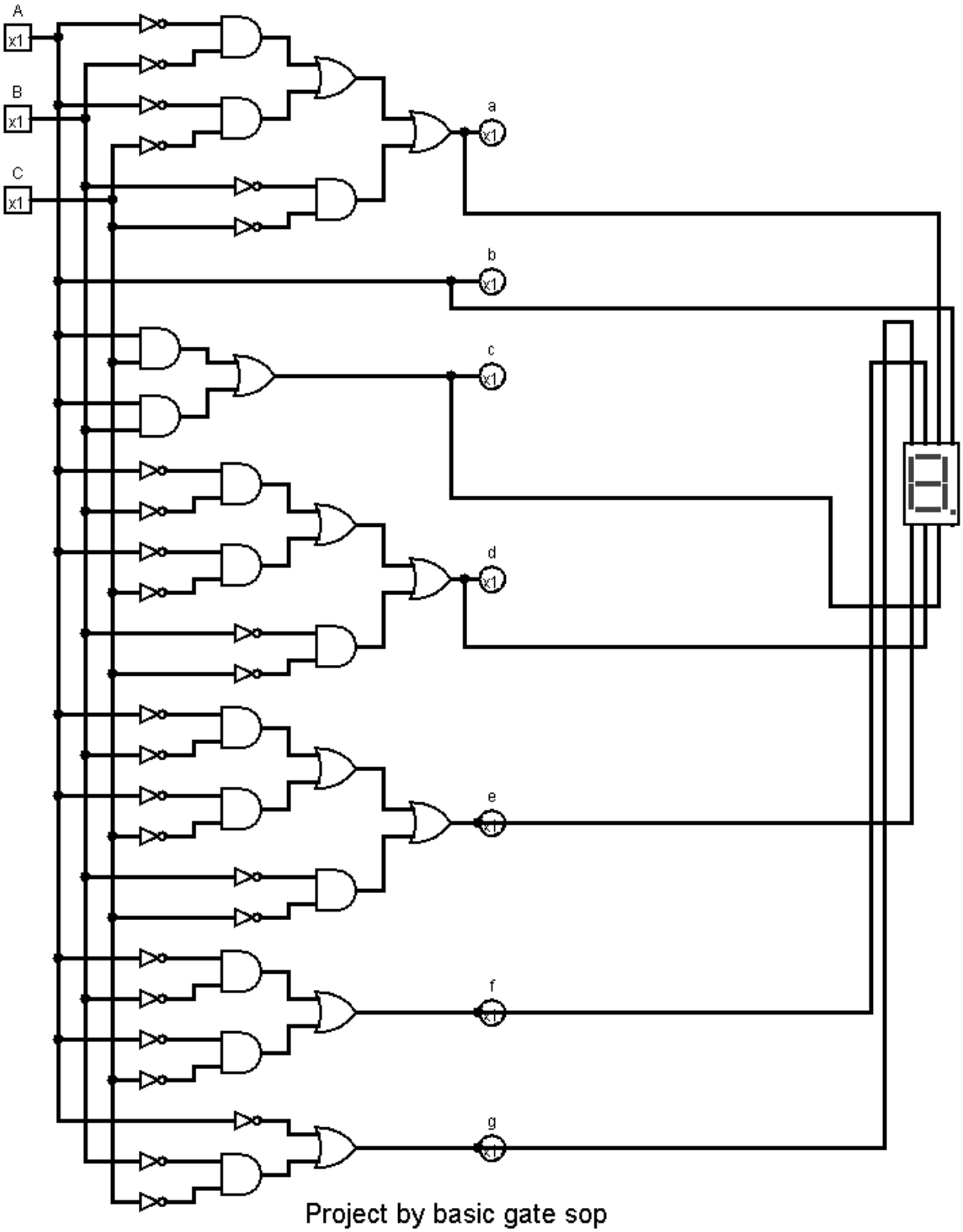
f = A'B'+A'C'

For - g :

A \ BC	0 0	0 1	1 1	1 0
0	1	1	1	1
1	1	0	x	0

g = A' + B'C'

Combinational Circuit for (EEE-211) by SOP:



Project by basic gate sop

K-Map:(POS)

For – a:

A \ BC	0 0	0 1	1 1	1 0
0	1	1	0	1
1	1	0	x	0

$$a = (B'+C')(A'+C')(A'+B')$$

For – b:

A \ BC	0 0	0 1	1 1	1 0
0	0	0	0	0
1	1	1	x	1

b = A

For – c:

A \ BC	0 0	0 1	1 1	1 0
0	0	0	0	0
1	0	1	x	1

c = A(B+C)

For - d :

A \ BC	0 0	0 1	1 1	1 0
0	1	1	0	1
1	1	0	x	0

d = (B'+C')(A'+C')(A'+B')

For - e :

Nbn

A \ BC	0 0	0 1	1 1	1 0
0	1	1	0	1
1	1	0	x	0

e = (B'+C')(A'+C')(A'+B')

For - f :

A \ BC	0 0	0 1	1 1	1 0
0	1	1	0	1
1	0	0	x	0

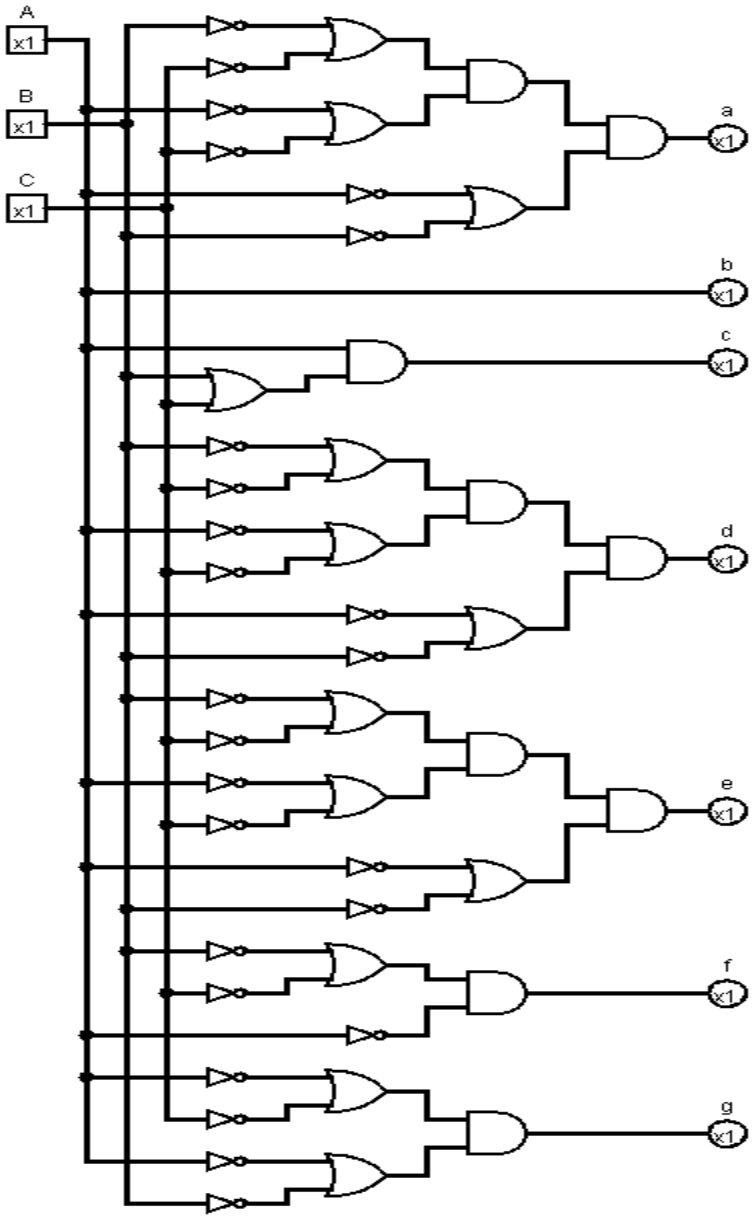
f = A'(B'+C')

For - g :

A \ BC	0 0	0 1	1 1	1 0
0	1	1	1	1
1	1	0	x	0

g =(A'+C')(A'+B')

Combinational Circuit for (EEE-211) by POS:



project by POS

Sequential Circuit Part:

Sequential circuit will produce our continuous input with the help of 555 timer. For sequential part we are going to use **Synchronous Counter by T-FlipFlop**.

Required Equipment:

555 Timer IC:

The **555 timer IC** is an **integrated circuit** (**chip**) used in a variety of **timer**, delay, pulse generation, and oscillator applications.

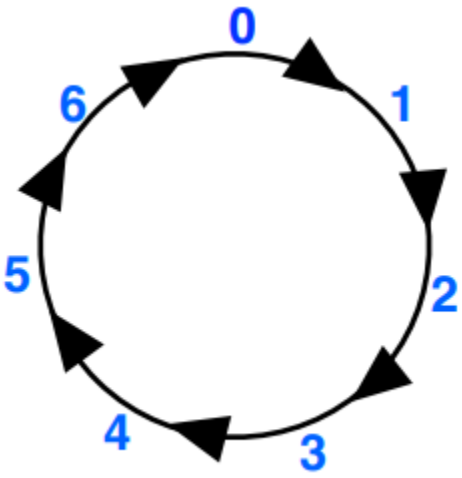
T-FlipFlop:

Toggle Flip-flops are sequential logic circuits frequently used as single bit bistable storage elements in counters, memory devices or as frequency dividers in response to a clock pulse

Sequential Circuit Making Process:

We have used 3 bit input for combinational circuit. Now to produce that 3 bit continuous input we are going to use **3 bit synchronous counter.**

Loop for synchronous counter:



Excitation Table for T-FlipFlop:

Q	Output	T
0	0	0
0	1	1
1	0	1
1	1	0

State Table:

Output in 7 segment display	Decimal number	Present state			Next State			Next State Decoder		
		Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	T_2	T_1	T_0
E	0	0	0	0	0	0	1	0	0	1
E	1	0	0	1	0	1	0	0	1	1
E	2	0	1	0	0	1	1	0	0	1
-	3	0	1	1	1	0	0	1	1	1
2	4	1	0	0	1	0	1	0	0	1
1	5	1	0	1	1	1	0	0	1	1
1	6	1	1	0	0	0	0	1	1	0
	7	1	1	1	0	0	0	1	1	1

K-map for T2:

Q2 \ Q1Q0	0 0	0 1	1 1	1 0
0	0	0	1	0
1	0	0	1	1

$$T2 = Q1Q0 + Q2Q1$$

K-map for T1:

Q2 \ Q1Q0	0 0	0 1	1 1	1 0
0	0	1	1	0
1	0	1	1	1

$$T1 = Q0 + Q2Q1$$

K-map for T0:

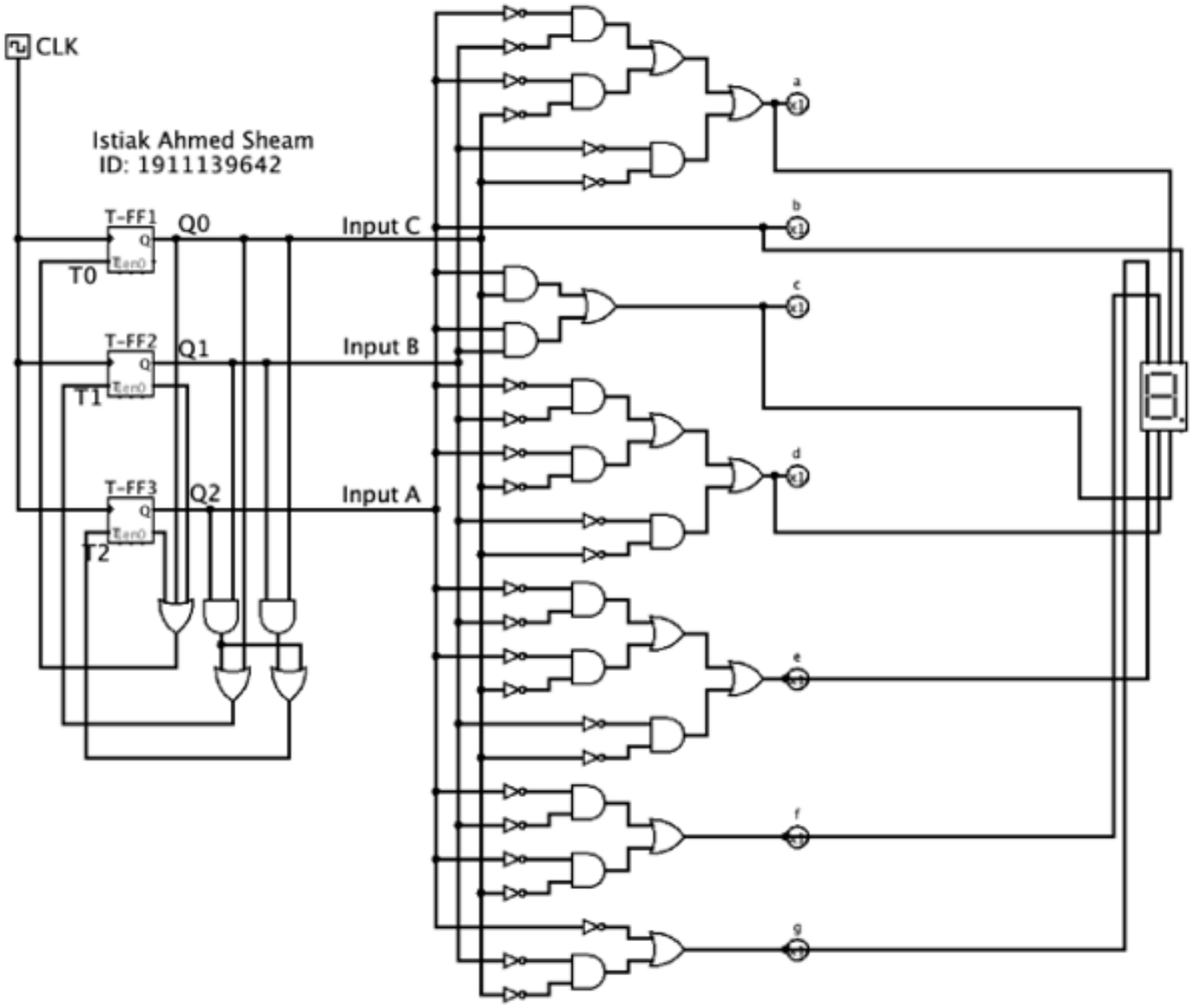
Q2 \ Q1Q0	0 0	0 1	1 1	1 0
0	1	1	1	1
1	1	1	1	0

T0= Q0+Q1'+Q2'Q0'

=Q0+Q1'+Q2

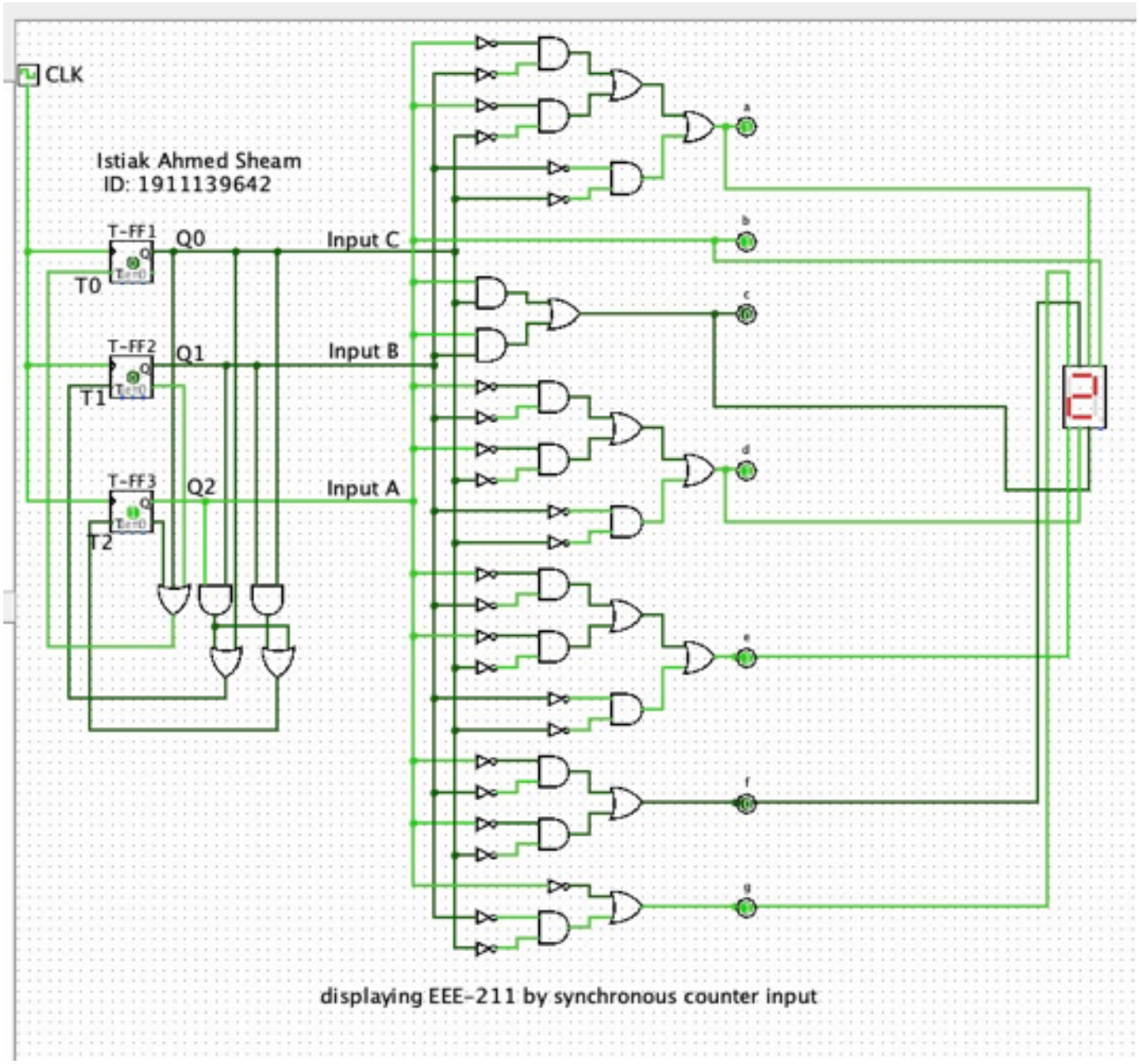
Logic Design for Sequential Circuit in Logisim:

To design this we need 555 Timer IC. But in logisim, we don't have 555 Timer IC. But we can use clock pulse in logisim instate of them.



displaying EEE-211 by synchronous counter input

Screenshots:



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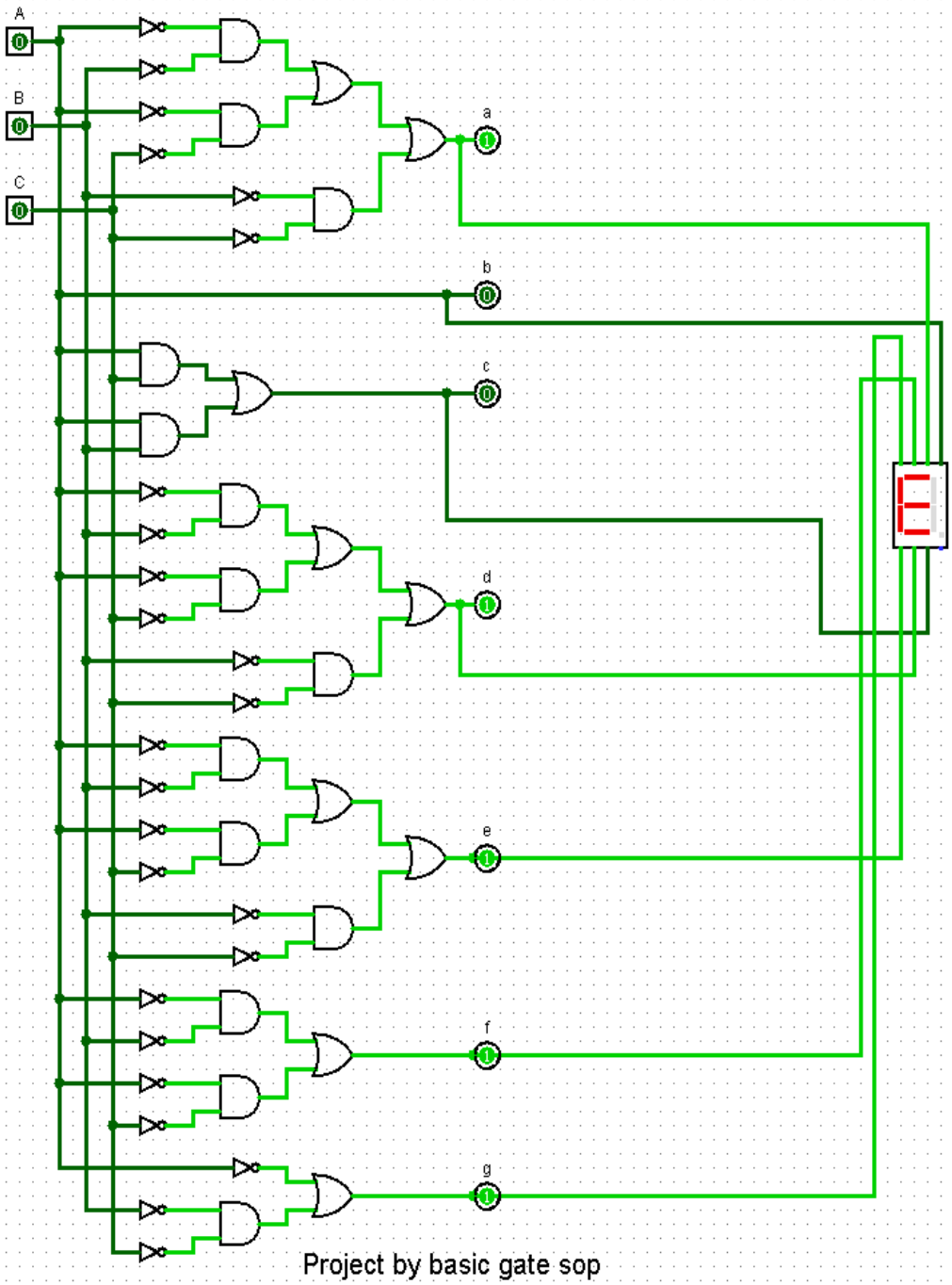

Project by basic gate sop

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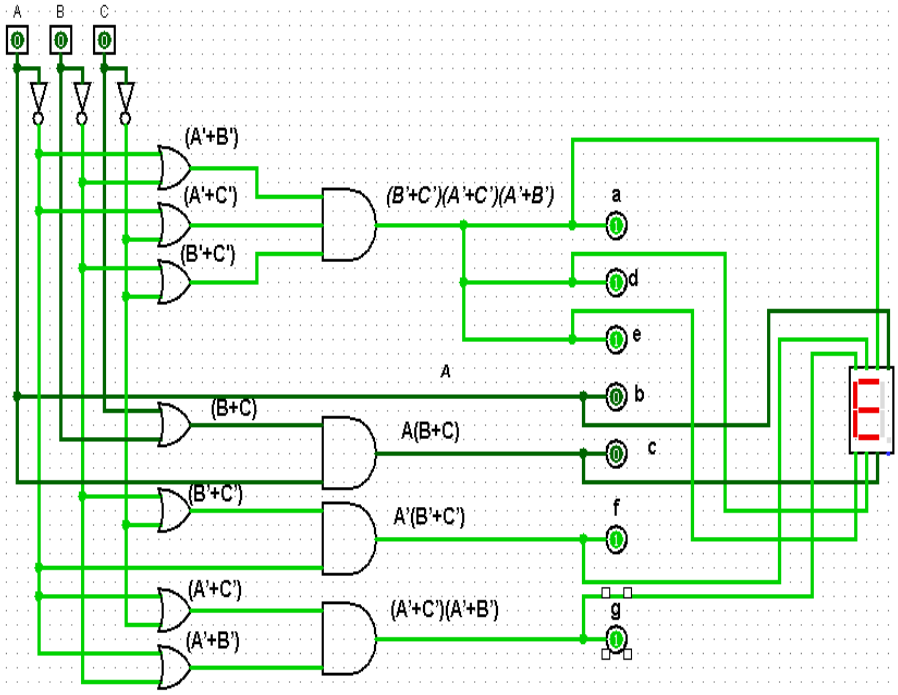
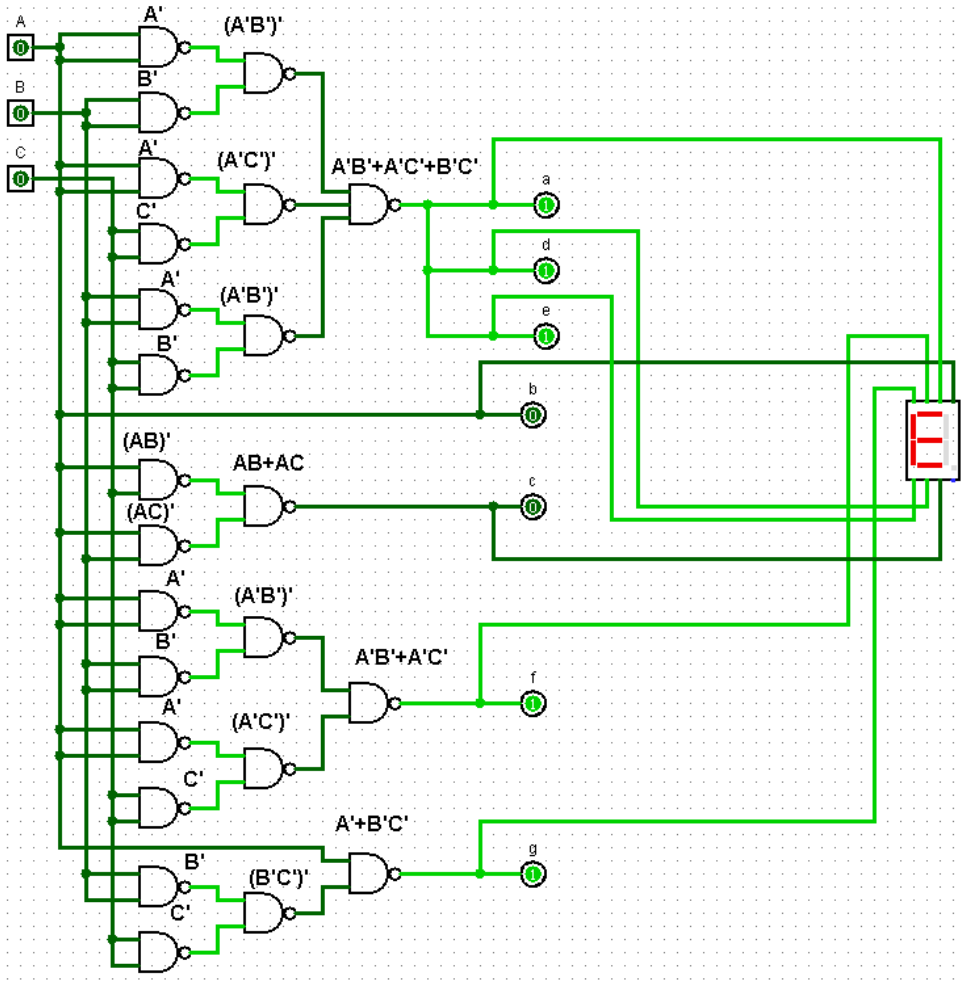
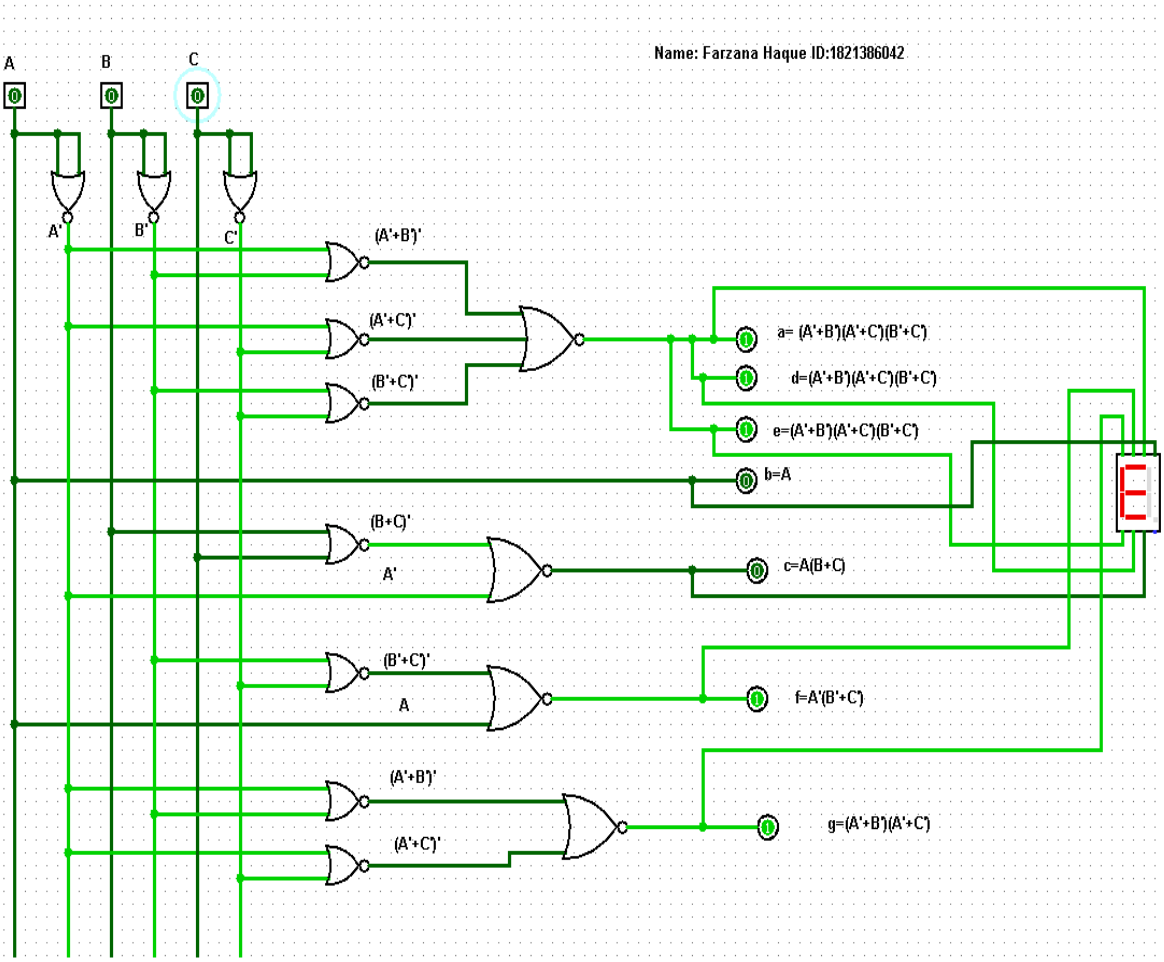


POS Circuit implementation with basic gates

Nur Kalam Mahin (1912254642)



SOP Circuit implementation with NAND



Implementation with NOR