

Problem 1:

a) Design and implement the following ~~two~~ Boolean function using 4x1 MUXs and necessary gates:

$$f(P, Q, R, S) = \Sigma(0, 2, 7, 10, 14, 15)$$

Solution:Truth table:

P	Q	R	S	f
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

Design and minimization:

		<u>R</u>					
		<u>RS</u>		00	01	11	10
P	Q	00	1				1
	01				1		
	11			1	1		
	10					1	
		<u>S</u>					

$I_0 = \bar{S}$

$I_1 = RS$

$I_3 = R$

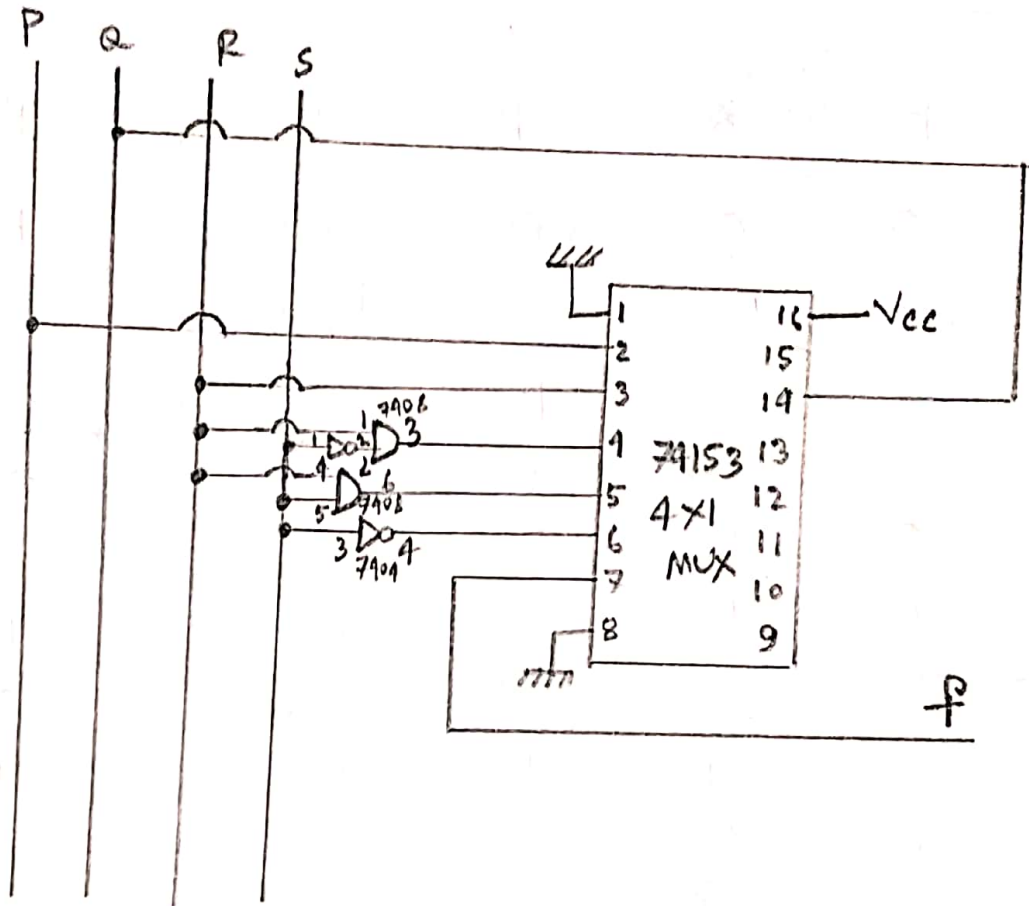
$I_2 = R\bar{S}$

Q

If we use P and Q as the selector bits for the 4x1 MUX, then the inputs are:

$$I_0 = \bar{S}, \quad I_1 = RS, \quad I_2 = R\bar{S} \quad \text{and} \quad I_3 = R$$

Circuit Diagram:



1.b) Design and implement the following Boolean function using 4x1 MUXs and necessary gates:

$$f(P, Q, R, S) = \prod(1, 2, 3, 4, 8, 9, 12)$$

Solution:

Truth table:

P	Q	R	S	f
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

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Design and minimization:

		R			
		S			
P	Q	00	01	11	10
	00		0	0	0
	01	0			
	11	0			
	10	0	0		

$$I_0 = (S+R)'$$

$$I_1 = R+S$$

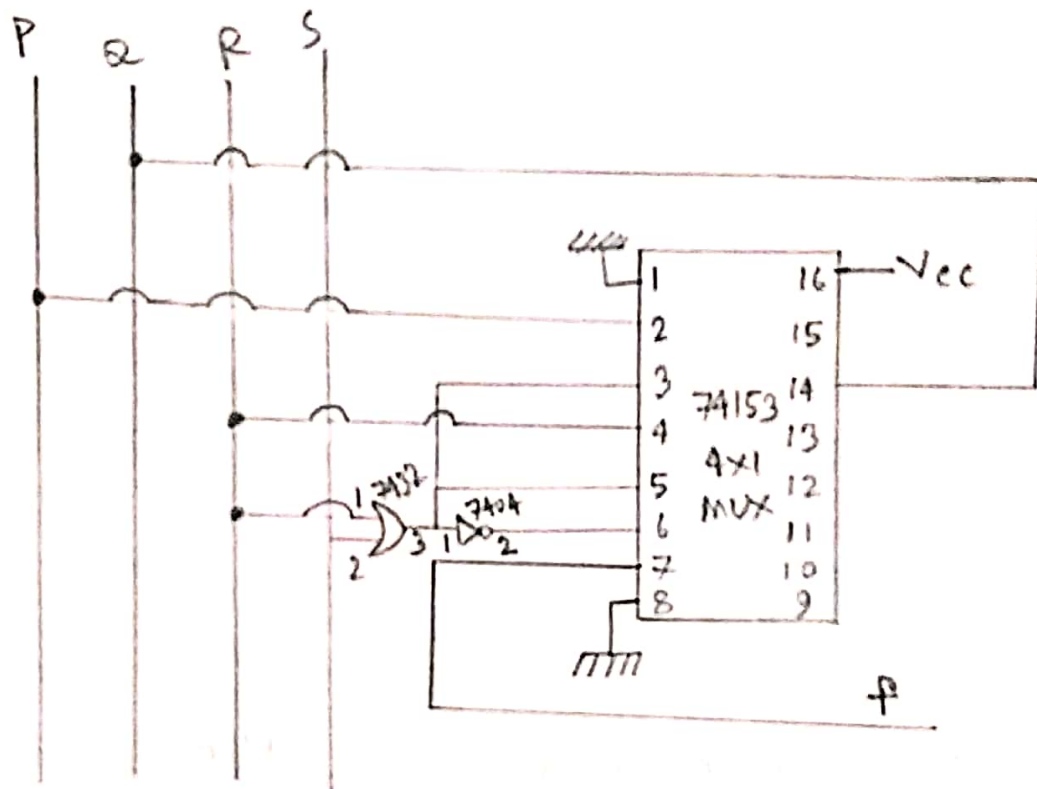
$$I_3 = R+S$$

$$I_2 = R$$

If we use P and Q as the selector bits for the 4x1 MUX, then the inputs are:

$$I_0 = (R+S)', I_1 = R+S, I_2 = R \text{ and } I_3 = R+S$$

Circuit Diagram:



Problem 2

Design a 16x1 MUX using 4x1 MUXs only. Using this 16x1 MUX implement the Boolean function $f(P, Q, R, S)$

$$= \Sigma(0, 2, 7, 10, 14, 15)$$

Solution:

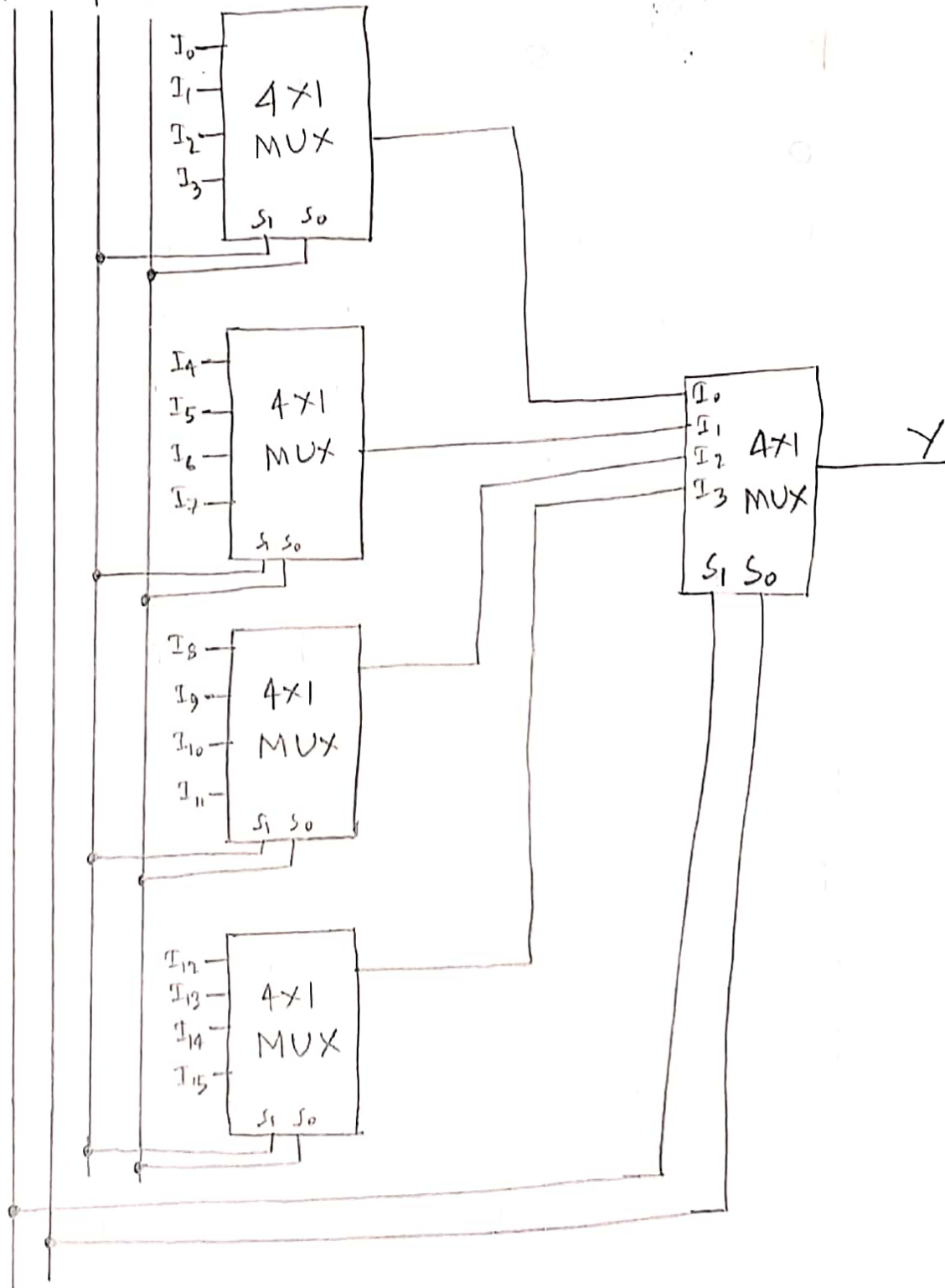
Truth table:

P	Q	R	S	F
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

Design of 16x1 MUX using 4x1 MUX:

(MSB)

P Q R S



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Circuit diagram:

