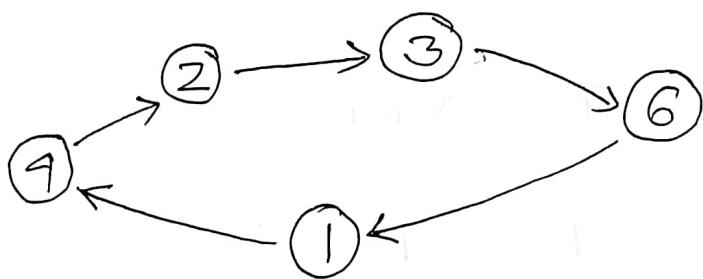


Topic: Counters.

problem is Design a synchronous counter with the sequence given below by using T flipflops and basic gates.



Answer:

Required instruments:

No	Name	Model	Quantity
1	Trainer board		1 piece
2	IC extractor		1 piece
3	wires		some.
4	T flipflop	7473	2 piece
5	OR gate	7432	1 piece

No of states = 5

No of T FFs = $\lceil \log_2 5 \rceil = 3$

Excitation requirement table of
T FFs

Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Let T_2, T_1, T_0 be the required FFs.

Truth table:

Present State (PS)			Next State (NS)			T input		
A_2	A_1	A_0	A_2^*	A_1^*	A_0^*	T_2	T_1	T_0
0	1	0	0	1	1	0	0	1
0	1	1	1	1	0	1	0	1
1	1	0	0	0	1	1	1	1
0	0	1	1	0	0	1	0	1
1	0	0	0	1	0	1	1	0

Function Simplification

T_2	A_2	$A_1 A_0$	00	01	11	10
0	X	1	1	1	0	
1	(1)	(X)	(X)	(1)		

$$\therefore T_2 = A_2 + A_0$$

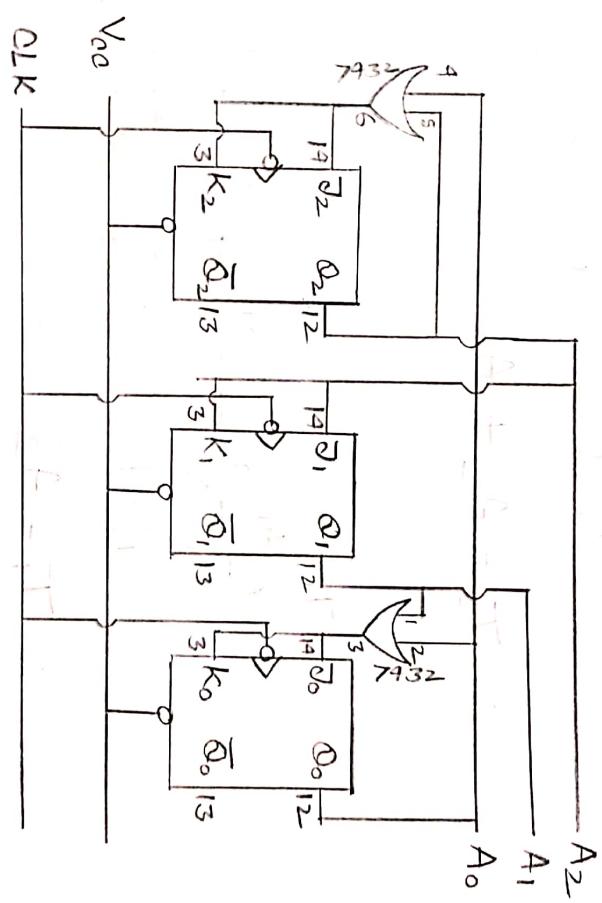
T_1	A_2	$A_1 A_0$	00	01	11	10
0	X	0	0	0	0	
1	(1)	X	X	X	D	

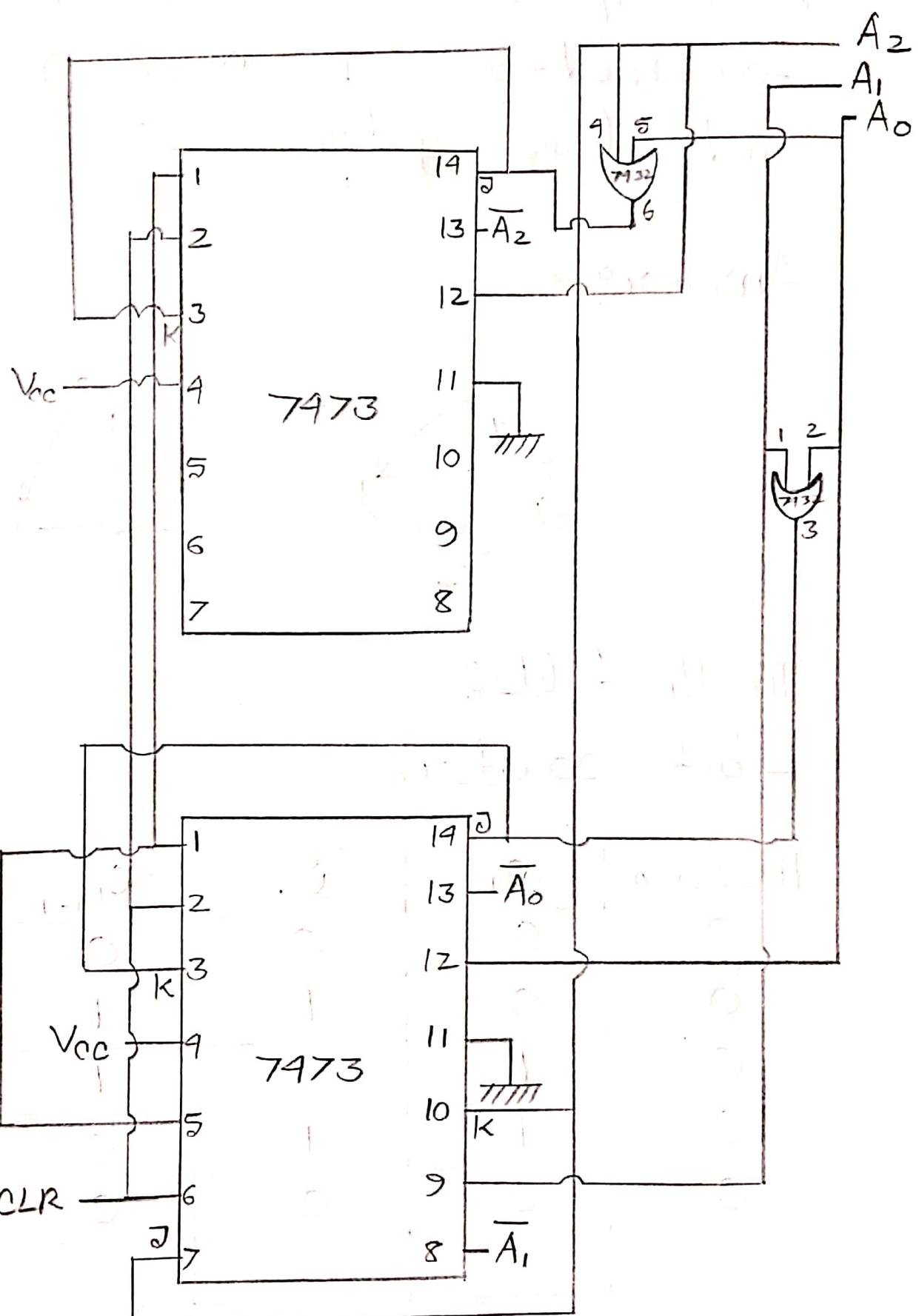
$$\therefore T_1 = A_2$$

T_0	A_2	$A_1 A_0$	00	01	11	10
0	X	1	1	1	1	
1	(1)	(X)	(X)	(1)		

$$\therefore T_0 = A_0 + A_1$$

Circuit Diagram

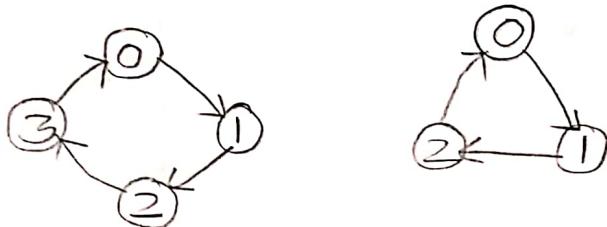




Block Diagram:

problem 2: Design a 2 bit asynchronous up counter with the provision for mod-3 by using D flipflops and basic gates.

Answer:



Truth table:

2 bit counter:

Provision	Q_1	Q_0	Q_{1n+1}	Q_{0n+1}
0	0	0	0	1
0	0	1	1	0
0	1	0	1	1
0	1	1	0	0
0	0	0	0	1

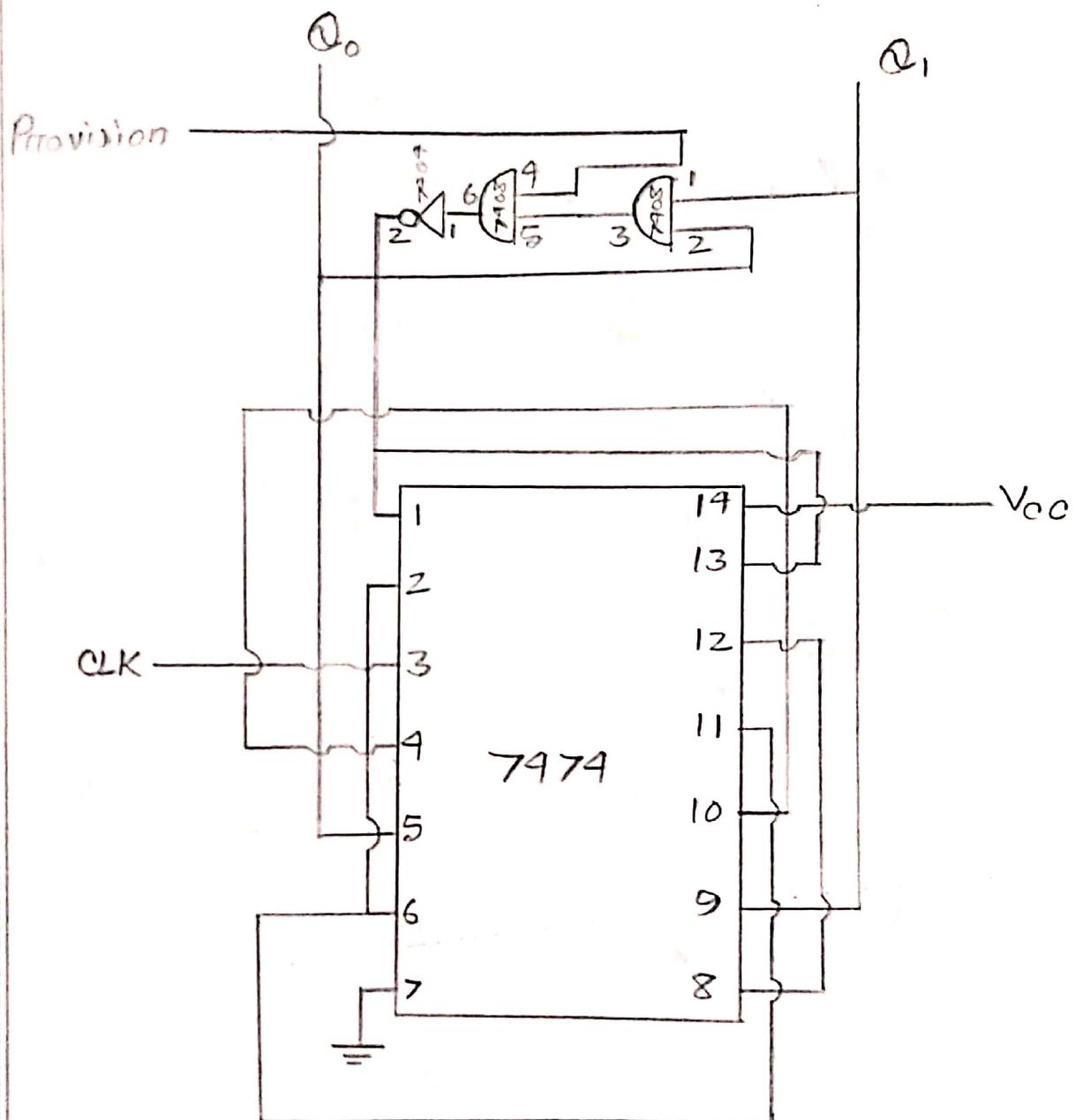
Mod - 3 Counter

Provision	Q_1	Q_0	Q_{in+1}	Q_{out+1}
1	0	0	0	1
1	0	1	1	0
1	1	0	0	0
1	0	0	0	1

Required instruments:

No	Name	Model	Quantity
1	Trainer board		1 piece
2	IC extractor		1 piece
3	wires		Some.
4	D flip flop	7479	1 piece
5.	AND gate	7908	1 piece
6	NOT gate	7909	1 piece

Circuito



Ques 1: Design mod-3 synchronous down counter using any type of Flip Flop.

Answer: Using D flip flop
Required instruments:

No.	Name	Model	Quantity
1.	Trainer board		1 piece
2.	IC extractor		1 piece
3.	wires		Some
4.	D flip flop	7479	1 piece
5.	AND gate	7408	1 piece

Truth Table:

V					
Present State (PS)	Next State (NS)	Input in D-terminal			
A ₁	A ₀	A ₁ *	A ₀ *	D ₁	D ₀
0	0	1	0	1	0
0	1	0	0	0	0
1	0	0	1	0	1

Function Simplification

$$D_I =$$

A_1	A_o	D_I
0	0	1

$$\therefore D_I = \overline{A_1} \overline{A_o}$$

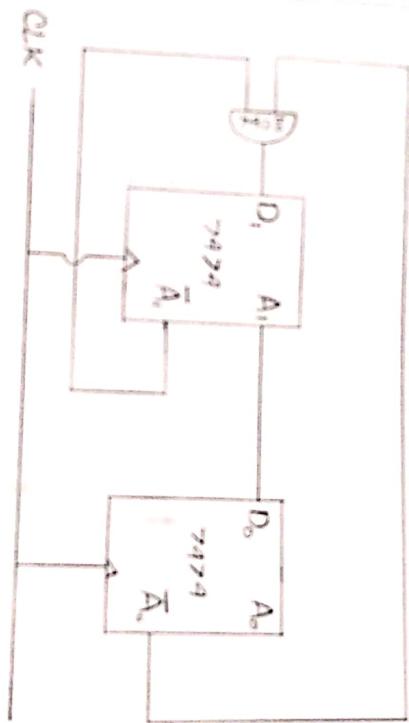
$$D_o =$$

A_1	A_o	D_o
0	0	1
1	X	1

$$\therefore D_o = A_1$$

∴ $D_o = A_1$

Circuit diagrams



Ques 2^o: Design a synchronous BCD counter with JK flip-flops. (Don't convert JK to T)

Answer:

Required instruments:

No.	Name	Model	Quantity
1.	Trainer board		1 piece
2.	IC extractor		1 piece
3.	wires		Some
4.	JK Flipflop	7473	2 pieces
5.	2 input AND gate	7408	1 piece
6.	3 input AND gate	7411	1 piece

Excitation table for JK flip-flop:

Q _t	J	K	Q _{t+1}
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Present and Next state with respect to J and K

Present State (PS)	Next State (NS)	J	K
Q ₄	Q ₄₊₁	Q	X
Q	Q	Q	X
I	Q	X	Q

Truth Table

Present State (PS)	Next State (NS)	Inputs in J and K of JK flip-flop															
A ₃	A ₂	A ₁	A ₀	A ₃ *	A ₂ *	A ₁ *	A ₀ *	J ₃	K ₃	J ₂	K ₂	J ₁	K ₁	J ₀	K ₀		
0	0	0	0	0	0	1	0	X	0	X	0	X	1	X	1	X	
0	0	0	1	0	0	1	0	0	X	0	X	1	X	1	X	1	
0	0	1	0	0	0	1	1	0	X	0	X	X	0	1	X	1	
0	0	1	1	0	1	0	0	X	1	X	X	1	X	1	X	1	
0	1	0	0	0	1	0	1	0	X	X	0	0	X	1	X	1	
0	1	0	1	0	1	1	0	X	X	0	1	X	1	X	1	X	
0	1	1	0	1	1	0	1	X	X	1	X	1	X	1	X	1	
0	1	1	1	1	0	0	0	1	X	X	1	X	1	X	1	X	
1	0	0	0	1	0	0	1	X	0	0	X	0	X	1	X	1	
1	0	0	1	0	0	0	0	X	1	0	X	0	X	1	X	1	

Function Simplification

(2)

For J_0 :

$A_1 A_2$	$\Delta_1 \Delta_2$	$\Delta_1 A_2$	$\Delta_2 A_1$	$\Delta_1 \Delta_2$	$\Delta_1 A_2$	$\Delta_2 A_1$	$\Delta_1 \Delta_2$
00	-	X	-	00	-	X	-
01	-	X	-	01	-	X	-
10	-	X	-	10	-	X	-
11	-	X	-	11	-	X	-

$J_0 = 1$

For K_0 : $\Delta_1 A_2$

10	11	01	00
X	X	X	X
-	X	-	-
X	X	-	-
X	X	X	X

$K_0 = 1$

of $= 1$

For $J_1 = 0$

		A ₃ A ₂				A ₁ A ₀			
		00	01	10	11	00	01	10	11
01	00	X	X	X	X	O	O	O	O
	01	X	X	-	O	X	X	X	X
10	00	X	X	X	X	O	O	O	O
	10	X	X	-	O	X	X	X	X

For $K_1 = 0$

$$\bar{J}_1 = A_3' A_0$$

		A ₃ A ₂				A ₁ 'A ₀			
		00	01	10	11	00	01	10	11
	00	X	X	X	X	O	O	O	O
	01	X	X	-	O	X	X	X	X
	10	X	X	X	X	O	O	O	O
	10	X	X	-	O	X	X	X	X

$$K_1 = A_0$$

		For \overline{J}_2^o			
		A_3A_2	A_1A_0	00	01
A_3A_2	00	0	0	1	0
	01	X	X	X	X
A_3A_2	11	X	X	X	X
	10	0	0	(X)	X

$$\overline{J}_2 = A_1A_0$$

For K_2^o

		For K_2^o			
		A_3A_2	A_1A_0	00	01
A_3A_2	00	X	X	(X)	X
	01	0	0	1	0
A_3A_2	11	X	X	X	X
	10	X	X	(X)	X

$$K_2 = A_1A_0$$

$F_{0r} \bar{J}_3^o$

		$A_3 A_2$		$A_1 A_0$			
		00	01	00	01	11	10
01	00	X	X	X	X	O	O
	01	X	X	X	X	O	O
11	00	X	X	X	X	X	X
	11	X	X	X	X	X	X
10	00	X	X	X	X	X	X
	10	X	X	X	X	X	X

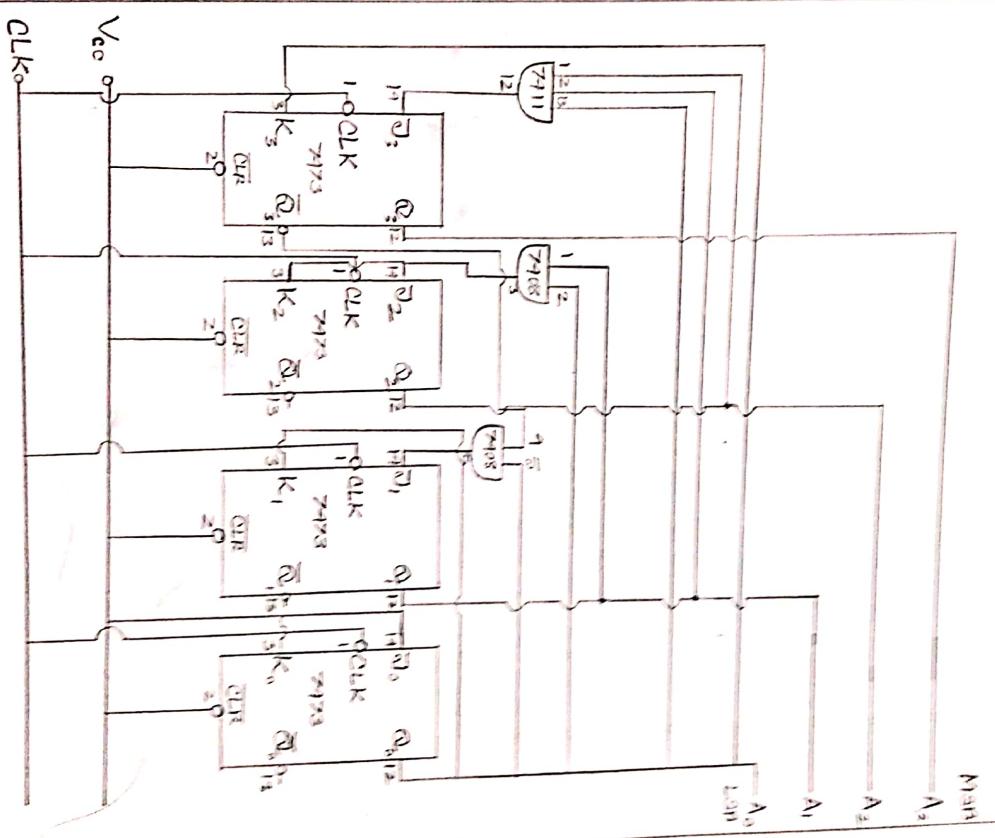
$$\bar{J}_3 = A_2 A_1 A_0$$

$F_{0r} K_3^o$

		$A_3 A_2$		$A_1 A_0$			
		00	01	00	01	11	10
01	00	X	X	X	X	X	X
	01	X	X	X	X	X	X
11	00	X	X	X	X	X	X
	11	X	X	X	X	X	X
10	00	X	X	X	X	X	X
	10	X	X	X	X	X	X

$$K_3 = A_0$$

Circuit diagram



Ques 3: Design a MOD 17 counter. Use any standard counter modules and gates.

Answer:

Required instruments:

No.	Name	Model	Quantity
1.	Trainer board		1 piece
2.	IC extractor		1 piece
3.	wires		Some

Truth table:

Count	Output				
	A _{msb}	B	C	D	E _{lsb}
0	0	0	0	0	0
1	0	0	0	0	0
2	0	0	0	0	1
3	0	0	0	1	0
4	0	0	0	1	1
5	0	0	1	0	0
6	0	0	1	0	1
7	0	0	1	1	0

P.T.O

Count	Output				
	A _{MSB}	B	C	D	E _{LSB}
8	0	1	0	0	0
9	0	1	0	0	1
10	0	1	0	1	0
11	0	1	0	1	1
12	0	1	1	0	0
13	0	1	1	0	1
14	0	1	1	1	0
15	0	1	1	1	1
16	1	0	0	0	0
17	1	0	0	0	1