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# MICROPROCESSOR

## DATA

# HAND BOOK



**Bangladesh University of Engineering and Technology**  
**Department of Computer Science and Engineering**

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## Quad Two-Input NAND G

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7400	9ns	8mA
74LS00	9.5ns	1.6mA
74S00	3ns	15mA

## ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$ ; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$ ; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7400N • N74LS00N N74S00N	
Plastic SO	N74LS00D N74S00D	
Ceramic DIP		S5400F • S54LS00F S54S00F
Flatpack		S5400W • S54LS00W S54S00W
LLCC		S54LS00G

## FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level

L = LOW voltage level

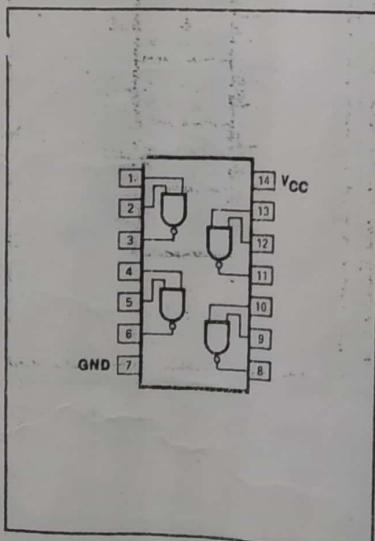
## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74S	54/74LS
A, B	Inputs	1 <ul style="list-style-type: none"></ul>	1 <ul style="list-style-type: none"></ul>	1 <ul style="list-style-type: none"></ul>
Y	Output	10 <ul style="list-style-type: none"></ul>	10 <ul style="list-style-type: none"></ul>	10 <ul style="list-style-type: none"></ul>

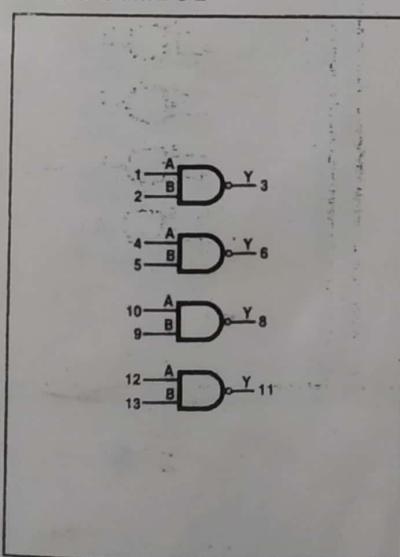
## NOTE

Where a 54/74 unit load (ul) is understood to be  $40\mu A I_{IH}$  and  $-1.6mA I_{IL}$ , a 54/74S unit load (Sul) is  $50\mu A I_{IH}$  and  $-2.0mA I_{IL}$ , and 54/74LS unit load (LSul) is  $20\mu A I_{IH}$  and  $-0.4mA I_{IL}$ .

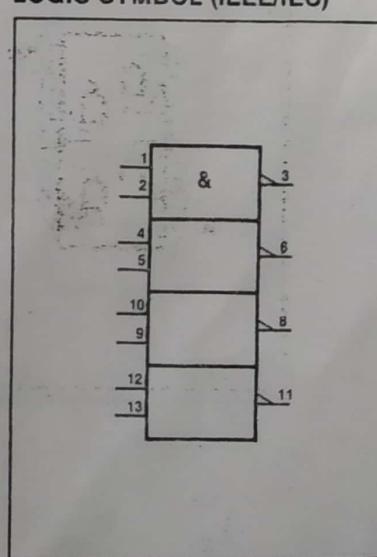
## PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



## Quad Two-Input NAND Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7400	9ns	8mA
74LS00	9.5ns	1.6mA
74S00	3ns	15mA

## ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$ ; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$ ; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7400N N74S00N	
Plastic SO	N74LS00D N74S00D	
Ceramic DIP		S5400F S54S00F
Flatpack		S5400W S54S00W
LLCC		S54LS00G

## FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

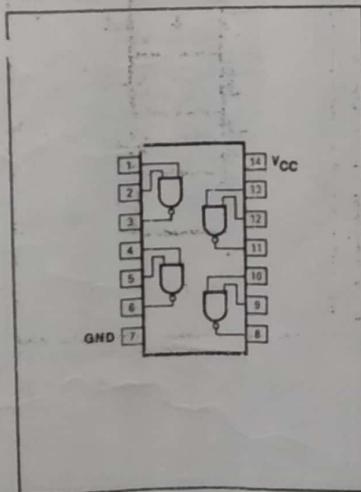
H = HIGH voltage level  
L = LOW voltage level

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

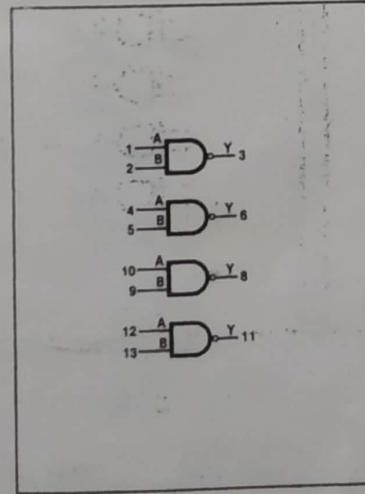
PINS	DESCRIPTION	54/74	54/74S	54/74LS
A, B	Inputs	1 <ul style="list-style-type: none"></ul>	1 <ul style="list-style-type: none"></ul>	1 <ul style="list-style-type: none"></ul>
Y	Output	10 <ul style="list-style-type: none"></ul>	10 <ul style="list-style-type: none"></ul>	10 <ul style="list-style-type: none"></ul>

NOTE  
Where a 54/74 unit load ( $u$ ) is understood to be  $40\mu A I_{IH}$  and  $-1.6mA I_{IL}$ , a 54/74S unit load ( $Su$ ) is  $50\mu A I_{IH}$  and  $-2.0mA I_{IL}$ , and 54/74LS unit load ( $LSu$ ) is  $20\mu A I_{IH}$  and  $-0.4mA I_{IL}$ .

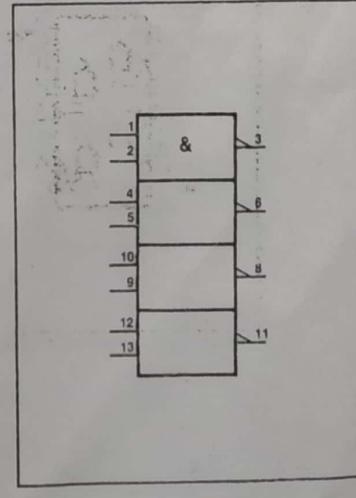
## PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



## Quad Two-Input NAND Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7400	9ns	8mA
74LS00	9.5ns	1.6mA
74S00	3ns	15mA

## ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$ ; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$ ; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7400N • N74LS00N N74S00N	
Plastic SO	N74LS00D N74S00D	
Ceramic DIP		S5400F • S54LS00F S54S00F
Flatpack		S5400W • S54LS00W S54S00W
LLCC		S54LS00G

## FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level

L = LOW voltage level

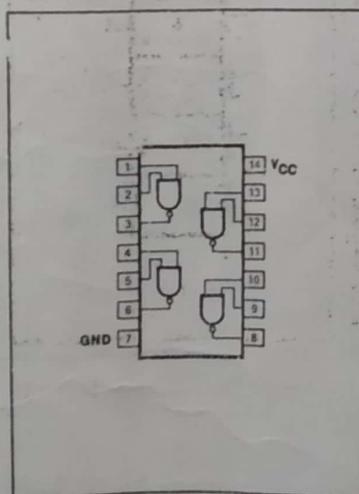
## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74S	54/74LS
A, B	Inputs	1 <ul style="list-style-type: none">i</ul>	1 <ul style="list-style-type: none">S</ul>	1 <ul style="list-style-type: none">LS</ul>
Y	Output	10 <ul style="list-style-type: none">i</ul>	10 <ul style="list-style-type: none">S</ul>	10 <ul style="list-style-type: none">LS</ul>

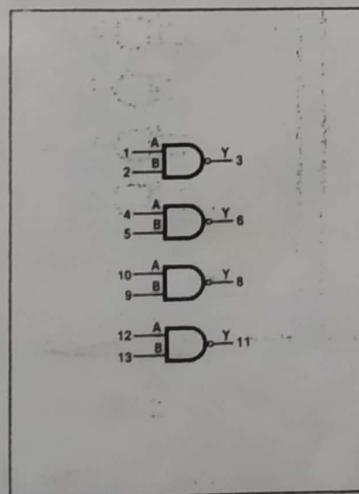
## NOTE

Where a 54/74 unit load ( $i_u$ ) is understood to be  $40\mu A$   $i_{IH}$  and  $-1.6mA$   $i_{IL}$ , a 54/74S unit load ( $S_u$ ) is  $50\mu A$   $i_{IH}$  and  $-2.0mA$   $i_{IL}$ , and 54/74LS unit load ( $LS_u$ ) is  $20\mu A$   $i_{IH}$  and  $-0.4mA$   $i_{IL}$ .

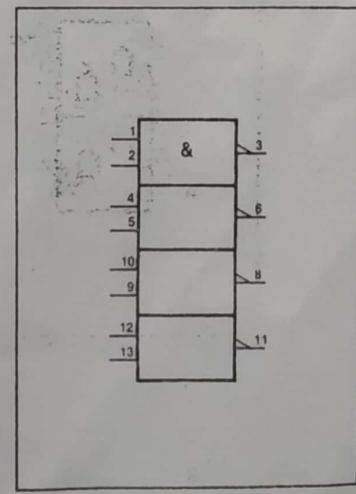
## PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



## Quad Two-Input NOR Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7402	10ns	11mA
74LS02	10ns	2.2mA
74S02	3.5ns	22mA

## ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$ ; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$ ; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7402N • N74LS02N N74S02N	
Plastic SO	N74LS02D • N74S02D	
Ceramic DIP		S54S02F • S54LS02F
Flatpack		S54S02W • S54LS02W
LLCC		S54LS02G

## FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

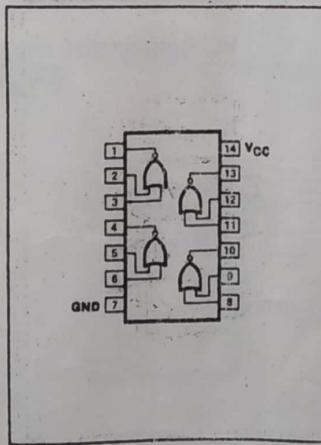
H = HIGH voltage level  
L = LOW voltage level

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

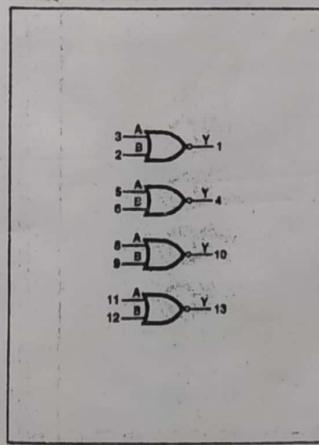
PINS	DESCRIPTION	54/74	54/74S	54/74LS
A, B	Inputs	1uA	1SuA	1LSuA
Y	Output	10uA	10SuA	10LSuA

NOTE  
Where a 54/74 unit load (uA) is understood to be 40 $\mu A$   $I_{IH}$  and -1.8mA  $I_{IL}$ , a 54/74S unit load (SuA) is 50 $\mu A$   $I_{IH}$  and -2.0mA  $I_{IL}$ , and 54/74LS unit load (LSuA) is 20 $\mu A$   $I_{IH}$  and -0.4mA  $I_{IL}$ .

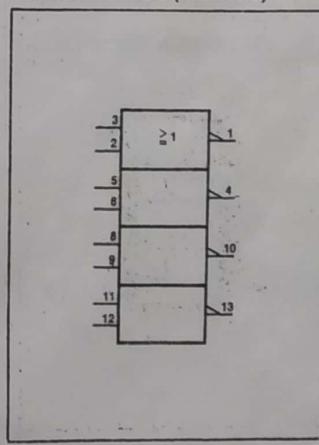
## PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



**INVERTERS**

54/7404, LS04, S04

**Hex Inverter**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7404	10ns	12mA
74LS04	9.5ns	2.4mA
74S04	3ns	22mA

**ORDERING CODE**

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$ ; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$ ; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7404N • N74LS04N N74S04N	
Plastic SO	N74LS04D • N74S04D	
Ceramic DIP		S5404F • S54LS04F S54S04F
Flatpack		S5404W • S54LS04W S54S04W
LLCC		S54LS04G

**FUNCTION TABLE**

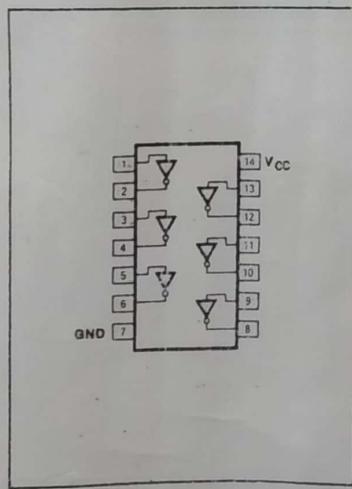
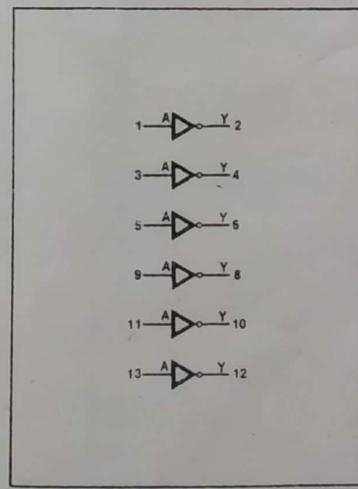
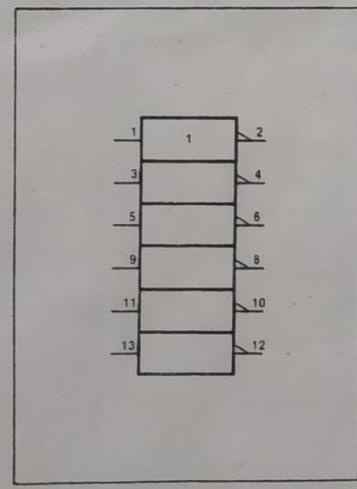
INPUT	OUTPUT
A	Y
L	H
H	L

H = HIGH voltage level  
L = LOW voltage level

**INPUT AND OUTPUT LOADING AND FAN-OUT TABLE**

PINS	DESCRIPTION	54/74	54/74S	54/74LS
A	Input	1 <ul style="list-style-type: none"></ul>	1 <ul style="list-style-type: none"></ul>	1 <ul style="list-style-type: none"></ul>
Y	Output	10 <ul style="list-style-type: none"></ul>	10 <ul style="list-style-type: none"></ul>	10 <ul style="list-style-type: none"></ul>

NOTE  
Where a 54/74 unit load (ul) is understood to be  $40\mu A I_{IH}$  and  $-1.6mA I_{IL}$ , a 54/74S unit load (Sul) is  $50\mu A I_{IH}$  and  $-2.0mA I_{IL}$ , and 54/74LS unit load (LSul) is  $20\mu A I_{IH}$  and  $-0.4mA I_{IL}$ .

**PIN CONFIGURATION****LOGIC SYMBOL****LOGIC SYMBOL (IEEE/IEC)**

**GATES****54/7408, LS08, S08****Quad Two-Input AND Gate**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7408	15ns	16mA
74LS08	9ns	3.4mA
74S08	5ns	25mA

**ORDERING CODE**

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$ ; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$ ; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7408N • N74LS08N N74S08N	
Plastic SO	N74LS08N • N74S08N	
Ceramic DIP		S54S08F • S54LS08F
Flatpack		S54S08W • S54LS08W
LLCC		S54LS08G

**FUNCTION TABLE**

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH voltage level

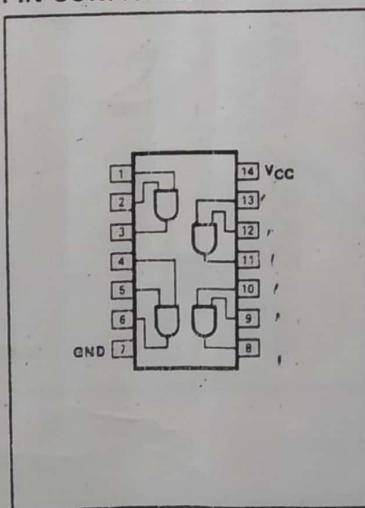
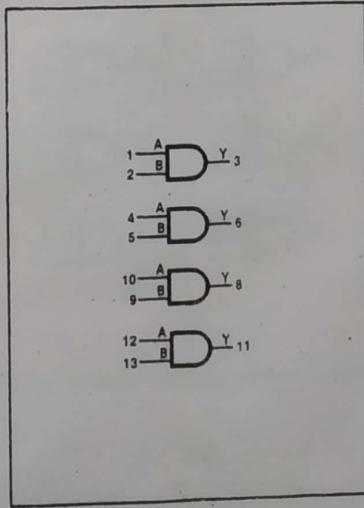
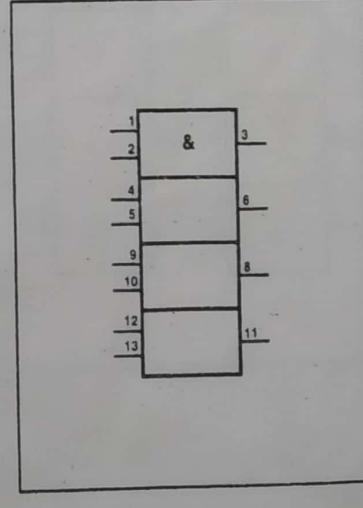
L = LOW voltage level

**INPUT AND OUTPUT LOADING AND FAN-OUT TABLE**

PINS	DESCRIPTION	54/74	54/74S	54/74LS
A, B	Inputs	1 <ul style="list-style-type: none"></ul>	1 <ul style="list-style-type: none"></ul>	1 <ul style="list-style-type: none"></ul>
Y	Output	10 <ul style="list-style-type: none"></ul>	10 <ul style="list-style-type: none"></ul>	10 <ul style="list-style-type: none"></ul>

## NOTE

Where a 54/74 unit load ( $u_l$ ) is understood to be  $40\mu A I_{IH}$  and  $-1.6mA I_{IL}$ , a 54/74S unit load ( $Su_l$ ) is  $50\mu A I_{IH}$  and  $-2.0mA I_{IL}$ , and 54/74LS unit load ( $LSu_l$ ) is  $20\mu A I_{IH}$  and  $-0.4mA I_{IL}$ .

**PIN CONFIGURATION****LOGIC SYMBOL****LOGIC SYMBOL (IEEE/IEC)**

## Triple Three-Input NAND ('10), AND ('11) Gates

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7410	9ns	6mA
74LS10	10ns	1.2mA
74S10	3ns	12mA
7411	10ns	11mA
74LS11	9ns	2.6mA
74S11	5ns	19mA

## ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$ ; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$ ; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP '10	N7410N • N74LS10N • N74S10N	
'11	N7411N • N74LS11N • N74S11N	
Plastic SO '10	N74LS10D • N74S10D	
Plastic SO '11	N74LS11D • N74S11D	
Ceramic DIP '10		S54S10F • S54LS10F
'11		S5411F • S54S11F
Flatpack '10		S54S10W • S54LS10W
'11		S5411W • S54S11W
LLCC '10		S54LS10G

## FUNCTION TABLE

INPUTS			OUTPUTS	
A	B	C	$Y('10)$	$Y('11)$
L	L	L	H	L
L	L	H	H	L
L	H	L	H	L
L	H	H	H	L
H	L	L	H	L
H	L	H	H	L
H	H	L	H	L
H	H	H	L	H

H = HIGH voltage level

L = LOW voltage level

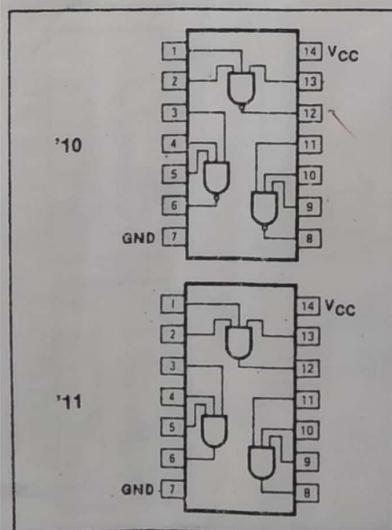
## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74S	54/74LS
A-C	Inputs	1 <ul style="list-style-type: none"></ul>	1 <ul style="list-style-type: none"></ul>	1 <ul style="list-style-type: none"></ul>
Y	Output	10 <ul style="list-style-type: none"></ul>	10 <ul style="list-style-type: none"></ul>	10 <ul style="list-style-type: none"></ul>

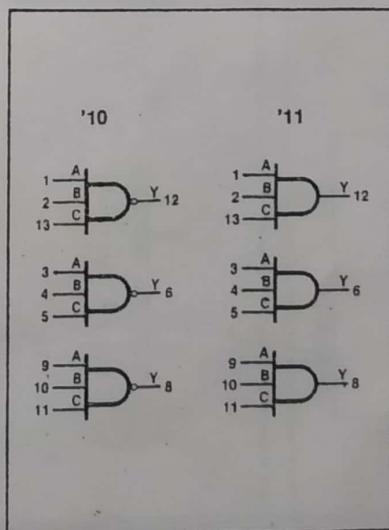
## NOTE

Where a 54/74 unit load ( $uL$ ) is understood to be  $40\mu A I_{IH}$  and  $-1.6mA I_{IL}$ , a 54/74S unit load ( $SuL$ ) is  $50\mu A I_{IH}$  and  $-2.0mA I_{IL}$ , and 54/74LS unit load ( $LSuL$ ) is  $20\mu A I_{IH}$  and  $-0.4mA I_{IL}$ .

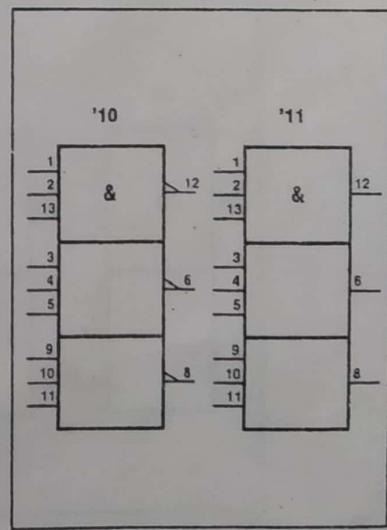
## PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



## Dual Four-Input NAND ('20), AND ('21) Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7420	10ns	8mA
74LS20	10ns	0.8mA
74S20	3ns	8mA
7421	12ns	8mA
74LS21	9ns	1.7mA

## ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$ ; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$ ; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP '20	N7420N • N74LS20N N74S20N	
'21	N7421N • N74LS21N	
Plastic SO	N74LS20D • N74S20D N74LS21D	
Ceramic DIP '20		S5420F • S54LS20F S54S20F
Flatpack '20		S5420W • S54LS20W S54S20W
LLCC		S54LS20G

## FUNCTION TABLE

INPUTS				OUTPUTS	
A	B	C	D	Y('20)	Y('21)
L	X	X	X	H	L
X	L	X	X	H	L
X	X	L	X	H	L
X	X	X	L	H	L
H	H	H	H	L	H

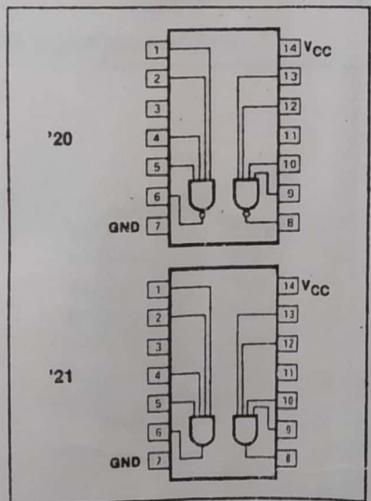
H = HIGH voltage level  
L = LOW voltage level  
X = Don't care

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

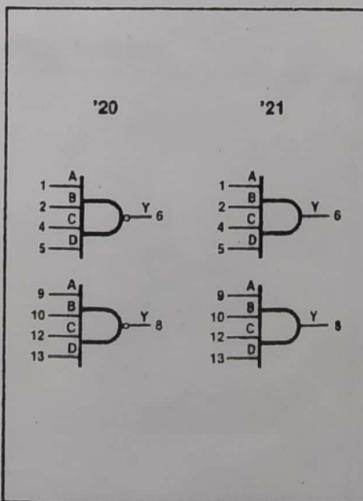
PINS	DESCRIPTION	54/74	54/74S	54/74LS
A-D	Inputs	1 <ul style="list-style-type: none"></ul>	1 <ul style="list-style-type: none"></ul>	1 <ul style="list-style-type: none"></ul>
Y	Output	10 <ul style="list-style-type: none"></ul>	10 <ul style="list-style-type: none"></ul>	10 <ul style="list-style-type: none"></ul>

NOTE  
Where a 54/74 unit load ( $u_l$ ) is understood to be  $40\mu A I_{IH}$  and  $-1.6mA I_{IL}$ , a 54/74S unit load ( $Su_l$ ) is  $50\mu A I_{IH}$  and  $-2.0mA I_{IL}$ , and 54/74LS unit load ( $LSu_l$ ) is  $20\mu A I_{IH}$  and  $-0.4mA I_{IL}$ .

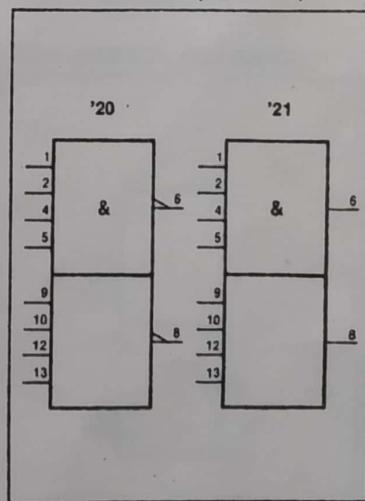
## PIN CONFIGURATION



## LOGIC SYMBOL



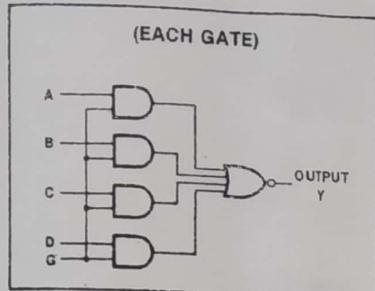
## LOGIC SYMBOL (IEEE/IEC)



## Dual Four-Input NOR Gate With Strobe

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7425	9ns	9mA

## LOGIC DIAGRAM



## ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$ ; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$ ; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7425N	
Ceramic DIP		S5425F
Flatpack		S5425W

## FUNCTION TABLE

INPUTS					OUTPUT
A	B	C	D	G	Y
X	X	X	X	L	H
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	X	X	H	H	L
L	L	L	L	H	H

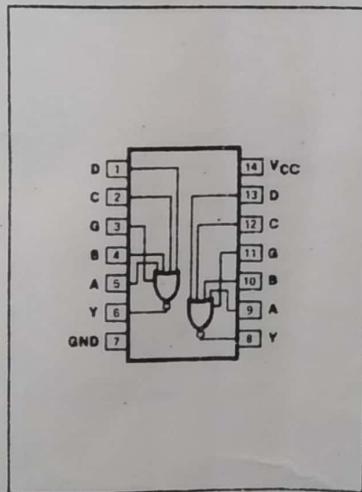
H = HIGH voltage level  
L = LOW voltage level  
X = Don't care

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

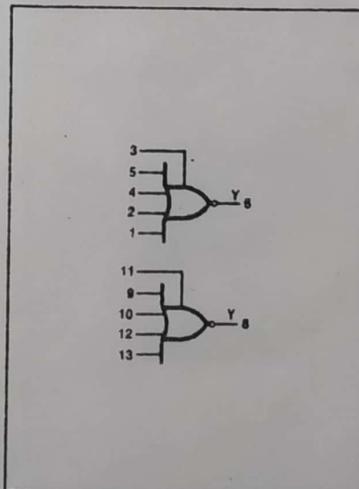
PINS	DESCRIPTION	54/74
A-D	Inputs	1ui
G	Input	4ui
Y	Output	10ui

NOTE  
Where a 54/74 unit load (ui) is understood to be  $40\mu A$   $I_{IH}$  and  $-1.6mA$   $I_{IL}$ .

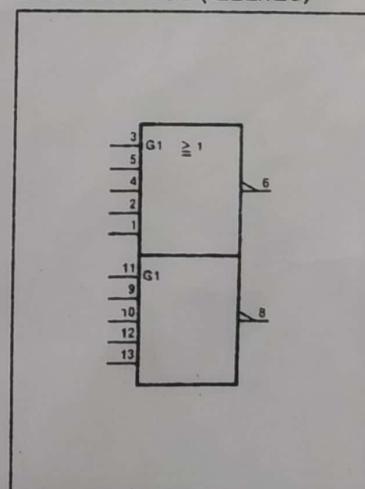
## PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



## Triple Three-Input NOR Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7427	9ns	13mA
74LS27	10ns	2.7mA

## ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$ ; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$ ; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7427N • N74LS27N	
Plastic SO	N74LS27D	

## FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
L	L	L	H
X	X	H	L
X	H	X	L
H	X	X	L

H = HIGH voltage level

L = LOW voltage level

X = Don't care

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74LS
A-C	Inputs	1 <ul style="list-style-type: none">i</ul>	1 <ul style="list-style-type: none">LS</ul> <ul style="list-style-type: none">i</ul>
Y	Output	10 <ul style="list-style-type: none">i</ul>	10 <ul style="list-style-type: none">LS</ul> <ul style="list-style-type: none">i</ul>

## NOTE

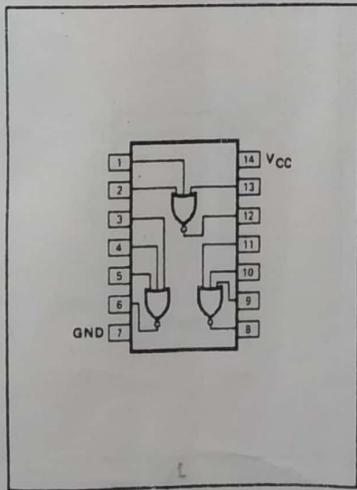
Where a 54/74 unit load (

i
) is understood to be 40 $\mu$ A  $I_{IH}$  and -1.6mA  $I_{IL}$ , a 54/74LS unit load (

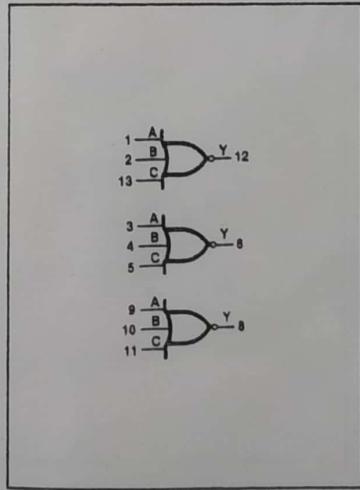
LS

i
) is 20 $\mu$ A  $I_{IH}$  and -0.4mA  $I_{IL}$ .

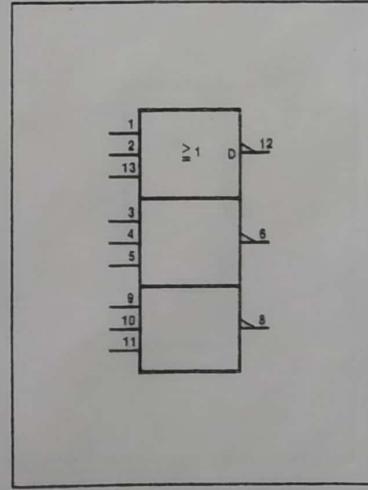
## PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



## GATES

54/7430, LS30

## Eight-Input NAND Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7430	11ns	2mA
74LS30	11ns	0.5mA

## ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$ ; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$ ; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7430N • N74LS30N	
Plastic SO	N74LS30D	
Ceramic DIP		S54LS30F
Flatpack		S54LS30W

## FUNCTION TABLE

INPUTS								OUTPUT
A	B	C	D	E	F	G	H	Y
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
H	H	H	H	H	H	H	H	L

H = HIGH voltage level

L = LOW voltage level

X = Don't care

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

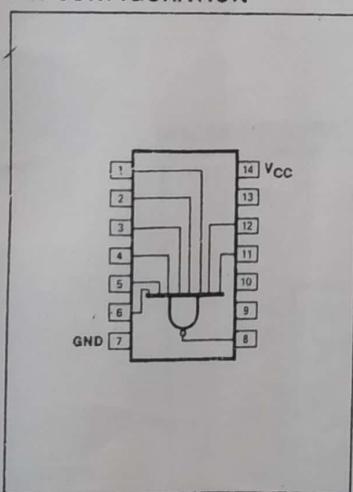
PINS	DESCRIPTION	54/74	54/74LS
A-H	Inputs	1 <ul style="list-style-type: none"></ul>	1LS <ul style="list-style-type: none"></ul>
Y	Output	10 <ul style="list-style-type: none"></ul>	10LS <ul style="list-style-type: none"></ul>

## NOTE

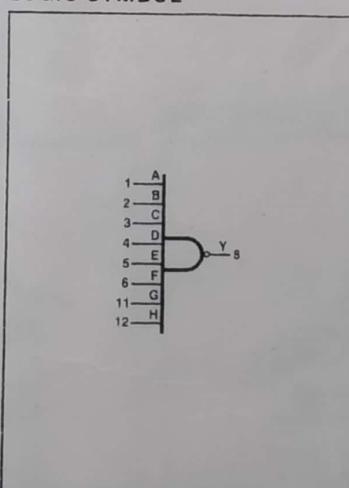
Where a 54/74 unit load ( $\mu A$ ) is understood to be  $40\mu A I_{IH}$  and  $-1.6mA I_{IL}$ , and 54/74LS unit load (LS


) is  $20\mu A I_{IH}$  and  $-0.4mA I_{IL}$ .

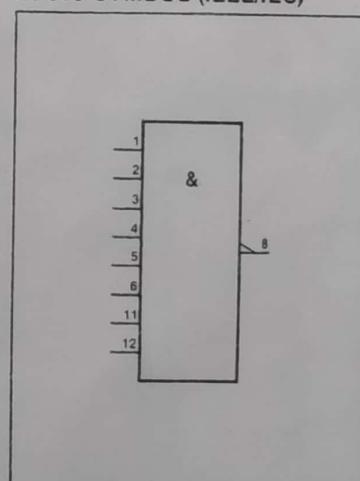
## PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



**GATES**

54/7432, LS32, S32

**Quad Two-Input OR Gate**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7432	12ns	19mA
74LS32	14ns	4.0mA
74S32	4ns	28mA

**ORDERING CODE**

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$ ; $T_A = 0^\circ C$ to $70^\circ C$	$V_{CC} = 5V \pm 10\%$ ; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7432N • N74LS32N N74S32N	
Plastic SO	N74LS32D • N74S32D	
Ceramic DIP		S5432F • S54LS32F
Flatpack		S5432W • S54LS32W
LLCC		S54LS32G

**FUNCTION TABLE**

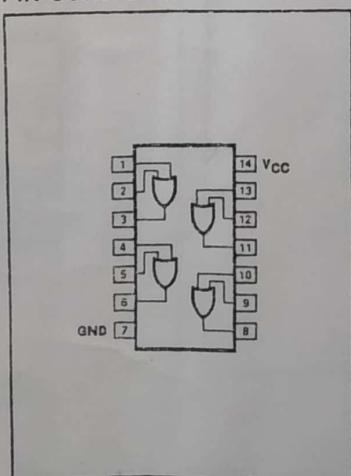
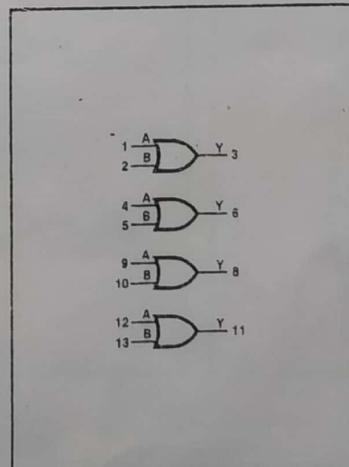
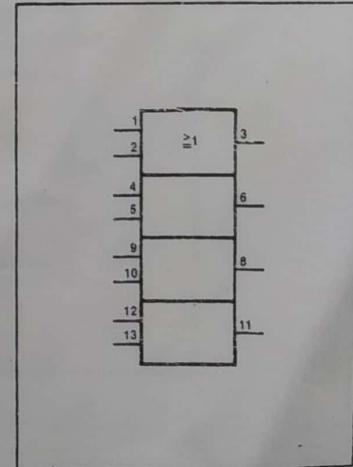
INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = HIGH voltage level  
L = LOW voltage level

**INPUT AND OUTPUT LOADING AND FAN-OUT TABLE**

PINS	DESCRIPTION	54/74	54/74S	54/74LS
A, B	Inputs	1 <ul style="list-style-type: none"></ul>	1 <ul style="list-style-type: none"></ul>	1 <ul style="list-style-type: none"></ul>
Y	Output	10 <ul style="list-style-type: none"></ul>	10 <ul style="list-style-type: none"></ul>	10 <ul style="list-style-type: none"></ul>

NOTE  
Where a 54/74 unit load ( $\mu$ l) is understood to be  $40\mu A$   $I_{IH}$  and  $-1.6mA$   $I_{IL}$ , a 54/74S unit load (Sul) is  $50\mu A$   $I_{IH}$  and  $-2.0mA$   $I_{IL}$ , and a 54/74LS unit load (LSul) is  $20\mu A$   $I_{IH}$  and  $-0.4mA$   $I_{IL}$ .

**PIN CONFIGURATION****LOGIC SYMBOL****LOGIC SYMBOL (IEEE/IEC)**

**BUFFERS**

54/7438, LS38, S38

**Quad Two-Input NAND Buffers (Open Collector)**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7438	13ns	28mA
74LS38	19ns	3.5mA
74S38	6.5ns	33mA

**ORDERING CODE**

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$ ; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$ ; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7438N • N74LS38N N74S38N	
Plastic SO	N74S38D • N74LS38D	

**FUNCTION TABLE**

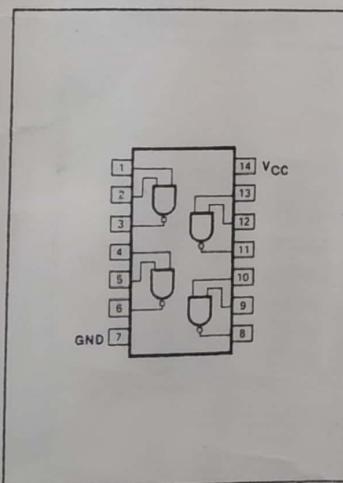
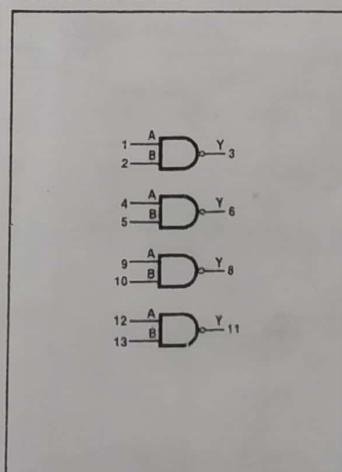
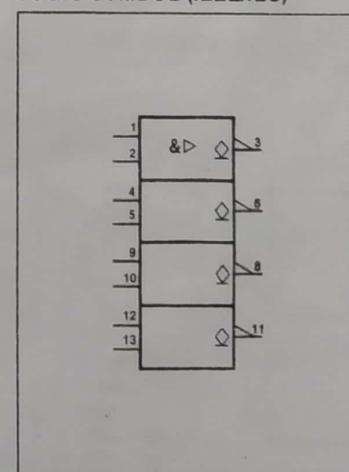
INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level  
L = LOW voltage level

**INPUT AND OUTPUT LOADING AND FAN-OUT TABLE**

PINS	DESCRIPTION	54/74	54/74S	54/74LS
A, B	Inputs	1 <ul style="list-style-type: none"></ul>	2 <ul style="list-style-type: none"></ul>	1LS <ul style="list-style-type: none"></ul>
Y	Output	30 <ul style="list-style-type: none"></ul>	30 <ul style="list-style-type: none"></ul>	30LS <ul style="list-style-type: none"></ul>

NOTE  
Where a 54/74 unit load (ul) is understood to be  $40\mu A I_{IH}$  and  $-1.6mA I_{IL}$ , a 54/74S unit load (Sul) is  $50\mu A I_{IH}$  and  $-2.0mA I_{IL}$ , and 54/74LS unit load (LSul) is  $20\mu A I_{IH}$  and  $-0.4mA I_{IL}$ .

**PIN CONFIGURATION****LOGIC SYMBOL****LOGIC SYMBOL (IEEE/IEC)**

**FLIP-FLOPS**

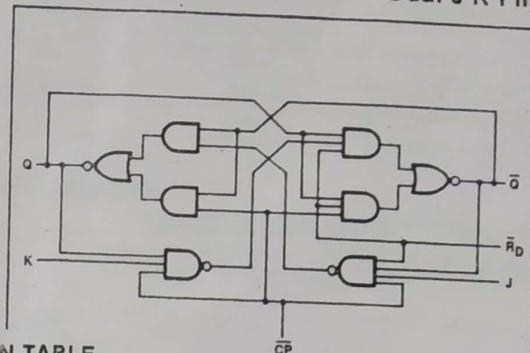
54/7473, LS73

**DESCRIPTION**

The '73 is a dual flip-flop with individual J, K, Clock and direct Reset inputs. The 7473 is positive pulse-triggered. JK information is loaded into the master while the Clock is HIGH and transferred to the slave on the HIGH-to-LOW transition. For the 7473, the J and K inputs should be stable while the Clock is HIGH for conventional operation.

The 74LS73 is a negative edge-triggered flip-flop. The J and K inputs must be stable one setup time prior to the HIGH-to-LOW Clock transition for predictable operation.

The Reset ( $\bar{R}_D$ ) is an asynchronous active LOW input. When LOW, it overrides the Clock and Data inputs, forcing the Q output LOW and the  $\bar{Q}$  output HIGH.

**LOGIC DIAGRAM****Dual J-K Flip-Flop****FUNCTION TABLE**

OPERATING MODE	INPUTS		OUTPUTS			
	$\bar{R}_D$	$\bar{C}P^{(b)}$	J	K	Q	$\bar{Q}$
Asynchronous Reset (Clear)	L	X	X	X	L	H
Toggle	H	↑	h	h	q	q
Load "0" (Reset)	H	↑	l	h	L	H
Load "1" (Set)	H	↑	l	h	H	L
Hold "no change"	H	↑	l	l	q	q

H = HIGH voltage level steady state.

h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.<sup>(a)</sup>

l = LOW voltage level steady state.

i = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.<sup>(a)</sup>

q = Lower case letters indicate the state of the referenced output prior to the HIGH-to-LOW Clock transition.

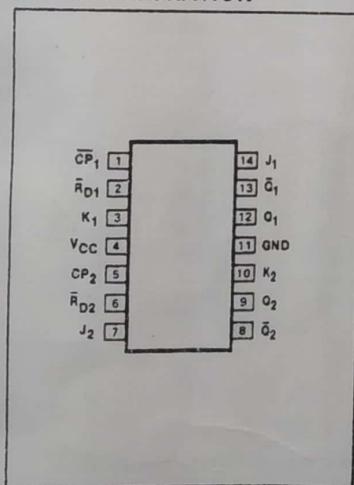
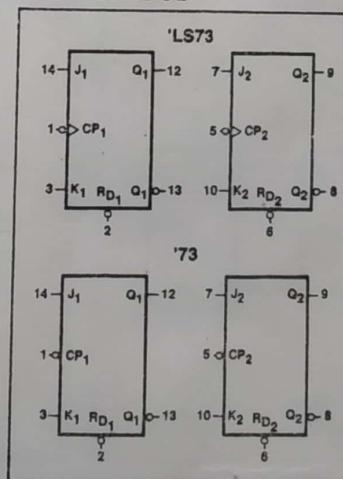
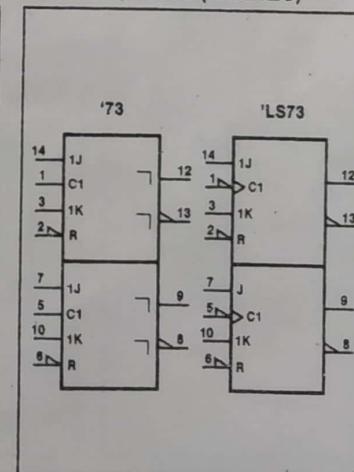
X = Don't care.

↑ = Positive Clock pulse.

**NOTES**

a. The J and K Inputs of the 7473 must be stable while the Clock is HIGH for conventional operation.

b. The 74LS73 is edge triggered. Data must be stable one setup time prior to the negative edge of the Clock for predictable operation.

**PIN CONFIGURATION****LOGIC SYMBOL****LOGIC SYMBOL (IEEE/IEC)**

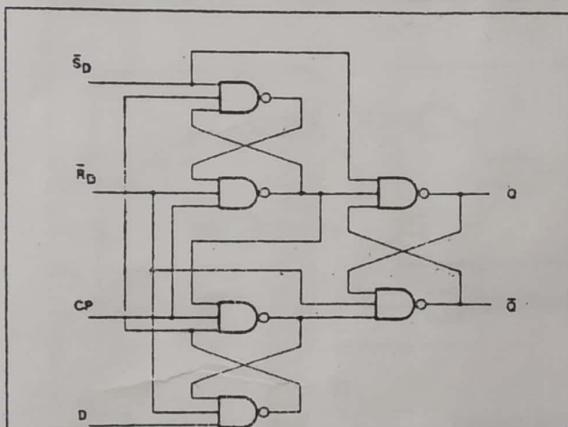
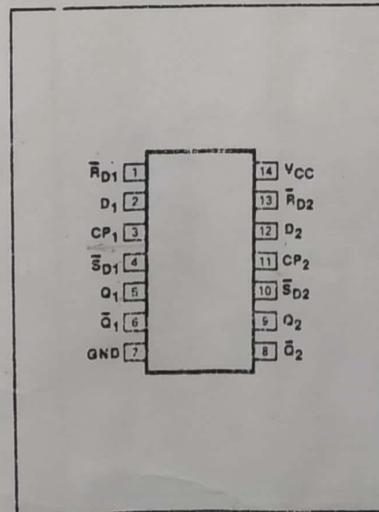
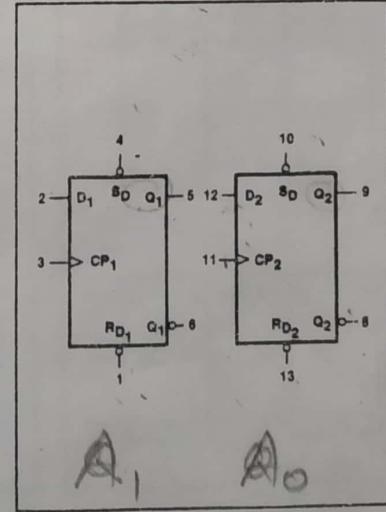
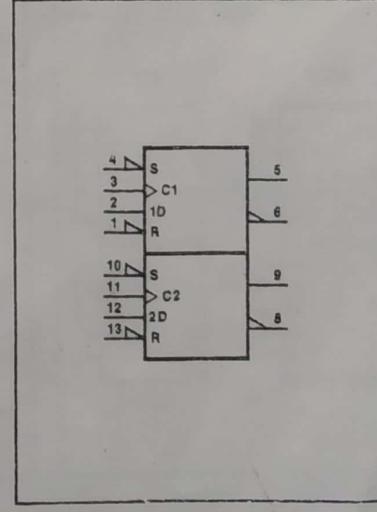
**FLIP-FLOPS**

54/7474, LS74A, 74

**Dual D-Type Flip-Flop****DESCRIPTION**

The '74 is a dual positive edge-triggered D-type flip-flop featuring individual Data, Clock, Set and Reset inputs; also complementary Q and  $\bar{Q}$  outputs.

Set ( $\bar{S}_D$ ) and Reset ( $\bar{R}_D$ ) are asynchronous active-LOW inputs and operate independently of the Clock input. Information on the Data (D) input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one setup time prior to the LOW-to-HIGH clock transition for predictable operation. Although the Clock input is level-sensitive, the positive transition of the clock pulse between the 0.8V and 2.0V levels should be equal to or less than the clock-to-output delay time for reliable operation.

**LOGIC DIAGRAM****PIN CONFIGURATION****LOGIC SYMBOL****LOGIC SYMBOL (IEEE/IEC)**

**FLIP-FLOPS**

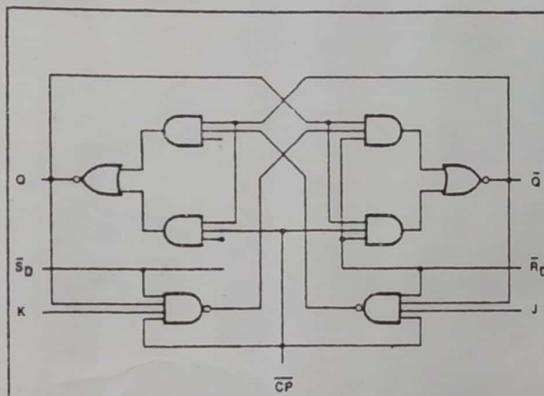
54/7476, LS76

**Dual J-K Flip-Flop****DESCRIPTION**

The '76 is a dual J-K flip-flop with individual J, K, Clock, Set and Reset inputs. The 7476 is positive pulse-triggered. JK information is loaded into the master while the Clock is HIGH and transferred to the slave on the HIGH-to-LOW Clock transition. The J and K inputs must be stable while the Clock is HIGH for conventional operation.

The 74LS76 is a negative edge-triggered flip-flop. The J and K inputs must be stable only one setup time prior to the HIGH-to-LOW Clock transition.

The Set ( $\bar{S}_D$ ) and Reset ( $\bar{R}_D$ ) are asynchronous active LOW inputs. When LOW, they override the Clock and Data inputs, forcing the outputs to the steady state levels as shown in the Function Table.

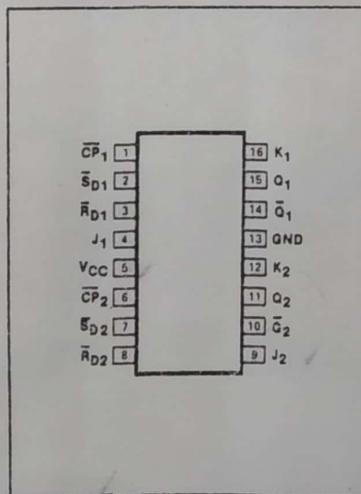
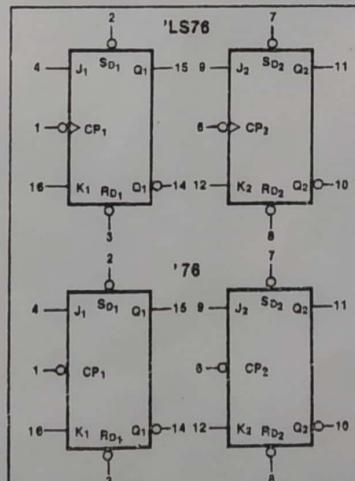
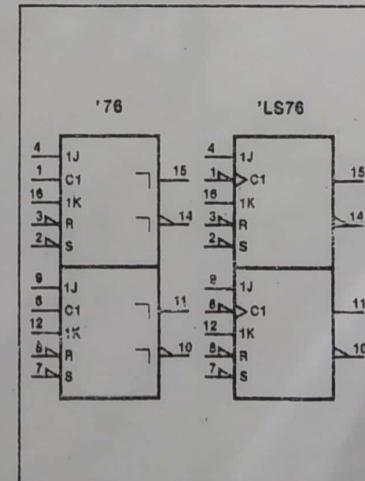
**LOGIC DIAGRAM****ORDERING CODE**

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$ ; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$ ; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7476N • N74LS76N	
Ceramic DIP		S5476F • S54LS76F
Flatpack		S5476W • S54LS76W

**FUNCTION TABLE**

OPERATING MODE	INPUTS				OUTPUTS		
	$\bar{S}_D$	$\bar{R}_D$	$\bar{CP}$	J	K	Q	$\bar{Q}$
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined <sup>(a)</sup>	L	L	X	X	X	H	H
Toggle	H	H	—	h	h	—	q
Load "0" (Reset)	H	H	—	l	h	L	H
Load "1" (Set)	H	H	—	h	l	H	L
Hold "no change"	H	H	—	l	l	q	—

- = HIGH voltage level steady state.
- = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.<sup>(c)</sup>
- = LOW voltage level steady state.
- = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.<sup>(c)</sup>
- = Lower case letters indicate the state of the referenced output prior to the HIGH-to-LOW Clock transition.

**PIN CONFIGURATION****LOGIC SYMBOL****LOGIC SYMBOL (IEEE/IEC)**

## ADDERS

54/7483, LS83A

## 4-Bit Full Adder

- High speed 4-bit binary addition
- Cascadeable in 4-bit increments
- LS83A has fast internal carry lookahead
- See '283 for corner power pin version

TYPE	TYPICAL ADD TIMES (Two 8-bit Words)	TYPICAL SUPPLY CURRENT (Total)
7483	23ns	66mA
74LS83A	25ns	19mA

## ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$ ; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$ ; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7483N • N74LS83AN	
Plastic SO	N74LS83AD	
Ceramic DIP		S5483F • S54LS83AF
Flatpack		S5483W • S54LS83AW

## DESCRIPTION

The '83 adds two 4-bit binary words ( $A_n$  plus  $B_n$ ) plus the incoming carry. The binary sum appears on the Sum outputs ( $\Sigma_1$ – $\Sigma_4$ ) and the outgoing carry ( $C_{OUT}$ ) according to the equation:

$$\begin{aligned} C_{IN} + (A_1 + B_1) + 2(A_2 + B_2) + 4(A_3 + B_3) \\ + 8(A_4 + B_4) = \Sigma_1 + 2\Sigma_2 + 4\Sigma_3 + 8\Sigma_4 \\ + 16C_{OUT} \end{aligned}$$

Where (+) = plus.

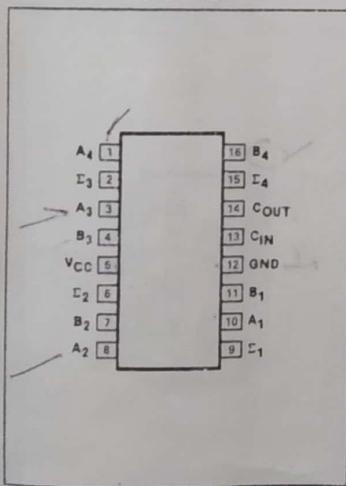
Due to the symmetry of the binary add function, the '83 can be used with either all active-HIGH operands (positive logic) or with all active-LOW operands (negative logic). See Function Table. With active-HIGH inputs,  $C_{IN}$  cannot be left open; it must be held LOW when no "carry in" is intended. Interchanging inputs of equal weight does not affect the operation, thus  $C_{IN}$ ,  $A_1$ ,  $B_1$ , can arbitrarily be assigned to pins 10, 11, 13, etc.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

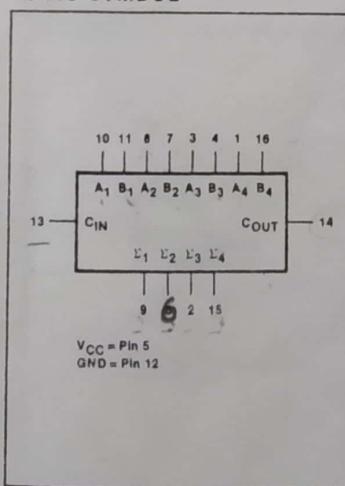
PINS	DESCRIPTION	54/74	54/74LS
$A_1, B_1, A_3, B_3, C_{IN}$	Inputs	2 <u>u</u> I	
$A_2, B_2, A_4, B_4$	Inputs	1 <u>u</u> I	
$A, B$	Inputs		2LS <u>u</u> I
$C_{IN}$	Input		1LS <u>u</u> I
Sum	Outputs	10 <u>u</u> I	10LS <u>u</u> I
Carry	Output	5 <u>u</u> I	10LS <u>u</u> I

NOTE  
Where a 54/74 unit load (uI) is understood to be  $40\mu A I_{IH}$  and  $-1.6mA I_{IL}$  and a 54/74LS unit load (LSuI) is  $20\mu A I_{IH}$  and  $-0.4mA I_{IL}$ .

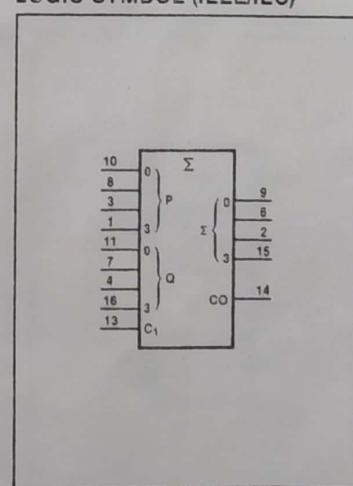
## PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



**GATES****54/7486, LS86, S86****Quad Two-Input Exclusive-OR Gate**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7486	14ns	30mA
74LS86	10ns	6.1mA
74S86	7ns	50mA

**ORDERING CODE**

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$ ; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$ ; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7486N • N74LS86N N74S86N	
Plastic SO	N74LS86D • N74S86D	
Ceramic DIP		S5486F • S54LS86F S54S86F
Flatpack		S5486W • S54LS86W S54S86W
LLCC		S54LS86G

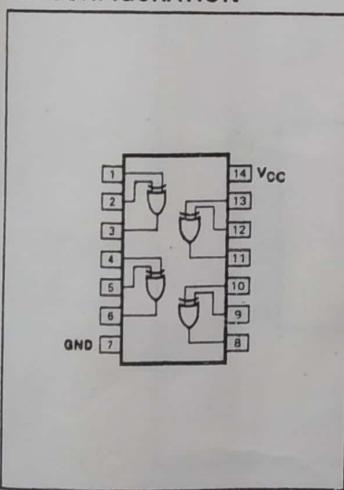
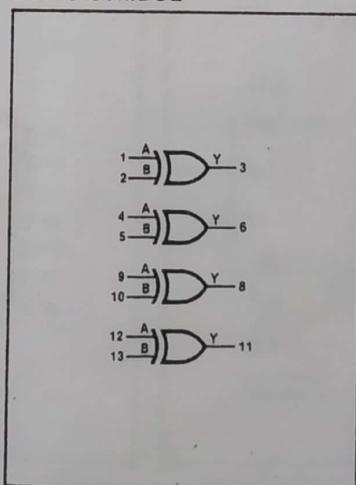
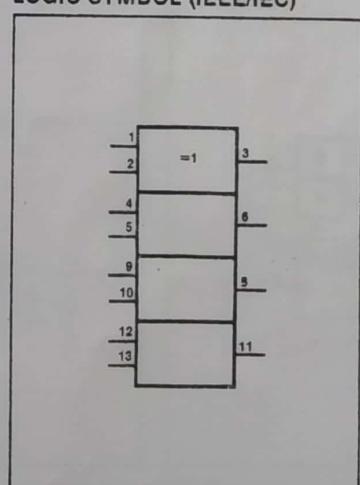
**FUNCTION TABLE**

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = HIGH voltage level  
L = LOW voltage level**INPUT AND OUTPUT LOADING AND FAN-OUT TABLE**

PINS	DESCRIPTION	54/74	54/74S	54/74LS
A, B	Inputs	1uI	1SuI	1LSuI
Y	Output	10uI	10SuI	10LSuI

## NOTE

Where a 54/74 unit load (uI) is understood to be  $40\mu A I_{IH}$  and  $-1.6mA I_{IL}$ , a 54/74S unit load (SuI) is  $50\mu A I_{IH}$  and  $-2.0mA I_{IL}$ , and a 54/74LS unit load (LSuI) is  $20\mu A I_{IH}$  and  $-0.4mA I_{IL}$ .**PIN CONFIGURATION****LOGIC SYMBOL****LOGIC SYMBOL (IEEE/IEC)**

**COUNTERS**

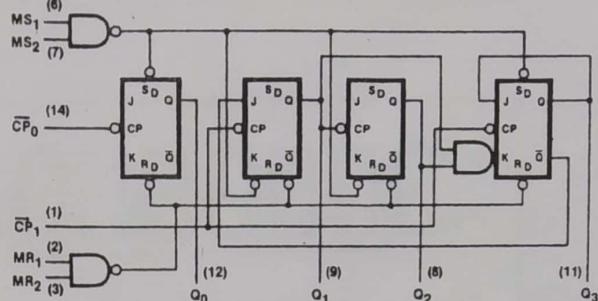
54/7490, LS90

**DESCRIPTION**

The '90 is a 4-bit, ripple-type Decade Counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-five section. Each section has a separate Clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous Master Reset ( $MR_1 \cdot MR_2$ ) is provided which overrides both clocks and resets (clears) all the flip-flops. Also provided is a gated AND asynchronous Master Set ( $MS_1 \cdot MS_2$ ) which overrides the clocks and the MR inputs, setting the outputs to nine (HLLH).

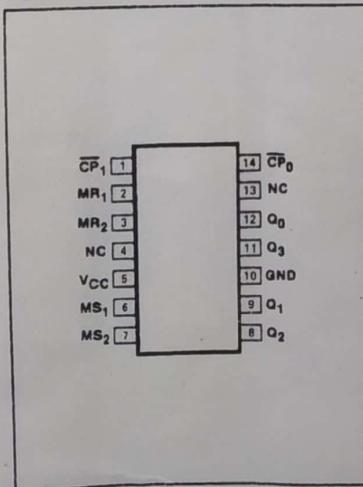
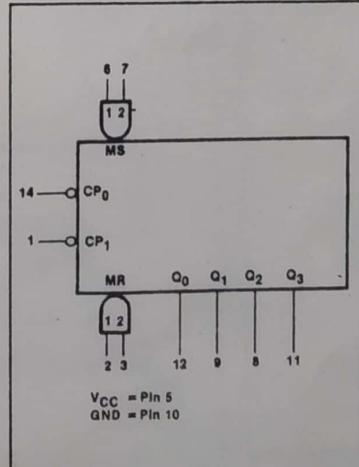
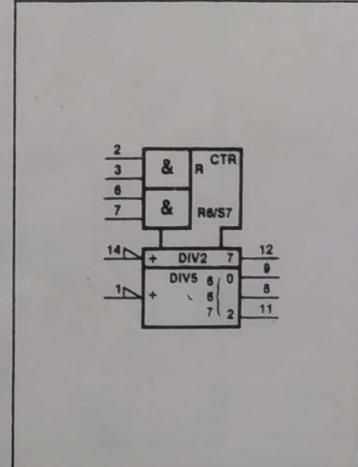
Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a BCD (8421) counter the  $\overline{CP}_1$  input must be externally connected to the  $Q_0$  output. The  $\overline{CP}_0$  input receives the incoming count producing a BCD count sequence. In a symmetrical Bi-quinary divide-by-ten counter the  $Q_3$  output must be connected externally to the  $\overline{CP}_0$  input. The input count is then applied to the  $CP_1$  input and a divide-by-ten square wave is obtained at

**LOGIC DIAGRAM****Decade Counter****MODE SELECTION—FUNCTION TABLE**

RESET/SET INPUTS				OUTPUTS			
MR <sub>1</sub>	MR <sub>2</sub>	MS <sub>1</sub>	MS <sub>2</sub>	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>
H	H	L	X	X	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	X	Count		
X	L	X	L	L	Count		
L	X	X	L	L	Count		
H	L	L	X	X	Count		

output  $Q_0$ . To operate as a divide-by-two and a divide-by-five counter no external interconnections are required. The first flip-flop is used as a binary element for the

divide-by-two function ( $\overline{CP}_0$  as the input and  $Q_0$  as the output). The  $\overline{CP}_1$  input is used to obtain a divide-by-five operation at the  $Q_3$  output.

**PIN CONFIGURATION****LOGIC SYMBOL****LOGIC SYMBOL (IEEE/IEC)**

**REGISTER**

54/7491A

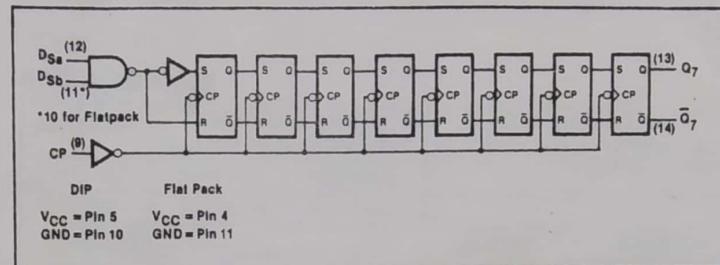
**8-Bit Shift Register**

- 8-bit serial-in-serial-out shift register
- Common buffered clock
- 2-input gate for serial data entry
- True and Complement outputs

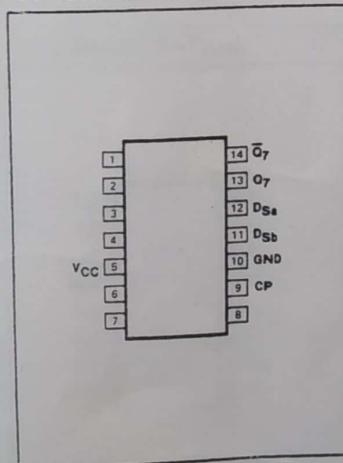
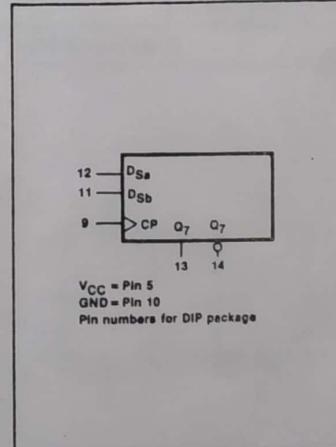
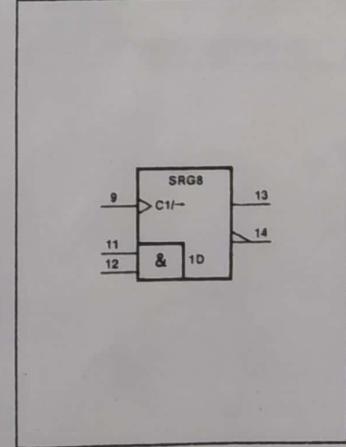
**DESCRIPTION**

The '91A is an 8-bit serial-in-serial-out shift register. The serial data is entered through a 2-input AND gate ( $D_{Sa}$  and  $D_{Sb}$ ). HIGH data is entered when both  $D_{Sa}$  and  $D_{Sb}$  are HIGH. LOW data is entered when either Serial Data input is LOW. The Data inputs are edge-triggered and must be stable just one setup time prior to the LOW-to-HIGH transition of the Clock input (CP) for predictable operation. The data is shifted one bit to the right ( $Q_0 - Q_2 \dots - Q_7$ ) synchronous with each LCW-to-HIGH clock transition. The '91A has no reset capacity, so initialization requires the shifting in of at least 8 bits of known data. Once the register is fully loaded, the Q output follows the Serial inputs delayed by eight clock pulses. The Complement ( $\bar{Q}$ ) output from the last stage is also available for simpler decoding applications.

TYPE	TYPICAL $f_{MAX}$	TYPICAL SUPPLY CURRENT (Total)
7491A	18MHz	35mA

**LOGIC DIAGRAM****MODE SELECT—FUNCTION TABLE**

OPERATING MODE	INPUTS			FIRST STAGE		OUTPUTS	
	CP	D <sub>Sa</sub>	D <sub>Sb</sub>	Q <sub>0</sub>	Q̄ <sub>0</sub>	Q <sub>7</sub>	Q̄ <sub>7</sub>
Shift, reset first stage	1	1	X	X	L	H	Q <sub>6</sub> Q̄ <sub>6</sub>
Shift, set first stage	1	X	1	1	L	H	Q <sub>6</sub> Q̄ <sub>6</sub>

**PIN CONFIGURATION****LOGIC SYMBOL****LOGIC SYMBOL (IEEE/IEC)**

## FLIP-FLOPS

54/74LS112, S112

## Dual J-K Edge-Triggered Flip-Flop

## DESCRIPTION

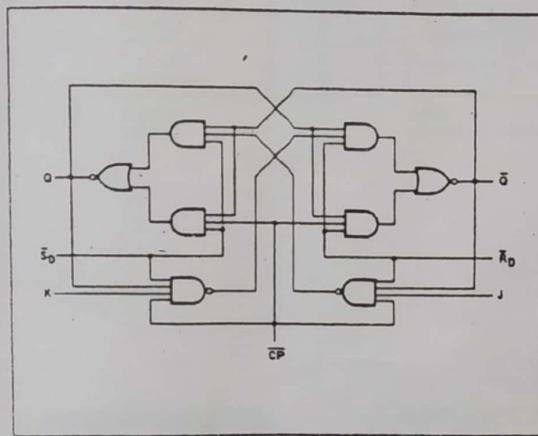
The '112 is a dual J-K negative edge-triggered flip-flop featuring individual J, K, Clock, Set and Reset inputs. The Set ( $S_D$ ) and Reset ( $\bar{R}_D$ ) inputs, when LOW, set or reset the outputs as shown in the Function Table regardless of the levels at the other inputs.

TYPE	TYPICAL $I_{MAX}$	TYPICAL SUPPLY CURRENT (Total)
74LS112	45MHz	4mA
74S112	125MHz	15mA

## ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$ ; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$ ; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74S112N • N74LS112N	
Plastic SO	N74LS112D • N74S112D	
Ceramic DIP		S54S112F • S54LS112F
Flatpack		S54S112W • S54LS112W
LLCC		S54LS112G

## LOGIC DIAGRAM



## FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$\bar{S}_D$	$\bar{R}_D$	$\bar{C}P$	J	K	Q	$\bar{Q}$
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined	L	L	X	X	X	H	H
Toggle	H	H	I	h	h	$\bar{q}$	q
Load "0" (Reset)	H	H	I	I	h	L	H
Load "1" (Set)	H	H	I	h	I	H	L
Hold "no change"	H	H	I	I	I	q	$\bar{q}$

H = HIGH voltage level steady state.

h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.

L = LOW voltage level steady state.

I = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.

q = Lower case letters indicate the state of the referenced output one setup time prior to the HIGH-to-LOW Clock transition.

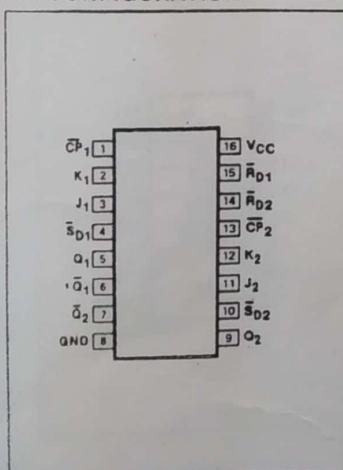
X = Don't care.

I = HIGH-to-LOW Clock transition.

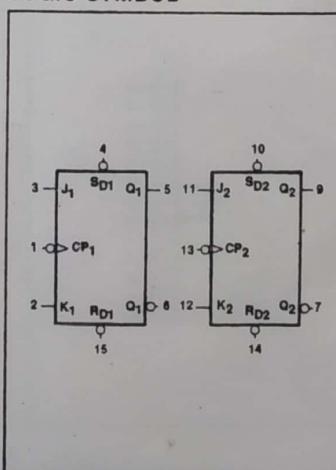
## NOTE

Both outputs will be HIGH while both  $\bar{S}_D$  and  $\bar{R}_D$  are LOW, but the output states are unpredictable if  $\bar{S}_D$  and  $\bar{R}_D$  go HIGH simultaneously.

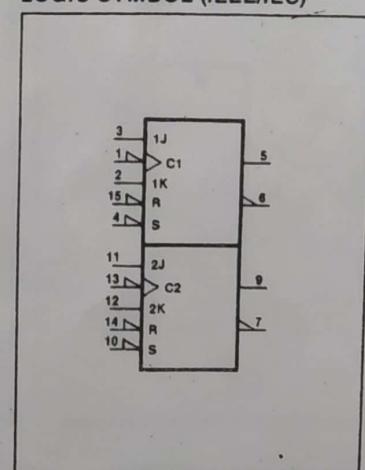
## PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



## GATE

54/74S133

## 13-Input NAND Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74S133	4ns	4mA

## ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$ ; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$ ; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74S133N	
Plastic SO	N74S133D	
Ceramic DIP		S54S133F
Flatpack		S54S133W

## FUNCTION TABLE

INPUTS	OUTPUT
A ... M	$\bar{Y}$
H ... H one input = L	L H

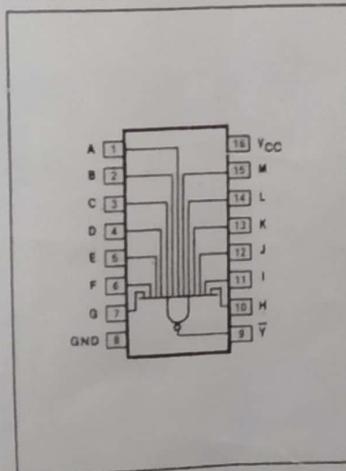
H = HIGH voltage level  
L = LOW voltage level

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

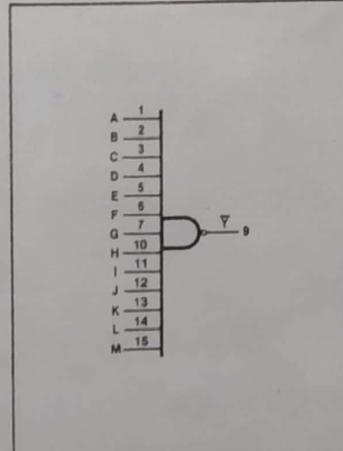
PINS	DESCRIPTION	54/74S
All	Inputs	1Sul
$\bar{Y}$	Output	10Sul

NOTE  
A 54/74S unit load (Sul) is understood to be  $50\mu A I_{IH}$  and  $-2.0mA I_{IL}$ .

## PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)

