CSE 306 (Computer Architecture Sessional)

Experiment No: 01

Name of the experiment:

ALU (Arithmetic Logic Unit) Software Implementation

Group No.	**06**
Section	A1
Department	CSE
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Introduction:

The prime objective of this assignment was to design an ALU (Arithmetic Logic Unit) which performs six arithmetic and logical operations according to the input selection bits. Three input selection bits were used for this purpose. The ALU was designed using some available logic gates for performing the operations.

Problem Specification:

An ALU (Arithmetic Logic Unit) has to be designed efficiently with the minimum number of ICs, that takes two of 4 bits input A and B, and 3 selection bits (CS2, CS1, CS0) . The ALU performs different operations according to the state of these selection bits. The change of the status flags (Carry Flag, Sign Flag, Overflow Flag, Zero Flag) also needs to be showed. The tasks which it will perform according to the selection bits are as follows :

Selection Bit			**Functions**
CS2 (Cin)	**CS1**	**CS0**	
0	0	0	Decrement A
0	1	0	Subtract with Borrow
1	0	0	Transfer A
1	1	0	Subtract
X	0	1	AND
X	1	1	XOR

Truth Tables:

CS1	CS0	X
0	0	Ai
0	1	Ai'+Bi'
1	0	Ai
1	1	Ai'

CS1	CS0	Y
0	0	1
0	1	1
1	0	Bi'
1	1	Bi'

CS1	CS0	Ci
0	0	CS2
0	1	0
1	0	CS2
1	1	0

Karnaugh Map and Equations:

Xi:

CS1 \ CS0	0	1
0	Ai	Ai' + Bi'
1	Ai	Ai'

Yi:

CS1 \ CS0	0	1
0	1	1
1	Bi'	Bi'

C_i:

CS1 \ CS0	0	1
0	CS2	0
1	CS2	0

Xi = $AiCS_0' + Ai' CS_0 CS_1 + (Ai' + Bi') CS_0 CS_1'$

= $AiCS_0' + Ai' CS_0 (CS_1' + CS_1) + Bi' CS_0 CS_1'$

= $AiCS_0' + Ai' CS_0 + Bi' CS_0 CS_1'$

= $Ai \oplus CS_0 + Bi' CS_1' CS_0$

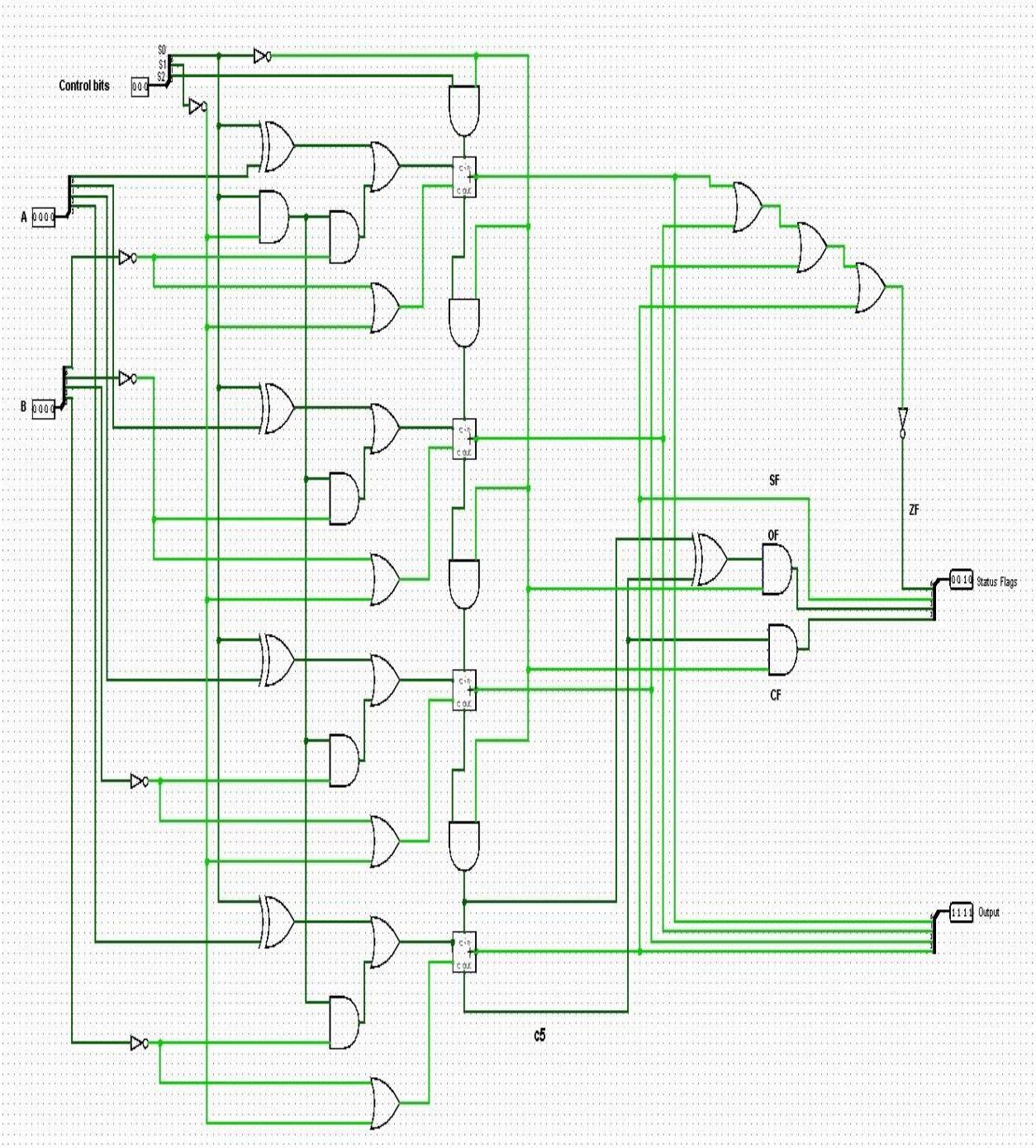
Yi = $Bi' CS_1 + CS_1'$

= $(CS_1' + CS_1) (CS_1' + Bi')$

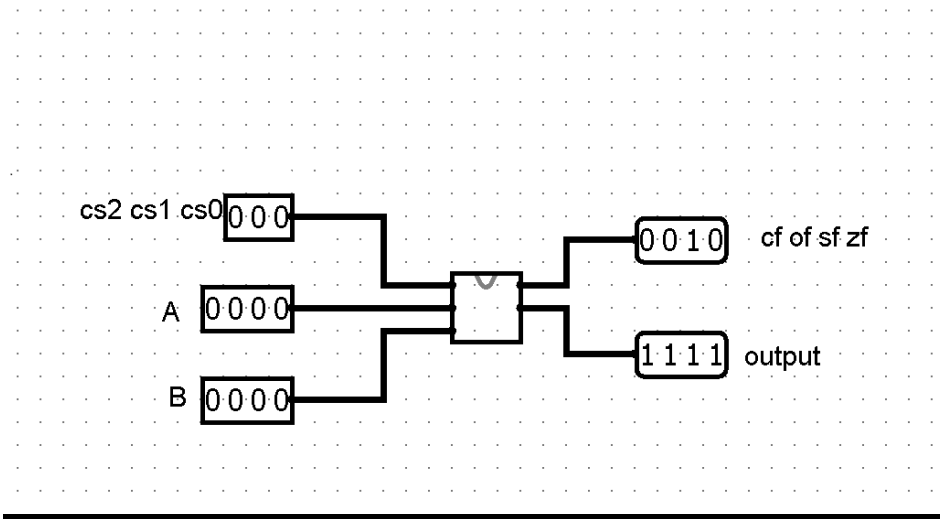
= $CS_1' + Bi'$

C_i = $CS_0' CS_2$

Circuit Diagram:



Block diagram:



IC Count:

Used IC	Operation	Count
IC 74LS04	NOT	2
IC 74LS08	AND	3
IC 74LS32	OR	3
IC 74LS86	XOR	2
IC 74LS83	Full Adder	1

Total Chips Needed: 11

Simulator Used: Logisim

Version Number: 2.7.1

Discussion:

In this assignment, a 4-bit ALU (Arithmetic Logic Unit) Simulation was designed using Logisim. This Arithmetic Logic Unit is a circuit which has two different modes of operation based on the mode variable cs0. It performs Arithmetic operations like Decrement, Subtract with borrow, Transfer, Subtract as well as Logical operations like AND, XOR. For arithmetic operations, the cs2 variable works as input carry but for logical operations, only two 4-bit numbers are needed, so it was kept as "don't care". All the flags were affected as per the rules of the Assembly Language during the arithmetic operations. The carry and overflow flags were kept 0 and the sign and zero flags were changed according to the output during logical operations.

The main focus of this assignment was to minimize the number of gates and ICs. Minimal circuits were obtained by using K-map to derive the equations and Boolean formulas to further reduce them as much as possible. Outputs of some of the gates were reused to minimize the circuit even more.

The connections were made carefully and the gates had fair distance and symmetry between them to avoid messiness and increase readability. The ALU was tested as much as possible to ensure that the circuit did not contain any error.