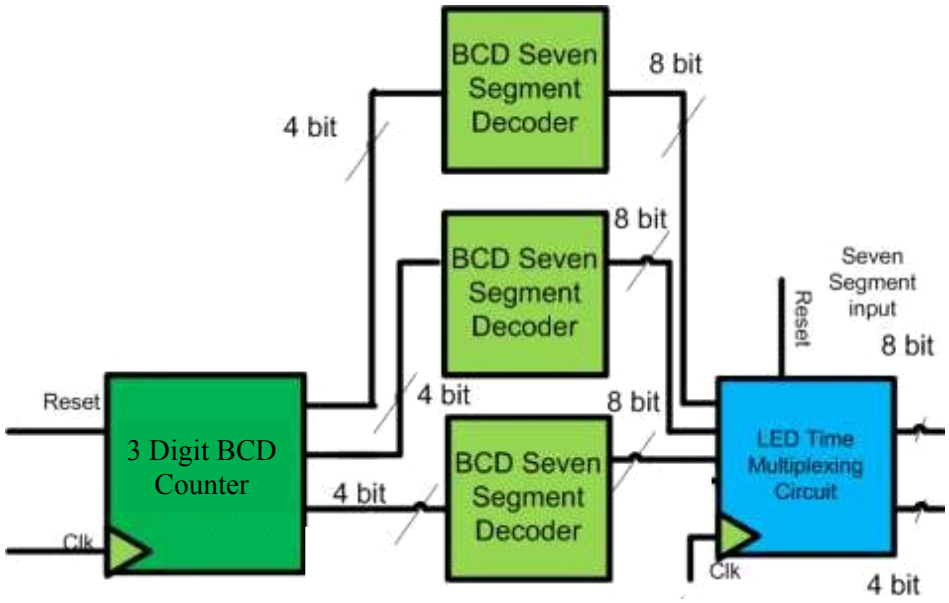
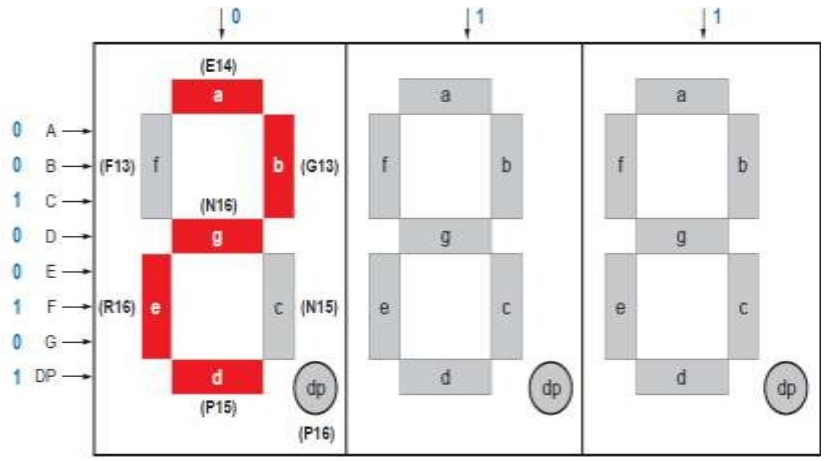
Lab No 6

4 digit BCD Counter on Multiplexed Seven Segment Display

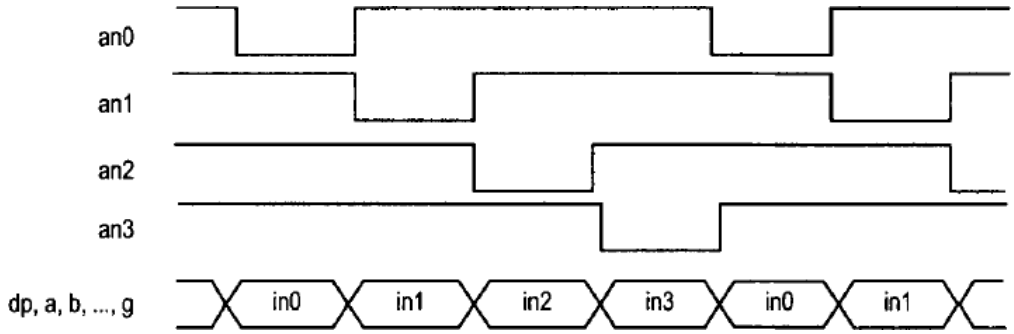
Objective: Learn to use time multiplexed 4 digit Seven Segment display

Block Diagram: The S6 board has four seven-segment LED displays, each containing seven bars and one small round dot. To reduce the use of FPGA's I/0 pins, the S6 board uses a time-multiplexing sharing scheme. In this scheme, the three displays have their individual enable signals but share eight common signals to light the segments. All signals are active low (i.e., enabled when a signal is 0). The schematic of displaying a "2" on the leftmost LED is shown in Figure.
Note that the enable signal (i.e., an) is "011". This configuration clearly can enable only one display at a time. We can time-multiplex the four LED patterns by enabling the four displays in turn, as shown in the simplified timing diagram. If the refreshing rate of the enable signal is fast enough, the human eye cannot distinguish the on and off intervals of the LEDs and perceives that all four displays are lit simultaneously. This scheme reduces the number of I/O pins from 32 to 11 (i.e., eight LED segments plus three enable signals) but requires a time-multiplexing circuit.





Timing Diagram of LED Multiplexing:



LED time Multiplexing:

The refresh rate of the enable signal has to be fast enough to fool our eyes but should be slow enough so that the LEDs can be turned on and off completely. The rate around the range 1000 Hz should work properly. In our design, we use an 18-bit binary counter for this purpose. The two MSBs are decoded to generate the enable signal and are used as the selection signal for multiplexing.

Lab Tasks:

Implement a BCD counter that runs from 000 to 999 and shows each BCD digit on the seven segment display.