**BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY**

# Gate Driver

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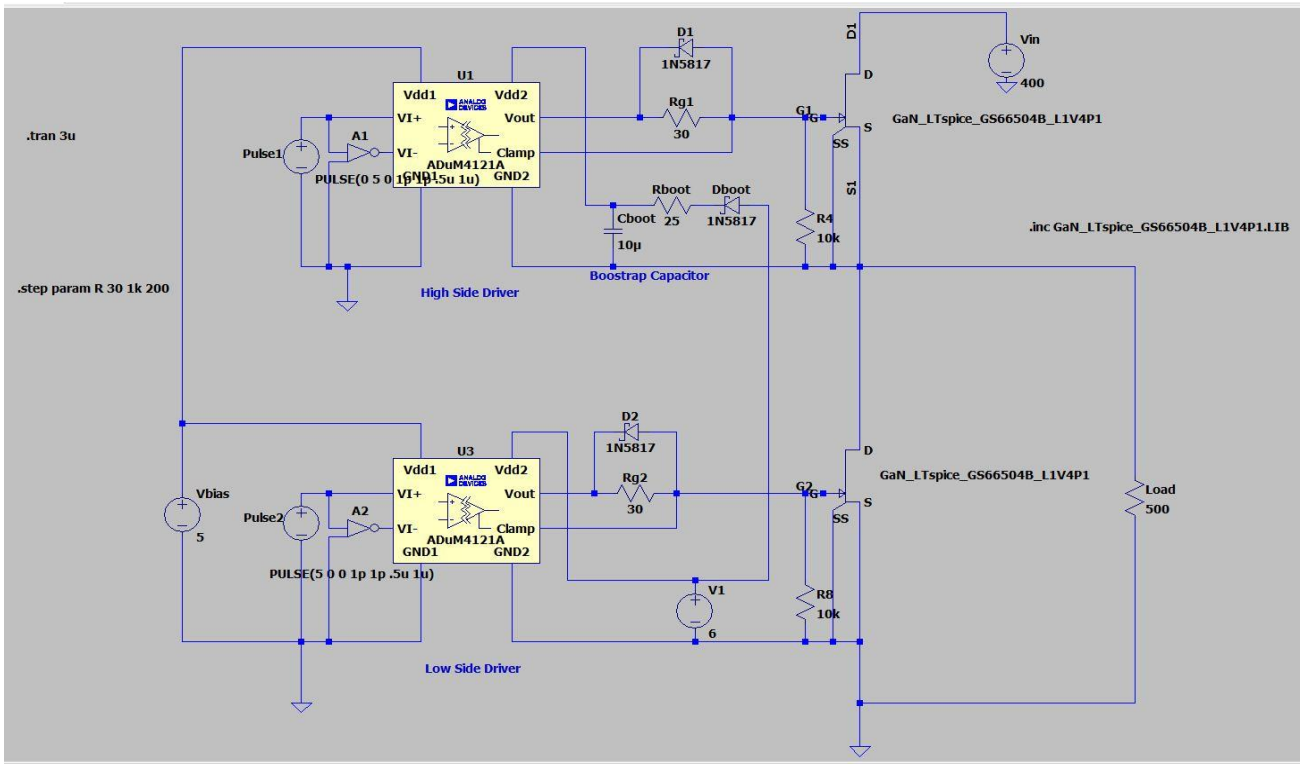
**Task:**

1. Build a half-bridge version with a similar dummy load.
2. You may still use the ideal floating sources for the gate drives, but eventually you'll need to look into possible power supply mechanisms, such as bootstrap circuit.
3. Do the maths to quantify the relationships among driver IC's output current capabilities, gate resistances, MOSFET's Qg, Ciss, Coss and other parameters, and verify by the simulations.

## 1.Schematic Diagram:




Here,

$V_{in}$ = 400V (Taken from SOA of MOSFET)

Switching_Frequency = 1MHz

Load = 500Ω (Pure resistive)

Load_current= $\frac{400}{500}$A= 0.8A

$$\mathbf{V_{Pulse}} = \begin{cases} \mathbf{0}; Keeps\ gate\ voltage\ low \\ \mathbf{5}; keeps\ gate\ voltage\ high \end{cases}$$

$$\mathbf{V_{GS}} = \begin{cases} \mathbf{0};\ \ switch\ off \\ \mathbf{6};\ \ switch\ on \end{cases}$$

**2.** $C_{boot}$ (Bootstrap Capacitor) = $\begin{cases} 406V\ ; when\ Pulse1\ is\ high \\ 6V\ ; when\ Pulse1\ is\ low \end{cases}$

## 3. Calculation and Output:

Here,

ADuM4121 IC:

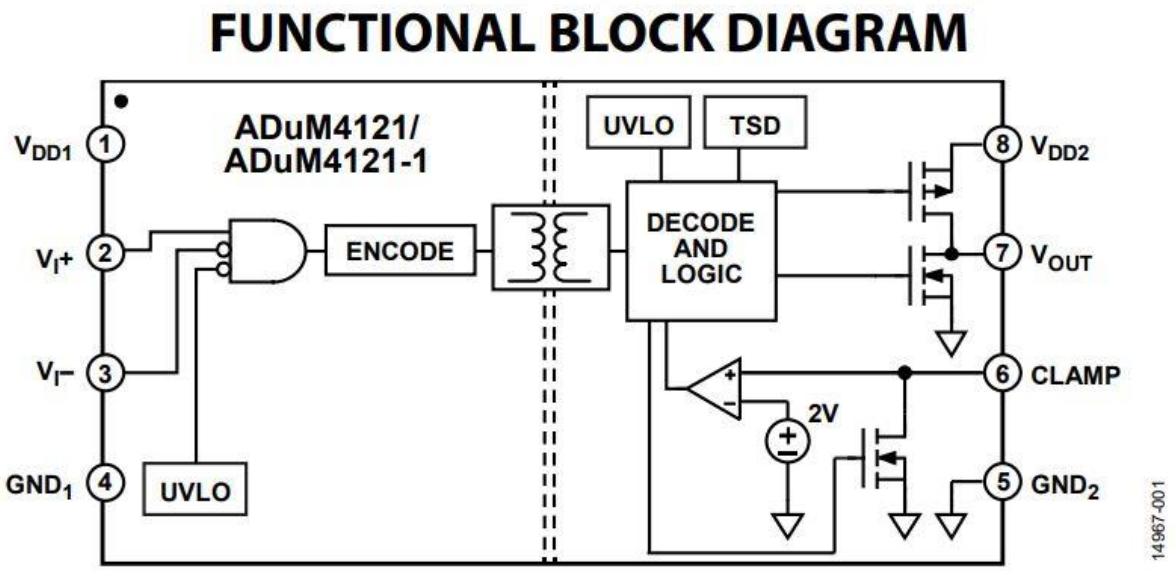



*Figure 1.*

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$V_{DD2}$ is high voltage input side → Provide $V_{GS}$ through $V_{OUT}$

$V_{OUT}$ is high voltage output side → MOSFET's gate voltage

**From Datasheet of ADuM4121:**

$I_{OUT}$ (max) = 2A

$V_{DD1}$ = 2.5 to 6.5 V

$V_{DD2}$ = 4.5 to 35 V

**From the Datasheet of GS660504B:**

Input Capacitance, $C_{ISS}$ = 130 pF

Output Capacitance, $C_{OSS}$ = 33 pF

Total gate charge, $Q_G$ = 3 nC

Rise time, $T_r$ = 4 ns

Fall Time, $T_f$ = 5.2 ns

Here,

IC's output current = MOSFET's gate current

So, Gate input current, $\mathbf{I_{G(on)} = \frac{Q_G}{T_r} = \frac{3}{4} = 750\ mA}$

Gate output current, $\mathbf{I_{G(off)} = \frac{Q_G}{T_f} = \frac{3}{5.2} = 576.92\ mA}$

**Gate Resistance Calculation:**

**Gate on Resistance:**

For first charging of gate capacitor, $\mathbf{T_r = R_{g(on)} C_{ISS}}$

$$\mathbf{R_{g(on)} = \frac{T_r}{C_{ISS}} = \frac{4\ ns}{130\ pF} = 30.76\ \Omega}$$

***Gate off resistance:**

Discharging of gate capacitor, $\mathbf{T_f = R_{g(off)}\ C_{ISS}}$

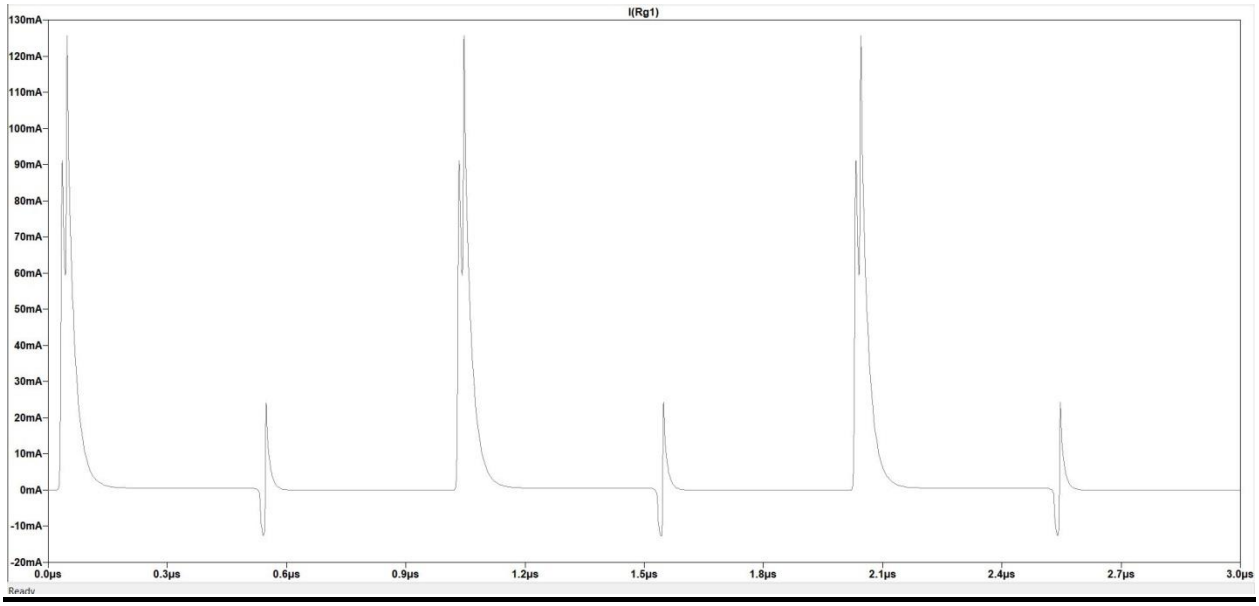
$$\mathbf{R_{g(off)} = \frac{T_f}{C_{ISS}} = \frac{5.2\ ns}{130\ pF} = 40\ \Omega}$$

***{But, $R_{g(off)}$ should be less than $R_{g(on)}$. So didn't use in the circuit}**

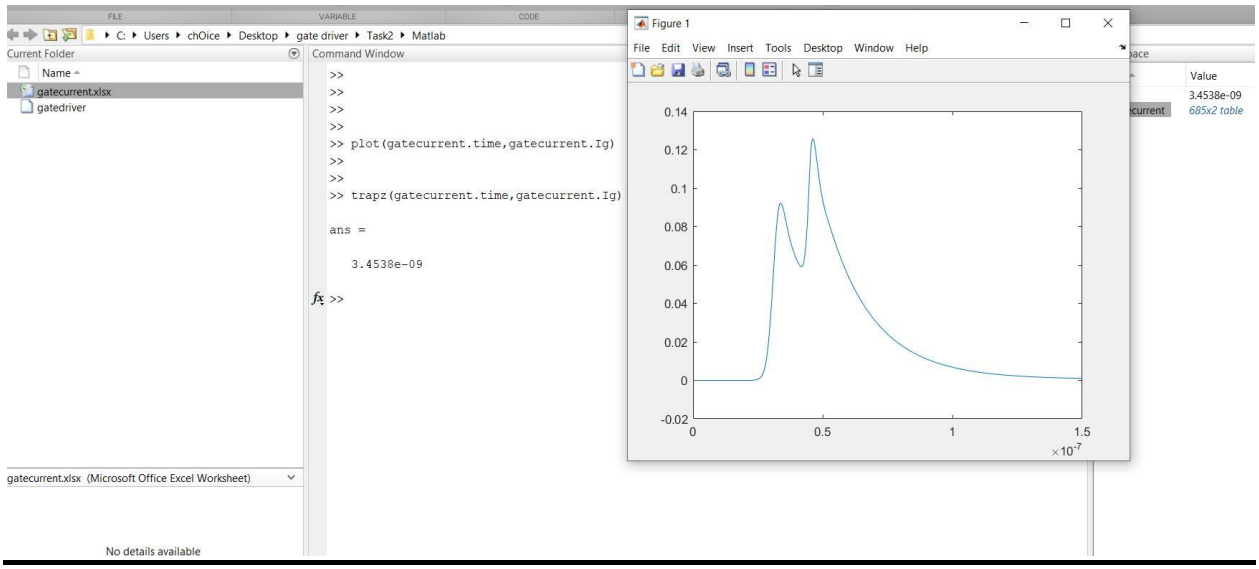
Reference for these equation: https://youtu.be/of_v2N5f788

## Simulation:

## $I_{G(on)}$ Vs time




## Gate charge test From MATLAB:




In a gate pulse we found from MATLAB, gate charge is needed **3.45nC.**

From datasheet we find $\mathbf{Q_G = 3\ nC}$. So, our finding value is very close to datasheet.

**Gate charge to Gate capacitance:**

We know,

$$C = \frac{dQ}{dV}$$

So, in this case,

$$C_{ISS} = \frac{dQ_G}{dV_{GS}}$$

During charging,

Gate charge, $Q_G$ rises 0 → 3.45 nC

⇨ $dQ_G$ = 3.45 nC

And

Gate to sourse voltage, $V_{GS}$ rises 0 → 6 V

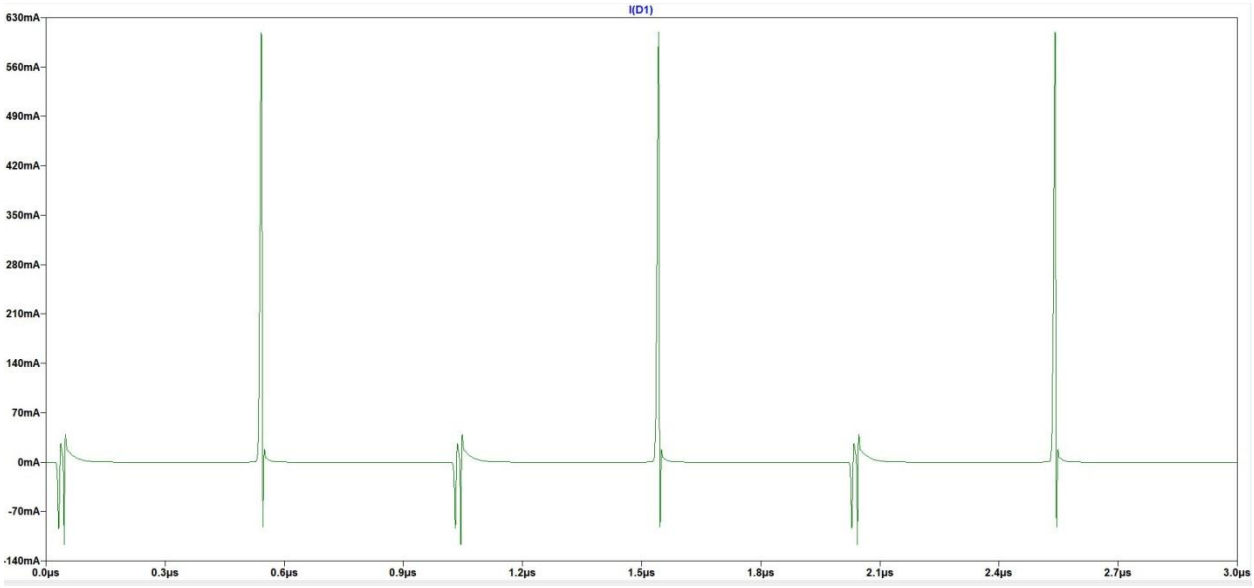
⇨ $dV_{GS}$ = 6 V

So,

$$\mathbf{C_{ISS} = \frac{3.45\ nC}{6\ V} = 575\ pF}$$

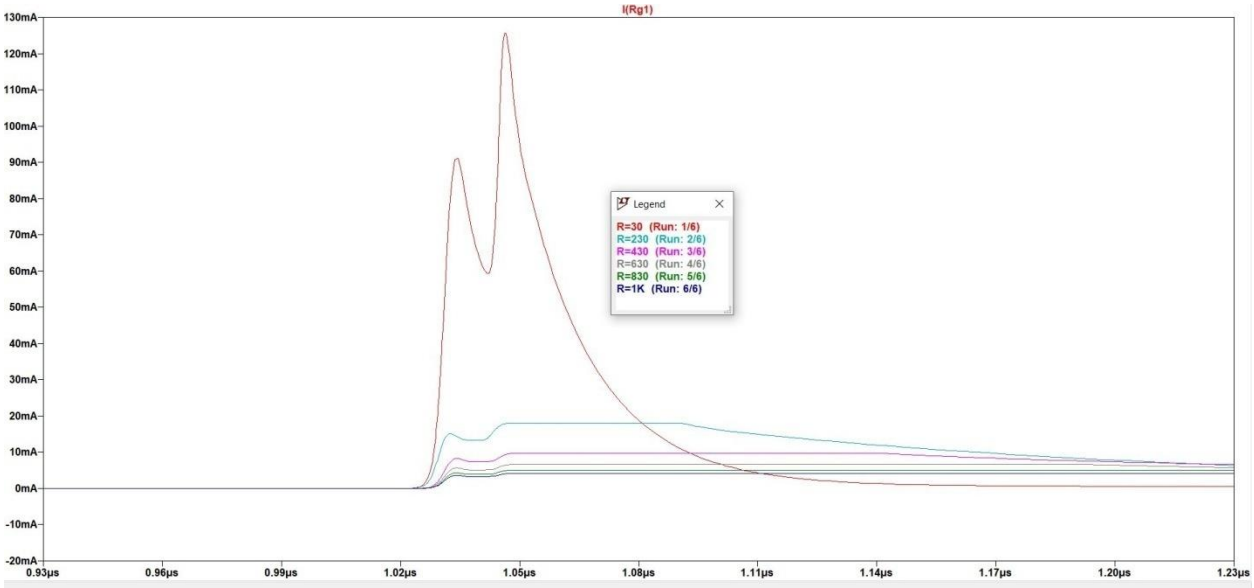
From, datasheet we find the value of $\mathbf{C_{ISS}}$ is 130 pF which is also close range of founded value from simulation.

## $I_{G(off)}$ Vs time




Calculated and simulated value is very close

## Gate Resistor VS Gate current:




Both from equation and simulated value we found that if resistance increases, charging time will also increase also power loss will increase.