

**BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY**



# Gate Driver

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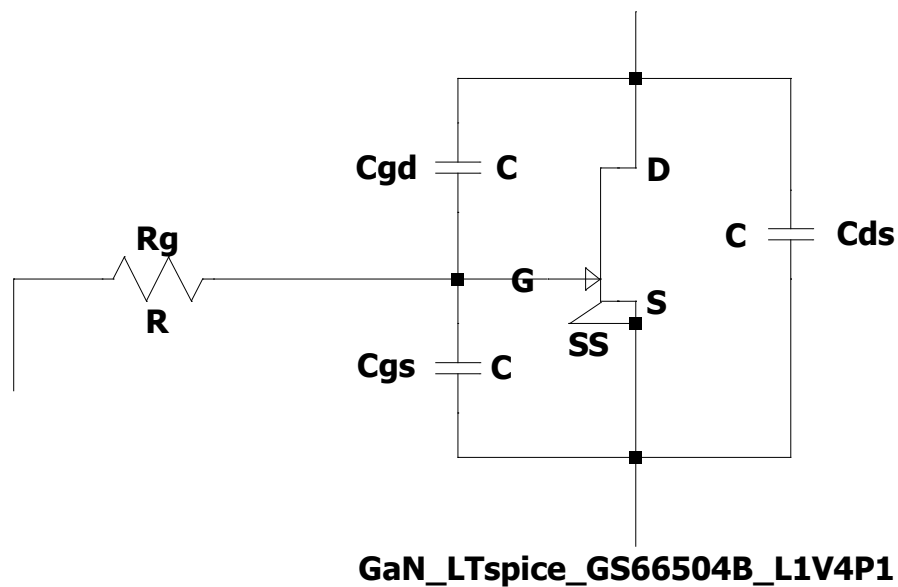
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## Task

Further look into why and how the gate current looks like this shape, and change the gate drive (e.g. an ideal voltage pulse source) and compare the gate curves.

### Parasitic Capacitors of MOSFET:



Here,

Gate to source capacitance,  $C_{GS}$

Gate to drain Capacitance,  $C_{GD}$  (Miller Capacitance)

Drain to source Capacitance,  $C_{DS}$

And,

Input Capacitance,  $C_{ISS} = C_{GS} + C_{GD}$

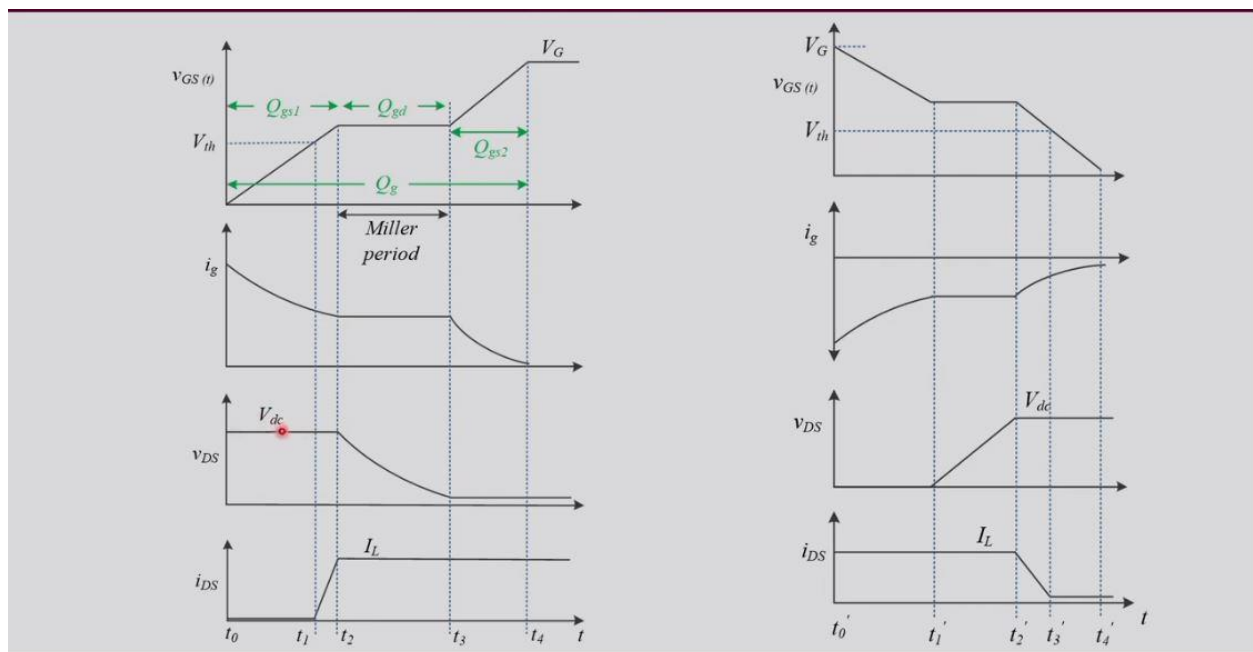
Output Capacitance,  $C_{OSS} = C_{DS} + C_{GD}$

Reverse Transfer Capacitance,  $C_{RSS} = C_{GD}$

“ $C_{GD}$  plays an important role to On and Off the MOSFET.”

### Gate Current:

From lecture video of **Prof. Shabari Nath(IIT,India)** we found,



Here,

Gate current is not smooth. First it will get a peak then decrease with time. After some time current remain constant for few moments. This is caused by “**Miller Effect**”.

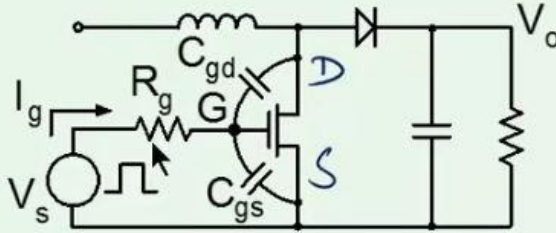
When the gate current and voltage waveshape is parallel to the time axis then it is called “**Miller Plateau**” region occurred by Miller Effect.

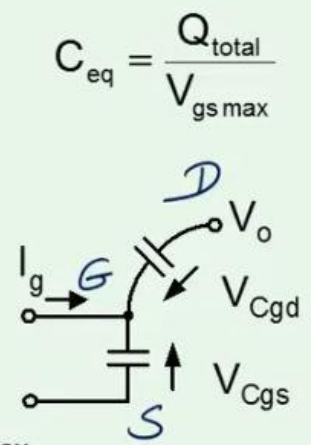
Here is the equation for this found from **Prof. S. Ben Yaakov's** lecture on Miller effect,

Prof. S. Ben-Yaakov , DC-DC Converters
[8- 7]

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## Gate capacitance





$$C_{eq} = \frac{Q_{total}}{V_{gs\ max}}$$

$$V_{Cgs}(0) = 0 \quad \Delta V_{Cgs}(\infty) = V_{GSmax}$$

$$V_{Cgd}(0) = -V_o \quad \Delta V_{Cdg}(\infty) = V_{GSmax}$$

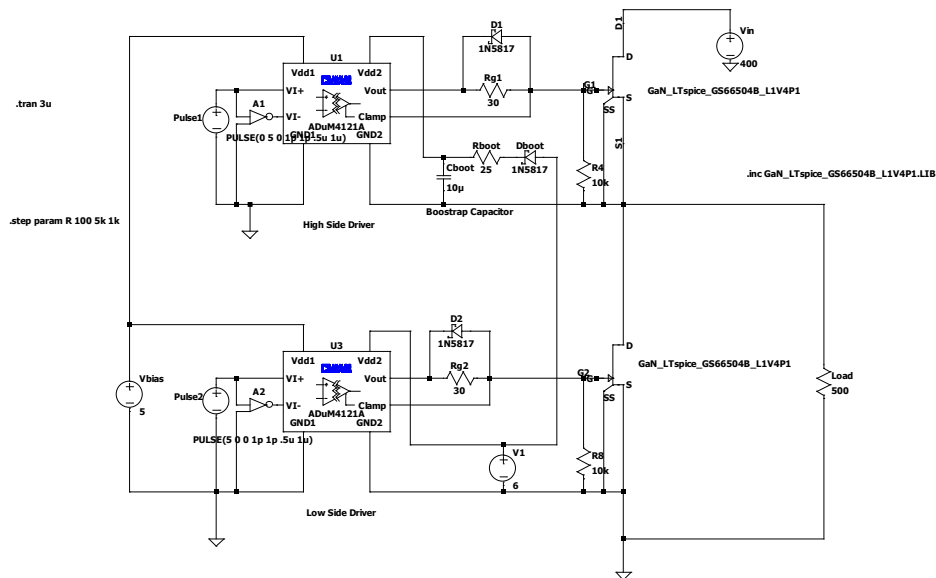
$$Q_{total} = V_{GS} C_{gs} + (V_{GS} + V_o) C_{gd}$$

$$C_{eq} = \frac{Q_{total}}{V_{GSmax}} = C_{gs} + C_{gd} \left( 1 + \frac{V_o}{V_{GSmax}} \right)$$

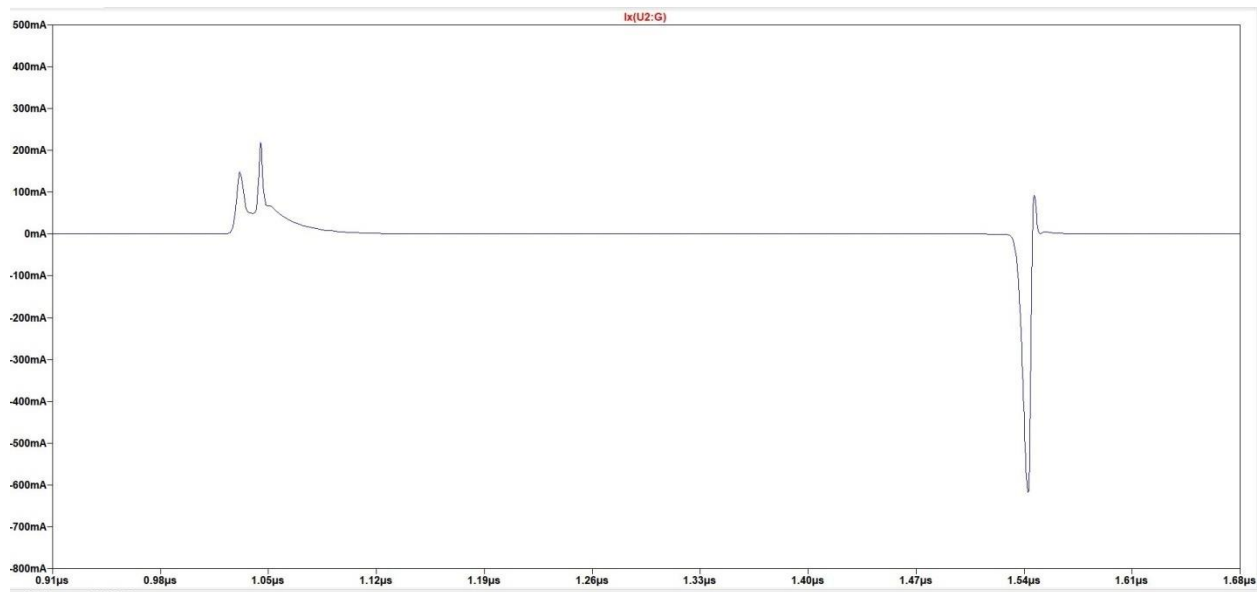
Miller Effect

This extra  $\frac{V_o}{V_{gs}}$   $C_{gd}$  capacitance causes Miller effect on the waveshape.

## Previous circuit(with Diode),



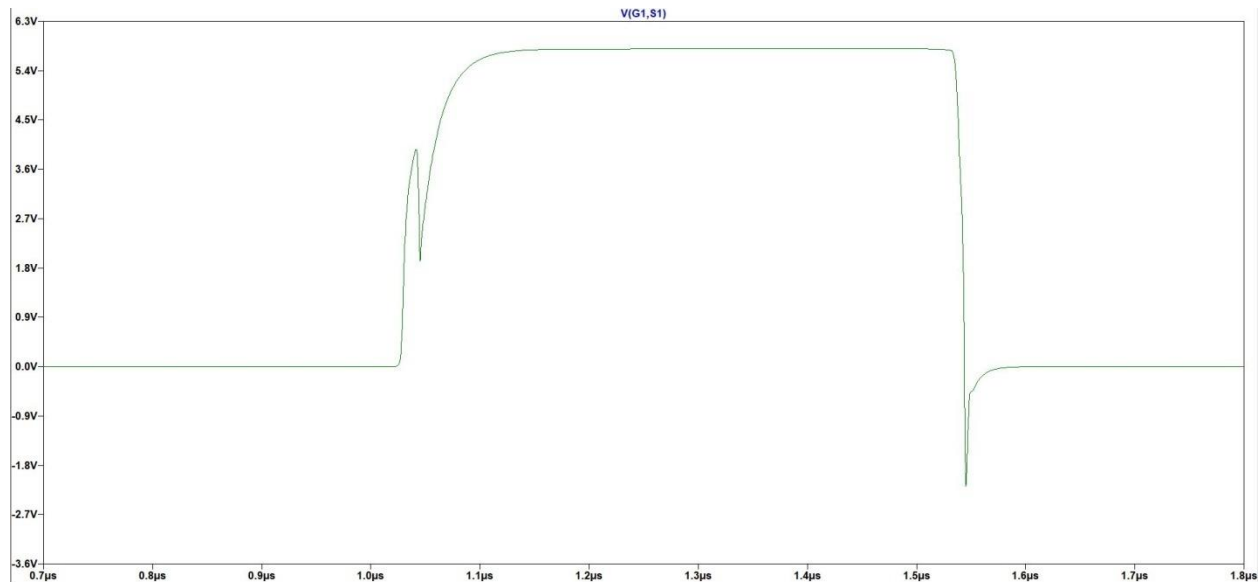
## On-Off Gate Current:



During On, gate pulse “Miller Plateau” and 2 peaks.

During off, gate pulse doesn't have a “Miller Plateau” region.

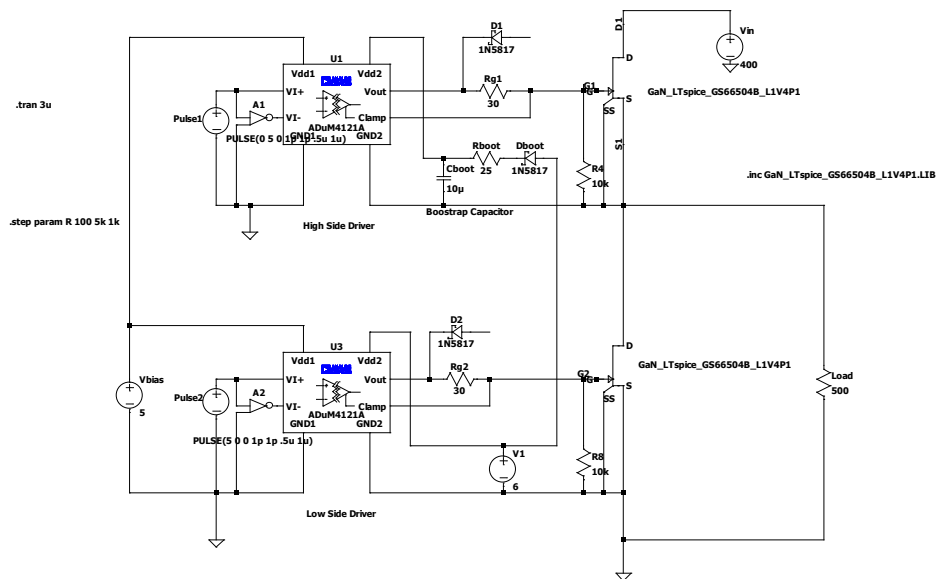
## Gate to source Voltage:



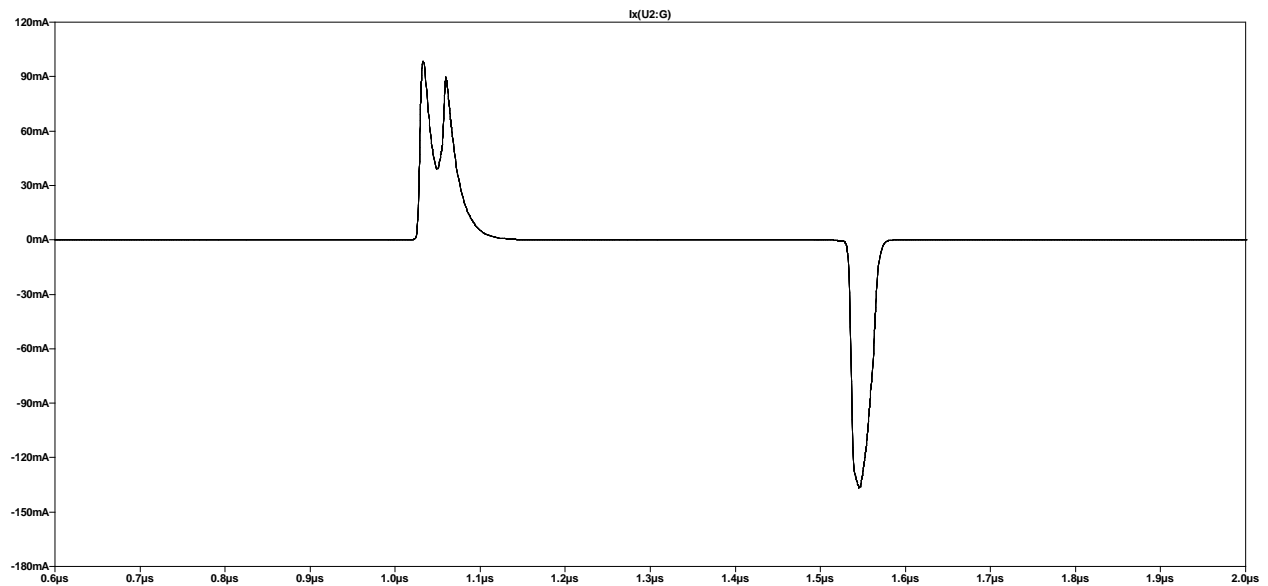
There is “Miller Plateau” during turning on, but not in turning off time rather having a negative voltage spike.

**If we Disconnect diode D1 and D2, the circuit:**

**(\*Datasheet suggest that diode part is optional)**



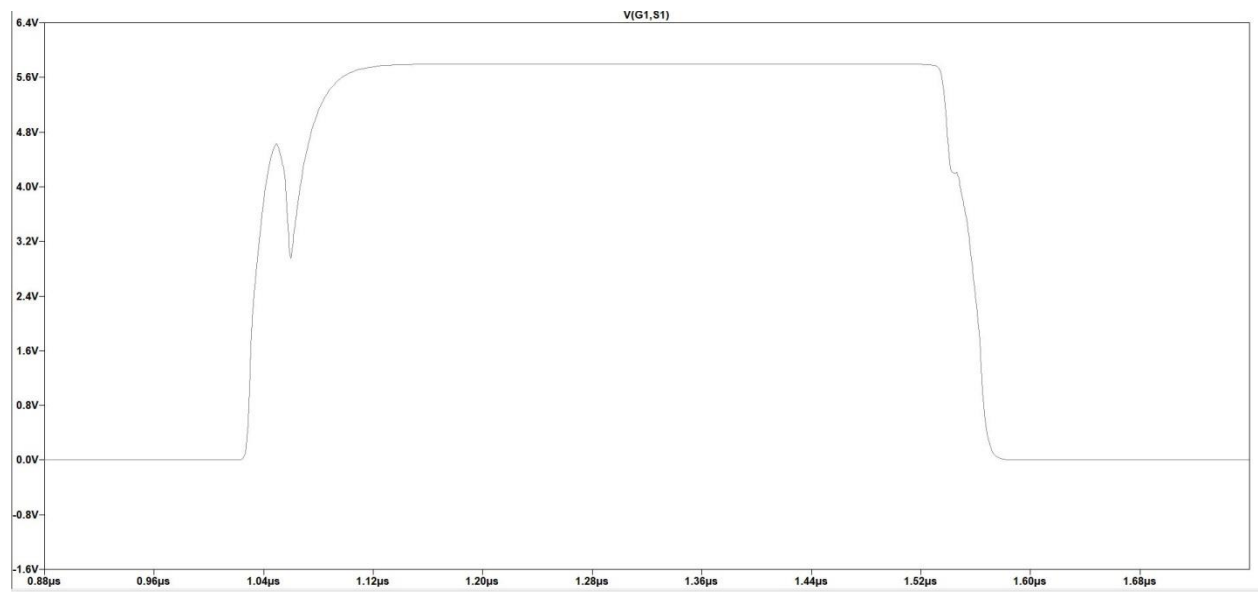
## Waveshape of Gate current:



During Turn On, waveshape showing “Miller plateau”.

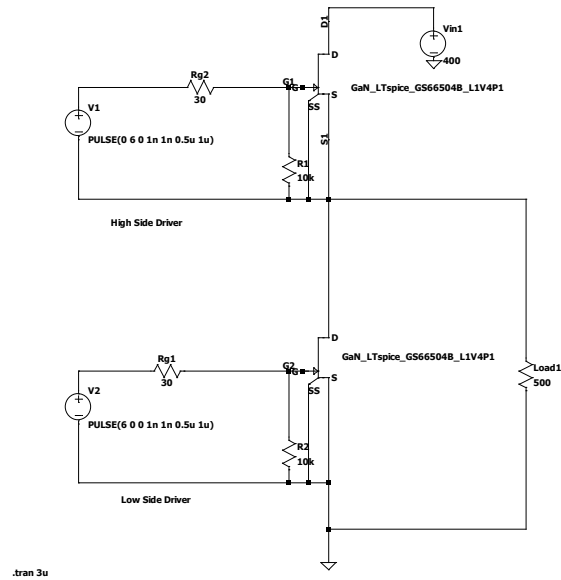
During Turn Off, again no “Miller plateau” region.

## Gate to Source voltage:

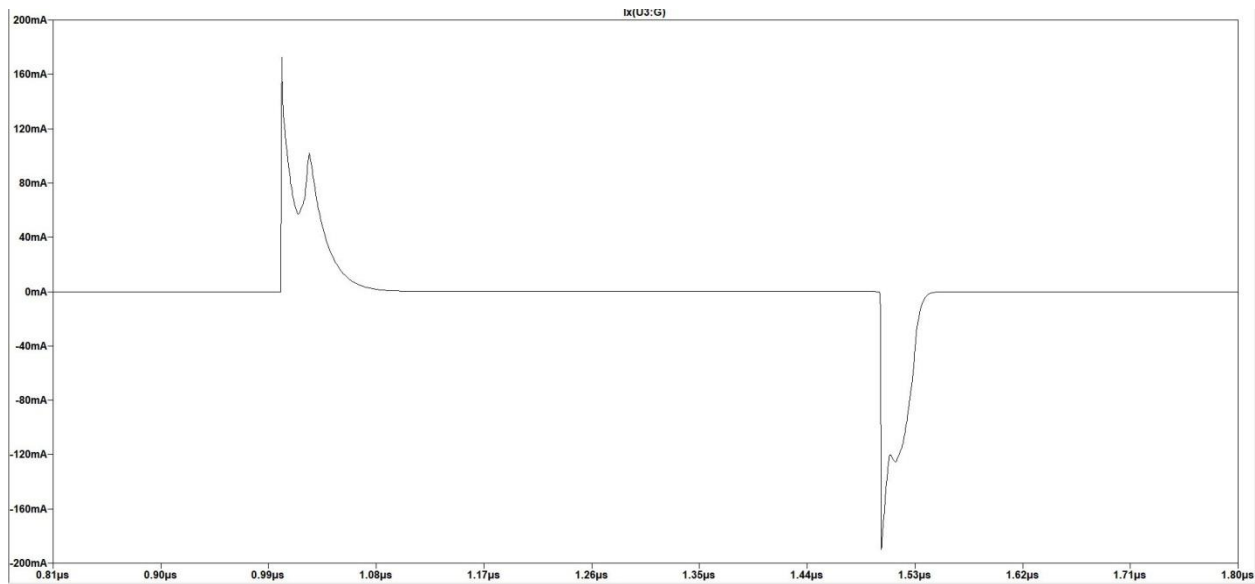


Reduction of “Miller plateau” in turning off time and no negative voltage spike.

## Circuit with Voltage Pulse(without driver):



## Gate Current:

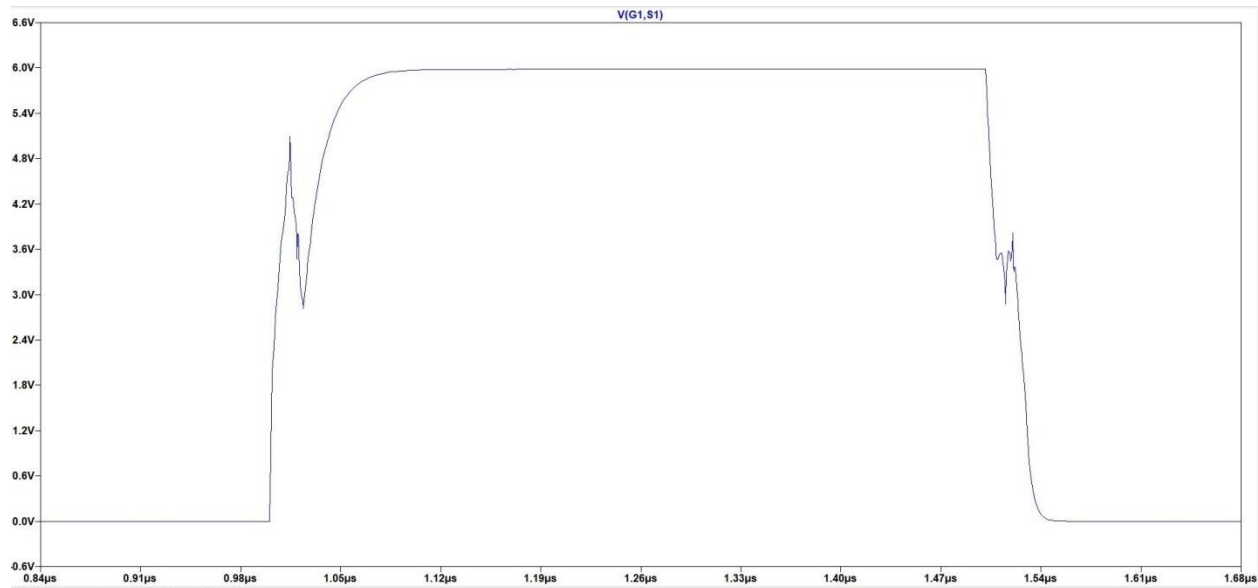


Here,

During on and off both time there is expected “Miller Plateau” region.



## Gate to source voltage:



Here is also found expected “Miller Plateau” region during on and off of the MOSFET.

## Comparison

**\*With driver circuit**, there is less Miller effect. But need to choose proper  $R_g$  on/off resistor & diode for better performance.

**\*Without driver**, more Miller effect.