BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY

H-Bridge with Phase Shifted PWM

Prepared by-

Sagar Kumar Das
Ratul Kundu
Shuvo Chandra Pall
MSc 22, BUET

Submitted to-

Dr. Cheng Zhang
Lecturer,
University of Manchester

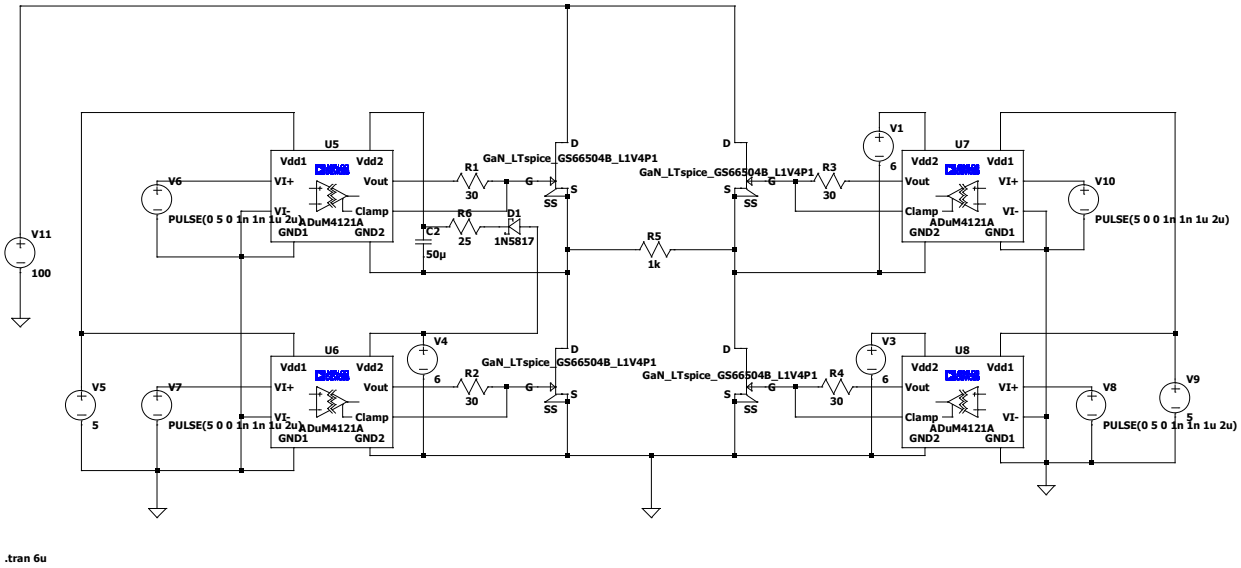
Supervised by-

Dr. Nadim Chowdhury
Assistant Professor, BUET

Task

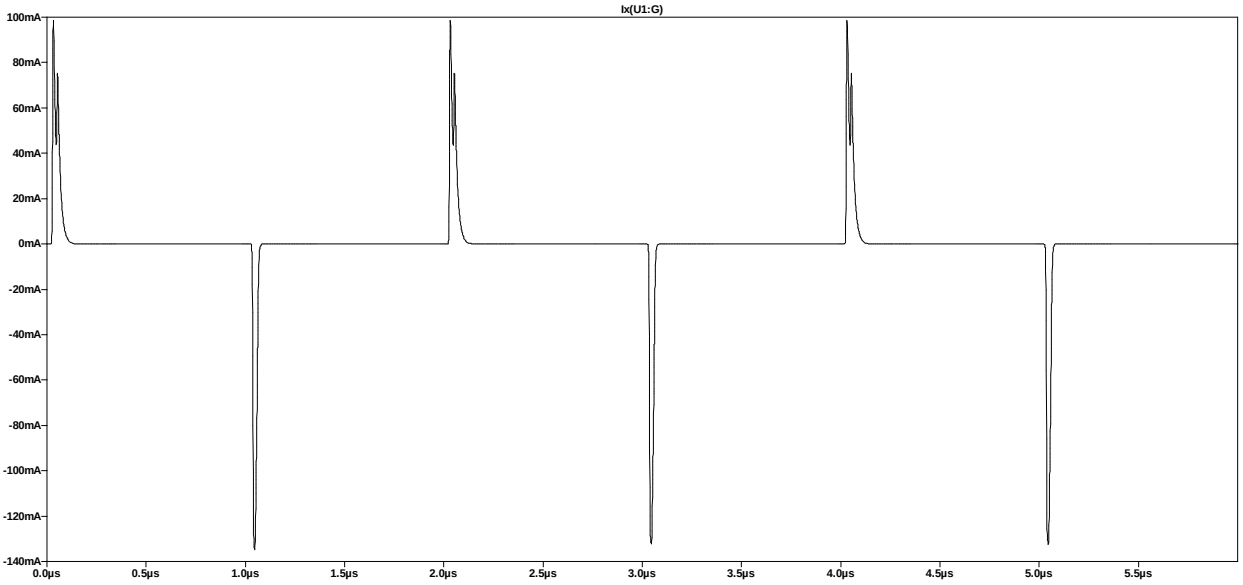
H-Bridge circuit with phase shifted PWM

H Bridge Circuit:



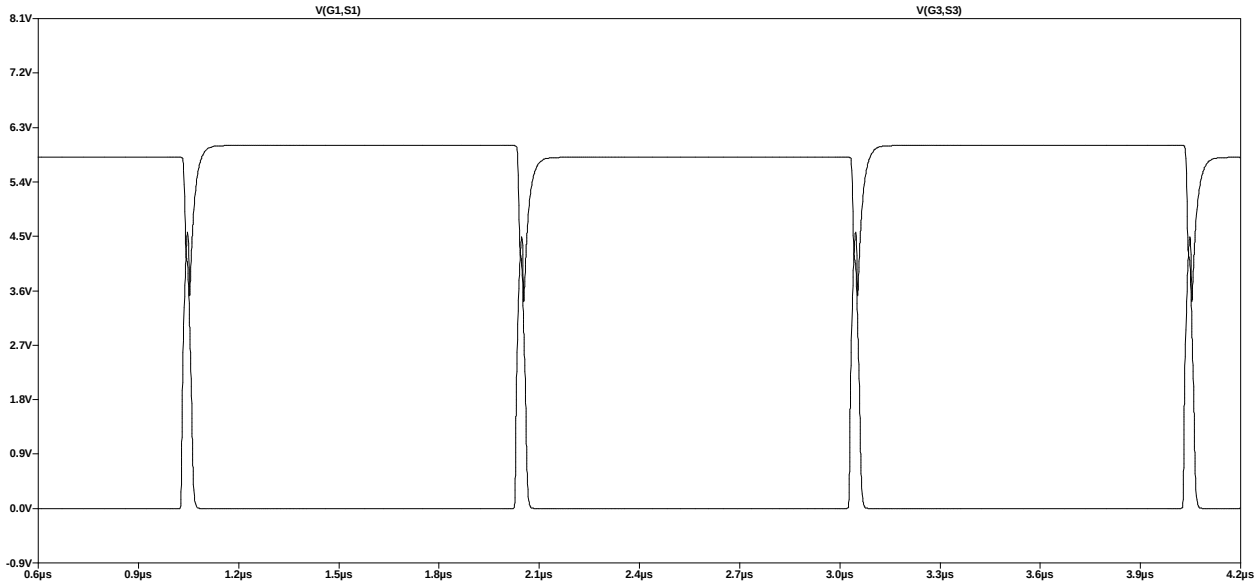
This circuit designed with **ADuM4121 gate driver** for 100V and 1K output resistance. Though Voltage and resistance can change.

Gate Current:



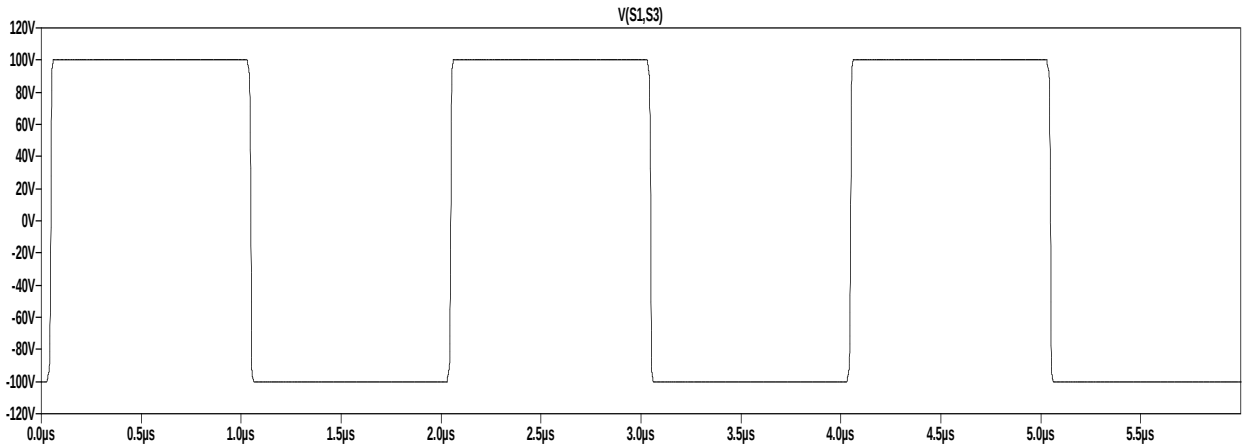
Gate current is showing same waveshape like previous assignment. So Circuit is working.

Gate to Source Voltage:



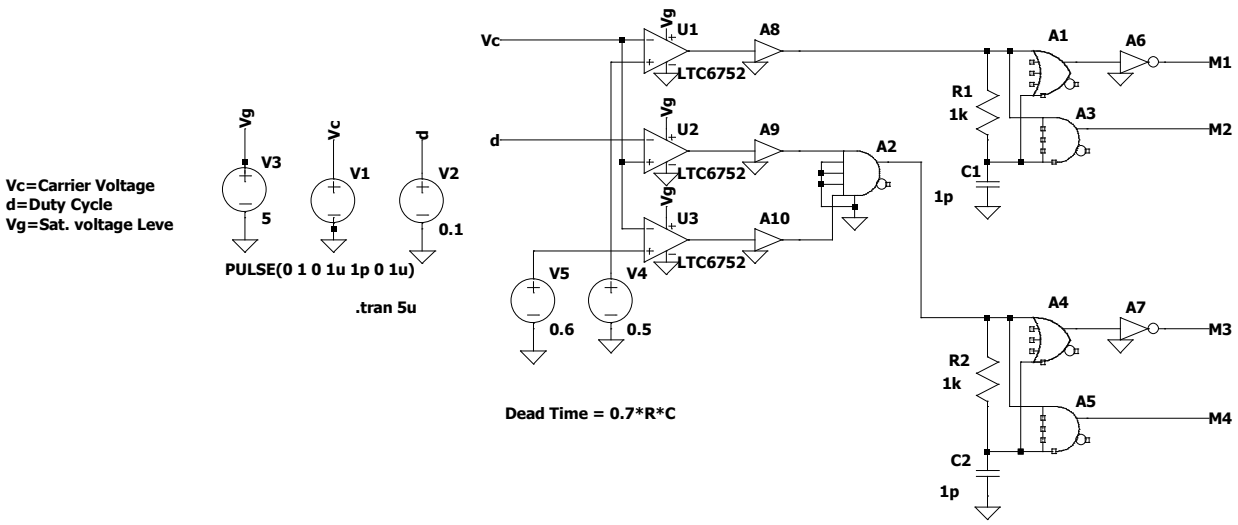
This waveshape is showing gate to source voltages from different side of the circuit. For this we take duty cycle of 0.5(half time on & half time off).

Output Voltage:



Output voltage is showing its ringing between +100 to -100V in 50% duty cycle.

Phase Shifted PWM generator circuit:



[Reference: https://youtu.be/0hgoZGzc3Vw]

Output(A8 and A2) with carrier and Duty cycle(D=0.1) :

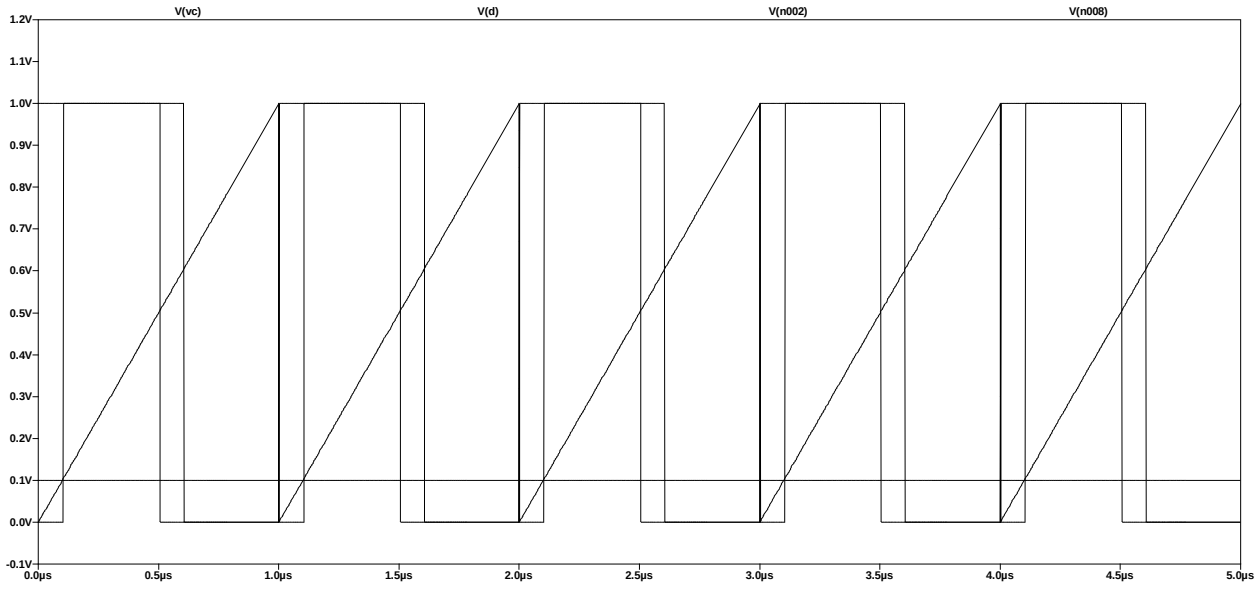
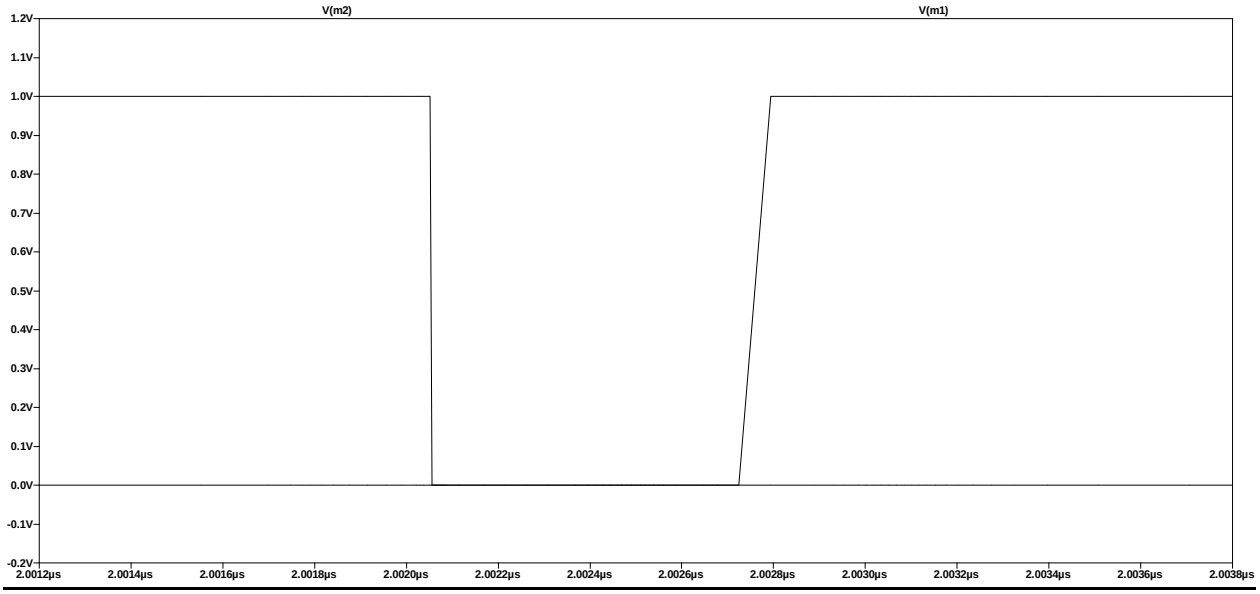


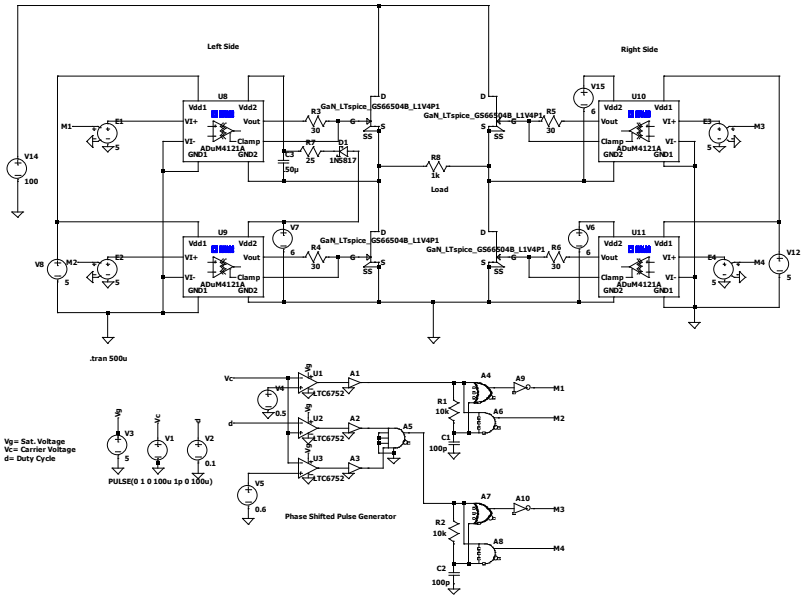
Figure showing that, Vc(ramp func.) and d=0.1V input of a comparator.

Dead Time:



From graph, we can see dead time is very close to calculated value of 0.0007µm. [Dead time means time difference between MOSFET's turning on-off to avoid overlap of switching.]

Signal Generator connected H-Bridge:



M1, M2, M3, M4 points are connected to the gate driver through VCVS with gain=5 that controls the gate to source voltage.

At D=0.1:

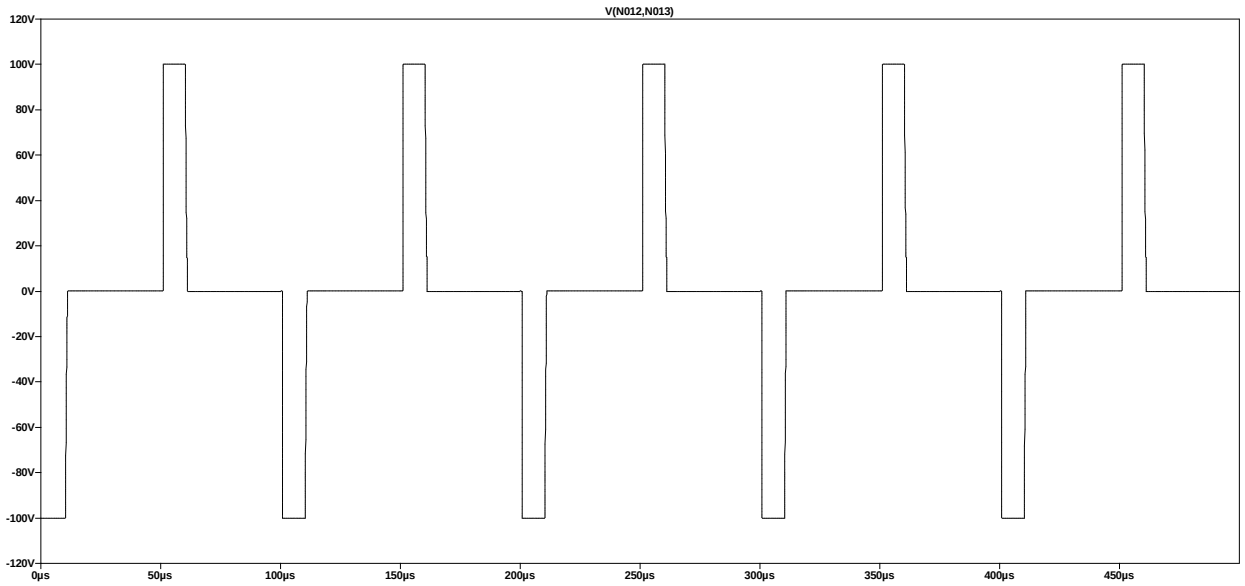


Figure showing voltage across the output resistor with duty cycle 0.1

At D=0.4:

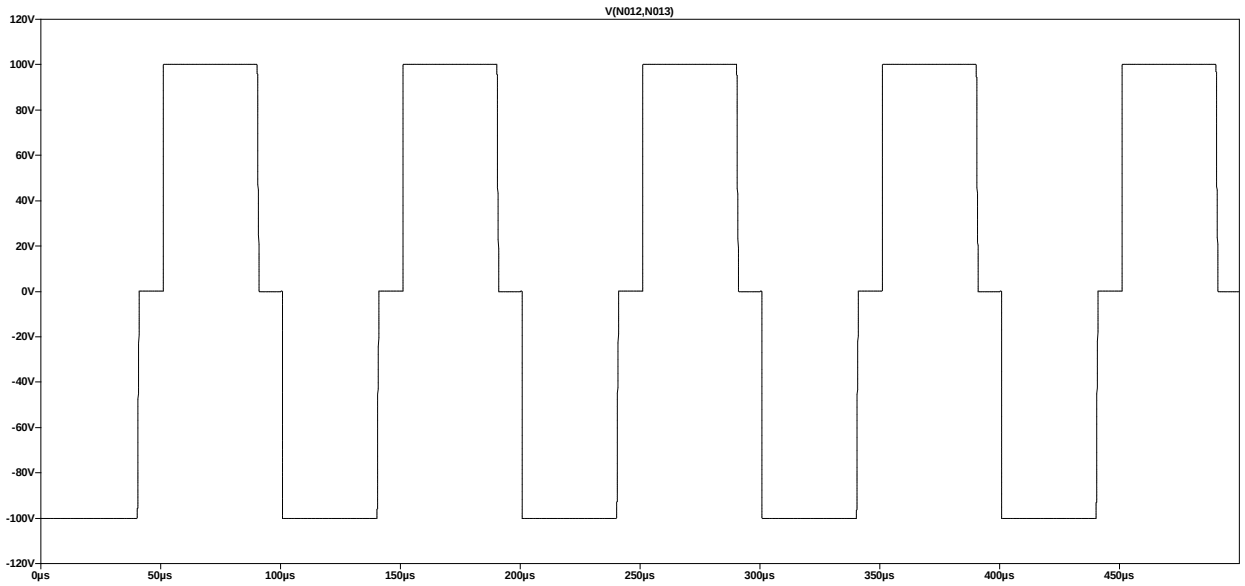


Figure showing voltage across the output resistor with duty cycle 0.4