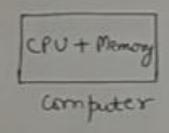
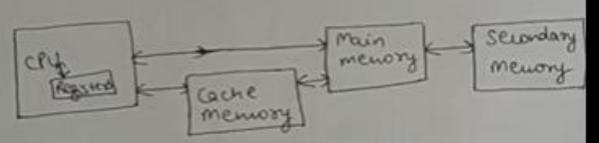
Memory Management

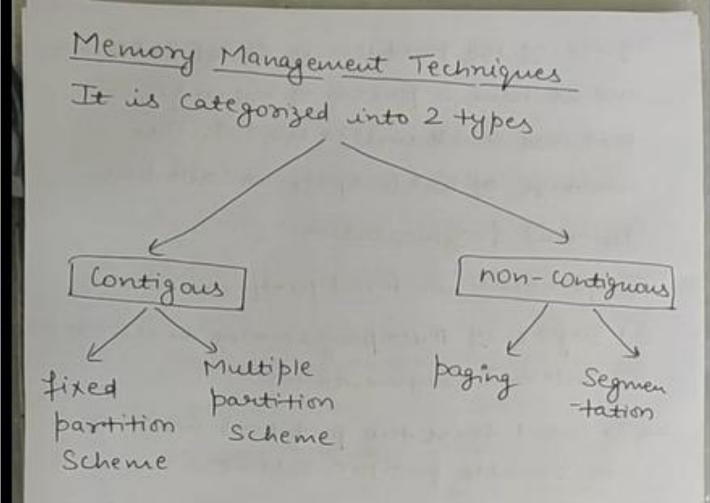


1) Size 2) Access Time 3 cost



Registers -> It is a temporary Storage area built in a CPU Access time of Register is below long, and registers have lowest capacity ie of few KB of words.

(ache Memory -) It is a high speed memory. The purpose of cache memory is to stoke those programs that are repentedly used or likely to be used in the near future.



-> Fixed partition Scheme

- · no of partitions are fixed in memory
- · Size of each partition may be same
- · foreg! we made 8 partitions in the memory so, the no. 8 is fixed.

In each partition only one process
can be placed. In this case, we is
can place only 8 processes out a time.
So, the degree of multiprogramming will be
restricted.

If one of the partition is of size soks, and we have a process of size 20kB, in that case 30kB will be wanted. This wastage of 30kB space is called as Internal fragmentation.

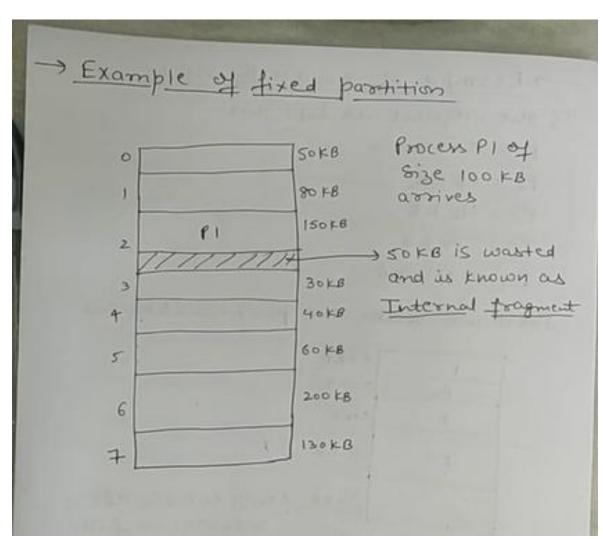
Twoproblems in fixed partition scheme

- 1 Degree of multiprogramming is restricted
- D Tinternal fragmentation.
- -> To avoid these two problems we mave to Variable partition scheme.
- -> Variable partition Scheme
- . In this, whenever the request of the process accordingly partition is made in memory:
 - · For eg! If a process of size 50kB

 arriver, a partition of 50kB is
 made in a memory.
- · In this case, there is no restriction on degree of Multiprogranning, as we can make

as many partition as possible till the memory is free.

Let us assume, after some various process one allocated and only 50 kB space is available in memory. And after sometime, a process of Size 80 kB armnes, but we have only 50 kB space left, my Therefore, we cannot accompdate the process of Size 80 kB thence, this 50 kB space is wasted and this wasted 50 kB space is known as External Fragmentation



> Example of variable partition If the request is like this -:

PI = SOKB

P2 = 20 KB

P3 = 40 KB

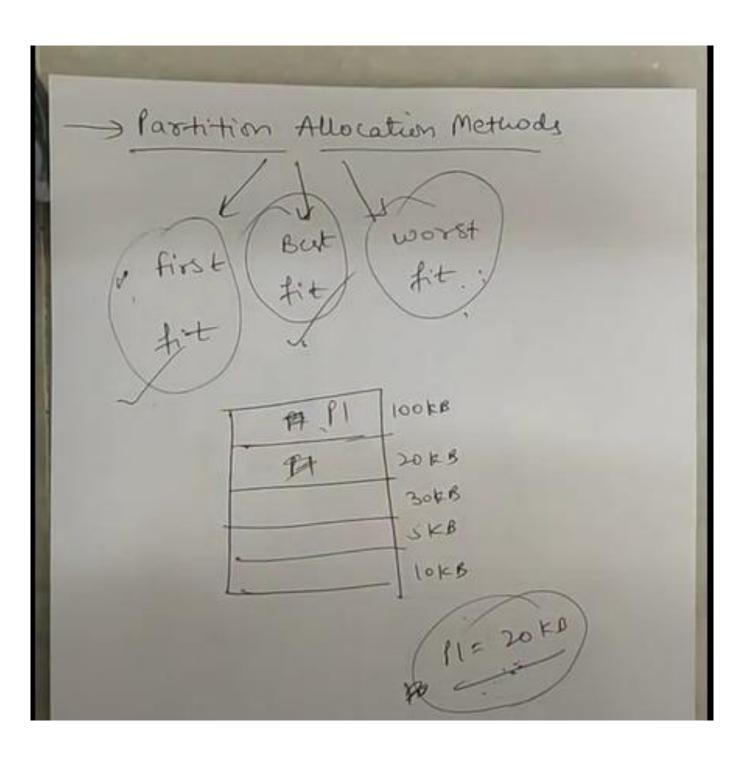
P4 = FOKB

P5 = 100 KB

then we make the partitions like this -!

PI	SOKB		
P2	20KB		
P 3	LIKB		
P4	FOKB		
11/1/1/1	60 KB	(only boke i	s left
Gexter	al	memoryi	4 full
4 extern	neut	how)	
-1			

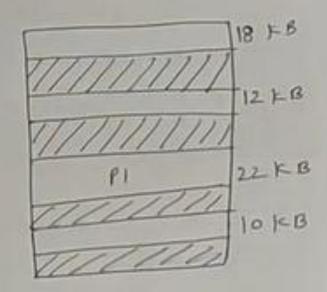
Therefore, we can not allocate Ps of Size 100 KB.



- -> Partition Allocation Methods
 - D First fit -> In this, allocate the process in a partition which is first sufficient partition from the top of the memory.
- Best fit > In this, allocate the process in a partition which is the Smallest Sufficient partition among the free available partition. To find the Smallest Sufficient partition it requires to search all the free partitions in the memory.
- (3) worst fit In this, allocate the process in a partition which is largest sufficient among the free available partition. To find the largest partition it requires to bearch all the free partitions in the memory.

> Example of first fit

P1 = 20 KB



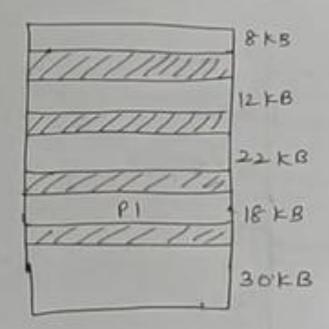
- tree partition

VIII -> busy partition

Suppose, Program Plarrines of Size

In case of first fit, PI (20KB) will be allocated in the botock frame of Size 22KB.

=> Example of Best fit

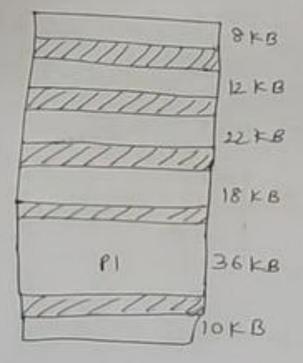


P1= 16 FB

Do tree partition

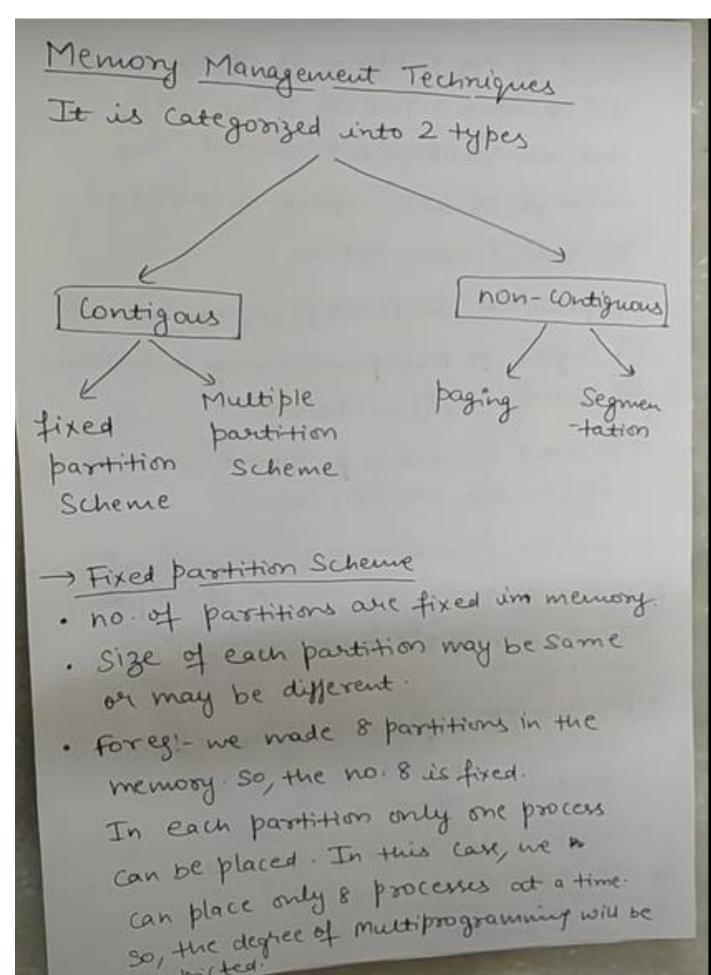
Suppose, PI of Size 16 KB arrives, In case of Best fit, PI will be placed at 18 KB partition.

Example of worst fit



P1 = 16 KB

Suppose, Pl of size 16 KB arrives. In case of worst fit Pl will be pa placed at 36 KB partition.

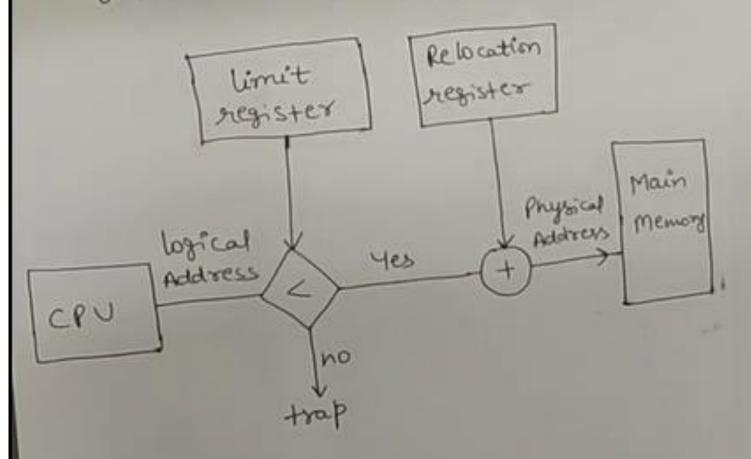


restricted

> Contigious Memory Allocation

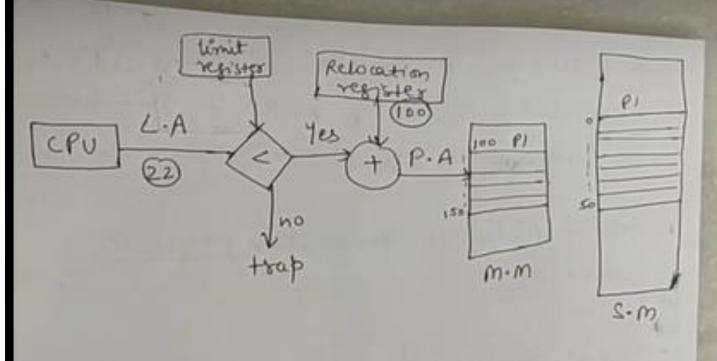
Address Translation

logical Address to Physical Address



- > Two (ssues we face in contiguous memory Allocation -: 1) Fragmentation Sixternal

 - 10 we have to translate logical Address to purpoical Address.



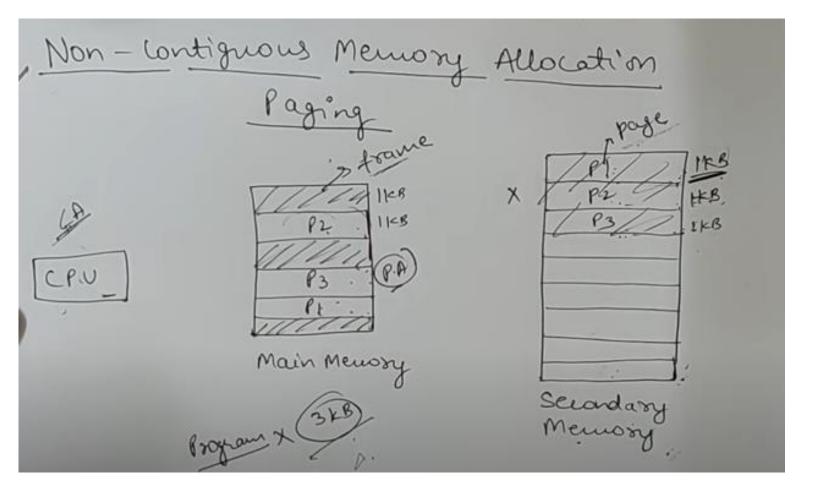
Explanation of this above diagram Suppose, we have a program PI which contains 50 instructions in Secondary Mennony. CPU wants to execute instruction no. 22. CPU generates the logical address (LA) 22. And the programs which are to be executed will reside in the mouin mennosy. 80, this PI program is stored in the Main Memory. Since main Memory generates the Phyrical address and CPU generates the logical address, we have to translate CA +OPA.

So, when CPU generates the Logical Address 22, we will check the limit register. Limit register contains the size of the program, in our example the size of the program is so. so, we will check 22 <50, if no it will go to trap, and if yes, then we will add the L'A (22) to relocation register to get the physical address. The relocation register contains the base address of the program in main memory re in own example base add sers is 100. So, we add 100+22 > (22) which is the physical As , we use contigious memory allocation address the instructions are stored in a continuous manney. In this way we

Can translate Logical address (LA) to physical Address (P.A)

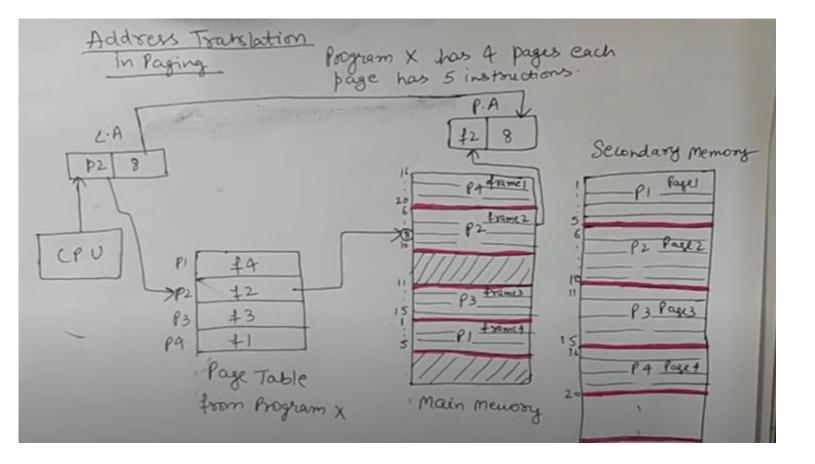
> Note:

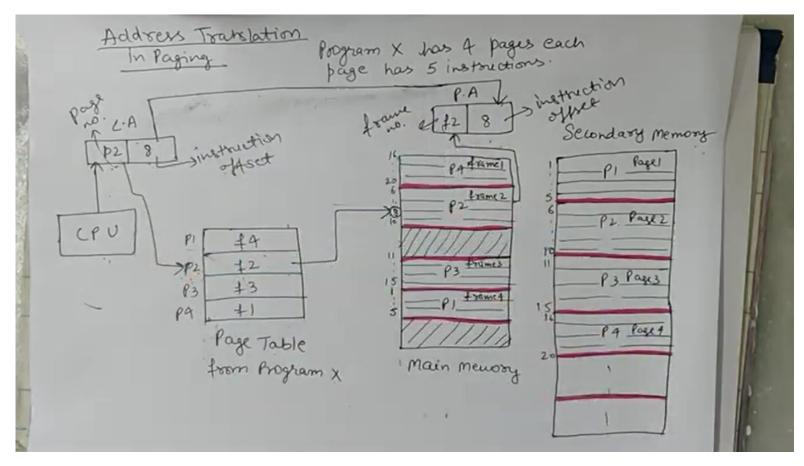
- D Set of Logical Addresses is known as Logical Address space (L.A.S)
- DSet of physical Addresses is known as Physical Address Space (P.A.S)
 - CPU generates Logical Address (LA)
 - (1) Main Memory Generates Physical Address



Defination of paging

Paging is a Memory Management Scheme by which a computer stores and retrienes data from Secondary Storage for use in main memory. Operating System reads data from secondary Storage in blocks called pages, all of which have identical Size. And the Blocks (identical size) in Main Memory are called frames.





Defination of Page Table - It is the data structure

Stored in Main Memory that stores the mapping
between Virtual addresses and Physical address.

Now CPU generates Logical address. The logical address

Consists of 2 parts - O Page no. O Instruction offset

then CPU refers the Page Table and finds out

which page no. is present at which frome no.

and hence translate the Physical address. Physical

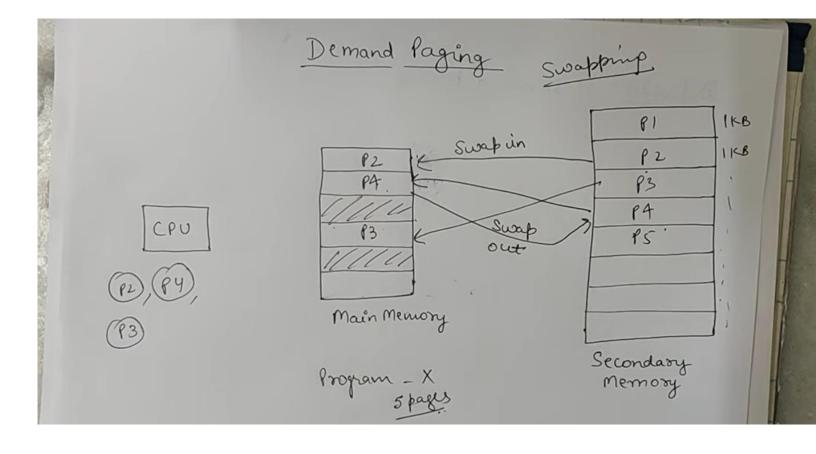
address consists of two parts - O frame no. O Tustruction

Offset. Foreg:- CPU wants to execute Page no. 1 and

Inside Page no. 1 instruction no. 5. I.e [PI 5]

L.A

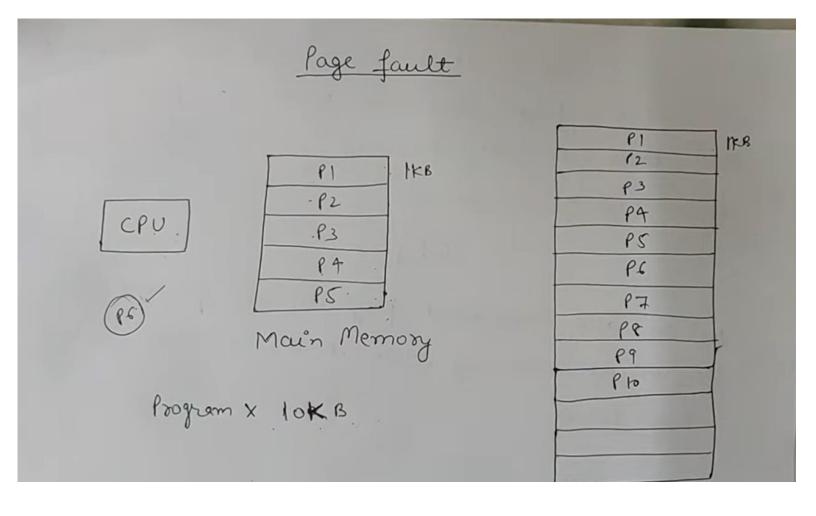
Plus page no. and 5 is the instruction effect now CPV refers Main memory and finds out 1 say Plus is present at frame no. 4 (fy). [44] 5 The instruction P.A Offset is same 5. CPV goes to frame no. 4 and bicks 5th instruction and executes it and gives the output. This is how we translate L.A to P.A in pagning.



Demand Paging

The Program resides in the secondary Memory, and pages are loaded in main Memory only on demand not in advance.

Defination of Demand Pagning - It is a type of swapping in which pages are copied from secondary memory to main memory when they are needed.

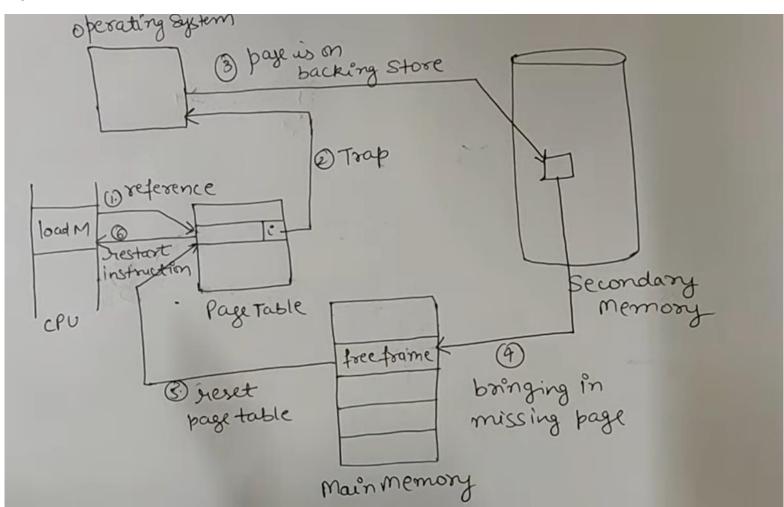


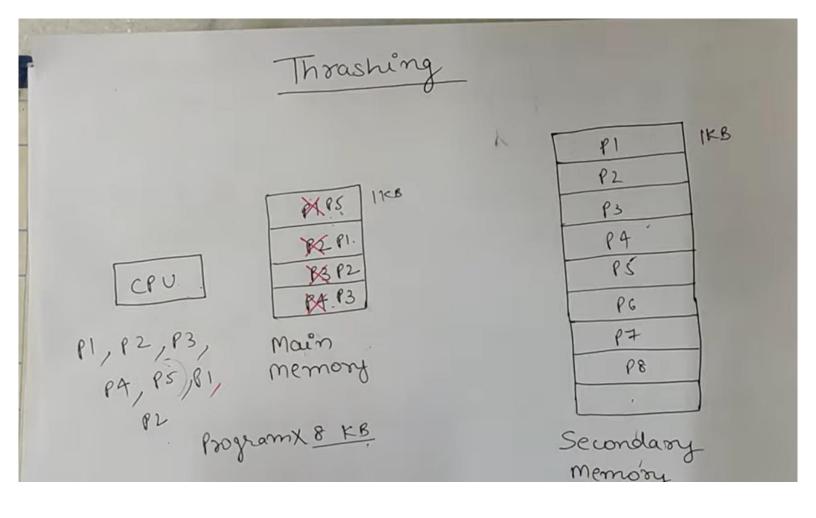
Defination of Page fault -> when a processor wants to access a page, and that particular page is not ours currently present in the main memory, then page fault occurs.

TOR

when the demanded page is not present in the main memory then it is called as Page fault.

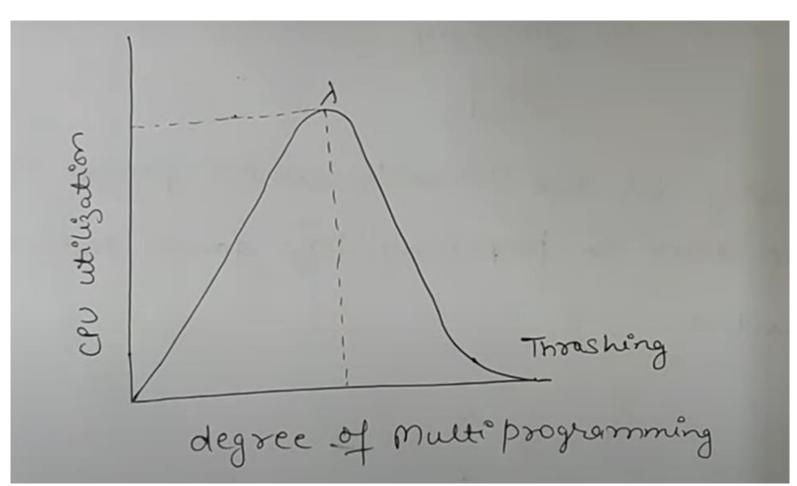
Page Fault Solution





- 1) In the initial Stage when we increase the degree of Multiprogramming, CPU utilization is very high upto 1.
- D'further, if we increase the degree of Multips--ogramming, CPU utilization is drastically falling down.
 - (3) This situation in the system is Thrashing.
 - (4) Thrashing degrades the performance of system

- So There can be a Situation when main memory is full of pages that are accessed frequently. A page fault will occur if the required page is not present.
- (6) In order to make space for swapping in the required page, on of the frequently accessed page is swapped out.
 - De Soon, the Swapped out page is required for execution and this again results in



Degree of Multiprogramming: Number of pages are being added.

Defination of Thrashing -> high paging activity is known as Thrashing.

OR

Thrashing is the Situation where process Spends more time in processing page faults rather than execution.

Viotual Memory

- · Virtual Memory gives an illusion to the programmer that programs of larger soize than actual physical memory can be executed.
- · Virtual memory doesn't really exists, but the paint of secondary memory are made as virtual memory.
- Defination of Viotual Memory
 Virtual Memory is a feature in 0.8, where large
 programs can store themselves in form of pages

Defination of Viotual Memory
Virtual Memory is a feature in 0.5, where lauge
programs can store themselves in form of pages
while their execution and only the required

pages on postions of processes are loaded into
the main memory.

Virtual Memory can be implemented by using—:

Demand
Paging

Demand
Segmentation

Race Condition Defination

when more thane one processes are executing the same code or resource or any shared variable in that condition there is a possibility that the output or that the lature of that Shared Variable is wrong, so for that all the process doing race to say that my output is correct, this condition is known as face condition.

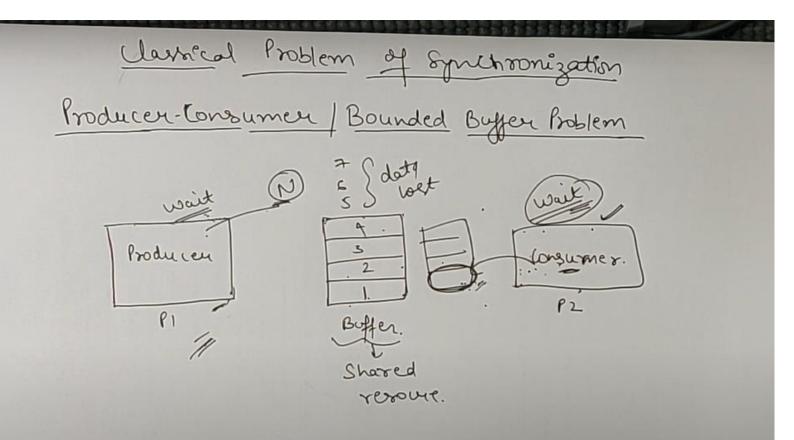
do

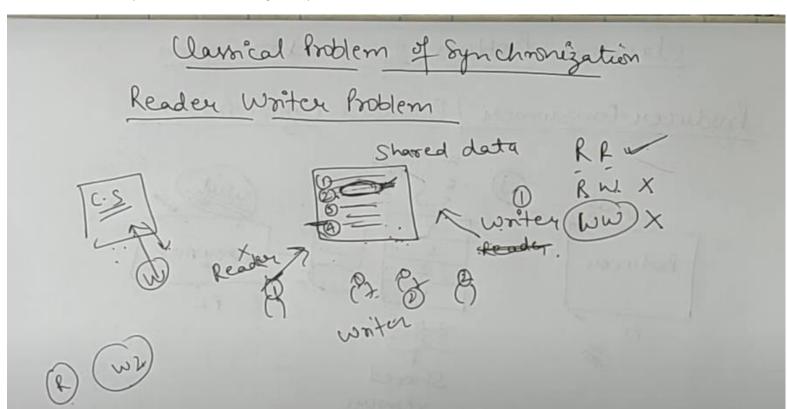
{
 controls the entry
 entry section into (.s and gets a lock
 on resources.

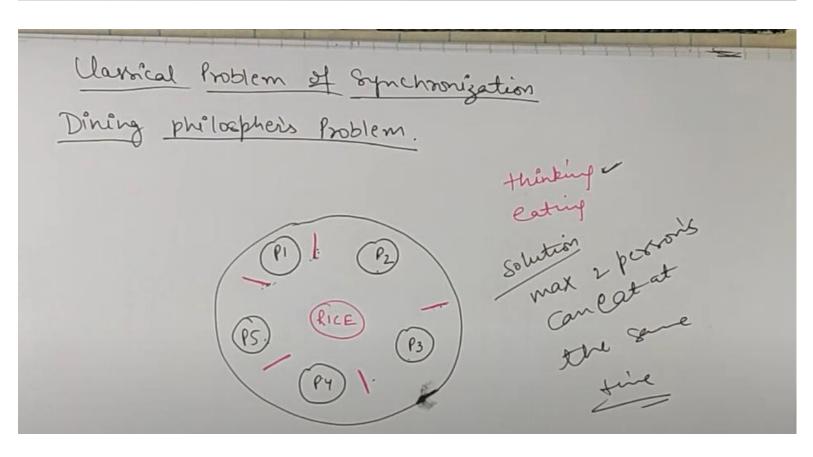
 contrical section
 exet section
 exet section +

 Remainder section

S while (Toure);



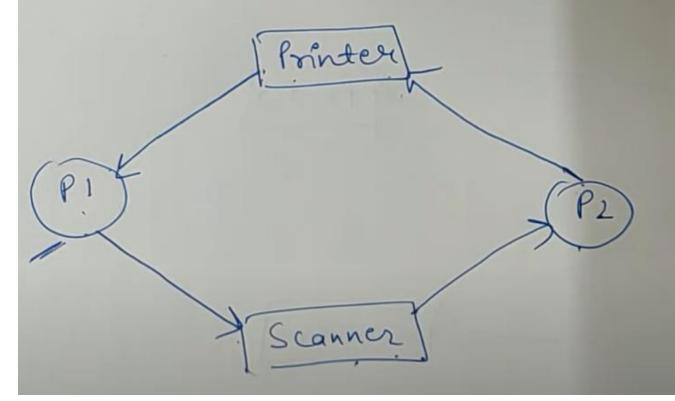


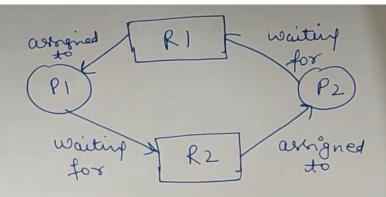


Semaphores in Operating system

Semaphore is an integer variable that solves the critical section problem. After initialization, it can only be accessed by two atomic operations—

Deadlock in Operating system





Defination of Deadlock -> Deadlock is a Situation where a set of processes are blocked because each process is hading a resource and waiting for another resource acquired by some other process.

- -> Four Necessary conditions for deadlock to occur
- 1) Mutal Exclusion -> one or more than one resource are non sharable (only one process can use it).
- D) Hold and wait -> A process is holding at least one resource and waiting for another resource.
- (3) No Preemption -> A resource cannot be taken from a process unless the process releases that resource.
- (A) circular wait -> A set of processes are waiting for

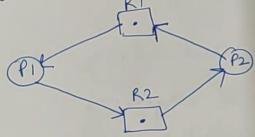
Resource Allocation Graph (RAG)

- · Wring RAG, deadlock can be earily detected.
- · It is a Graph that represents the State of a System pictorially.
 - · It has vertices and edges.
 - · It has two types of edges -:
 - 10 Request edge Pi-Rj
 - (2) Arroignment edge Rj->Pi

Rules to detect deadlock using RAG

Rule-1 -> In RAG, where all the resources are Single instance -:

> @ If a cycle is being formed, then the System is in a deadlock State.



(b) If no cycle is being formed then the system is not in a deadlock state.

Rule-2 -> In RAG, where all the resources are multiple instances -:

or not.

(a) If a cycle is being formed, then system may de may not be in a deadlock state.

In this Case we use Banker's algorithm to confirm whether a system is in deadlock state

6) If no cycle, then system is not in a deadlor State.

RAM, with multiple instances but no deadlock

R1

P2

P2

P3

Bankeris Algo rithm (Deadlock Avoidance Algo)						
		Total A .= 10. B=\$ C=7				
Process	Allocation	Max need	Available	Remainingneed		
	A B C	A B C	ABC	ABC		
PI	0 10	7 5 3	332	743 Ph		
P 2	200	3 2 2	5 3 2	12.2.12		
R3	3 0 2	902	を対る	600 13		
PY	21.	422	7 4 5.	2 1 1		
	0. 0. 2.	5 3 3	755	53 } #5.		
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$						
Cale Ses						

Remaining need = Max need – allocation; for all

A1 (Available 1) = Total (A, B, C) - Allocation (sum (A, dim=1), sum (B, dim=1), sum (C, dim=1)); #dim 1 means column

Available for P1 = A1

Now execute the processing by looking at the remaining need and focusing on the available column;