CH: 12 Processor Structure and Fun

* Processor Organization.
the structure and arrangement of components with a central processing unit.
• The organization of a processor involves several h components.
-> Control Unit
-> ALU
-> Registers
-> Cache memory
-> Bus. (Comunication pathway)

• Processor things that it must to

1. Fetch Instruction: reads inst from memory (Rg. cache, mai

2. Interpret Instruction: What action is required.

3. Fetch data: read from memory or I/O.
4. Process data: execution of Instruction. Performing operation.
5. Write data:
write. data To I/O or memory

* Register Organization

the way registers are structured and used within a computer system. Register are small high speed memory units located within the processor.

- User-visible register:

the register that can be directly accessed and utilized by programmers in assembly language programs. these Register used for storing and manipulating data during program execution.

- General Purpose Registers:

the register used for various purpose during program execution. arithmetic and logical operation data manipulation and temporary storage.

- AX : Arithmetic operation
- BX : Used for pointer to data in memory.
- CX : loop and Counting.
- DX : I/O operation and holding data.

- Data Registers:

Designed for storing data numerical and characters.

AX, BX, CX, DX, these register also serve as data registers capable.

- Address Registers.
  Used to hold memory allocation addresses. & for Indexing. memory Instruction
  IP: address of the next
  SP: Point to the top of Stack.
  SI: Used for String. Source.
  DI: Used for String destination.

~~Condition Code Registers.~~
~~also know as~~

- segment Pointers:
  CS, DS, SS, ES
- Index Registers:
  SI, DI, BX
- Stack Pointer
  SP

- Condition Code Registers.
  also know as flag register
  Store the status of the process
  for executing certain instruction.
  - Zero flag (ZF): when result of operation is zero.
  - Sign Flag (SF): MSB indicate the negative value SF set 1 to MSB.

- Overflow flag (OF): operation exceeds the range. result can't be represented in available number of bits.

* Control and Status Registers. the registers within the processor that are used to control its operation. not visible to users. accessed by control Unit.

1. Program Counter (PC): address of next Instruction. to be Fetched
2. Instruction Register: Current Instruction fetched from memory.
3. Memory address Register (MAR): address of a memory location accessed by processor. Read/write.
4. Memory Buffer Register (MBR): Store the actual Data. written or read.

* These used for movement of data processor to memory.

- PSW (Program Status Word): Set of register within the processor that holds important status information and controls various aspects.

used by prosseser to make decision branching, handle intessupts, executio
- Sign Flag:
- Zero Flag:
- Cassy Flag: It is set one and addition opsation.
- over flow:
- Intessupt flag: Intessupt is enable or disable.
- Supesvisor flag: Program executing in supesvisor or user mode.

* Instruction Cycle:
Instructin Cycle is the sequence of steps that a processor goes through to fetch, interpret and execute instruction.
Fetch: Read the next Instruction from memory into the processor

Execute: perfom the operation In Instruction.

Intessupts: If Intessupts are enable and an intessupt has occussed save the current process state and sesve the intessupt.

* The Indirect Cycle:

The indirect cycle is an additional stage in the execution of Instructions that involves fetching operands from memory especially when indirect addressing is used. This stage is added to normal instruction cycle.

Ex: Find a house. direct and Indirect. Pg: Pointers.

* Data Flow:

In data flow during the fetch cycle of an instruction several components of the processor work together to retrieve the next instruction from memory.

Processor's fetch cycle:

PC, MAR, MBR, IR.

- After the fetch cycle the control unit exmines the contents of the IR to check if it contains an operand specifier that indirect addressing. the Indirect cycle is performed.

* Instruction Pipelining :-
It is a technique used in processor to improve their performance by allowing multiple instructions to be processed simultaneously.

- It divide the execution of Instructions into smaller sequential stages. each & stage has its own task.

- Pipelining Strategy.