Sukkur IBA University Kandhkot Campus

Department of Computer Science BS(CS) III (Fall 2020)

ESE-201: Digital Logic Design Syllabus

General Information

Course Number	ESE-201
Credit Hours	3+1 (Theory Credit Hour = 3, Lab Credit Hours = 1)
Prerequisite	Basic Electronics (ESE-150)
Course Coordinator	Not Specified
Consulting Hours	Wednesday: 11:00 AM to 1:00 PM
Office Location	Faculty Room#04

Course Objectives

This course focuses on understating and designing basic building blocks of a digital system, specifically digital computer. First part of this course covers combinational logic circuits, which includes concepts of digital and analog systems, number systems, logic gates, logic simplification using Boolean algebra and K-Map, SOP, POS, truth table, waveforms, universal gates, adders, comparators, encoders, decoders, seven segment display, multiplexer, demultiplexer etc. Second part of this course covers sequential logic circuits, which covers latches, gated lathes, flip-flops, various shift registers and counters.

Catalog Description

ESE-201

Course Content

Weeks	Topics	Suggested Reading *(author/page)*
1	**Introduction** Introductions about course contents, exams etc Digital and Analog Quantities Binary Digits, Logic Levels, and Digital Waveforms Basic Logic Functions Logic Functions Fixed-Function Logic Devices Test and measurement instruments	(Floyd/Chapter 1)
2	**Number Systems** Decimal-to-Binary Conversion Binary Arithmetic Complements of Binary Numbers Signed Numbers Arithmetic Operations with Signed Numbers Hexadecimal Numbers Octal Numbers Binary Coded Decimal (BCD) Digital Codes Even and Odd parity	(Floyd/Chapter 2)
3	**Logic Gates** The Inverter The AND Gate The OR Gate The NAND Gate The NOR Gate The Exclusive-OR and Exclusive-NOR Gates	(Floyd/Chapter 3)

4,5	**Boolean Algebra and Logic Simplification** Boolean Operations and Expressions Laws and Rules of Boolean Algebra De-Morgan's Theorems Boolean Analysis of Logic Circuits Logic Simplification Using Boolean Algebra Standard Forms of Boolean Expressions Boolean Expressions and Truth Tables The Karnaugh Map	(Floyd/Chapter 4)
6	**Midterm-I Examination,practice, consultation, review and preparation**	
7	**Combinational Logic Analysis** Basic Combinational Logic Circuits Implementing Combinational Logic The Universal Property of NAND andNOR Gates Combinational Logic Using NAND andNOR Gates Pulse Waveform Operation	(Floyd/Chapter 5)
8,9	**Functions of Combinational Logic** Half and Full Adders Parallel Binary Adders Comparators Decoders Encoders Code Converters Multiplexers (Data Selectors) Demultiplexers Parity Generators/Checkers	(Floyd/Chapter 6)

10,11	**Latches, Flip-Flops, and Timers** S-R Latch D-Latch Gated S-R Latch Gated D Latch D-Flip-Flop J-K Flip-Flop Flip-Flop Applications 555 Timer IC	(Floyd/Chapter 7)
12	**Midterm-II Examination, practice, consultation, review and preparation**	
13,14	**Shift Registers** Shift Register Operations Types of Shift Register Data I/Os Bidirectional Shift Registers Shift Register Counters Shift Register Applications	(Floyd/Chapter 8)
15,16	**Counters** Finite State Machines Asynchronous Counters Synchronous Counters Up/Down Synchronous Counters Design of Synchronous Counters Cascaded Counters Counter Decoding Counter Applications	(Floyd/Chapter 9)
17,18		
	practice, consultation, review and preparation, **Final Examination**	

Text Book

1. Floyd, T. L. Digital Fundamentals, 11/e. Pearson Education.

Reference Material

1. M. Morris R. Mano, Charles R. Kime, Tom Martin - Logic and computer design fundamentals (2015, Prentice Hall)
2. Tocci, R. J. **(1996)**. Digital Systems: principles and applications. Pearson Education.

Course Learning Outcomes

	Course Learning Outcomes (CLO)
1	To applythe techniques/methods for simplification of complex logic circuits/expressions/truth tables.
2	To implement the combinational and sequential circuits according to their applications.
3	To use simulation software and hardware kit to analyze combinational and sequential logic circuits.

CLO-SO Map

	SO IDs											
CLO ID	**GA1**	**GA2**	**GA3**	**GA4**	**GA5**	**GA6**	**GA7**	**GA8**	**GA9**	**GA10**	**GA11**	**GA12**
CLO 1	1	0	0	0	0	0	0	0	0	0	0	0
CLO 2	0	0	1	0	0	0	0	0	0	0	0	0
CLO 3	0	0	0	0	1	0	0	0	0	0	0	0

Approvals

Instructor	Adil Khan
Approved By	Not Specified
Last Update	15-Sep-2020