Interconnection Structure

- Computer is network of three modules:
  - Processor
  - Memory
  - I/O
- Path for connecting these three modules is called interconnection structure

Interconnection Structure

- Memory:
  - N words from 0 to N-1
  - Read/Write
  - Location is specified through address
- I/O:
  - Read/Write
  - I/O module controls more than one device, by assigning each device a unique port address
  - Can Send Interrupt signals to the processor

Interconnection Structure

- Processor:
  - Reads data, processes and writes data

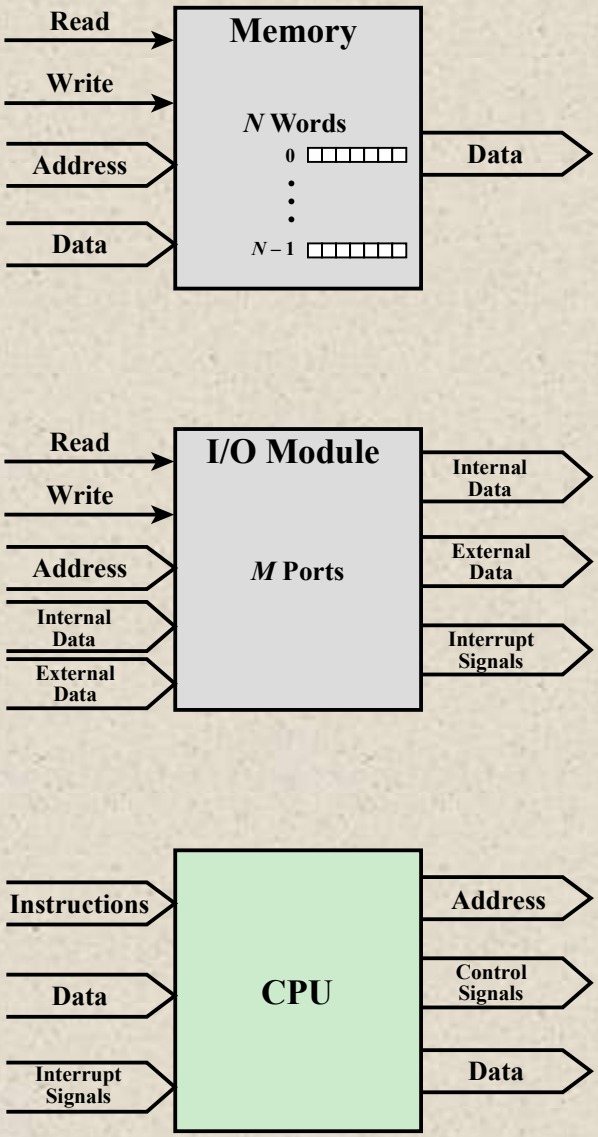


Figure 3.15 Computer Modules

The interconnection structure must support the following types of transfers:

Memory to processor	Processor to memory	I/O to processor	Processor to I/O	I/O to or from memory
Processor reads an instruction or a unit of data from memory	Processor writes a unit of data to memory	Processor reads data from an I/O device via an I/O module	Processor sends data to the I/O device	An I/O module is allowed to exchange data directly with memory without going through the processor using direct memory access

Bus Interconnection

A communication pathway connecting two or more devices

- Key characteristic is that it is a shared transmission medium

Signals transmitted by any one device are available for reception by all other devices attached to the bus

- If two devices transmit during the same time period their signals will overlap and become garbled

Typically consists of multiple communication lines

- Each line is capable of transmitting signals representing binary 1 and binary 0

Computer systems contain a number of different buses that provide pathways between components at various levels of the computer system hierarchy

System bus

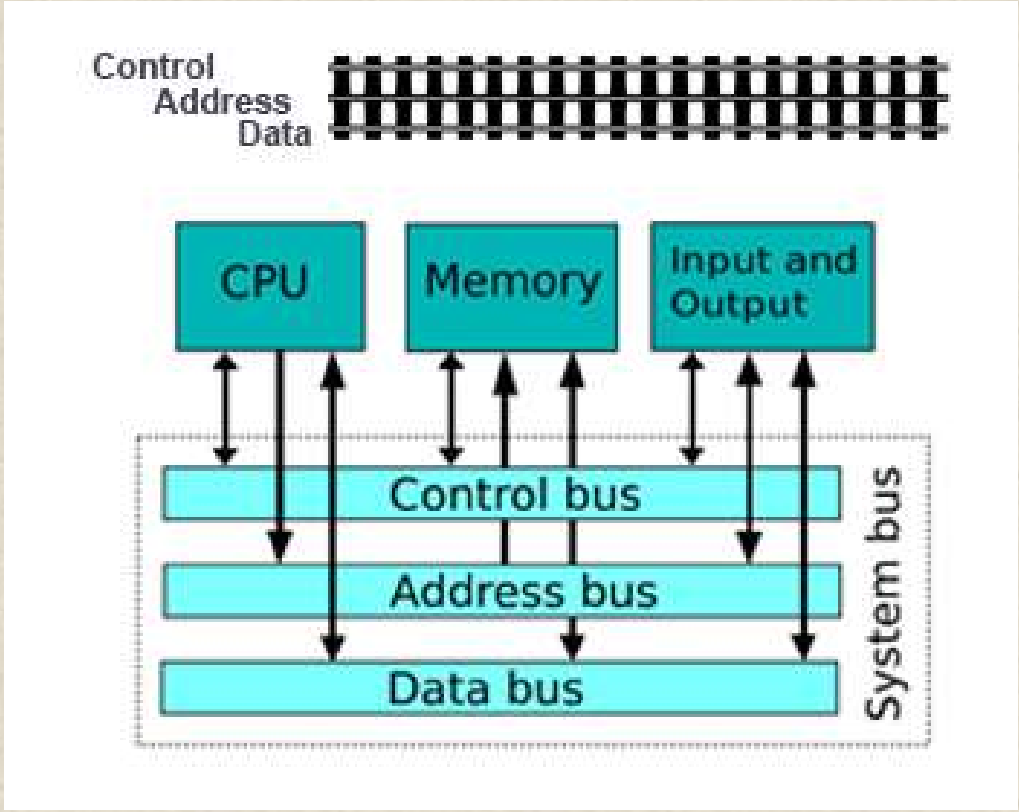
- A bus that connects major computer components (processor, memory, I/O)

The most common computer interconnection structures are based on the use of one or more system buses

Bus Structure

- System Bus:
  - 50 to hundred separate lines
  - Each line dedicated for a particular function from following functional groups:
    - Data lines
    - Control lines
    - Address lines

Bus Structure



Data Bus

- Data lines provide a path for:
  - Moving data among system modules
  - Data line collectively called Data Bus
- Width of Data Bus:
  - Number of lines in data bus
  - Each line carries one or more bit
  - 32, 64, 128 or even more
  - Number of Lines (Width) determine the amount of data which can be transferred.

Data Bus

- Width of Data Bus is key component for system performance:
  - Instruction 64 bits
  - Data bus 32 bits
  - During Instruction fetch memory visited twice.

Address Bus

- Address lines:
  - Determine the source/destination of data over data bus
  - Collectively called address Bus
- Processor wishes to read a word of 16, 32 or 64 bit from memory:
  - Puts the address of word on Address Bus
  - Width Determines maximum possible memory capacity of system

Address Bus

- Also used to address I/O Ports/Memory Locations:
  - 8 bit address bus
  - 01111111, higher order bit refers to the memory module 0 and 128 locations in memory module zero
  - 10000000, 1 refers to I/O module

Control Bus

- Data and address lines are shared by all the components
- So their use must be monitored:
  - Monitored through control lines
- Control lines given different commands shown in next slide

Typical control lines include:

- • **Memory write:** causes data on the bus to be written into the addressed location
- • **Memory read:** causes data from the addressed location to be placed on the bus
- • **I/O write:** causes data on the bus to be output to the addressed I/O port
- • **I/O read:** causes data from the addressed I/O port to be placed on the bus
- • **Transfer ACK**: indicates that data have been accepted from or placed on the bus
- • **Bus request:** indicates that a module needs to gain control of the bus
- • **Bus grant:** indicates that a requesting module has been granted control of the bus

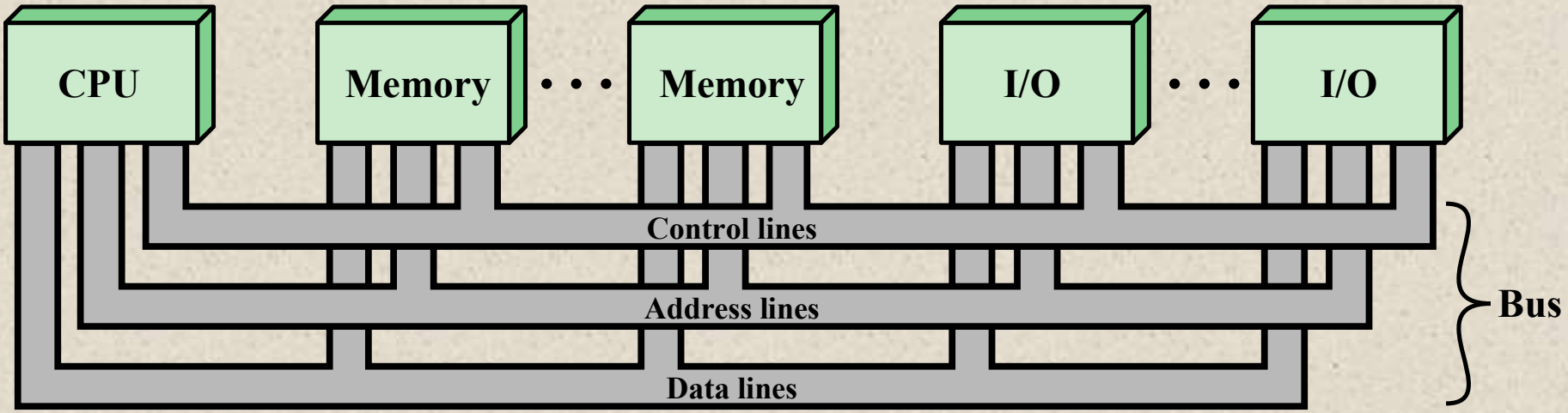
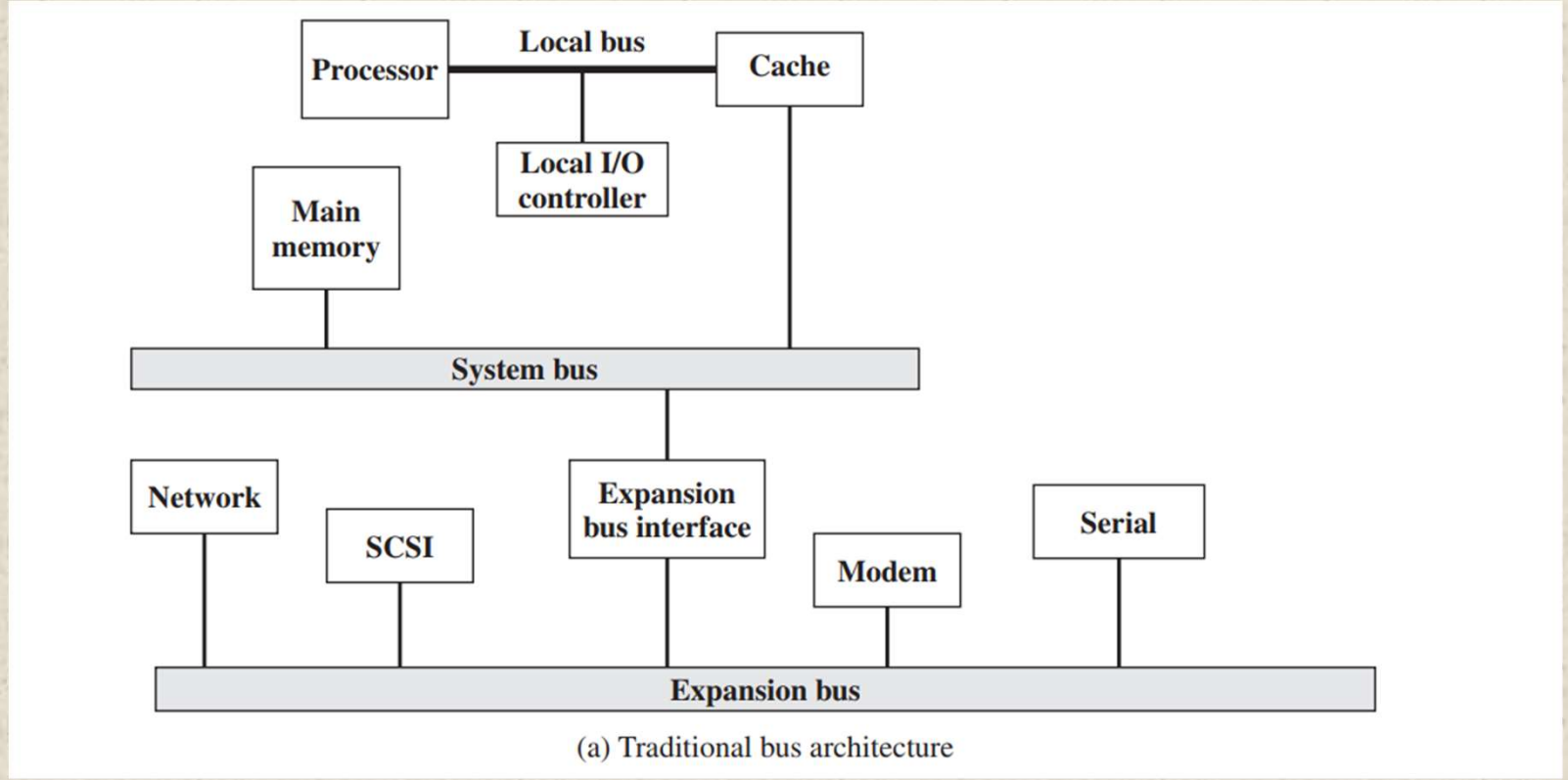


Figure 3.16 Bus Interconnection Scheme

Bus Interconnection Scheme

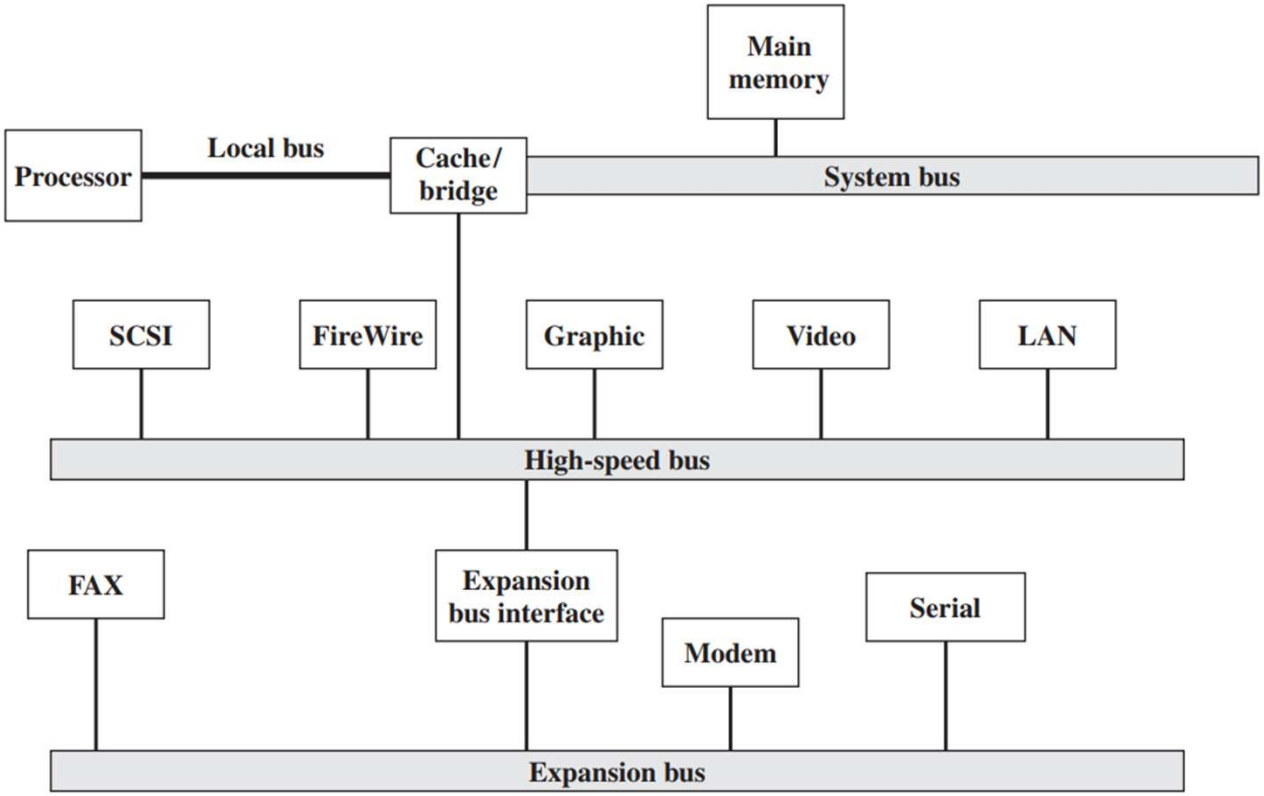
- Operation of the bus is as follows:
  - Obtain use of bus, bus granted, transfer data
  - If one module wishes to request data from another, Obtain use of bus, bus granted, request data, wait for response
- On chip bus (local bus) / on-board bus - Modern computers tend to have all major components on board and with more elements on same chip as the processor so
  - On-chip bus connecting processor & cache
  - On-board bus may connect processor to main memory and other components

Traditional Bus Architecture



(a) Traditional bus architecture

High Performance Bus Architecture



(b) High-performance architecture

Design Elements

- Type (Dedicated, Multiplexed)
- Method of Arbitration (Centralized, Decentralized)
- Timing (Synchronous, Asynchronous)
- Data transfer type (Read, Write, Read-Modify-Write, Read after Write, Block)

Bus Types

Two generic types:

- Dedicated
  - Separate data & address lines
  - Cost increases
  - Address Bus for Address
  - Data Bus for Data

Multiplexed

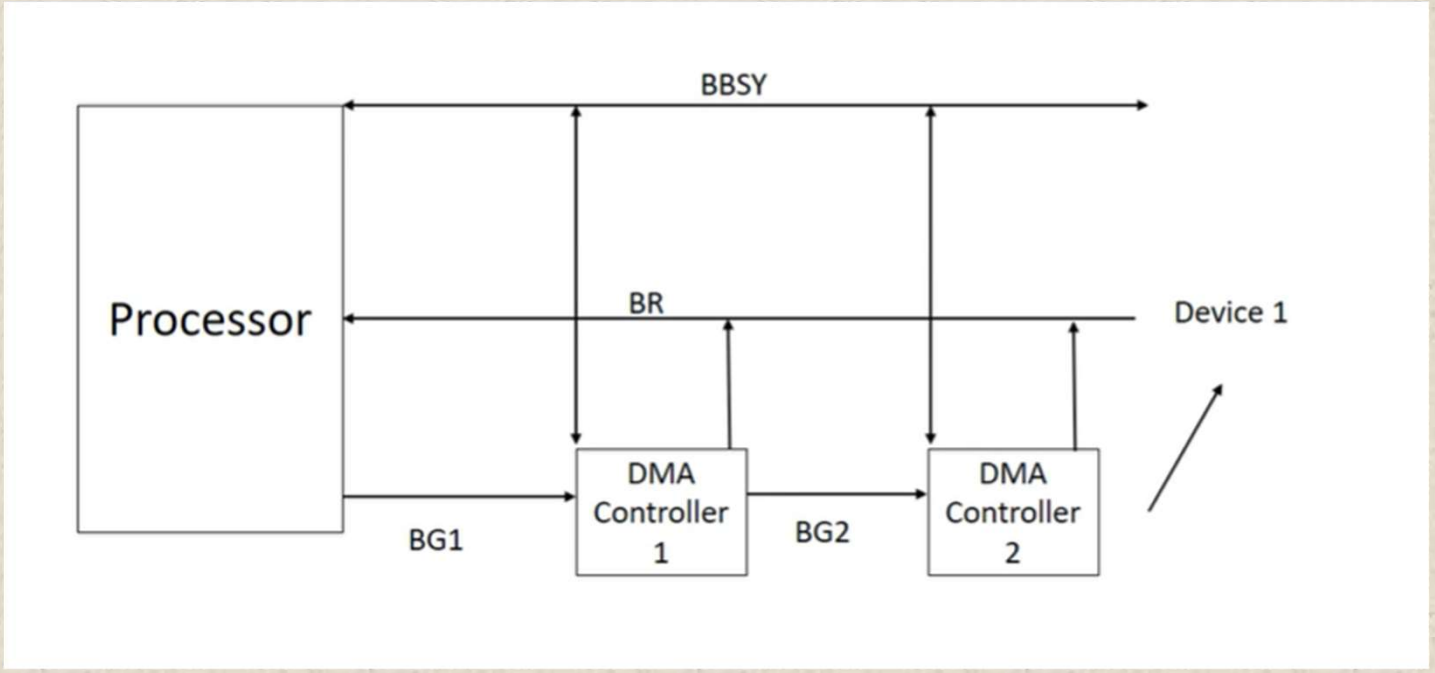
- Multiplexed
  - Shared lines for data and addresses
  - Address valid or data valid control line:
    - First address is copied and its activated
    - After determining the address, its deactivated and data is copied
  - Advantage - fewer lines
  - Disadvantages
    - More complex control
    - Reduction in performance:
      - CPU to I/O in progress, memory will have to wait

Bus Arbitration

- More than one module controlling the bus
  - e.g. CPU and DMA controller
- Only one module may control bus at one time
  - Read and Write
- **Bus Arbitration** refers to the process by which the current bus master accesses and then leaves the control of the bus and passes it to another bus requesting processor unit.
- Arbitration may be centralised or distributed

Centralised or Distributed Arbitration

- Centralised
  - Single hardware device controlling bus access
    - Bus Controller or Arbiter
  - May be part of CPU or a separate device
- Distributed
  - In which every device takes part in choosing the new bus master.
  - Sometimes few devices may be ignored always, because of low priority



Timing

- Refers to the way in which events are co-ordinated on bus – **Synchronous/ Asynchronous**

- Synchronous
  - Events determined by clock signals
  - Control Bus includes clock line
  - A single 1-0 is a **bus cycle!!! Clock cycle**
  - All devices can read clock line

  - **Asynchronous**
  - → The occurrence of one event on a bus follows and depends on the occurrence of a previous event