EE275 **Spring 2017**

San Jose State University
Department of Electrical Engineering

Mini-Project I (Due Feb. 27)

Design and simulate the working of a 5-stage pipelined IEEE single-precision floating-point adder, as discussed in class.

Your design should proceed in two steps:

1) First, design an un-pipelined SP FP adder, and show that it works using the test cases shown below.

2) Next, change the design to the 5-stage pipelined FP adder as described below. Then show that it works for the six pairs of inputs as shown below. Note that it will take 11 cycles to output all 6 cases.

   Stage 1: Compare the exponents and determine the amount of shifts required to align the mantissa to make the exponents equal (alignment-1).
   Stage 2: Right-shift the mantissa of the smaller exponent by the required amount (alignment-2).
   Stage 3: Compare the two aligned mantissas and determine which is the smaller of the two. Take 2's complement of the smaller mantissa if the signs of the two numbers are different (addition).
   Stage 4: Add the two mantissas. Then, determine the amount of shifts required and the corresponding direction to normalize the result (normalization-1).
   Stage 5: Shift the mantissa to the required direction by the required amount. Adjust the exponent accordingly and check for any exceptional condition (normalization-2).

Your report should include well-commented Verilog or VHDL, or C/C++ source code and the hardcopy of the simulation results, including timing diagrams, if in Verilog, or register-level status diagram, if in C/C++, for the following cases.

Test Case	A	B
1	99	178
2	97	-79
3	-55	75
4	-280	-69
5	0	0
6	0	-113

NOTE: To show the authenticity of your work, attach the last two digits of your student ID to every signal and variable name used in your Verilog/ VHDL/C/C++ code. For example, if your SID is 123456789, signal names should be x89, a89, etc. Each of the screen-captures of your code and simulation results should bear these signal names.