SAN JOSÉ STATE UNIVERSITY
Charles W. Davidson College of Engineering
DEPARTMENT OF ELECTRICAL ENGINEERING

EE 271 – Advanced Digital System Design and Synthesis

Fall 2016 Final Project Report

Implementing a 64-bit Signed Binary Multiplier & Divider Circuit

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Executive Summary

While Designing digital circuits, Area and speed are usually conflicting factors. If one try to improve speed by adjusting clock frequency, it results mostly in bigger areas on the other hand low power consumption and smaller area are desirable for better performance. Multipliers and Dividers are one of the most important component of many systems. This project designs a 64-bit Signed Binary Multiplier & Divider Circuit and further Optimized in terms circuit performance.

I. General Project Information

Table I.1: List of EDA Tools Used

EDA Tool Name	Company	You Used it for
VCS	Synopsys	Simulation & test
ModelSim	Mentor Graphics	Simulation & test
Design Vision	Synopsys	Synthesis & optimization

Table I.2: List of Libraries Used

Library file name	Used with (EDA tool name)	The library is at (directories on eecad systems)
WCCOM Toshiba	Synopsys Design Compiler	/apps/Toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25
BCCOM Toshiba	Synopsys Design Compiler	/apps/Toshiba/sjsu/synopsys/tc240c/tc240c.db_BCCOM25
NOMIN Toshiba	Synopsys Design Compiler	/apps/Toshiba/sjsu/synopsys/tc240c/tc240c.db_NOMIN25

Table I.3: List of Verilog Modules (both design and test modules)

64 – bit Binary Signed Multiplier

Module Name	Ports	Short Description
mul	result, valid, clock, reset, start, opera1, opera2, muordi	64 – bit Binary Signed Multiplier
testmul	result, valid, clock, reset, start, opera1, opera2, muordi	64 – bit Binary Signed Multiplier Testbench
Add_rca64	sum, c_out, a, b, c_in	64 – bit Full Adder
Add_rca	sum, c_out, a, b, c_in	32 – bit Full Adder
Add_rca_4	sum, c_out, a, b, c_in	4 - bit Full Adder
Add_full	sum, c_out, a, b, c_in	Full Adder
Add_half	sum, c_out, a, b	Half Adder

64 – bit Binary Signed Divider

Module Name	Ports	Short Description
div	result, valid, clock, reset, start, opera1, opera2, muordi	64 – bit Binary Signed Divider
testdiv	result, valid, clock, reset, start, opera1, opera2, muordi	64 – bit Binary Signed Divider Testbench
Add_rca64	sum, c_out, a, b, c_in	64 – bit Full Adder
Add_rca	sum, c_out, a, b, c_in	32 – bit Full Adder
Add_rca_4	sum, c_out, a, b, c_in	4 - bit Full Adder
Add_full	sum, c_out, a, b, c_in	Full Adder
Add_half	sum, c_out, a, b	Half Adder

64 – bit Binary Signed Multiplier and Divider

Module Name	Ports	Short Description
muldiv	result, valid, clock, reset, start, opera1, opera2, muordi	64 – bit Binary Signed Multiplier and Divider
testmuldiv	result, valid, clock, reset, start, opera1, opera2, muordi	64 – bit Binary Signed Multiplier and Divider Testbench
Add_rca64	sum, c_out, a, b, c_in	64 – bit Full Adder
Add_rca	sum, c_out, a, b, c_in	32 – bit Full Adder
Add_rca_4	sum, c_out, a, b, c_in	4 - bit Full Adder
Add_full	sum, c_out, a, b, c_in	Full Adder
Add_half	sum, c_out, a, b	Half Adder

II. Implementation Overview

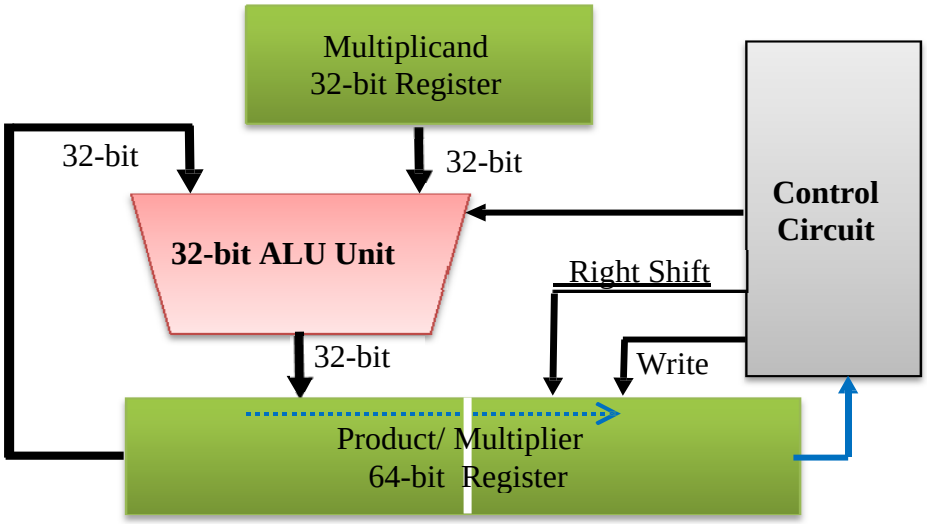

Figure 1: Architecture of Multiplier

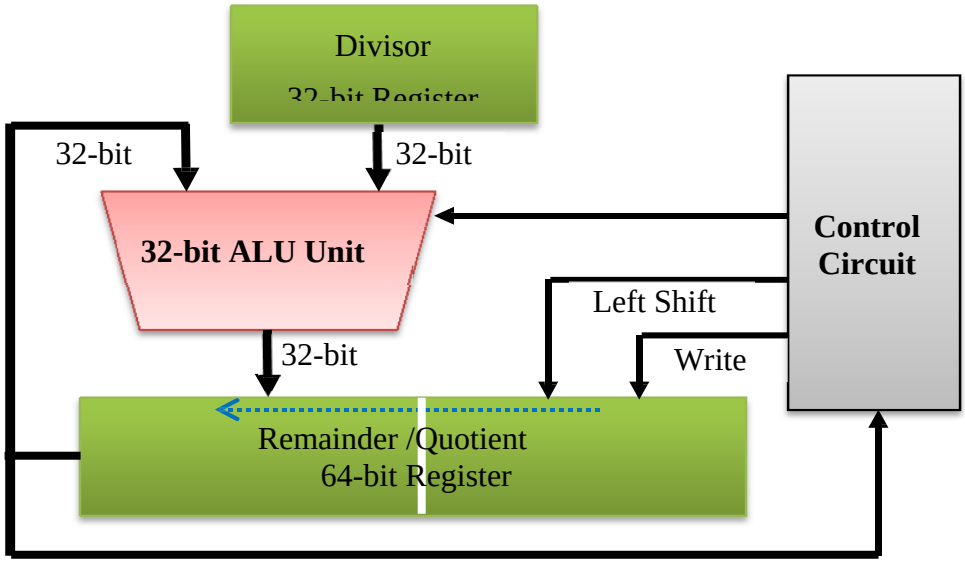

Figure 2: Architecture of Divider (non-restoring scheme)

Figure II.1: Block Diagram of 32-bit ALU unit

In this report we have designed 64bit signed multiplier and divider circuit where we are using 32 bit ALU to perform given numbers. We just need to make change in value of “muordi” as it is generalized code for multiplier and divider. In design we have control unit whenever reset is active low and start signal is active high puts circuit in working condition it generates result after 32 clock cycles for multiplier and 33 clock cycles for divider circuit. Design specifications are

such that multiplier takes use of right shift and divider takes use of left shift in operation. We have OPE flag and valid register in the design. Whenever valid register is 1 the result is ready for the operator and OPE flag have different role in both multiplier and divider design. We are saving the cost by using 64bit result register as product/multiplier register in multiplication and remainder/quotient register in division process.

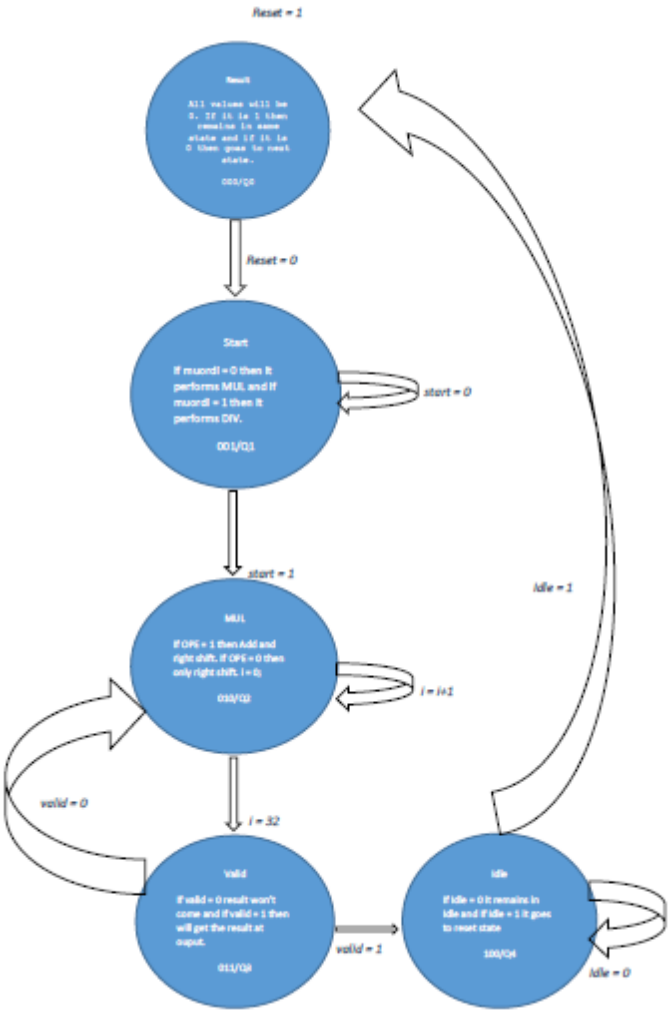

Figure II.2: State Transition Diagram of Sequential Multiplier

There are mainly 5 states as shown in figure. Stage 000/Q0 is a reset state. State 001/Q1 is for Startd 010/Q2 for Multiplication operation. State 011/Q3 is for Valid and 100/Q4 is for Idle. All the conditions and transitions are shown in Control diagram above. When count is equals to 32 valid signal goes HIGH and prodt is available at the outpit.

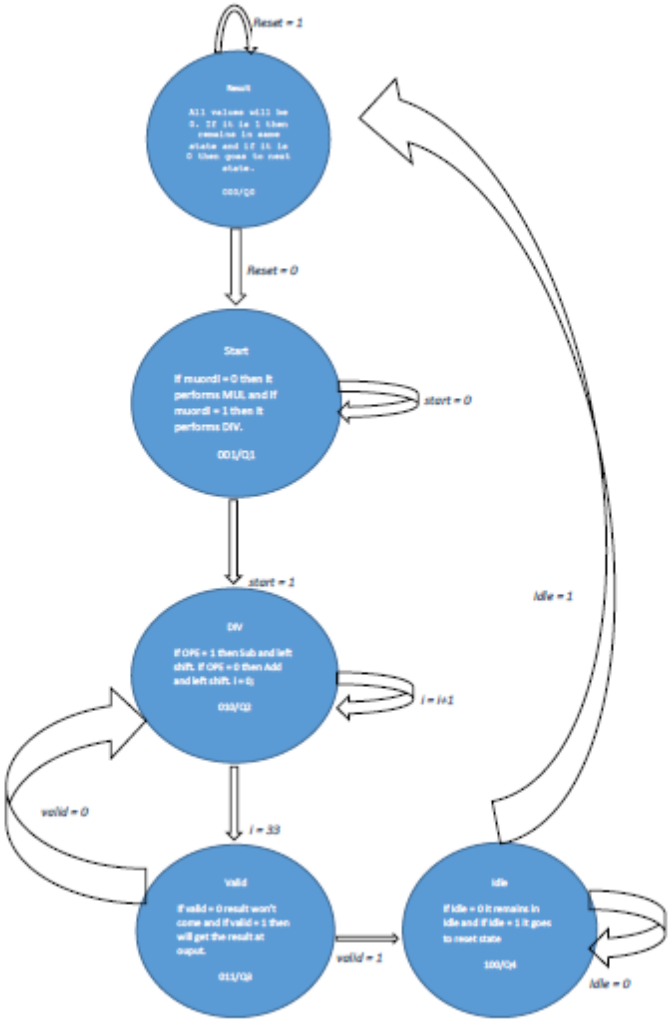

Figure II.3: State Transition Diagram of Sequential Divider

There are mainly 5 states as shown in figure. Stage 000/Q0 is a reset state. State 001/Q1 is for Startd 010/Q2 for Division operation. State 011/Q3 is for Valid and 100/Q4 is for Idle. All the conditions and transitions are shown in Control diagram above. When count is equals to 33 valid signal goes HIGH and prodt is available at the outpit.

III. RTL-Level (Pre-synthesis) Simulations/Tests

Testbench used are generalized for both 64 bit binary signed Multiplier and Divider circuit where we just need to make sure that we provide right value of clock such that after post synthesis we get correct output and No slack violation. We have to give 0 or 1 to "muordi" to perform Multiplication or Division respectively. The multiplier and divider starts working when reset signal becomes active low and start signal becomes active high. Even in the middle of calculation if reset becomes active high, the circuit stops calculation and returns to the initial state. The calculation starts again with the current set of inputs. So, the testbench includes all such possibilities and exhibits the proper functioning of the circuit. These test cases provide the worst case timing delays for the post synthesis simulation.

Table III.1 – Four Selected Test Data for Multiplier Circuit

Test Case	`opera1` (hex)	`opra2` (hex)	`result (hex)`
1	-32'h45454545	32'h12121212	-64'hFB1C3D5E89684726
2	32'h24681357	-32'h54545454	-64'hF401DB8302F51B74
3	32'h19283746	32'h56473829	64'h087A823DABF22A36
4	-32'h24681012	-32'h36912151	64'h07C29711D53167B2

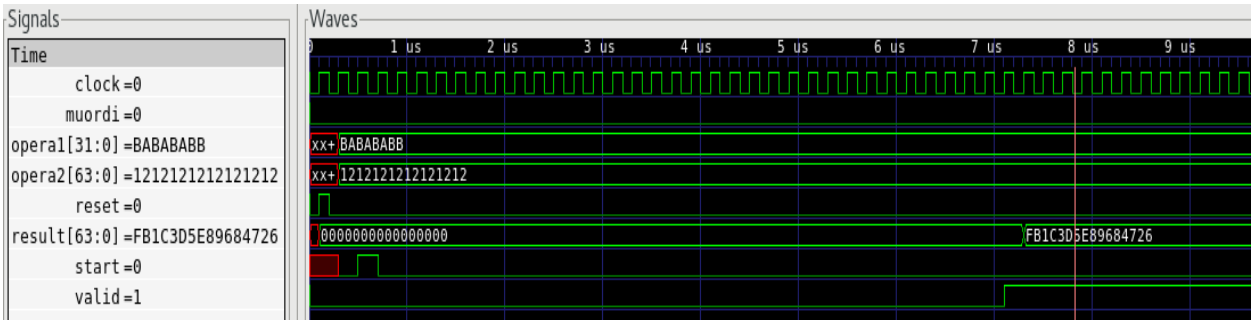

Figure III.1a: RTL simulation waveform that contains test case #1

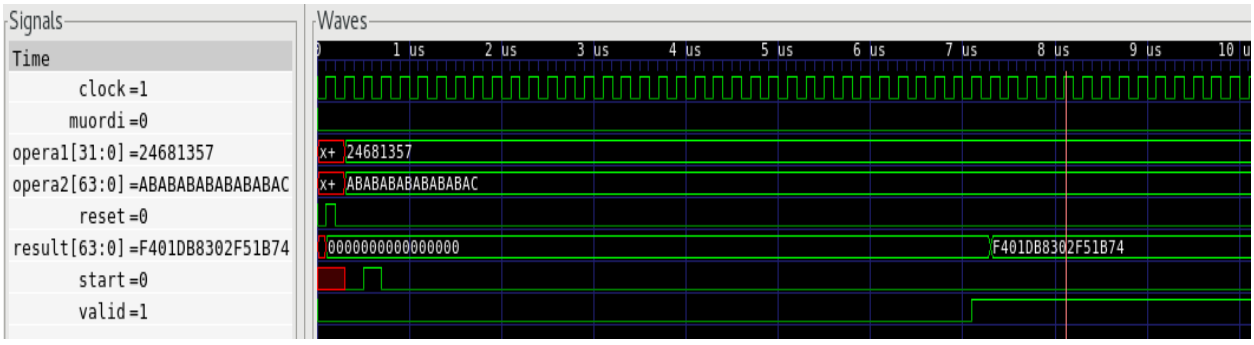

Figure III.1b: RTL simulation waveform that contains test case #2

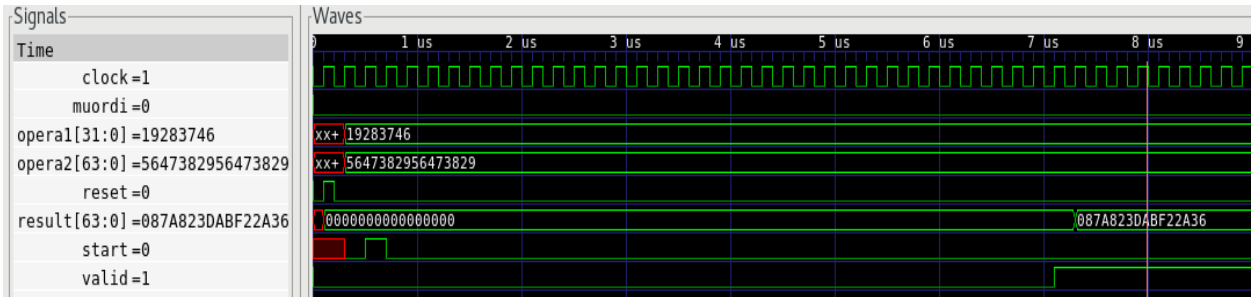

Figure III.1c: RTL simulation waveform that contains test case #3

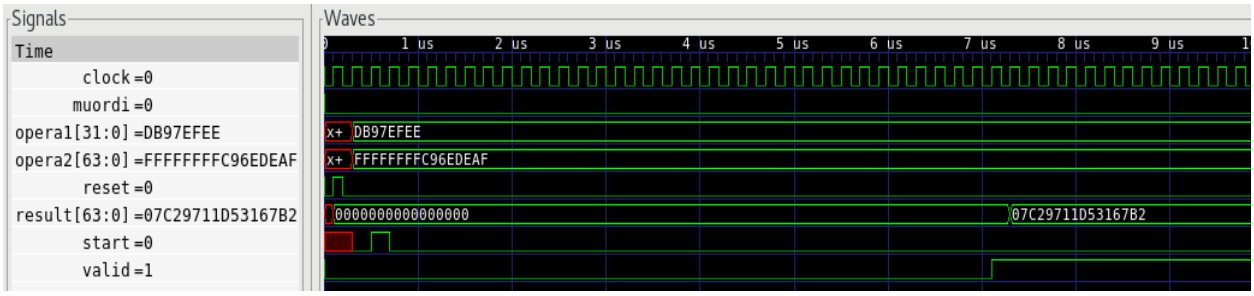

Figure III.1d: RTL simulation waveform that contains test case #4

Table III.2 – Four Selected Test Data for Divider Circuit

Test Case	**`opera1`** (hex)	**`opra2`** (hex)	**`result (hex)`**
1	**-32'h45454545**	**64'h1212121212121212**	**-64'hE4E4E4E4-BD37A6F5**
2	**32'h12121212**	**-64'h2323232323232323**	**-64'hF2F2F2F2-0E38E38D**
3	**32'h54545454**	**64'h12345678123456 78**	**64'h488CD114-37437435**
4	**-32'h34343434**	**-64'h1432143214231423**	**64'h2A572A57-6309457F**

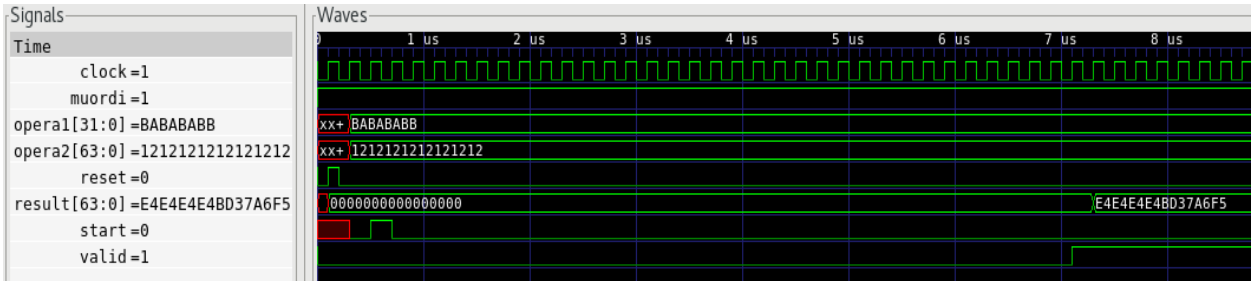

Figure III.2a: RTL simulation waveform that contains test case #1

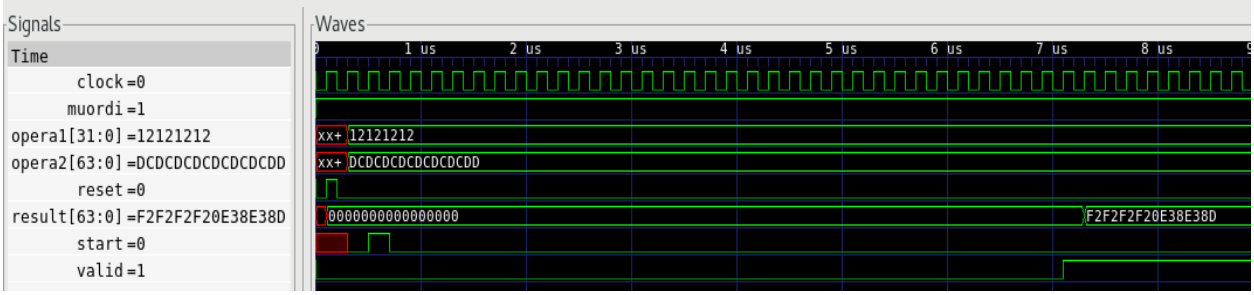

Figure III.2b: RTL simulation waveform that contains test case #2

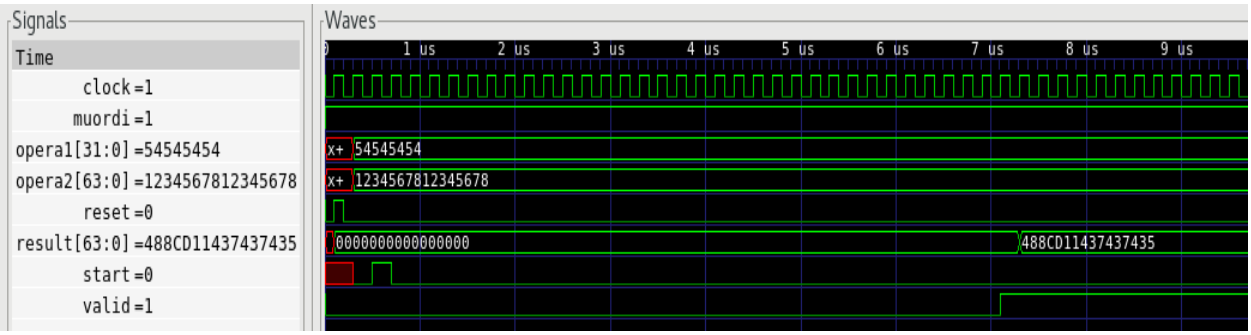

Figure III.2c: RTL simulation waveform that contains test case #3

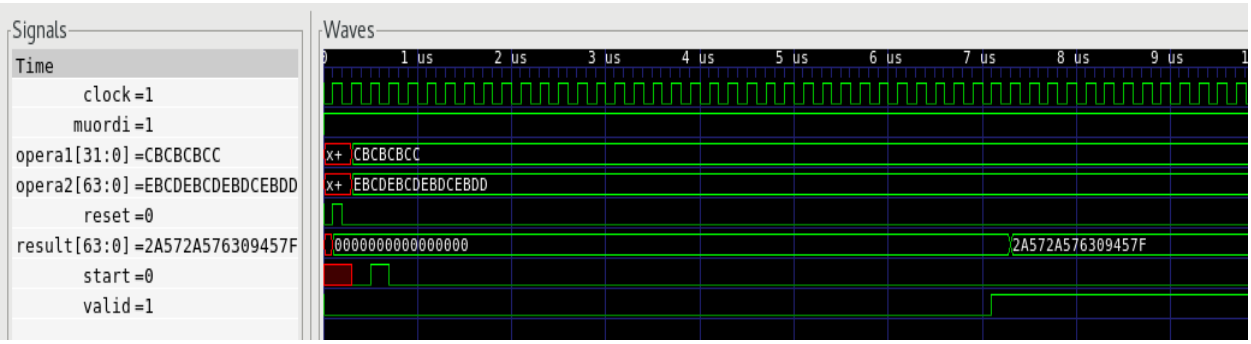

Figure III.2d: RTL simulation waveform that contains test case #4

IV. Synthesis and Optimizations

Table IV.1: Synthesis Constraints and Results for Multiplier

Trial #	**Your design constraint settings** (such as area, clock, delay, etc.)	**Results after synthesis** (such as area, time slack, power, etc.)
1	Area = 1000 Clock = 1ns	Area = 5329.00 Time Slack = -19.32 (violation) Power = 61.5276mW Data Arrival Time = 19.76
2	Area = 1000 Clock =15ns	Area = 5048.50 Time Slack = -4.91 (violation) Power = 3.6893mW Data Arrival Time = 19.31
3	Area = 1000 Clock =20ns	Area = 4808.50 Time Slack = -0.15 (violation) Power = 2.6677mW Data Arrival Time = 19.58
4	Area = 1000 Clock =21ns	Area = 4613.00 Time Slack = 0.00 Power = 2.5182mW Data Arrival Time = 20.43
5	Area = 1000 Clock =30ns	Area = 4190.00 Time Slack = 1.58 Power = 1.7316mW Data Arrival Time = 24.39
6	Area = 1000 Clock =28ns	Area = 4294.00 Time Slack = 0.01 Power = 1.9565mW Data Arrival Time = 27.28

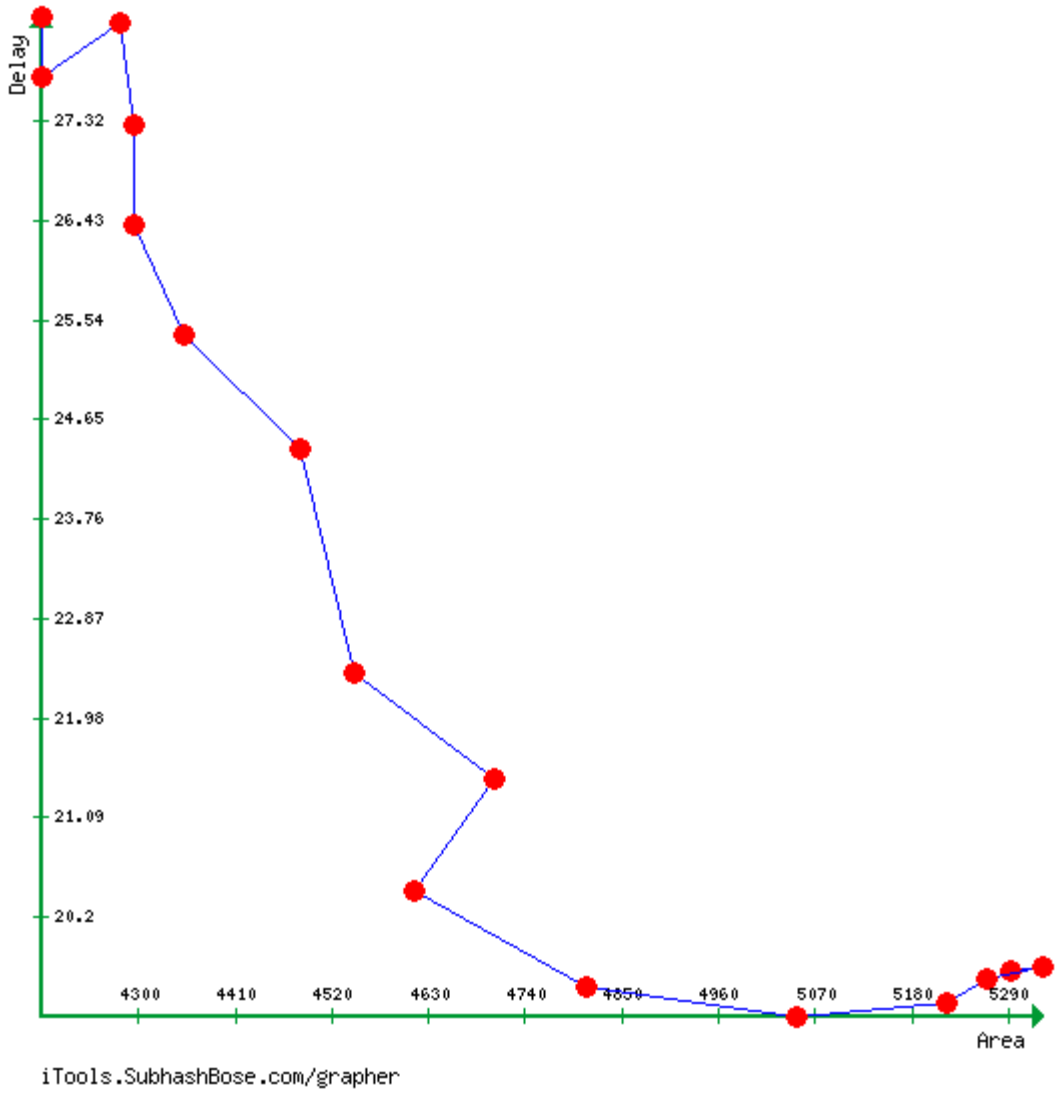

Figure IV.1: Area vs. Delay Curve of Multiplier

Table IV.2: Synthesis Constraints and Results for Divider

Trial #	**Your design constraint settings** (such as area, clock, delay, etc.)	**Results after synthesis** (such as area, time slack, power, etc.)
1	Area = 1000 Clock = 1ns	Area = 6550.00 Time Slack = -19.10 (violation) Power = 75.5802mW Data Arrival Time = 19.50
2	Area = 1000 Clock = 15ns	Area = 6081.50 Time Slack = -5.56 (violation) Power = 4.7866mW Data Arrival Time = 19.99
3	Area = 1000 Clock = 20ns	Area = 6147.50 Time Slack = -0.38 (violation) Power = 3.4253mW Data Arrival Time = 19.81

4	Area = 1000 Clock = 21ns	Area = 6041.50 Time Slack = 0.00 Power = 3.1950mW Data Arrival Time = 20.43
5	Area = 1000 Clock = 30ns	Area = 4879.50 Time Slack = 0.87 Power = 2.2428mW Data Arrival Time = 28.40
6	Area = 1000 Clock = 29ns	Area = 5102.50 Time Slack = 0.03 Power = 2.3098mW Data Arrival Time = 28.25

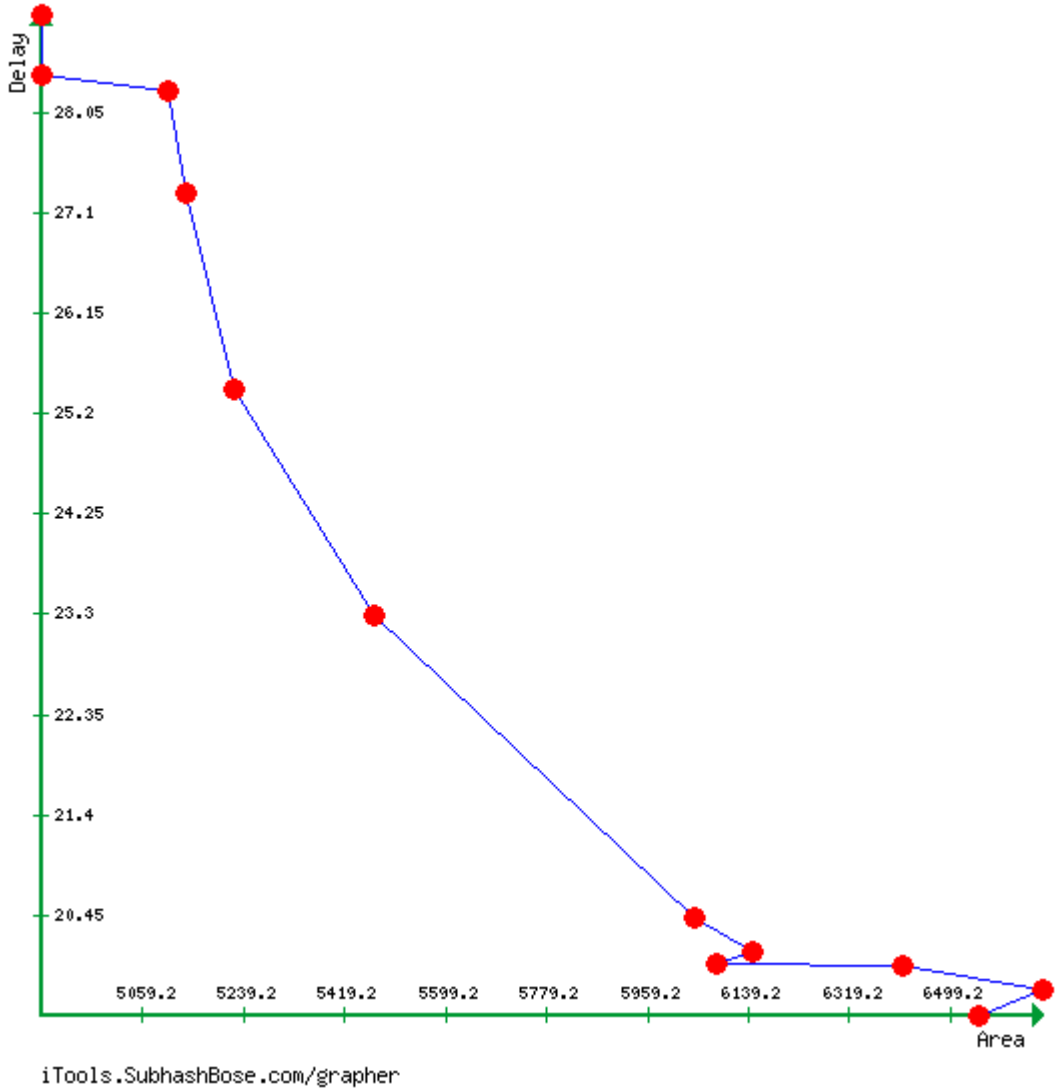

Figure IV.2: Area vs. Delay Curve of Divider

For Values of clock 20ns or less we are getting time slack negative, hence we can say 20ns is most optimized clock possible. Note that to get area minimum we have given clock more than 20ns. The slack is 0.00 and 0.01 between 21ns to 28ns for multiplier and 0.00 to 0.01 between 21ns to 29ns for divider. We can see that our circuit will not work below certain frequency 1/20nS, 50 MHz with 20ns of clock time period in both cases. If we increase clock time period now then Area and Power decreases and Time slack increase depending upon value of clock, but if we take increased clock time period between 21ns to 29ns that won't make any difference in time slack and area, power consumption will decrease which simply means that we can make circuit which works little slower by increasing clock but area and power will decrease which will save cost. Power and Area has inverse relationship with clock, one increases other one decreases. Above graphs clearly plots area and delay inverse relationship when we change the clock period.

V. Gate-Level (Post-synthesis) Dynamic Simulations/Tests

Table V.1 – Four Selected Test Data for Multiplier Circuit

Test Case	`opera1` (hex)	`opra2` (hex)	`Time Delay (in time unit)`
1	-32'h45454545	32'h12121212	60ns = 600ps
2	32'h24681357	-32'h54545454	60ns = 600ps
3	32'h19283746	32'h56473829	60ns = 600ps
4	-32'h24681012	-32'h36912151	60ns = 600ps

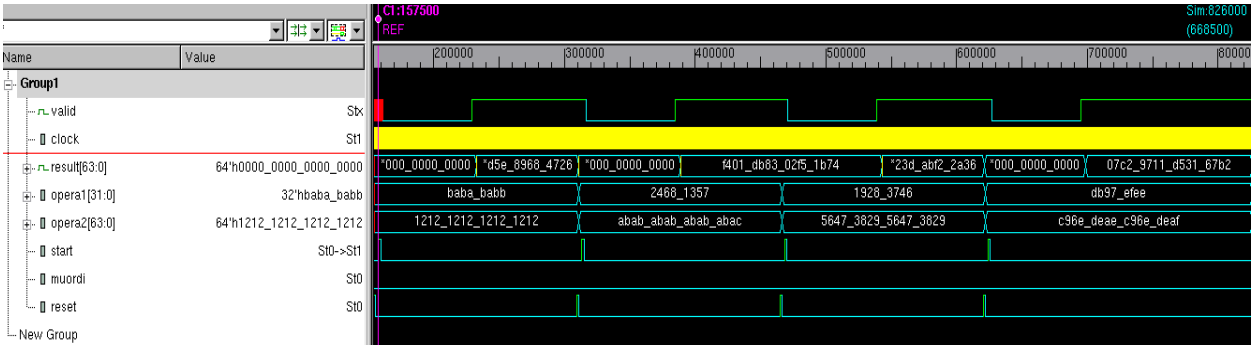

Figure V.1: Gate-level simulation waveform that contains test cases

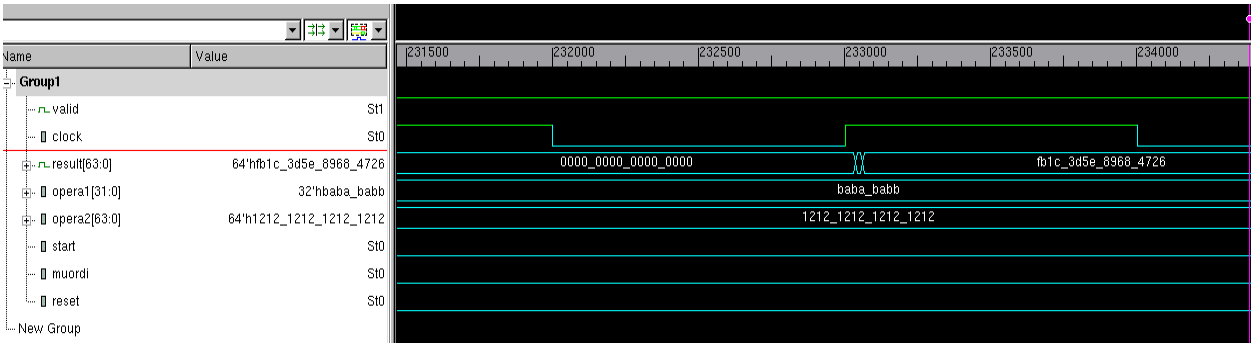

Figure V.1a: Gate-level simulation waveform that contains test case #1

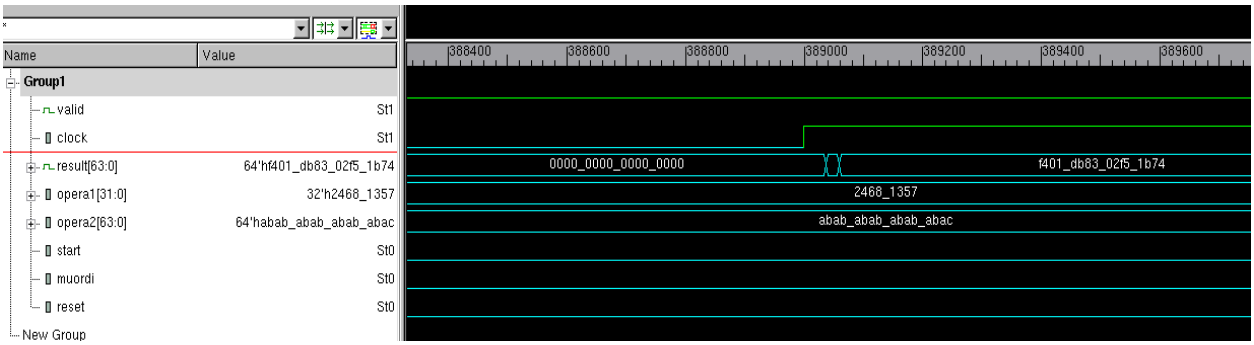

Figure V.1b: Gate-level simulation waveform that contains test case #2

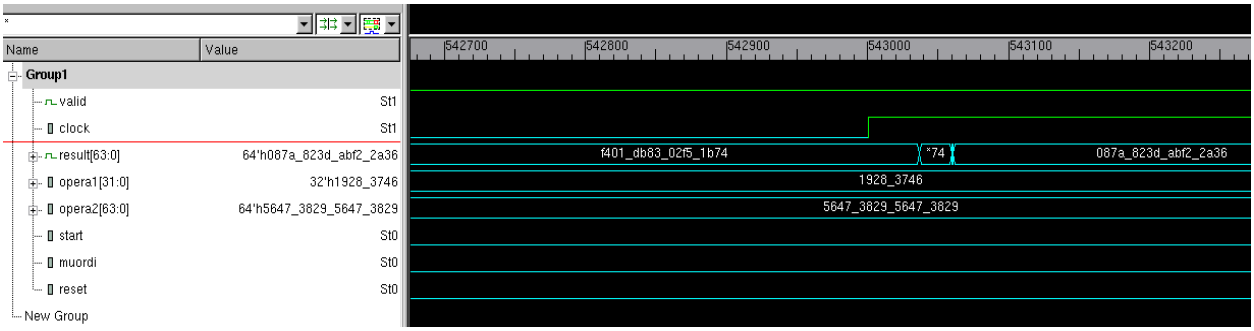

Figure V.1c: Gate-level simulation waveform that contains test case #3

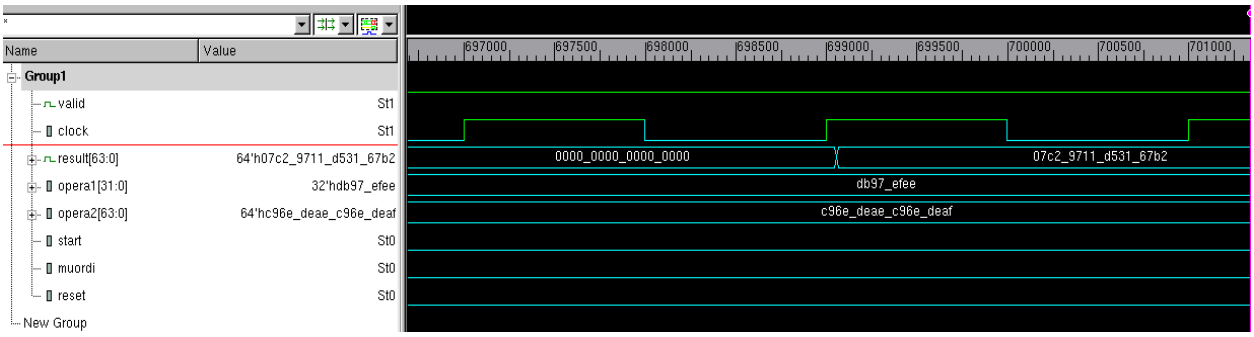

Figure V.1d: Gate-level simulation waveform that contains test case #4

Table V.2 – Four Selected Test Data for Divider Circuit

Test Case	**opera1** (hex)	**opra2** (hex)	**Time Delay (in time unit)**
1	-32'h45454545	64'h1212121212121212	60ns = 600ps
2	32'h12121212	-64'h2323232323232323	60ns = 600ps
3	32'h54545454	64'h1234567812345678	60ns = 600ps
4	-32'h34343434	-64'h1432143214231423	60ns = 600ps

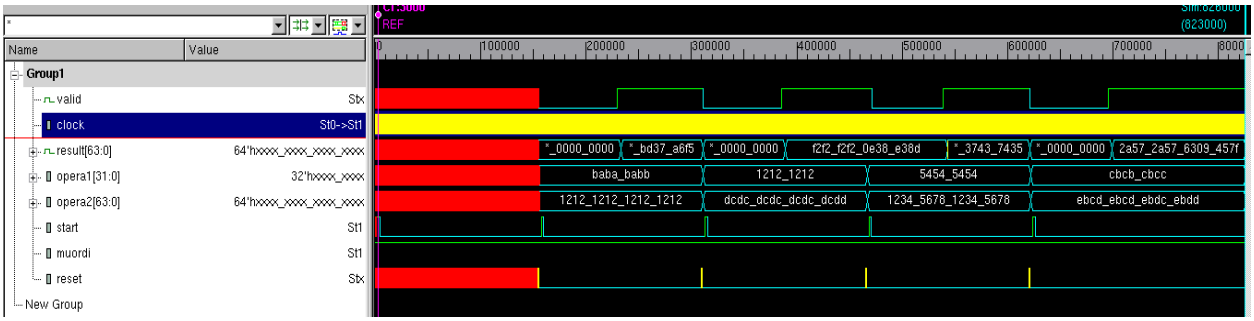

Figure V.2a: Gate-level simulation waveform that contains test cases

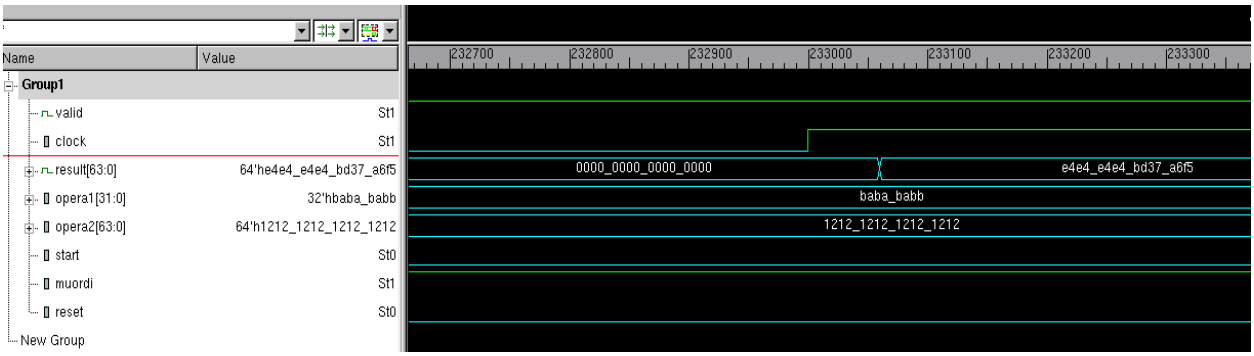

Figure V.2a: Gate-level simulation waveform that contains test case #1

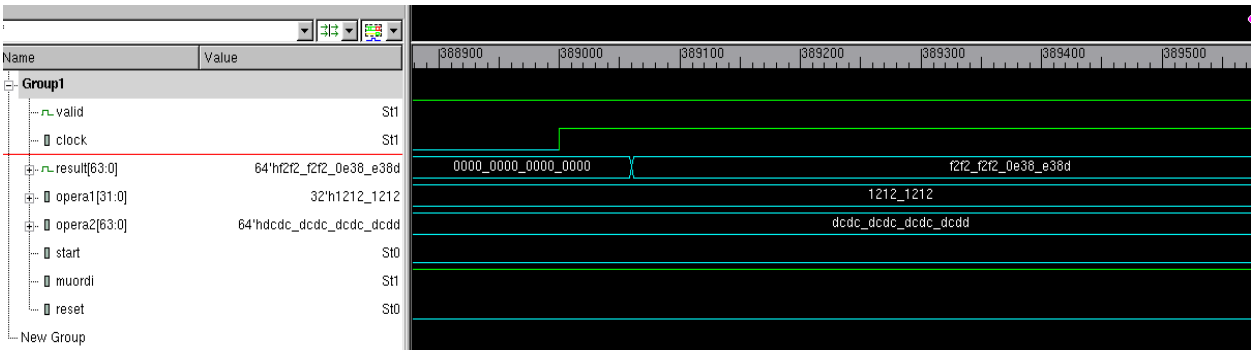

Figure V.2b: Gate-level simulation waveform that contains test case #2

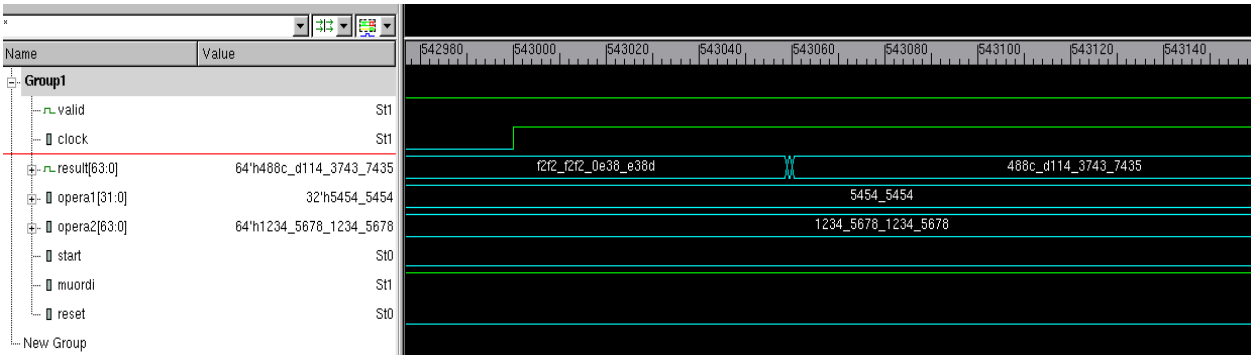

Figure V.2c: Gate-level simulation waveform that contains test case #3

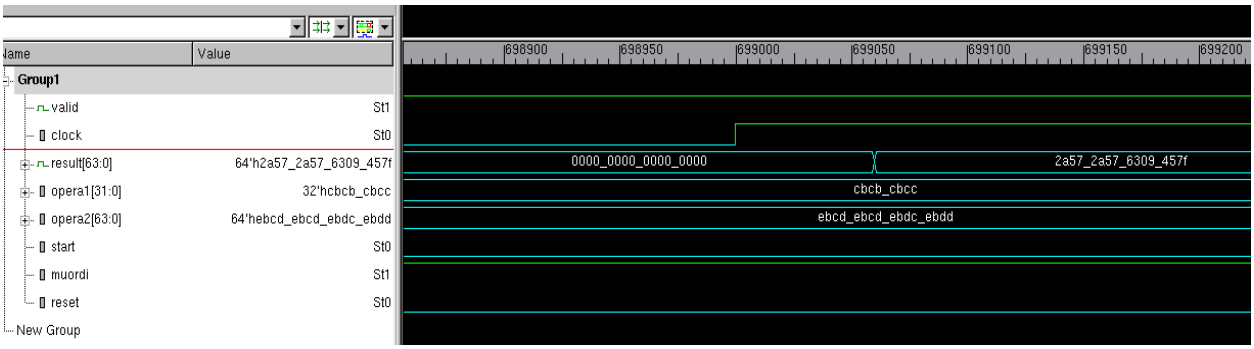

Figure V.2d: Gate-level simulation waveform that contains test case #4

When we do Gate level simulation with testbench and netlist file which was generated by synthesis script file, resultant output waveforms are not same as the RTL level waveforms. Actual circuit consist of many Gates and wires and hence 'Delay' comes in picture. If we adjust the output waveforms correctly and zoom in the difference between actual result time should be and delayed result time which we have obtained. In both multiplication and division, we are getting delay of 60ns (600ps). In multiplication when we give inputs opera1 and opera2 it should take 32 cycles to give result, but as we can see from waveforms result is coming with delay of 600ps. In division the clock should take 33 cycles but it is taking more 600ps of delay. Any type of delay will affect the performance of the circuit. We should try to minimize the delay by using better constrains.

VI. Conclusion

The above analysis clearly exhibits that the 64bit Divider consumes more area and power as it has more combinational logic as compared to 64bit Multiplier and also works at lower frequency than the 64bit multiplier. In multiplication the result is always as expected but in division if quotient is bigger then 32 bit then result will give only the 32bit and won't carry overflow value. If we take only Multiplier circuit the optimised clock is 28ns and time slack is 0.01 with area and power of 4294 and 1.9565mW. If we take only Divider circuit the optimised clock is 29ns and time slack is 0.03 with area and power of 5102.50 and 2.3098mW. It is clear from above specs, if we use multiplier and divider circuit separately the cost will be almost same for two different arithmetic operations. If we combine both in one design it will save power area and cost of other design with small addition of cost and area, power, clock. If we take both Multiplier and Divider circuit the optimised clock is 29ns and time slack is 0.02 with area and power of 5465.00 and 2.5365mW. Signed numbers are also converted to unsigned with the help of two's compliment method.

Appendix A

A.1 Contents from EDA Tool Configurations and Setup Files

```
#set link_library {/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_NOMIN25}
#set link_library {/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_BCCOM25}
set link_library {/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25}
#set target_library {/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_NOMIN25}
#set target_library {/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_BCCOM25}
set target_library {/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25}
#set symbol_library {/apps/toshiba/sjsu/synopsys/tc240c/tc240c.workview.sdb}
set synthetic_library {dw_foundation.sldb standard.sldb}
set_min_library     /apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25     -
min_version /apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_BCCOM25
```

A.2 Commands and/or Scripts Used for Simulation and Synthesis

```
#set link_library {/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_NOMIN25}
#set link_library {/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_BCCOM25}
set link_library {/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25}
#set target_library {/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_NOMIN25}
#set target_library {/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_BCCOM25}
set target_library {/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25}
#set symbol_library {/apps/toshiba/sjsu/synopsys/tc240c/tc240c.workview.sdb}
set synthetic_library {dw_foundation.sldb standard.sldb}
set_min_library     /apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25     -
min_version /apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_BCCOM25

analyze -format verilog "mul.v"
elaborate "mul"
link
check_design

create_clock clock -name clock -period 28
set_clock_uncertainty 0.25 clock
set_propagated_clock clock




set_max_area 1000
set_fix_hold clock
compile -map_effort high
report_cell
report_net
update_timing
report_timing -max_paths 5
report_timing >> report_time.txt
report_area >> report_area.txt
report_power >> report_power.txt
write -hierarchy -format verilog -output mul_netlist.v
quit
```

Compile:

```
vcs +v2k “mul.v” “testmul.v”
```

Simulation:

```
./simv
```

Presynthesis

Waveform:

```
gtkwave mul.vcd &
```

synthesis:

```
dc_shell -xg -f synthesis.script | tee report.txt
```

Post synthesis Simulation:

```
vcs +v2k –debug_all –gui –y /apps/toshiba/sjsu/verilog/tc240c
+libext+.tsbvlibp testmul.v mul_netlist.v
```

Appendix B
Completed Verilog Source Codes and Testbenches

For 64bit Multiplier

```
`timescale 10ns/1ns
module mul (result, valid, opera1, opera2, clock, reset, start,  muordi);

output [63:0] result;
output valid;

input [31:0] opera1;
input [63:0] opera2;
input  start, reset, muordi, clock;

reg  valid, OPE, w2, w3, w4, idle;
reg [63:0] result, result_copy, result_not, opera2_copy, opera2_not;
reg [31:0] opera1_copy, opera1_not;
wire  reset, start, muordi,cin, cin1a, cin2a, cina, carry, w5, w6;
wire [31:0] opera1;
wire [31:0] w1, w10, w13, w9;
wire [31:0] D, A;
wire [63:0] opera2, B, w11, w12;
integer i;

assign carry =1'b0;
assign A = 1'b0;
assign B = 1'b0;

Add_rca M1 ( w10, , opera1_not, A, cin1a);
Add_rca64 M2 ( w11, , opera2_not, B, cin2a);
Add_rca64 M4 ( w12, , result_not, B, cina);


notif1 A1(cin1a, carry, w2);
bufif0 A2 (cin1a, carry, w2);
notif1 A5(cin2a, carry, w3);
bufif0 A6 (cin2a, carry, w3);
notif1 A7(cina, carry, w4);
bufif0 A8 (cina, carry, w4);

always @(opera1) begin
 w2 = opera1 [31];
if (w2 == 1)begin
opera1_not = ~opera1;
end else begin
opera1_not = opera1;
end
end

always @(opera2) begin
w3 = opera2 [63];
if (w3 == 1) begin
opera2_not = ~opera2;
```

```
end else begin
opera2_not = opera2;
end
end

initial begin
valid=0;
end

assign w5 = w2;
assign w6 = w3;

reg [2:0] cust, nest;
parameter Q0 = 3'b000,
          Q1 = 3'b001,
          Q2 = 3'b010,
          Q3 = 3'b011,
          Q4 = 3'b100;


always@(posedge clock or posedge reset)
begin
    if (reset)
    begin
        cust = Q0;
    end
    else
    begin
        if (start)
        begin
               cust = Q1;
        end
        else
        begin
            cust = nest;
        end
    end
end

assign cin=0;
assign D= result_copy [63:32];

always @(posedge clock)
case (cust)
Q0: //reset
     if (reset) begin
      result = 0;
      i = 35;
      nest = cust;
      end

Q1: // start
        if (muordi == 1'b0) begin
        w4 = w5^w6;
        i = 0;
        valid = 0;
```

```
        OPE =0;

       if (w5==1) begin
       opera1_copy = w10;
       end else begin
       opera1_copy = opera1;
       end

       if (w6==1) begin
       opera2_copy = w11;
       end else begin
       opera2_copy = opera2;
       end



        result_copy [31:0] = opera2_copy [31:0];
        result_copy [63:32] = 32'h00000000;

        nest = Q2;
      end else begin
      end

Q2: // Multiplication

if(i<32) begin
nest = cust;
i = i+1;

if (i>=0) begin
OPE = result_copy[0];

if( result_copy[0]==1 ) begin
result_copy [63:32] = w1;
result_copy = result_copy >> 1;
end

else if (result_copy[0]==0) begin
result_copy = result_copy >> 1;
end

end

end

else if (i==32) begin
nest = Q3;
valid = 1'b1;
result_not = ~result_copy;
end else begin
valid = 1'b0;

end


Q3: //valid
```

```
if (valid) begin

if (w4==1) begin

result = w12;
nest = Q4;
idle =1;
end else begin
result = result_copy;
end

end


Q4 : // idle state
if (idle)
begin
end

default: nest = Q0;
endcase

Add_rca M3 ( w1, , opera1_copy, D,cin);

endmodule
`timescale 10ns/1ns
module Add_rca64 (sum, c_out, a, b, c_in);
output [63:0] sum;
output c_out;
  input [63:0] a, b;
input c_in;
wire c_in32, c_out;
wire [63:0] sum;
  Add_rca M1 (sum[31:0], c_in32, a[31:0], b[31:0], c_in);
  Add_rca M2 (sum[63:32], c_out, a[63:32], b[63:32], c_in32);
endmodule

`timescale 10ns/1ns
module Add_rca (sum, c_out, a, b, c_in);
output [31:0] sum;
output c_out;
  input [31:0] a, b;
input c_in;
wire c_in4, c_in8, c_in12, c_in16, c_in20, c_in24, c_in28, c_out;
wire [31:0] sum;
  Add_rca_4 M1 (sum[3:0], c_in4, a[3:0], b[3:0], c_in);
  Add_rca_4 M2 (sum[7:4], c_in8, a[7:4], b[7:4], c_in4);
  Add_rca_4 M3 (sum[11:8], c_in12, a[11:8], b[11:8], c_in8);
  Add_rca_4 M4 (sum[15:12], c_in16, a[15:12], b[15:12], c_in12);
  Add_rca_4 M5 (sum[19:16], c_in20, a[19:16], b[19:16], c_in16);
  Add_rca_4 M6 (sum[23:20], c_in24, a[23:20], b[23:20], c_in20);
  Add_rca_4 M7 (sum[27:24], c_in28, a[27:24], b[27:24], c_in24);
  Add_rca_4 M8 (sum[31:28], c_out, a[31:28], b[31:28], c_in28);
endmodule

`timescale 10ns/1ns
module Add_rca_4 (sum, c_out, a, b, c_in);
```

```
  output [3: 0] sum;
output c_out;
  input [3: 0] a, b;
input c_in;
wire [3: 0] sum;
wire c_in2, c_in3, c_in4;
Add_full M1 (sum[0], c_in2, a[0], b[0], c_in);
Add_full M2 (sum[1], c_in3, a[1], b[1], c_in2);
Add_full M3 (sum[2], c_in4, a[2], b[2], c_in3);
Add_full M4 (sum[3], c_out, a[3], b[3], c_in4);
endmodule

`timescale 10ns/1ns
module Add_full (sum, c_out, a, b, c_in);
output sum, c_out;
input a, b, c_in;
wire w1, w2, w3;
Add_half M1 (w1, w2, a, b);
Add_half M2 (sum, w3, w1, c_in);
or M3 (c_out, w2, w3);
endmodule

`timescale 10ns/1ns
module Add_half (sum, c_out, a, b);
output sum, c_out;
input a, b;
xor M1 (sum, a, b);
and M2 (c_out, a, b);
endmodule
```

Test Bench for Multiplier

```
// Code your testbench here

// or browse Examples

`timescale 1 ns/10 ps

//`include "mul.v"
module test_mul();

reg [31:0] opera1;

reg [63:0] opera2;

reg start, clock, muordi, reset;

wire valid;

wire [63:0] result;


mul M1 (result, valid, opera1, opera2, clock, reset, start,  muordi);


initial begin
```

```
$monitor ($time,,"opera1=%b, opera2=%b, start=%b, clock=%b, muordi=%b, reset=%b, valid=%b, result=%b", opera1, opera2, start, clock, muordi, reset, valid, result);
end


initial begin

// clock=0;

muordi = 0;

#20 start = 1;

#20 start =0;

#1500 reset = 1;

#15 reset = 0;

opera1 = -32'h45454545;

opera2 = 64'h1212121212121212;

#20 start = 1;

#20 start =0;

#1500 reset = 1;

#15 reset = 0;

opera1 = 32'h24681357;

opera2 = -64'h5454545454545454;

#20 start = 1;

#20 start =0;

#1500 reset = 1;

#15 reset = 0;

opera1 = 32'h19283746;

opera2 = 64'h5647382956473829;

#20 start = 1;

#20 start =0;

#1500 reset = 1;

#15 reset = 0;

opera1 = -32'h24681012;
```

```
opera2 = -64'h3691215136912151;
#20 start = 1;
#20 start =0;
#2000 $finish;
end


initial begin
$dumpfile("mul.vcd");
$dumpvars(0, test_mul);
end


//clock assigned
initial begin
clock =0;
forever begin
#10 clock=~clock;
end
end
endmodule
```

For 64bit Divider

```
`timescale 10ns/1ns
module div (result, valid, opera1, opera2, clock, reset, start,  muordi);

output [63:0] result;
output valid;

input [31:0] opera1;
input [63:0] opera2;
input  start, reset, muordi, clock;

reg  valid, OPE, w2, w3, w4, idle;
reg [63:0] result, result_copy, result_not, opera2_copy, opera2_not;
reg [31:0] opera1_copy, opera1_copydiv, opera1_not, opera1_copy_not;
wire  reset, start, muordi,cin, cin1a, cin1b, cin2a, cina, carry, w5, w6;
wire [31:0] opera1;
wire [31:0] w1, w10, w13, w9;
wire [31:0] D, A;
wire [63:0] opera2, B, w11, w12;
integer i;

assign carry =1'b0;
assign A = 1'b0;
assign B = 1'b0;


Add_rca M1 ( w10, , opera1_not, A, cin1a);
Add_rca M6 ( w13, , opera1_copy_not, A, cin1b);
Add_rca64 M2 ( w11, , opera2_not, B, cin2a);
Add_rca64 M4 ( w12, , result_not, B, cina);


notif1 A1(cin1a, carry, w2);
bufif0 A2 (cin1a, carry, w2);
notif1 A5(cin2a, carry, w3);
bufif0 A6 (cin2a, carry, w3);
notif0 A3 (cin1b, carry, w2);
bufif1 A4 (cin1b, carry, w2);
notif1 A7(cina, carry, w4);
bufif0 A8 (cina, carry, w4);

always @(opera1) begin
 w2 = opera1 [31];
if (w2 == 1)begin
opera1_not = ~opera1;
opera1_copy_not = opera1;
end else begin
opera1_not = opera1;
opera1_copy_not = ~opera1;
end
end

always @(opera2) begin
w3 = opera2 [63];
if (w3 == 1) begin
```

```
opera2_not = ~opera2;
end else begin
opera2_not = opera2;
end
end

initial begin
valid=0;
end

assign w5 = w2;
assign w6 = w3;

reg [2:0] cust, nest;
parameter Q0 = 3'b000,
          Q1 = 3'b001,
          Q2 = 3'b010,
          Q3 = 3'b011,
          Q4 = 3'b100;


always@(posedge clock or posedge reset)
begin
    if (reset)
    begin
        cust = Q0;
    end
    else
    begin
        if (start)
        begin
               cust = Q1;
        end
        else
        begin
            cust = nest;
        end
    end
end

assign cin=0;
assign D= result_copy [63:32];

always @(posedge clock)
case (cust)
Q0: //reset
     if (reset) begin
      result = 0;
     // opera1_copy = 0;
      //opera2_copy =0;
      valid = 0;
      result_not = 64'h0;
      result_copy = 64'h0;
      //w2 = 0;
      //w3 = 0;
      //w4 = 0;*/
      i = 35;
```

```
      nest = cust;
      end

Q1: // start
        if (muordi == 1'b1) begin

     w4 = w5^w6;
     OPE =1;
     i = 0;
     valid = 0;

     opera1_copy = w10;

     opera1_copydiv = w13;

     opera2_copy = w11;

     result_copy [63:0] = opera2_copy [63:0];
       nest = Q2;
      end


Q2 : // division state
if (i<32) begin
valid= 1'b0;
i =i+1;

   if(OPE==1) begin
    result_copy [63:32] = w9;

if (result_copy[63]==0) begin
result_copy   = result_copy  << 1;
result_copy [0] = 1'b1;
OPE = 1'b1;
end

else if (result_copy[63]==1) begin
result_copy  = result_copy  << 1;
result_copy [0] = 1'b0;
OPE = 1'b0;
end

   end

   else if (OPE==0) begin
   result_copy [63:32] = w1;

if (result_copy[63]==0) begin
result_copy   = result_copy  << 1;
result_copy [0] = 1'b1;
OPE = 1'b1;
end

else if (result_copy[63]==1) begin
result_copy  = result_copy  << 1;
result_copy [0] = 1'b0;
OPE = 1'b0;
```

```
end

   end

 end



else if (i==32) begin
nest = Q3;
valid =1'b1;
i= i+1;


if(OPE==1) begin
result_copy [63:32] = w9;

if (result_copy[63]==0) begin

result_copy [31:0]  = result_copy [31:0] << 1;
result_copy [0] = 1'b1;
OPE = 1'b1;
end

else if (result_copy[63]==1) begin

result_copy [31:0]  = result_copy [31:0] << 1;
result_copy [0] = 1'b0;
OPE = 1'b0;
end

end

else if (OPE==0) begin
result_copy [63:32] = w1;

if (result_copy[63]==0) begin
result_copy [31:0]  = result_copy [31:0] << 1;
result_copy [0] = 1'b1;
OPE = 1'b1;
end

else if (result_copy[63]==1) begin
result_copy [31:0] = result_copy [31:0] << 1;
result_copy [0] = 1'b0;
OPE = 1'b0;
end

end
result_not = ~result_copy;
end


Q3: //valid

if (valid) begin
```

```
if (w4==1) begin

result = w12;
nest = Q4;
idle =1;
end else begin
result = result_copy;
end

end


Q4 : // idle state
if (idle)
begin
end

default: nest = Q0;
endcase

Add_rca M3 ( w1, , opera1_copy, D,cin);
Add_rca M5 ( w9, , opera1_copydiv, D,cin);

endmodule
`timescale 10ns/1ns
module Add_rca64 (sum, c_out, a, b, c_in);
output [63:0] sum;
output c_out;
  input [63:0] a, b;
input c_in;
wire c_in32, c_out;
wire [63:0] sum;
  Add_rca M1 (sum[31:0], c_in32, a[31:0], b[31:0], c_in);
  Add_rca M2 (sum[63:32], c_out, a[63:32], b[63:32], c_in32);
endmodule

`timescale 10ns/1ns
module Add_rca (sum, c_out, a, b, c_in);
output [31:0] sum;
output c_out;
  input [31:0] a, b;
input c_in;
wire c_in4, c_in8, c_in12, c_in16, c_in20, c_in24, c_in28, c_out;
wire [31:0] sum;
  Add_rca_4 M1 (sum[3:0], c_in4, a[3:0], b[3:0], c_in);
  Add_rca_4 M2 (sum[7:4], c_in8, a[7:4], b[7:4], c_in4);
  Add_rca_4 M3 (sum[11:8], c_in12, a[11:8], b[11:8], c_in8);
  Add_rca_4 M4 (sum[15:12], c_in16, a[15:12], b[15:12], c_in12);
  Add_rca_4 M5 (sum[19:16], c_in20, a[19:16], b[19:16], c_in16);
  Add_rca_4 M6 (sum[23:20], c_in24, a[23:20], b[23:20], c_in20);
  Add_rca_4 M7 (sum[27:24], c_in28, a[27:24], b[27:24], c_in24);
  Add_rca_4 M8 (sum[31:28], c_out, a[31:28], b[31:28], c_in28);
endmodule

`timescale 10ns/1ns
module Add_rca_4 (sum, c_out, a, b, c_in);
  output [3: 0] sum;
```

```
output c_out;
  input [3: 0] a, b;
input c_in;
wire [3: 0] sum;
wire c_in2, c_in3, c_in4;
Add_full M1 (sum[0], c_in2, a[0], b[0], c_in);
Add_full M2 (sum[1], c_in3, a[1], b[1], c_in2);
Add_full M3 (sum[2], c_in4, a[2], b[2], c_in3);
Add_full M4 (sum[3], c_out, a[3], b[3], c_in4);
endmodule

`timescale 10ns/1ns
module Add_full (sum, c_out, a, b, c_in);
output sum, c_out;
input a, b, c_in;
wire w1, w2, w3;
Add_half M1 (w1, w2, a, b);
Add_half M2 (sum, w3, w1, c_in);
or M3 (c_out, w2, w3);
endmodule

`timescale 10ns/1ns
module Add_half (sum, c_out, a, b);
output sum, c_out;
input a, b;
xor M1 (sum, a, b);
and M2 (c_out, a, b);
endmodule
```

Test Bench for Divider

```
// Code your testbench here

// or browse Examples

`timescale 1 ns/10 ps

module test_div();

reg [31:0] opera1;

reg [63:0] opera2;

reg start, clock, muordi, reset;

wire valid;

wire [63:0] result;


div M1 (result, valid, opera1, opera2, clock, reset, start,  muordi);


initial begin
```

```
$monitor ($time,,"opera1=%b, opera2=%b, start=%b, clock=%b, muordi=%b,
reset=%b, valid=%b, result=%b", opera1, opera2, start, clock, muordi, reset,
valid, result);
end


initial begin

muordi = 1;

#20 start = 1;

#20 start =0;

#1500 reset = 1;

#15 reset = 0;

opera1 = -32'h45454545;

opera2 =  64'h1212121212121212;

#20 start = 1;

#20 start =0;

#1500 reset = 1;

#15 reset = 0;

opera1 = 32'h12121212;

opera2 = -64'h2323232323232323;

#20 start = 1;

#20 start =0;

#1500 reset = 1;

#15 reset = 0;

opera1 = 32'h54545454;

opera2 = 64'h1234567812345678;

#20 start = 1;

#20 start =0;

#1500 reset = 1;

#15 reset = 0;

opera1 = -32'h34343434;

opera2 = -64'h1432143214231423;
```

```
#20 start = 1;
#20 start =0;
#2000 $finish;
end


initial begin
$dumpfile("div.vcd");
$dumpvars(0, test_div);
end


//clock assigned
initial begin
clock =0;
forever begin
#10 clock=~clock;
end
end
endmodule
```

For 64bit Multiplier and Divider

```
`timescale 10ns/1ns
module muldiv (result, valid, clock, reset, start, opera1, opera2, muordi);

output [63:0] result;
output valid;

input [31:0] opera1;
input [63:0] opera2;
input  start, reset, muordi, clock;

reg  valid, OPE, w2, w3, w4, idle;
reg [63:0] result, result_copy, result_not, opera2_copy, opera2_not;
reg [31:0] opera1_copy, opera1_copydiv, opera1_not, opera1_copy_not;
wire  reset, start, muordi,cin, cin1a, cin1b, cin2a, cina, carry, w5, w6;
wire [31:0] opera1;
wire [31:0] w1, w10, w13, w9;
wire [31:0] D, A;
wire [63:0] opera2, B, w11, w12;
integer i;

assign carry =1'b0;
assign A = 1'b0;
assign B = 1'b0;


Add_rca M1 ( w10, , opera1_not, A, cin1a);
Add_rca M6 ( w13, , opera1_copy_not, A, cin1b);
Add_rca64 M2 ( w11, , opera2_not, B, cin2a);
Add_rca64 M4 ( w12, , result_not, B, cina);


notif1 A1(cin1a, carry, w2);
bufif0 A2 (cin1a, carry, w2);
notif1 A5(cin2a, carry, w3);
bufif0 A6 (cin2a, carry, w3);
notif0 A3 (cin1b, carry, w2);
bufif1 A4 (cin1b, carry, w2);
notif1 A7(cina, carry, w4);
bufif0 A8 (cina, carry, w4);

always @(opera1) begin
 w2 = opera1 [31];
if (w2 == 1)begin
opera1_not = ~opera1;
opera1_copy_not = opera1;
end else begin
opera1_not = opera1;
opera1_copy_not = ~opera1;
end
end

always @(opera2) begin
w3 = opera2 [63];
if (w3 == 1) begin
```

```
opera2_not = ~opera2;
end else begin
opera2_not = opera2;
end
end

initial begin
valid=0;
end

assign w5 = w2;
assign w6 = w3;

reg [2:0] cust, nest;
parameter Q0 = 3'b000,
          Q1 = 3'b001,
          Q2 = 3'b010,
          Q3 = 3'b011,
          Q4 = 3'b100,
          Q5 = 3'b101;

always@(posedge clock or posedge reset)
begin
    if (reset)
    begin
        cust = Q0;
    end
    else
    begin
        if (start)
        begin
               cust = Q1;
        end
        else
        begin
            cust = nest;
        end
    end
end

assign cin=0;
assign D= result_copy [63:32];

always @(posedge clock)
case (cust)
Q0: //reset
     if (reset) begin
      result = 0;
      /*opera1_copy = 0;
      opera2_copy =0;
      valid = 0;
      result_not = 64'h0;
      result_copy = 64'h0;
      w2 = 0;
      w3 = 0;
      w4 = 0;*/
      i = 35;
```

```
      nest = cust;
      end

Q1: // start
        if (muordi == 1'b0) begin
        w4 = w5^w6;
        i = 0;
        valid = 0;

        OPE =0;
        //result_copy = result;
       if (w5==1) begin
       opera1_copy = w10;
       end else begin
       opera1_copy = opera1;
       end

       if (w6==1) begin
       opera2_copy = w11;
       end else begin
       opera2_copy = opera2;
       end



        result_copy [31:0] = opera2_copy [31:0];
        result_copy [63:32] = 32'h00000000;

        nest = Q2;
      end else if (muordi ==1'b1) begin
       // Division
     w4 = w5^w6;
     OPE =1;
     i = 0;
     valid = 0;

     opera1_copy = w10;

     opera1_copydiv = w13;

     opera2_copy = w11;

     result_copy [63:0] = opera2_copy [63:0];
       nest = Q3;
      end

Q2: // Multiplication

if(i<32) begin
nest = cust;
i = i+1;

if (i>=0) begin
OPE = result_copy[0];

if( result_copy[0]==1 ) begin
result_copy [63:32] = w1;
```

```
result_copy = result_copy >> 1;
end

else if (result_copy[0]==0) begin
result_copy = result_copy >> 1;
end

end

end

else if (i==32) begin
nest = Q4;
valid = 1'b1;
result_not = ~result_copy;
end else begin
valid = 1'b0;

end

Q3 : // division state
if (i<32) begin
valid= 1'b0;
i =i+1;

   if(OPE==1) begin
    result_copy [63:32] = w9;

if (result_copy[63]==0) begin
result_copy   = result_copy  << 1;
result_copy [0] = 1'b1;
OPE = 1'b1;
end

else if (result_copy[63]==1) begin
result_copy  = result_copy  << 1;
result_copy [0] = 1'b0;
OPE = 1'b0;
end

   end

   else if (OPE==0) begin
   result_copy [63:32] = w1;

if (result_copy[63]==0) begin
result_copy   = result_copy  << 1;
result_copy [0] = 1'b1;
OPE = 1'b1;
end

else if (result_copy[63]==1) begin
result_copy  = result_copy  << 1;
result_copy [0] = 1'b0;
OPE = 1'b0;
end
```

```
   end

 end



else if (i==32) begin
nest = Q4;
valid =1'b1;
i= i+1;


if(OPE==1) begin
result_copy [63:32] = w9;

if (result_copy[63]==0) begin

result_copy [31:0]  = result_copy [31:0] << 1;
result_copy [0] = 1'b1;
OPE = 1'b1;
end

else if (result_copy[63]==1) begin

result_copy [31:0]  = result_copy [31:0] << 1;
result_copy [0] = 1'b0;
OPE = 1'b0;
end

end

else if (OPE==0) begin
result_copy [63:32] = w1;

if (result_copy[63]==0) begin
result_copy [31:0]  = result_copy [31:0] << 1;
result_copy [0] = 1'b1;
OPE = 1'b1;
end

else if (result_copy[63]==1) begin
result_copy [31:0] = result_copy [31:0] << 1;
result_copy [0] = 1'b0;
OPE = 1'b0;
end

end
result_not = ~result_copy;
end

Q4: //valid

if (valid) begin

if (w4==1) begin

result = w12;
```

```
nest = Q5;
idle =1;
end else begin
result = result_copy;
end

end


Q5 : // idle state
if (idle)
begin
end

default: nest = Q0;
endcase

Add_rca M3 ( w1, , opera1_copy, D,cin);
Add_rca M5 ( w9, , opera1_copydiv, D,cin);

endmodule

`timescale 10ns/1ns
module Add_rca64 (sum, c_out, a, b, c_in);
output [63:0] sum;
output c_out;
  input [63:0] a, b;
input c_in;
wire c_in32, c_out;
wire [63:0] sum;
  Add_rca M1 (sum[31:0], c_in32, a[31:0], b[31:0], c_in);
  Add_rca M2 (sum[63:32], c_out, a[63:32], b[63:32], c_in32);
endmodule

`timescale 10ns/1ns
module Add_rca (sum, c_out, a, b, c_in);
output [31:0] sum;
output c_out;
  input [31:0] a, b;
input c_in;
wire c_in4, c_in8, c_in12, c_in16, c_in20, c_in24, c_in28, c_out;
wire [31:0] sum;
  Add_rca_4 M1 (sum[3:0], c_in4, a[3:0], b[3:0], c_in);
  Add_rca_4 M2 (sum[7:4], c_in8, a[7:4], b[7:4], c_in4);
  Add_rca_4 M3 (sum[11:8], c_in12, a[11:8], b[11:8], c_in8);
  Add_rca_4 M4 (sum[15:12], c_in16, a[15:12], b[15:12], c_in12);
  Add_rca_4 M5 (sum[19:16], c_in20, a[19:16], b[19:16], c_in16);
  Add_rca_4 M6 (sum[23:20], c_in24, a[23:20], b[23:20], c_in20);
  Add_rca_4 M7 (sum[27:24], c_in28, a[27:24], b[27:24], c_in24);
  Add_rca_4 M8 (sum[31:28], c_out, a[31:28], b[31:28], c_in28);
endmodule

`timescale 10ns/1ns
module Add_rca_4 (sum, c_out, a, b, c_in);
  output [3: 0] sum;
output c_out;
  input [3: 0] a, b;
```

```
input c_in;
wire [3: 0] sum;
wire c_in2, c_in3, c_in4;
Add_full M1 (sum[0], c_in2, a[0], b[0], c_in);
Add_full M2 (sum[1], c_in3, a[1], b[1], c_in2);
Add_full M3 (sum[2], c_in4, a[2], b[2], c_in3);
Add_full M4 (sum[3], c_out, a[3], b[3], c_in4);
endmodule

`timescale 10ns/1ns
module Add_full (sum, c_out, a, b, c_in);
output sum, c_out;
input a, b, c_in;
wire w1, w2, w3;
Add_half M1 (w1, w2, a, b);
Add_half M2 (sum, w3, w1, c_in);
or M3 (c_out, w2, w3);
endmodule

`timescale 10ns/1ns
module Add_half (sum, c_out, a, b);
output sum, c_out;
input a, b;
xor M1 (sum, a, b);
and M2 (c_out, a, b);
endmodule
```

Test Bench for 64 bit Multiplier and Divider

```
// Code your testbench here

// or browse Examples

`timescale 1 ns/10 ps

`include "muldiv.v"

module test_muldiv();

reg [31:0] opera1;

reg [63:0] opera2;

reg start, clock, muordi, reset;

wire valid;

wire [63:0] result;


muldiv M1 (result, valid, opera1, opera2, clock, reset, start,  muordi);


initial begin
```

```
$monitor ($time,,"opera1=%b, opera2=%b, start=%b, clock=%b, muordi=%b,
reset=%b, valid=%b, result=%b", opera1, opera2, start, clock, muordi, reset,
valid, result);
end


initial begin
//MUL

muordi = 0;

#20 start = 1;

#20 start =0;

#1500 reset = 1;

#15 reset = 0;

opera1 = -32'h45454545;

opera2 = 64'h1212121212121212;

#20 start = 1;

#20 start =0;

#1500 reset = 1;

#15 reset = 0;

opera1 = 32'h24681357;

opera2 = -64'h5454545454545454;

#20 start = 1;

#20 start =0;

#1500 reset = 1;

#15 reset = 0;

opera1 = 32'h19283746;

opera2 = 64'h5647382956473829;

#20 start = 1;

#20 start =0;

#1500 reset = 1;

#15 reset = 0;

opera1 = -32'h24681012;
```

```
opera2 = -64'h3691215136912151;
#20 start = 1;
#20 start =0;
#1500 reset = 1;
#15 reset = 0;
//DIV
muordi = 1;
#20 start = 1;
#20 start =0;
#1500 reset = 1;
#15 reset = 0;
opera1 = -32'h45454545;
opera2 =  64'h1212121212121212;
#20 start = 1;
#20 start =0;
#1500 reset = 1;
#15 reset = 0;
opera1 = 32'h12121212;
opera2 = -64'h2323232323232323;
#20 start = 1;
#20 start =0;
#1500 reset = 1;
#15 reset = 0;
opera1 = 32'h54545454;
opera2 = 64'h1234567812345678;
#20 start = 1;
#20 start =0;
#1500 reset = 1;
#15 reset = 0;
```

```
opera1 = -32'h34343434;
opera2 = -64'h1432143214231423;
#20 start = 1;
#20 start =0;
#5000 $finish;
end


initial begin
$dumpfile("muldiv.vcd");
$dumpvars(0, test_muldiv);
end


//clock assigned
initial begin
clock =0;
forever begin
#10 clock=~clock;
end
end
endmodule
```

Appendix C
Reports and Circuits from EDA Tools

C.1 Contents of Selected Reports from RTL (Pre-synthesis) Simulations (VCS or NCVERILOG)

For Multiplier

```
Chronologic VCS simulator copyright 1991-2014
Contains Synopsys proprietary information.
Compiler version I-2014.03-2; Runtime version I-2014.03-2;  Dec 11 08:57 2016
                   0 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=x,
clock=0, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                  10 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=x,
clock=1, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                  20 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=1,
clock=0, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                  30 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=1,
clock=1, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                  40 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                  50 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                  60 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                  70 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                  80 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                  90 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                 100 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                 110 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                 120 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                 130 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                 140 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                 150 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                 160 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                 170 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                 180 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                 190 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                 200 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                 210 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
```

```
                220 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                230 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                240 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                250 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                260 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                270 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                280 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                290 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                300 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                310 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                320 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                330 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                340 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                350 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                360 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                370 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                380 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                390 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                400 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                410 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                420 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                430 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                440 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                450 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                460 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                470 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                480 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                490 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
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                500 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                510 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                520 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                530 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                540 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                550 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                560 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                570 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                580 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                590 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                600 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                610 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                620 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                630 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                640 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                650 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                660 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                670 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                680 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=0, result=xxxxxxxxxxxxxxx
                690 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=1, result=xxxxxxxxxxxxxxx
                700 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=1, result=xxxxxxxxxxxxxxx
                710 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=1, result=00000000xxxxxxx
                720 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=1, result=00000000xxxxxxx
                730 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=1, result=00000000xxxxxxx
                740 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=1, result=00000000xxxxxxx
                750 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=1, result=00000000xxxxxxx
                760 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=1, result=00000000xxxxxxx
                770 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=1, result=00000000xxxxxxx
```

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                780 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=1, result=00000000xxxxxxxx
                790 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=1, result=00000000xxxxxxxx
                800 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=1, result=00000000xxxxxxxx
                810 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=1, result=00000000xxxxxxxx
                820 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=1, result=00000000xxxxxxxx
                830 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=1, result=00000000xxxxxxxx
                840 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=1, result=00000000xxxxxxxx
                850 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=1, result=00000000xxxxxxxx
                860 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=1, result=00000000xxxxxxxx
                870 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=1, result=00000000xxxxxxxx
                880 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=1, result=00000000xxxxxxxx
                890 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=1, result=00000000xxxxxxxx
                900 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=1, result=00000000xxxxxxxx
                910 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=1, result=00000000xxxxxxxx
                920 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=1, result=00000000xxxxxxxx
                930 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=1, result=00000000xxxxxxxx
                940 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=1, result=00000000xxxxxxxx
                950 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=1, result=00000000xxxxxxxx
                960 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=1, result=00000000xxxxxxxx
                970 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=1, result=00000000xxxxxxxx
                980 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=1, result=00000000xxxxxxxx
                990 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=1, result=00000000xxxxxxxx
               1000 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=1, result=00000000xxxxxxxx
               1010 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=1, muordi=0, reset=x, valid=1, result=00000000xxxxxxxx
               1020 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=0,
clock=0, muordi=0, reset=x, valid=1, result=00000000xxxxxxxx
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                8110 opera1=db97efee, opera2=c96edeaec96edeaf, start=0,
clock=1, muordi=0, reset=0, valid=1, result=07c29711d53167b2
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clock=0, muordi=0, reset=0, valid=1, result=07c29711d53167b2
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clock=0, muordi=0, reset=0, valid=1, result=07c29711d53167b2
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clock=1, muordi=0, reset=0, valid=1, result=07c29711d53167b2
$finish called from file "testmul.v", line 87.
```

```
$finish at simulation time                82600
           V C S   S i m u l a t i o n   R e p o r t
Time: 82600 ns
CPU Time:      0.220 seconds;       Data structure size:   0.0Mb
Sun Dec 11 08:57:21 2016
```

For Divider

```
Chronologic VCS simulator copyright 1991-2014
Contains Synopsys proprietary information.
Compiler version I-2014.03-2; Runtime version I-2014.03-2;  Dec 11 09:03 2016
                   0 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxx, start=x,
clock=0, muordi=1, reset=x, valid=0, result=xxxxxxxxxxxxxxx
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                7140 opera1=cbcbcbcc, opera2=ebcdebcdebdcebdd, start=0,
clock=0, muordi=1, reset=0, valid=1, result=2a572a576309457f
```

```
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clock=1, muordi=1, reset=0, valid=1, result=2a572a576309457f
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clock=0, muordi=1, reset=0, valid=1, result=2a572a576309457f
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clock=1, muordi=1, reset=0, valid=1, result=2a572a576309457f
                7180 opera1=cbcbcbcc, opera2=ebcdebcdebdcebdd, start=0,
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                7200 opera1=cbcbcbcc, opera2=ebcdebcdebdcebdd, start=0,
clock=0, muordi=1, reset=0, valid=1, result=2a572a576309457f
                7210 opera1=cbcbcbcc, opera2=ebcdebcdebdcebdd, start=0,
clock=1, muordi=1, reset=0, valid=1, result=2a572a576309457f
                7220 opera1=cbcbcbcc, opera2=ebcdebcdebdcebdd, start=0,
clock=0, muordi=1, reset=0, valid=1, result=2a572a576309457f
                7230 opera1=cbcbcbcc, opera2=ebcdebcdebdcebdd, start=0,
clock=1, muordi=1, reset=0, valid=1, result=2a572a576309457f
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clock=0, muordi=1, reset=0, valid=1, result=2a572a576309457f
                7310 opera1=cbcbcbcc, opera2=ebcdebcdebdcebdd, start=0,
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clock=0, muordi=1, reset=0, valid=1, result=2a572a576309457f
```

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clock=1, muordi=1, reset=0, valid=1, result=2a572a576309457f
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clock=1, muordi=1, reset=0, valid=1, result=2a572a576309457f
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clock=0, muordi=1, reset=0, valid=1, result=2a572a576309457f
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clock=1, muordi=1, reset=0, valid=1, result=2a572a576309457f
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```

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                7740 opera1=cbcbcbcc, opera2=ebcdebcdebdcebdd, start=0,
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clock=1, muordi=1, reset=0, valid=1, result=2a572a576309457f
                7760 opera1=cbcbcbcc, opera2=ebcdebcdebdcebdd, start=0,
clock=0, muordi=1, reset=0, valid=1, result=2a572a576309457f
                7770 opera1=cbcbcbcc, opera2=ebcdebcdebdcebdd, start=0,
clock=1, muordi=1, reset=0, valid=1, result=2a572a576309457f
                7780 opera1=cbcbcbcc, opera2=ebcdebcdebdcebdd, start=0,
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clock=0, muordi=1, reset=0, valid=1, result=2a572a576309457f
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clock=0, muordi=1, reset=0, valid=1, result=2a572a576309457f
                7970 opera1=cbcbcbcc, opera2=ebcdebcdebdcebdd, start=0,
clock=1, muordi=1, reset=0, valid=1, result=2a572a576309457f
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clock=0, muordi=1, reset=0, valid=1, result=2a572a576309457f
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clock=1, muordi=1, reset=0, valid=1, result=2a572a576309457f
$finish called from file "testdiv.v", line 86.
$finish at simulation time                82600
           V C S   S i m u l a t i o n   R e p o r t
```

```
Time: 82600 ns
CPU Time:      0.220 seconds;       Data structure size:   0.0Mb
Sun Dec 11 09:03:22 2016
```

C.2 Contents of Selected Reports from Netlist (Post-synthesis) Simulations (VCS or NCVERILOG)

For Multiplier

```
ncverilog: 14.10-p001: (c) Copyright 1995-2014 Cadence Design Systems,
Inc.
file: testmul.v
      module worklib.test_mul:v
            errors: 0, warnings: 0
file: mul_netlist.v
      module worklib.Add_half_0:v
            errors: 0, warnings: 0
      module worklib.Add_half_383:v
            errors: 0, warnings: 0
      module worklib.Add_full_0:v
            errors: 0, warnings: 0
      module worklib.Add_half_382:v
            errors: 0, warnings: 0
      module worklib.Add_half_381:v
            errors: 0, warnings: 0
      module worklib.Add_full_191:v
            errors: 0, warnings: 0
      module worklib.Add_half_380:v
            errors: 0, warnings: 0
      module worklib.Add_half_379:v
            errors: 0, warnings: 0
      module worklib.Add_full_190:v
            errors: 0, warnings: 0
      module worklib.Add_half_378:v
            errors: 0, warnings: 0
      module worklib.Add_half_377:v
            errors: 0, warnings: 0
      module worklib.Add_full_189:v
            errors: 0, warnings: 0
      module worklib.Add_rca_4_0:v
            errors: 0, warnings: 0
      module worklib.Add_half_376:v
            errors: 0, warnings: 0
      module worklib.Add_half_375:v
            errors: 0, warnings: 0
      module worklib.Add_full_188:v
            errors: 0, warnings: 0
      module worklib.Add_half_374:v
            errors: 0, warnings: 0
      module worklib.Add_half_373:v
            errors: 0, warnings: 0
      module worklib.Add_full_187:v
            errors: 0, warnings: 0
      module worklib.Add_half_372:v
```

```
      errors: 0, warnings: 0
module worklib.Add_half_371:v
      errors: 0, warnings: 0
module worklib.Add_full_186:v
      errors: 0, warnings: 0
module worklib.Add_half_370:v
      errors: 0, warnings: 0
module worklib.Add_half_369:v
      errors: 0, warnings: 0
module worklib.Add_full_185:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_47:v
      errors: 0, warnings: 0
module worklib.Add_half_368:v
      errors: 0, warnings: 0
module worklib.Add_half_367:v
      errors: 0, warnings: 0
module worklib.Add_full_184:v
      errors: 0, warnings: 0
module worklib.Add_half_366:v
      errors: 0, warnings: 0
module worklib.Add_half_365:v
      errors: 0, warnings: 0
module worklib.Add_full_183:v
      errors: 0, warnings: 0
module worklib.Add_half_364:v
      errors: 0, warnings: 0
module worklib.Add_half_363:v
      errors: 0, warnings: 0
module worklib.Add_full_182:v
      errors: 0, warnings: 0
module worklib.Add_half_362:v
      errors: 0, warnings: 0
module worklib.Add_half_361:v
      errors: 0, warnings: 0
module worklib.Add_full_181:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_46:v
      errors: 0, warnings: 0
module worklib.Add_half_360:v
      errors: 0, warnings: 0
module worklib.Add_half_359:v
      errors: 0, warnings: 0
module worklib.Add_full_180:v
      errors: 0, warnings: 0
module worklib.Add_half_358:v
      errors: 0, warnings: 0
module worklib.Add_half_357:v
      errors: 0, warnings: 0
module worklib.Add_full_179:v
      errors: 0, warnings: 0
module worklib.Add_half_356:v
```

```
      errors: 0, warnings: 0
module worklib.Add_half_355:v
      errors: 0, warnings: 0
module worklib.Add_full_178:v
      errors: 0, warnings: 0
module worklib.Add_half_354:v
      errors: 0, warnings: 0
module worklib.Add_half_353:v
      errors: 0, warnings: 0
module worklib.Add_full_177:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_45:v
      errors: 0, warnings: 0
module worklib.Add_half_352:v
      errors: 0, warnings: 0
module worklib.Add_half_351:v
      errors: 0, warnings: 0
module worklib.Add_full_176:v
      errors: 0, warnings: 0
module worklib.Add_half_350:v
      errors: 0, warnings: 0
module worklib.Add_half_349:v
      errors: 0, warnings: 0
module worklib.Add_full_175:v
      errors: 0, warnings: 0
module worklib.Add_half_348:v
      errors: 0, warnings: 0
module worklib.Add_half_347:v
      errors: 0, warnings: 0
module worklib.Add_full_174:v
      errors: 0, warnings: 0
module worklib.Add_half_346:v
      errors: 0, warnings: 0
module worklib.Add_half_345:v
      errors: 0, warnings: 0
module worklib.Add_full_173:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_44:v
      errors: 0, warnings: 0
module worklib.Add_half_344:v
      errors: 0, warnings: 0
module worklib.Add_half_343:v
      errors: 0, warnings: 0
module worklib.Add_full_172:v
      errors: 0, warnings: 0
module worklib.Add_half_342:v
      errors: 0, warnings: 0
module worklib.Add_half_341:v
      errors: 0, warnings: 0
module worklib.Add_full_171:v
      errors: 0, warnings: 0
module worklib.Add_half_340:v
```

```
      errors: 0, warnings: 0
module worklib.Add_half_339:v
      errors: 0, warnings: 0
module worklib.Add_full_170:v
      errors: 0, warnings: 0
module worklib.Add_half_338:v
      errors: 0, warnings: 0
module worklib.Add_half_337:v
      errors: 0, warnings: 0
module worklib.Add_full_169:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_43:v
      errors: 0, warnings: 0
module worklib.Add_half_336:v
      errors: 0, warnings: 0
module worklib.Add_half_335:v
      errors: 0, warnings: 0
module worklib.Add_full_168:v
      errors: 0, warnings: 0
module worklib.Add_half_334:v
      errors: 0, warnings: 0
module worklib.Add_half_333:v
      errors: 0, warnings: 0
module worklib.Add_full_167:v
      errors: 0, warnings: 0
module worklib.Add_half_332:v
      errors: 0, warnings: 0
module worklib.Add_half_331:v
      errors: 0, warnings: 0
module worklib.Add_full_166:v
      errors: 0, warnings: 0
module worklib.Add_half_330:v
      errors: 0, warnings: 0
module worklib.Add_half_329:v
      errors: 0, warnings: 0
module worklib.Add_full_165:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_42:v
      errors: 0, warnings: 0
module worklib.Add_half_328:v
      errors: 0, warnings: 0
module worklib.Add_half_327:v
      errors: 0, warnings: 0
module worklib.Add_full_164:v
      errors: 0, warnings: 0
module worklib.Add_half_326:v
      errors: 0, warnings: 0
module worklib.Add_half_325:v
      errors: 0, warnings: 0
module worklib.Add_full_163:v
      errors: 0, warnings: 0
module worklib.Add_half_324:v
```

```
      errors: 0, warnings: 0
module worklib.Add_half_323:v
      errors: 0, warnings: 0
module worklib.Add_full_162:v
      errors: 0, warnings: 0
module worklib.Add_half_322:v
      errors: 0, warnings: 0
module worklib.Add_half_321:v
      errors: 0, warnings: 0
module worklib.Add_full_161:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_41:v
      errors: 0, warnings: 0
module worklib.Add_rca_0:v
      errors: 0, warnings: 0
module worklib.Add_half_256:v
      errors: 0, warnings: 0
module worklib.Add_half_255:v
      errors: 0, warnings: 0
module worklib.Add_full_128:v
      errors: 0, warnings: 0
module worklib.Add_half_254:v
      errors: 0, warnings: 0
module worklib.Add_half_253:v
      errors: 0, warnings: 0
module worklib.Add_full_127:v
      errors: 0, warnings: 0
module worklib.Add_half_252:v
      errors: 0, warnings: 0
module worklib.Add_half_251:v
      errors: 0, warnings: 0
module worklib.Add_full_126:v
      errors: 0, warnings: 0
module worklib.Add_half_250:v
      errors: 0, warnings: 0
module worklib.Add_half_249:v
      errors: 0, warnings: 0
module worklib.Add_full_125:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_32:v
      errors: 0, warnings: 0
module worklib.Add_half_248:v
      errors: 0, warnings: 0
module worklib.Add_half_247:v
      errors: 0, warnings: 0
module worklib.Add_full_124:v
      errors: 0, warnings: 0
module worklib.Add_half_246:v
      errors: 0, warnings: 0
module worklib.Add_half_245:v
      errors: 0, warnings: 0
module worklib.Add_full_123:v
```

```
      errors: 0, warnings: 0
module worklib.Add_half_244:v
      errors: 0, warnings: 0
module worklib.Add_half_243:v
      errors: 0, warnings: 0
module worklib.Add_full_122:v
      errors: 0, warnings: 0
module worklib.Add_half_242:v
      errors: 0, warnings: 0
module worklib.Add_half_241:v
      errors: 0, warnings: 0
module worklib.Add_full_121:v
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module worklib.Add_rca_4_31:v
      errors: 0, warnings: 0
module worklib.Add_half_240:v
      errors: 0, warnings: 0
module worklib.Add_half_239:v
      errors: 0, warnings: 0
module worklib.Add_full_120:v
      errors: 0, warnings: 0
module worklib.Add_half_238:v
      errors: 0, warnings: 0
module worklib.Add_half_237:v
      errors: 0, warnings: 0
module worklib.Add_full_119:v
      errors: 0, warnings: 0
module worklib.Add_half_236:v
      errors: 0, warnings: 0
module worklib.Add_half_235:v
      errors: 0, warnings: 0
module worklib.Add_full_118:v
      errors: 0, warnings: 0
module worklib.Add_half_234:v
      errors: 0, warnings: 0
module worklib.Add_half_233:v
      errors: 0, warnings: 0
module worklib.Add_full_117:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_30:v
      errors: 0, warnings: 0
module worklib.Add_half_232:v
      errors: 0, warnings: 0
module worklib.Add_half_231:v
      errors: 0, warnings: 0
module worklib.Add_full_116:v
      errors: 0, warnings: 0
module worklib.Add_half_230:v
      errors: 0, warnings: 0
module worklib.Add_half_229:v
      errors: 0, warnings: 0
module worklib.Add_full_115:v
```

```
      errors: 0, warnings: 0
module worklib.Add_half_228:v
      errors: 0, warnings: 0
module worklib.Add_half_227:v
      errors: 0, warnings: 0
module worklib.Add_full_114:v
      errors: 0, warnings: 0
module worklib.Add_half_226:v
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module worklib.Add_half_225:v
      errors: 0, warnings: 0
module worklib.Add_full_113:v
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module worklib.Add_rca_4_29:v
      errors: 0, warnings: 0
module worklib.Add_half_224:v
      errors: 0, warnings: 0
module worklib.Add_half_223:v
      errors: 0, warnings: 0
module worklib.Add_full_112:v
      errors: 0, warnings: 0
module worklib.Add_half_222:v
      errors: 0, warnings: 0
module worklib.Add_half_221:v
      errors: 0, warnings: 0
module worklib.Add_full_111:v
      errors: 0, warnings: 0
module worklib.Add_half_220:v
      errors: 0, warnings: 0
module worklib.Add_half_219:v
      errors: 0, warnings: 0
module worklib.Add_full_110:v
      errors: 0, warnings: 0
module worklib.Add_half_218:v
      errors: 0, warnings: 0
module worklib.Add_half_217:v
      errors: 0, warnings: 0
module worklib.Add_full_109:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_28:v
      errors: 0, warnings: 0
module worklib.Add_half_216:v
      errors: 0, warnings: 0
module worklib.Add_half_215:v
      errors: 0, warnings: 0
module worklib.Add_full_108:v
      errors: 0, warnings: 0
module worklib.Add_half_214:v
      errors: 0, warnings: 0
module worklib.Add_half_213:v
      errors: 0, warnings: 0
module worklib.Add_full_107:v
```

```
      errors: 0, warnings: 0
module worklib.Add_half_212:v
      errors: 0, warnings: 0
module worklib.Add_half_211:v
      errors: 0, warnings: 0
module worklib.Add_full_106:v
      errors: 0, warnings: 0
module worklib.Add_half_210:v
      errors: 0, warnings: 0
module worklib.Add_half_209:v
      errors: 0, warnings: 0
module worklib.Add_full_105:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_27:v
      errors: 0, warnings: 0
module worklib.Add_half_208:v
      errors: 0, warnings: 0
module worklib.Add_half_207:v
      errors: 0, warnings: 0
module worklib.Add_full_104:v
      errors: 0, warnings: 0
module worklib.Add_half_206:v
      errors: 0, warnings: 0
module worklib.Add_half_205:v
      errors: 0, warnings: 0
module worklib.Add_full_103:v
      errors: 0, warnings: 0
module worklib.Add_half_204:v
      errors: 0, warnings: 0
module worklib.Add_half_203:v
      errors: 0, warnings: 0
module worklib.Add_full_102:v
      errors: 0, warnings: 0
module worklib.Add_half_202:v
      errors: 0, warnings: 0
module worklib.Add_half_201:v
      errors: 0, warnings: 0
module worklib.Add_full_101:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_26:v
      errors: 0, warnings: 0
module worklib.Add_half_200:v
      errors: 0, warnings: 0
module worklib.Add_half_199:v
      errors: 0, warnings: 0
module worklib.Add_full_100:v
      errors: 0, warnings: 0
module worklib.Add_half_198:v
      errors: 0, warnings: 0
module worklib.Add_half_197:v
      errors: 0, warnings: 0
module worklib.Add_full_99:v
```

```
      errors: 0, warnings: 0
module worklib.Add_half_196:v
      errors: 0, warnings: 0
module worklib.Add_half_195:v
      errors: 0, warnings: 0
module worklib.Add_full_98:v
      errors: 0, warnings: 0
module worklib.Add_half_194:v
      errors: 0, warnings: 0
module worklib.Add_half_193:v
      errors: 0, warnings: 0
module worklib.Add_full_97:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_25:v
      errors: 0, warnings: 0
module worklib.Add_rca_4:v
      errors: 0, warnings: 0
module worklib.Add_half_192:v
      errors: 0, warnings: 0
module worklib.Add_half_191:v
      errors: 0, warnings: 0
module worklib.Add_full_96:v
      errors: 0, warnings: 0
module worklib.Add_half_190:v
      errors: 0, warnings: 0
module worklib.Add_half_189:v
      errors: 0, warnings: 0
module worklib.Add_full_95:v
      errors: 0, warnings: 0
module worklib.Add_half_188:v
      errors: 0, warnings: 0
module worklib.Add_half_187:v
      errors: 0, warnings: 0
module worklib.Add_full_94:v
      errors: 0, warnings: 0
module worklib.Add_half_186:v
      errors: 0, warnings: 0
module worklib.Add_half_185:v
      errors: 0, warnings: 0
module worklib.Add_full_93:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_24:v
      errors: 0, warnings: 0
module worklib.Add_half_184:v
      errors: 0, warnings: 0
module worklib.Add_half_183:v
      errors: 0, warnings: 0
module worklib.Add_full_92:v
      errors: 0, warnings: 0
module worklib.Add_half_182:v
      errors: 0, warnings: 0
module worklib.Add_half_181:v
```

```
      errors: 0, warnings: 0
module worklib.Add_full_91:v
      errors: 0, warnings: 0
module worklib.Add_half_180:v
      errors: 0, warnings: 0
module worklib.Add_half_179:v
      errors: 0, warnings: 0
module worklib.Add_full_90:v
      errors: 0, warnings: 0
module worklib.Add_half_178:v
      errors: 0, warnings: 0
module worklib.Add_half_177:v
      errors: 0, warnings: 0
module worklib.Add_full_89:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_23:v
      errors: 0, warnings: 0
module worklib.Add_half_176:v
      errors: 0, warnings: 0
module worklib.Add_half_175:v
      errors: 0, warnings: 0
module worklib.Add_full_88:v
      errors: 0, warnings: 0
module worklib.Add_half_174:v
      errors: 0, warnings: 0
module worklib.Add_half_173:v
      errors: 0, warnings: 0
module worklib.Add_full_87:v
      errors: 0, warnings: 0
module worklib.Add_half_172:v
      errors: 0, warnings: 0
module worklib.Add_half_171:v
      errors: 0, warnings: 0
module worklib.Add_full_86:v
      errors: 0, warnings: 0
module worklib.Add_half_170:v
      errors: 0, warnings: 0
module worklib.Add_half_169:v
      errors: 0, warnings: 0
module worklib.Add_full_85:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_22:v
      errors: 0, warnings: 0
module worklib.Add_half_168:v
      errors: 0, warnings: 0
module worklib.Add_half_167:v
      errors: 0, warnings: 0
module worklib.Add_full_84:v
      errors: 0, warnings: 0
module worklib.Add_half_166:v
      errors: 0, warnings: 0
module worklib.Add_half_165:v
```

```
      errors: 0, warnings: 0
module worklib.Add_full_83:v
      errors: 0, warnings: 0
module worklib.Add_half_164:v
      errors: 0, warnings: 0
module worklib.Add_half_163:v
      errors: 0, warnings: 0
module worklib.Add_full_82:v
      errors: 0, warnings: 0
module worklib.Add_half_162:v
      errors: 0, warnings: 0
module worklib.Add_half_161:v
      errors: 0, warnings: 0
module worklib.Add_full_81:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_21:v
      errors: 0, warnings: 0
module worklib.Add_half_160:v
      errors: 0, warnings: 0
module worklib.Add_half_159:v
      errors: 0, warnings: 0
module worklib.Add_full_80:v
      errors: 0, warnings: 0
module worklib.Add_half_158:v
      errors: 0, warnings: 0
module worklib.Add_half_157:v
      errors: 0, warnings: 0
module worklib.Add_full_79:v
      errors: 0, warnings: 0
module worklib.Add_half_156:v
      errors: 0, warnings: 0
module worklib.Add_half_155:v
      errors: 0, warnings: 0
module worklib.Add_full_78:v
      errors: 0, warnings: 0
module worklib.Add_half_154:v
      errors: 0, warnings: 0
module worklib.Add_half_153:v
      errors: 0, warnings: 0
module worklib.Add_full_77:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_20:v
      errors: 0, warnings: 0
module worklib.Add_half_152:v
      errors: 0, warnings: 0
module worklib.Add_half_151:v
      errors: 0, warnings: 0
module worklib.Add_full_76:v
      errors: 0, warnings: 0
module worklib.Add_half_150:v
      errors: 0, warnings: 0
module worklib.Add_half_149:v
```

```
      errors: 0, warnings: 0
module worklib.Add_full_75:v
      errors: 0, warnings: 0
module worklib.Add_half_148:v
      errors: 0, warnings: 0
module worklib.Add_half_147:v
      errors: 0, warnings: 0
module worklib.Add_full_74:v
      errors: 0, warnings: 0
module worklib.Add_half_146:v
      errors: 0, warnings: 0
module worklib.Add_half_145:v
      errors: 0, warnings: 0
module worklib.Add_full_73:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_19:v
      errors: 0, warnings: 0
module worklib.Add_half_144:v
      errors: 0, warnings: 0
module worklib.Add_half_143:v
      errors: 0, warnings: 0
module worklib.Add_full_72:v
      errors: 0, warnings: 0
module worklib.Add_half_142:v
      errors: 0, warnings: 0
module worklib.Add_half_141:v
      errors: 0, warnings: 0
module worklib.Add_full_71:v
      errors: 0, warnings: 0
module worklib.Add_half_140:v
      errors: 0, warnings: 0
module worklib.Add_half_139:v
      errors: 0, warnings: 0
module worklib.Add_full_70:v
      errors: 0, warnings: 0
module worklib.Add_half_138:v
      errors: 0, warnings: 0
module worklib.Add_half_137:v
      errors: 0, warnings: 0
module worklib.Add_full_69:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_18:v
      errors: 0, warnings: 0
module worklib.Add_half_136:v
      errors: 0, warnings: 0
module worklib.Add_half_135:v
      errors: 0, warnings: 0
module worklib.Add_full_68:v
      errors: 0, warnings: 0
module worklib.Add_half_134:v
      errors: 0, warnings: 0
module worklib.Add_half_133:v
```

```
      errors: 0, warnings: 0
module worklib.Add_full_67:v
      errors: 0, warnings: 0
module worklib.Add_half_132:v
      errors: 0, warnings: 0
module worklib.Add_half_131:v
      errors: 0, warnings: 0
module worklib.Add_full_66:v
      errors: 0, warnings: 0
module worklib.Add_half_130:v
      errors: 0, warnings: 0
module worklib.Add_half_129:v
      errors: 0, warnings: 0
module worklib.Add_full_65:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_17:v
      errors: 0, warnings: 0
module worklib.Add_rca_3:v
      errors: 0, warnings: 0
module worklib.Add_rca64_0:v
      errors: 0, warnings: 0
module worklib.Add_half_128:v
      errors: 0, warnings: 0
module worklib.Add_half_127:v
      errors: 0, warnings: 0
module worklib.Add_full_64:v
      errors: 0, warnings: 0
module worklib.Add_half_126:v
      errors: 0, warnings: 0
module worklib.Add_half_125:v
      errors: 0, warnings: 0
module worklib.Add_full_63:v
      errors: 0, warnings: 0
module worklib.Add_half_124:v
      errors: 0, warnings: 0
module worklib.Add_half_123:v
      errors: 0, warnings: 0
module worklib.Add_full_62:v
      errors: 0, warnings: 0
module worklib.Add_half_122:v
      errors: 0, warnings: 0
module worklib.Add_half_121:v
      errors: 0, warnings: 0
module worklib.Add_full_61:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_16:v
      errors: 0, warnings: 0
module worklib.Add_half_120:v
      errors: 0, warnings: 0
module worklib.Add_half_119:v
      errors: 0, warnings: 0
module worklib.Add_full_60:v
```

```
      errors: 0, warnings: 0
module worklib.Add_half_118:v
      errors: 0, warnings: 0
module worklib.Add_half_117:v
      errors: 0, warnings: 0
module worklib.Add_full_59:v
      errors: 0, warnings: 0
module worklib.Add_half_116:v
      errors: 0, warnings: 0
module worklib.Add_half_115:v
      errors: 0, warnings: 0
module worklib.Add_full_58:v
      errors: 0, warnings: 0
module worklib.Add_half_114:v
      errors: 0, warnings: 0
module worklib.Add_half_113:v
      errors: 0, warnings: 0
module worklib.Add_full_57:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_15:v
      errors: 0, warnings: 0
module worklib.Add_half_112:v
      errors: 0, warnings: 0
module worklib.Add_half_111:v
      errors: 0, warnings: 0
module worklib.Add_full_56:v
      errors: 0, warnings: 0
module worklib.Add_half_110:v
      errors: 0, warnings: 0
module worklib.Add_half_109:v
      errors: 0, warnings: 0
module worklib.Add_full_55:v
      errors: 0, warnings: 0
module worklib.Add_half_108:v
      errors: 0, warnings: 0
module worklib.Add_half_107:v
      errors: 0, warnings: 0
module worklib.Add_full_54:v
      errors: 0, warnings: 0
module worklib.Add_half_106:v
      errors: 0, warnings: 0
module worklib.Add_half_105:v
      errors: 0, warnings: 0
module worklib.Add_full_53:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_14:v
      errors: 0, warnings: 0
module worklib.Add_half_104:v
      errors: 0, warnings: 0
module worklib.Add_half_103:v
      errors: 0, warnings: 0
module worklib.Add_full_52:v
```

```
      errors: 0, warnings: 0
module worklib.Add_half_102:v
      errors: 0, warnings: 0
module worklib.Add_half_101:v
      errors: 0, warnings: 0
module worklib.Add_full_51:v
      errors: 0, warnings: 0
module worklib.Add_half_100:v
      errors: 0, warnings: 0
module worklib.Add_half_99:v
      errors: 0, warnings: 0
module worklib.Add_full_50:v
      errors: 0, warnings: 0
module worklib.Add_half_98:v
      errors: 0, warnings: 0
module worklib.Add_half_97:v
      errors: 0, warnings: 0
module worklib.Add_full_49:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_13:v
      errors: 0, warnings: 0
module worklib.Add_half_96:v
      errors: 0, warnings: 0
module worklib.Add_half_95:v
      errors: 0, warnings: 0
module worklib.Add_full_48:v
      errors: 0, warnings: 0
module worklib.Add_half_94:v
      errors: 0, warnings: 0
module worklib.Add_half_93:v
      errors: 0, warnings: 0
module worklib.Add_full_47:v
      errors: 0, warnings: 0
module worklib.Add_half_92:v
      errors: 0, warnings: 0
module worklib.Add_half_91:v
      errors: 0, warnings: 0
module worklib.Add_full_46:v
      errors: 0, warnings: 0
module worklib.Add_half_90:v
      errors: 0, warnings: 0
module worklib.Add_half_89:v
      errors: 0, warnings: 0
module worklib.Add_full_45:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_12:v
      errors: 0, warnings: 0
module worklib.Add_half_88:v
      errors: 0, warnings: 0
module worklib.Add_half_87:v
      errors: 0, warnings: 0
module worklib.Add_full_44:v
```

```
      errors: 0, warnings: 0
module worklib.Add_half_86:v
      errors: 0, warnings: 0
module worklib.Add_half_85:v
      errors: 0, warnings: 0
module worklib.Add_full_43:v
      errors: 0, warnings: 0
module worklib.Add_half_84:v
      errors: 0, warnings: 0
module worklib.Add_half_83:v
      errors: 0, warnings: 0
module worklib.Add_full_42:v
      errors: 0, warnings: 0
module worklib.Add_half_82:v
      errors: 0, warnings: 0
module worklib.Add_half_81:v
      errors: 0, warnings: 0
module worklib.Add_full_41:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_11:v
      errors: 0, warnings: 0
module worklib.Add_half_80:v
      errors: 0, warnings: 0
module worklib.Add_half_79:v
      errors: 0, warnings: 0
module worklib.Add_full_40:v
      errors: 0, warnings: 0
module worklib.Add_half_78:v
      errors: 0, warnings: 0
module worklib.Add_half_77:v
      errors: 0, warnings: 0
module worklib.Add_full_39:v
      errors: 0, warnings: 0
module worklib.Add_half_76:v
      errors: 0, warnings: 0
module worklib.Add_half_75:v
      errors: 0, warnings: 0
module worklib.Add_full_38:v
      errors: 0, warnings: 0
module worklib.Add_half_74:v
      errors: 0, warnings: 0
module worklib.Add_half_73:v
      errors: 0, warnings: 0
module worklib.Add_full_37:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_10:v
      errors: 0, warnings: 0
module worklib.Add_half_72:v
      errors: 0, warnings: 0
module worklib.Add_half_71:v
      errors: 0, warnings: 0
module worklib.Add_full_36:v
```

```
      errors: 0, warnings: 0
module worklib.Add_half_70:v
      errors: 0, warnings: 0
module worklib.Add_half_69:v
      errors: 0, warnings: 0
module worklib.Add_full_35:v
      errors: 0, warnings: 0
module worklib.Add_half_68:v
      errors: 0, warnings: 0
module worklib.Add_half_67:v
      errors: 0, warnings: 0
module worklib.Add_full_34:v
      errors: 0, warnings: 0
module worklib.Add_half_66:v
      errors: 0, warnings: 0
module worklib.Add_half_65:v
      errors: 0, warnings: 0
module worklib.Add_full_33:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_9:v
      errors: 0, warnings: 0
module worklib.Add_rca_2:v
      errors: 0, warnings: 0
module worklib.Add_half_64:v
      errors: 0, warnings: 0
module worklib.Add_half_63:v
      errors: 0, warnings: 0
module worklib.Add_full_32:v
      errors: 0, warnings: 0
module worklib.Add_half_62:v
      errors: 0, warnings: 0
module worklib.Add_half_61:v
      errors: 0, warnings: 0
module worklib.Add_full_31:v
      errors: 0, warnings: 0
module worklib.Add_half_60:v
      errors: 0, warnings: 0
module worklib.Add_half_59:v
      errors: 0, warnings: 0
module worklib.Add_full_30:v
      errors: 0, warnings: 0
module worklib.Add_half_58:v
      errors: 0, warnings: 0
module worklib.Add_half_57:v
      errors: 0, warnings: 0
module worklib.Add_full_29:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_8:v
      errors: 0, warnings: 0
module worklib.Add_half_56:v
      errors: 0, warnings: 0
module worklib.Add_half_55:v
```

```
      errors: 0, warnings: 0
module worklib.Add_full_28:v
      errors: 0, warnings: 0
module worklib.Add_half_54:v
      errors: 0, warnings: 0
module worklib.Add_half_53:v
      errors: 0, warnings: 0
module worklib.Add_full_27:v
      errors: 0, warnings: 0
module worklib.Add_half_52:v
      errors: 0, warnings: 0
module worklib.Add_half_51:v
      errors: 0, warnings: 0
module worklib.Add_full_26:v
      errors: 0, warnings: 0
module worklib.Add_half_50:v
      errors: 0, warnings: 0
module worklib.Add_half_49:v
      errors: 0, warnings: 0
module worklib.Add_full_25:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_7:v
      errors: 0, warnings: 0
module worklib.Add_half_48:v
      errors: 0, warnings: 0
module worklib.Add_half_47:v
      errors: 0, warnings: 0
module worklib.Add_full_24:v
      errors: 0, warnings: 0
module worklib.Add_half_46:v
      errors: 0, warnings: 0
module worklib.Add_half_45:v
      errors: 0, warnings: 0
module worklib.Add_full_23:v
      errors: 0, warnings: 0
module worklib.Add_half_44:v
      errors: 0, warnings: 0
module worklib.Add_half_43:v
      errors: 0, warnings: 0
module worklib.Add_full_22:v
      errors: 0, warnings: 0
module worklib.Add_half_42:v
      errors: 0, warnings: 0
module worklib.Add_half_41:v
      errors: 0, warnings: 0
module worklib.Add_full_21:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_6:v
      errors: 0, warnings: 0
module worklib.Add_half_40:v
      errors: 0, warnings: 0
module worklib.Add_half_39:v
```

```
      errors: 0, warnings: 0
module worklib.Add_full_20:v
      errors: 0, warnings: 0
module worklib.Add_half_38:v
      errors: 0, warnings: 0
module worklib.Add_half_37:v
      errors: 0, warnings: 0
module worklib.Add_full_19:v
      errors: 0, warnings: 0
module worklib.Add_half_36:v
      errors: 0, warnings: 0
module worklib.Add_half_35:v
      errors: 0, warnings: 0
module worklib.Add_full_18:v
      errors: 0, warnings: 0
module worklib.Add_half_34:v
      errors: 0, warnings: 0
module worklib.Add_half_33:v
      errors: 0, warnings: 0
module worklib.Add_full_17:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_5:v
      errors: 0, warnings: 0
module worklib.Add_half_32:v
      errors: 0, warnings: 0
module worklib.Add_half_31:v
      errors: 0, warnings: 0
module worklib.Add_full_16:v
      errors: 0, warnings: 0
module worklib.Add_half_30:v
      errors: 0, warnings: 0
module worklib.Add_half_29:v
      errors: 0, warnings: 0
module worklib.Add_full_15:v
      errors: 0, warnings: 0
module worklib.Add_half_28:v
      errors: 0, warnings: 0
module worklib.Add_half_27:v
      errors: 0, warnings: 0
module worklib.Add_full_14:v
      errors: 0, warnings: 0
module worklib.Add_half_26:v
      errors: 0, warnings: 0
module worklib.Add_half_25:v
      errors: 0, warnings: 0
module worklib.Add_full_13:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_4:v
      errors: 0, warnings: 0
module worklib.Add_half_24:v
      errors: 0, warnings: 0
module worklib.Add_half_23:v
```

```
      errors: 0, warnings: 0
module worklib.Add_full_12:v
      errors: 0, warnings: 0
module worklib.Add_half_22:v
      errors: 0, warnings: 0
module worklib.Add_half_21:v
      errors: 0, warnings: 0
module worklib.Add_full_11:v
      errors: 0, warnings: 0
module worklib.Add_half_20:v
      errors: 0, warnings: 0
module worklib.Add_half_19:v
      errors: 0, warnings: 0
module worklib.Add_full_10:v
      errors: 0, warnings: 0
module worklib.Add_half_18:v
      errors: 0, warnings: 0
module worklib.Add_half_17:v
      errors: 0, warnings: 0
module worklib.Add_full_9:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_3:v
      errors: 0, warnings: 0
module worklib.Add_half_16:v
      errors: 0, warnings: 0
module worklib.Add_half_15:v
      errors: 0, warnings: 0
module worklib.Add_full_8:v
      errors: 0, warnings: 0
module worklib.Add_half_14:v
      errors: 0, warnings: 0
module worklib.Add_half_13:v
      errors: 0, warnings: 0
module worklib.Add_full_7:v
      errors: 0, warnings: 0
module worklib.Add_half_12:v
      errors: 0, warnings: 0
module worklib.Add_half_11:v
      errors: 0, warnings: 0
module worklib.Add_full_6:v
      errors: 0, warnings: 0
module worklib.Add_half_10:v
      errors: 0, warnings: 0
module worklib.Add_half_9:v
      errors: 0, warnings: 0
module worklib.Add_full_5:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_2:v
      errors: 0, warnings: 0
module worklib.Add_half_8:v
      errors: 0, warnings: 0
module worklib.Add_half_7:v
```

```
      errors: 0, warnings: 0
module worklib.Add_full_4:v
      errors: 0, warnings: 0
module worklib.Add_half_6:v
      errors: 0, warnings: 0
module worklib.Add_half_5:v
      errors: 0, warnings: 0
module worklib.Add_full_3:v
      errors: 0, warnings: 0
module worklib.Add_half_4:v
      errors: 0, warnings: 0
module worklib.Add_half_3:v
      errors: 0, warnings: 0
module worklib.Add_full_2:v
      errors: 0, warnings: 0
module worklib.Add_half_2:v
      errors: 0, warnings: 0
module worklib.Add_half_1:v
      errors: 0, warnings: 0
module worklib.Add_full_1:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_1:v
      errors: 0, warnings: 0
module worklib.Add_rca_1:v
      errors: 0, warnings: 0
module worklib.Add_rca64_1:v
      errors: 0, warnings: 0
module worklib.Add_half_320:v
      errors: 0, warnings: 0
module worklib.Add_half_319:v
      errors: 0, warnings: 0
module worklib.Add_full_160:v
      errors: 0, warnings: 0
module worklib.Add_half_318:v
      errors: 0, warnings: 0
module worklib.Add_half_317:v
      errors: 0, warnings: 0
module worklib.Add_full_159:v
      errors: 0, warnings: 0
module worklib.Add_half_316:v
      errors: 0, warnings: 0
module worklib.Add_half_315:v
      errors: 0, warnings: 0
module worklib.Add_full_158:v
      errors: 0, warnings: 0
module worklib.Add_half_314:v
      errors: 0, warnings: 0
module worklib.Add_half_313:v
      errors: 0, warnings: 0
module worklib.Add_full_157:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_40:v
```

```
      errors: 0, warnings: 0
module worklib.Add_half_312:v
      errors: 0, warnings: 0
module worklib.Add_half_311:v
      errors: 0, warnings: 0
module worklib.Add_full_156:v
      errors: 0, warnings: 0
module worklib.Add_half_310:v
      errors: 0, warnings: 0
module worklib.Add_half_309:v
      errors: 0, warnings: 0
module worklib.Add_full_155:v
      errors: 0, warnings: 0
module worklib.Add_half_308:v
      errors: 0, warnings: 0
module worklib.Add_half_307:v
      errors: 0, warnings: 0
module worklib.Add_full_154:v
      errors: 0, warnings: 0
module worklib.Add_half_306:v
      errors: 0, warnings: 0
module worklib.Add_half_305:v
      errors: 0, warnings: 0
module worklib.Add_full_153:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_39:v
      errors: 0, warnings: 0
module worklib.Add_half_304:v
      errors: 0, warnings: 0
module worklib.Add_half_303:v
      errors: 0, warnings: 0
module worklib.Add_full_152:v
      errors: 0, warnings: 0
module worklib.Add_half_302:v
      errors: 0, warnings: 0
module worklib.Add_half_301:v
      errors: 0, warnings: 0
module worklib.Add_full_151:v
      errors: 0, warnings: 0
module worklib.Add_half_300:v
      errors: 0, warnings: 0
module worklib.Add_half_299:v
      errors: 0, warnings: 0
module worklib.Add_full_150:v
      errors: 0, warnings: 0
module worklib.Add_half_298:v
      errors: 0, warnings: 0
module worklib.Add_half_297:v
      errors: 0, warnings: 0
module worklib.Add_full_149:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_38:v
```

```
      errors: 0, warnings: 0
module worklib.Add_half_296:v
      errors: 0, warnings: 0
module worklib.Add_half_295:v
      errors: 0, warnings: 0
module worklib.Add_full_148:v
      errors: 0, warnings: 0
module worklib.Add_half_294:v
      errors: 0, warnings: 0
module worklib.Add_half_293:v
      errors: 0, warnings: 0
module worklib.Add_full_147:v
      errors: 0, warnings: 0
module worklib.Add_half_292:v
      errors: 0, warnings: 0
module worklib.Add_half_291:v
      errors: 0, warnings: 0
module worklib.Add_full_146:v
      errors: 0, warnings: 0
module worklib.Add_half_290:v
      errors: 0, warnings: 0
module worklib.Add_half_289:v
      errors: 0, warnings: 0
module worklib.Add_full_145:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_37:v
      errors: 0, warnings: 0
module worklib.Add_half_288:v
      errors: 0, warnings: 0
module worklib.Add_half_287:v
      errors: 0, warnings: 0
module worklib.Add_full_144:v
      errors: 0, warnings: 0
module worklib.Add_half_286:v
      errors: 0, warnings: 0
module worklib.Add_half_285:v
      errors: 0, warnings: 0
module worklib.Add_full_143:v
      errors: 0, warnings: 0
module worklib.Add_half_284:v
      errors: 0, warnings: 0
module worklib.Add_half_283:v
      errors: 0, warnings: 0
module worklib.Add_full_142:v
      errors: 0, warnings: 0
module worklib.Add_half_282:v
      errors: 0, warnings: 0
module worklib.Add_half_281:v
      errors: 0, warnings: 0
module worklib.Add_full_141:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_36:v
```

```
      errors: 0, warnings: 0
module worklib.Add_half_280:v
      errors: 0, warnings: 0
module worklib.Add_half_279:v
      errors: 0, warnings: 0
module worklib.Add_full_140:v
      errors: 0, warnings: 0
module worklib.Add_half_278:v
      errors: 0, warnings: 0
module worklib.Add_half_277:v
      errors: 0, warnings: 0
module worklib.Add_full_139:v
      errors: 0, warnings: 0
module worklib.Add_half_276:v
      errors: 0, warnings: 0
module worklib.Add_half_275:v
      errors: 0, warnings: 0
module worklib.Add_full_138:v
      errors: 0, warnings: 0
module worklib.Add_half_274:v
      errors: 0, warnings: 0
module worklib.Add_half_273:v
      errors: 0, warnings: 0
module worklib.Add_full_137:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_35:v
      errors: 0, warnings: 0
module worklib.Add_half_272:v
      errors: 0, warnings: 0
module worklib.Add_half_271:v
      errors: 0, warnings: 0
module worklib.Add_full_136:v
      errors: 0, warnings: 0
module worklib.Add_half_270:v
      errors: 0, warnings: 0
module worklib.Add_half_269:v
      errors: 0, warnings: 0
module worklib.Add_full_135:v
      errors: 0, warnings: 0
module worklib.Add_half_268:v
      errors: 0, warnings: 0
module worklib.Add_half_267:v
      errors: 0, warnings: 0
module worklib.Add_full_134:v
      errors: 0, warnings: 0
module worklib.Add_half_266:v
      errors: 0, warnings: 0
module worklib.Add_half_265:v
      errors: 0, warnings: 0
module worklib.Add_full_133:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_34:v
```

```
            errors: 0, warnings: 0
      module worklib.Add_half_264:v
            errors: 0, warnings: 0
      module worklib.Add_half_263:v
            errors: 0, warnings: 0
      module worklib.Add_full_132:v
            errors: 0, warnings: 0
      module worklib.Add_half_262:v
            errors: 0, warnings: 0
      module worklib.Add_half_261:v
            errors: 0, warnings: 0
      module worklib.Add_full_131:v
            errors: 0, warnings: 0
      module worklib.Add_half_260:v
            errors: 0, warnings: 0
      module worklib.Add_half_259:v
            errors: 0, warnings: 0
      module worklib.Add_full_130:v
            errors: 0, warnings: 0
      module worklib.Add_half_258:v
            errors: 0, warnings: 0
      module worklib.Add_half_257:v
            errors: 0, warnings: 0
      module worklib.Add_full_129:v
            errors: 0, warnings: 0
      module worklib.Add_rca_4_33:v
            errors: 0, warnings: 0
      module worklib.Add_rca_5:v
            errors: 0, warnings: 0
      module worklib.mul_DW01_inc_0:v
            errors: 0, warnings: 0
      module worklib.mul:v
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CEOX1.tsbvlibp
      module tc240c.CEOX1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CAN2X1.tsbvlibp
      module tc240c.CAN2X1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/COR2X1.tsbvlibp
      module tc240c.COR2X1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CIVX2.tsbvlibp
      module tc240c.CIVX2:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CENX1.tsbvlibp
      module tc240c.CENX1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CEOXL.tsbvlibp
      module tc240c.CEOXL:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CNR2X1.tsbvlibp
```

```
      module tc240c.CNR2X1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CND2IX1.tsbvlibp
      module tc240c.CND2IX1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CND2XL.tsbvlibp
      module tc240c.CND2XL:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CND2X1.tsbvlibp
      module tc240c.CND2X1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CIVXL.tsbvlibp
      module tc240c.CIVXL:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CAN2XL.tsbvlibp
      module tc240c.CAN2XL:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CHA1X1.tsbvlibp
      module tc240c.CHA1X1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CTSX2.tsbvlibp
      module tc240c.CTSX2:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CAOR2X1.tsbvlibp
      module tc240c.CAOR2X1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CAOR1X1.tsbvlibp
      module tc240c.CAOR1X1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CNR8X1.tsbvlibp
      module tc240c.CNR8X1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/COR4X1.tsbvlibp
      module tc240c.COR4X1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/COR8X1.tsbvlibp
      module tc240c.COR8X1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CAN3X2.tsbvlibp
      module tc240c.CAN3X2:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CFD1QXL.tsbvlibp
      module tc240c.CFD1QXL:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CFD2XL.tsbvlibp
      module tc240c.CFD2XL:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CFD1XL.tsbvlibp
      module tc240c.CFD1XL:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CFD1QX1.tsbvlibp
      module tc240c.CFD1QX1:tsbvlibp
```

```
           errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CFD1QX2.tsbvlibp
     module tc240c.CFD1QX2:tsbvlibp
           errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CAOR2X4.tsbvlibp
     module tc240c.CAOR2X4:tsbvlibp
           errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/COND1X1.tsbvlibp
     module tc240c.COND1X1:tsbvlibp
           errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/COND1XL.tsbvlibp
     module tc240c.COND1XL:tsbvlibp
           errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CND3XL.tsbvlibp
     module tc240c.CND3XL:tsbvlibp
           errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CIVDX1.tsbvlibp
     module tc240c.CIVDX1:tsbvlibp
           errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CIVX3.tsbvlibp
     module tc240c.CIVX3:tsbvlibp
           errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CIVX1.tsbvlibp
     module tc240c.CIVX1:tsbvlibp
           errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CAOR2X2.tsbvlibp
     module tc240c.CAOR2X2:tsbvlibp
           errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CNIVX1.tsbvlibp
     module tc240c.CNIVX1:tsbvlibp
           errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CANR2XL.tsbvlibp
     module tc240c.CANR2XL:tsbvlibp
           errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/COND3X2.tsbvlibp
     module tc240c.COND3X2:tsbvlibp
           errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CNIVXL.tsbvlibp
     module tc240c.CNIVXL:tsbvlibp
           errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CND2IXL.tsbvlibp
     module tc240c.CND2IXL:tsbvlibp
           errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CNR2IXL.tsbvlibp
     module tc240c.CNR2IXL:tsbvlibp
           errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CDLY1XL.tsbvlibp
     module tc240c.CDLY1XL:tsbvlibp
           errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CAOR2XL.tsbvlibp
     module tc240c.CAOR2XL:tsbvlibp
           errors: 0, warnings: 0
```

```
file: /apps/toshiba/sjsu/verilog/tc240c/CANR1XL.tsbvlibp
      module tc240c.CANR1XL:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CNR2IX1.tsbvlibp
      module tc240c.CNR2IX1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/COND11X1.tsbvlibp
      module tc240c.COND11X1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/COR3X1.tsbvlibp
      module tc240c.COR3X1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CANR2X1.tsbvlibp
      module tc240c.CANR2X1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CNR3XL.tsbvlibp
      module tc240c.CNR3XL:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CAN8X1.tsbvlibp
      module tc240c.CAN8X1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CNR4X1.tsbvlibp
      module tc240c.CNR4X1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CND4X1.tsbvlibp
      module tc240c.CND4X1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/COND3X1.tsbvlibp
      module tc240c.COND3X1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/COR6X1.tsbvlibp
      module tc240c.COR6X1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/tsbCFD1QXL.tsbvlibp
      module tc240c.tsbCFD1QXL:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/tsbCFD2XL.tsbvlibp
      module tc240c.tsbCFD2XL:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/tsbCFD1XL.tsbvlibp
      module tc240c.tsbCFD1XL:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/tsbCFD1QX1.tsbvlibp
      module tc240c.tsbCFD1QX1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/tsbCFD1QX2.tsbvlibp
      module tc240c.tsbCFD1QX2:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/TFDPNOprim.tsbvlibp
      primitive tc240c.TFDPNOprim:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/TFDPRBNOprim.tsbvlibp
```

```
      primitive tc240c.TFDPRBNOprim:tsbvlibp
            errors: 0, warnings: 0
            Caching library 'tc240c' ....... Done
            Caching library 'worklib' ....... Done
      Elaborating the design hierarchy:
  Add_rca_0 M1 ( .sum(w10), .a({1'b0, opera1_not[30:0]}), .b({1'b0,
1'b0, 1'b0,
               |
ncelab: *W,CUVWSP (./mul_netlist.v,7376|13): 1 output port was not
connected:
ncelab: (./mul_netlist.v,1149): c_out

  Add_rca64_0 M2 ( .sum({SYNOPSYS_UNCONNECTED__0,
SYNOPSYS_UNCONNECTED__1,
                 |
ncelab: *W,CUVWSP (./mul_netlist.v,7380|15): 1 output port was not
connected:
ncelab: (./mul_netlist.v,3512): c_out

  Add_rca64_1 M4 ( .sum(w12), .a({1'b1, result_not[62:0]}), .b({1'b0,
1'b0,
                 |
ncelab: *W,CUVWSP (./mul_netlist.v,7403|15): 1 output port was not
connected:
ncelab: (./mul_netlist.v,5886): c_out

  Add_rca_5 M3 ( .sum(w1), .a(opera1_copy), .b({1'b0, D[30:0]}),
.c_in(1'b0)
               |
ncelab: *W,CUVWSP (./mul_netlist.v,7410|13): 1 output port was not
connected:
ncelab: (./mul_netlist.v,7046): c_out

  CFD1XL \nest_reg[1]  ( .D(n541), .CP(clock), .QN(n1103) );
                       |
ncelab: *W,CUVWSP (./mul_netlist.v,7671|21): 1 output port was not
connected:
ncelab: (/apps/toshiba/sjsu/verilog/tc240c/CFD1XL.tsbvlibp,7): Q

  CFD1XL \nest_reg[2]  ( .D(n540), .CP(clock), .Q(n18) );
                       |
ncelab: *W,CUVWSP (./mul_netlist.v,7672|21): 1 output port was not
connected:
ncelab: (/apps/toshiba/sjsu/verilog/tc240c/CFD1XL.tsbvlibp,7): QN

      Building instance overlay tables: ..................... Done
      Generating native compiled code:
            tc240c.CANR1XL:tsbvlibp <0x5b3d9c36>
                  streams:   0, words:     0
            tc240c.CANR2X1:tsbvlibp <0x759f56f5>
                  streams:   0, words:     0
            tc240c.CANR2XL:tsbvlibp <0x0bda707f>
```

```
            streams:   0, words:     0
          tc240c.CAOR1X1:tsbvlibp <0x108972c0>
            streams:   0, words:     0
          tc240c.CAOR2X1:tsbvlibp <0x638225ab>
            streams:   0, words:     0
          tc240c.CAOR2X2:tsbvlibp <0x6454edba>
            streams:   0, words:     0
          tc240c.CAOR2X4:tsbvlibp <0x29c615e0>
            streams:   0, words:     0
          tc240c.CAOR2XL:tsbvlibp <0x79bd3f40>
            streams:   0, words:     0
          tc240c.CENX1:tsbvlibp <0x4a8c49cd>
            streams:   0, words:     0
          tc240c.CEOX1:tsbvlibp <0x4400a8d7>
            streams:   0, words:     0
          tc240c.CEOXL:tsbvlibp <0x098af818>
            streams:   0, words:     0
          tc240c.CHA1X1:tsbvlibp <0x30760590>
            streams:   0, words:     0
          tc240c.COND11X1:tsbvlibp <0x165630b3>
            streams:   0, words:     0
          tc240c.COND1X1:tsbvlibp <0x69c0ce76>
            streams:   0, words:     0
          tc240c.COND1XL:tsbvlibp <0x36ede661>
            streams:   0, words:     0
          tc240c.COND3X1:tsbvlibp <0x3c28d710>
            streams:   0, words:     0
          tc240c.COND3X2:tsbvlibp <0x795bf7d1>
            streams:   0, words:     0
          tc240c.tsbCFD1QX1:tsbvlibp <0x1f1b900c>
            streams:   0, words:     0
          tc240c.tsbCFD1QX2:tsbvlibp <0x304ca27b>
            streams:   0, words:     0
          tc240c.tsbCFD1QXL:tsbvlibp <0x0755e884>
            streams:   0, words:     0
          tc240c.tsbCFD1XL:tsbvlibp <0x355406e0>
            streams:   0, words:     0
          tc240c.tsbCFD2XL:tsbvlibp <0x6725408c>
            streams:   0, words:     0
          worklib.Add_rca64_0:v <0x73760c11>
            streams:   2, words:   409
          worklib.Add_rca64_1:v <0x78f25dd2>
            streams:   2, words:   409
          worklib.mul:v <0x5db60616>
            streams:   2, words:   324
          worklib.test_mul:v <0x1126b2ed>
            streams:  11, words: 12635
Building instance specific data structures.
Loading native compiled code:     ..................... Done
```

```
Design hierarchy summary:
                            Instances  Unique
          Modules:               3168     692
          UDPs:                   262       2
          Primitives:            8553      10
          Timing outputs:        2311      32
          Registers:              268      13
          Scalar wires:          2591       -
          Expanded wires:         256       7
          Vectored wires:           2       -
          Initial blocks:           4       4
          Pseudo assignments:      12      12
          Timing checks:         1581     532
          Simulation timescale:  10ps
     Writing initial simulation snapshot: worklib.test_mul:v
Loading snapshot worklib.test_mul:v ..................... Done
ncsim> source /apps/cadence/INCISIV141/tools/inca/files/ncsimrc
ncsim> run
                    0 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxxx,
start=x, clock=0, muordi=0, reset=x, valid=x, result=xxxxxxxxxxxxxxxx
                   10 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxxx,
start=x, clock=1, muordi=0, reset=x, valid=x, result=xxxxxxxxxxxxxxxx
                   20 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxxx,
start=1, clock=0, muordi=0, reset=x, valid=x, result=xxxxxxxxxxxxxxxx
                   30 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxxx,
start=1, clock=1, muordi=0, reset=x, valid=x, result=xxxxxxxxxxxxxxxx
                   40 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxxx,
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                   50 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxxx,
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                  150 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxxx,
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                  160 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxxx,
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Warning!  Timing violation
           $hold( posedge CP &&& D_CD_low:3110 NS, CD:3110100 PS,
0.52 : 520 PS );
            File:
/apps/toshiba/sjsu/verilog/tc240c/tsbCFD2XL.tsbvlibp, line = 39
           Scope: test_mul.M1.\cust_reg[2] .tsbCFD2XL_1
            Time: 3110100 PS

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                9660 opera1=db97efee, opera2=c96edeaec96edeaf,
start=0, clock=0, muordi=0, reset=0, valid=1, result=0000000000000000
                9670 opera1=db97efee, opera2=c96edeaec96edeaf,
start=0, clock=1, muordi=0, reset=0, valid=1, result=0000000000000000
                9680 opera1=db97efee, opera2=c96edeaec96edeaf,
start=0, clock=0, muordi=0, reset=0, valid=1, result=0000000000000000
                9690 opera1=db97efee, opera2=c96edeaec96edeaf,
start=0, clock=1, muordi=0, reset=0, valid=1, result=0000000000000000
                9700 opera1=db97efee, opera2=c96edeaec96edeaf,
start=0, clock=0, muordi=0, reset=0, valid=1, result=0000000000000000
                9710 opera1=db97efee, opera2=c96edeaec96edeaf,
start=0, clock=1, muordi=0, reset=0, valid=1, result=0000000000000000
                9720 opera1=db97efee, opera2=c96edeaec96edeaf,
start=0, clock=0, muordi=0, reset=0, valid=1, result=0000000000000000
                9730 opera1=db97efee, opera2=c96edeaec96edeaf,
start=0, clock=1, muordi=0, reset=0, valid=1, result=0000000000000000
```

```
                9740 opera1=db97efee, opera2=c96edeaec96edeaf,
start=0, clock=0, muordi=0, reset=0, valid=1, result=0000000000000000
                9750 opera1=db97efee, opera2=c96edeaec96edeaf,
start=0, clock=1, muordi=0, reset=0, valid=1, result=0000000000000000
                9760 opera1=db97efee, opera2=c96edeaec96edeaf,
start=0, clock=0, muordi=0, reset=0, valid=1, result=0000000000000000
                9770 opera1=db97efee, opera2=c96edeaec96edeaf,
start=0, clock=1, muordi=0, reset=0, valid=1, result=0000000000000000
Simulation complete via $finish(1) at time 9775 NS + 0
./testmul.v:91 #2000 $finish;
ncsim> exit
```

For Divider

```
ncverilog: 14.10-p001: (c) Copyright 1995-2014 Cadence Design Systems,
Inc.
file: testdiv.v
      module worklib.test_div:v
            errors: 0, warnings: 0
file: div_netlist.v
      module worklib.Add_half_0:v
            errors: 0, warnings: 0
      module worklib.Add_half_511:v
            errors: 0, warnings: 0
      module worklib.Add_full_0:v
            errors: 0, warnings: 0
      module worklib.Add_half_510:v
            errors: 0, warnings: 0
      module worklib.Add_half_509:v
            errors: 0, warnings: 0
      module worklib.Add_full_255:v
            errors: 0, warnings: 0
      module worklib.Add_half_508:v
            errors: 0, warnings: 0
      module worklib.Add_half_507:v
            errors: 0, warnings: 0
      module worklib.Add_full_254:v
            errors: 0, warnings: 0
      module worklib.Add_half_506:v
            errors: 0, warnings: 0
      module worklib.Add_half_505:v
            errors: 0, warnings: 0
      module worklib.Add_full_253:v
            errors: 0, warnings: 0
      module worklib.Add_rca_4_0:v
            errors: 0, warnings: 0
      module worklib.Add_half_504:v
            errors: 0, warnings: 0
      module worklib.Add_half_503:v
            errors: 0, warnings: 0
      module worklib.Add_full_252:v
```

```
      errors: 0, warnings: 0
module worklib.Add_half_502:v
      errors: 0, warnings: 0
module worklib.Add_half_501:v
      errors: 0, warnings: 0
module worklib.Add_full_251:v
      errors: 0, warnings: 0
module worklib.Add_half_500:v
      errors: 0, warnings: 0
module worklib.Add_half_499:v
      errors: 0, warnings: 0
module worklib.Add_full_250:v
      errors: 0, warnings: 0
module worklib.Add_half_498:v
      errors: 0, warnings: 0
module worklib.Add_half_497:v
      errors: 0, warnings: 0
module worklib.Add_full_249:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_63:v
      errors: 0, warnings: 0
module worklib.Add_half_496:v
      errors: 0, warnings: 0
module worklib.Add_half_495:v
      errors: 0, warnings: 0
module worklib.Add_full_248:v
      errors: 0, warnings: 0
module worklib.Add_half_494:v
      errors: 0, warnings: 0
module worklib.Add_half_493:v
      errors: 0, warnings: 0
module worklib.Add_full_247:v
      errors: 0, warnings: 0
module worklib.Add_half_492:v
      errors: 0, warnings: 0
module worklib.Add_half_491:v
      errors: 0, warnings: 0
module worklib.Add_full_246:v
      errors: 0, warnings: 0
module worklib.Add_half_490:v
      errors: 0, warnings: 0
module worklib.Add_half_489:v
      errors: 0, warnings: 0
module worklib.Add_full_245:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_62:v
      errors: 0, warnings: 0
module worklib.Add_half_488:v
      errors: 0, warnings: 0
module worklib.Add_half_487:v
      errors: 0, warnings: 0
module worklib.Add_full_244:v
```

```
      errors: 0, warnings: 0
module worklib.Add_half_486:v
      errors: 0, warnings: 0
module worklib.Add_half_485:v
      errors: 0, warnings: 0
module worklib.Add_full_243:v
      errors: 0, warnings: 0
module worklib.Add_half_484:v
      errors: 0, warnings: 0
module worklib.Add_half_483:v
      errors: 0, warnings: 0
module worklib.Add_full_242:v
      errors: 0, warnings: 0
module worklib.Add_half_482:v
      errors: 0, warnings: 0
module worklib.Add_half_481:v
      errors: 0, warnings: 0
module worklib.Add_full_241:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_61:v
      errors: 0, warnings: 0
module worklib.Add_half_480:v
      errors: 0, warnings: 0
module worklib.Add_half_479:v
      errors: 0, warnings: 0
module worklib.Add_full_240:v
      errors: 0, warnings: 0
module worklib.Add_half_478:v
      errors: 0, warnings: 0
module worklib.Add_half_477:v
      errors: 0, warnings: 0
module worklib.Add_full_239:v
      errors: 0, warnings: 0
module worklib.Add_half_476:v
      errors: 0, warnings: 0
module worklib.Add_half_475:v
      errors: 0, warnings: 0
module worklib.Add_full_238:v
      errors: 0, warnings: 0
module worklib.Add_half_474:v
      errors: 0, warnings: 0
module worklib.Add_half_473:v
      errors: 0, warnings: 0
module worklib.Add_full_237:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_60:v
      errors: 0, warnings: 0
module worklib.Add_half_472:v
      errors: 0, warnings: 0
module worklib.Add_half_471:v
      errors: 0, warnings: 0
module worklib.Add_full_236:v
```

```
      errors: 0, warnings: 0
module worklib.Add_half_470:v
      errors: 0, warnings: 0
module worklib.Add_half_469:v
      errors: 0, warnings: 0
module worklib.Add_full_235:v
      errors: 0, warnings: 0
module worklib.Add_half_468:v
      errors: 0, warnings: 0
module worklib.Add_half_467:v
      errors: 0, warnings: 0
module worklib.Add_full_234:v
      errors: 0, warnings: 0
module worklib.Add_half_466:v
      errors: 0, warnings: 0
module worklib.Add_half_465:v
      errors: 0, warnings: 0
module worklib.Add_full_233:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_59:v
      errors: 0, warnings: 0
module worklib.Add_half_464:v
      errors: 0, warnings: 0
module worklib.Add_half_463:v
      errors: 0, warnings: 0
module worklib.Add_full_232:v
      errors: 0, warnings: 0
module worklib.Add_half_462:v
      errors: 0, warnings: 0
module worklib.Add_half_461:v
      errors: 0, warnings: 0
module worklib.Add_full_231:v
      errors: 0, warnings: 0
module worklib.Add_half_460:v
      errors: 0, warnings: 0
module worklib.Add_half_459:v
      errors: 0, warnings: 0
module worklib.Add_full_230:v
      errors: 0, warnings: 0
module worklib.Add_half_458:v
      errors: 0, warnings: 0
module worklib.Add_half_457:v
      errors: 0, warnings: 0
module worklib.Add_full_229:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_58:v
      errors: 0, warnings: 0
module worklib.Add_half_456:v
      errors: 0, warnings: 0
module worklib.Add_half_455:v
      errors: 0, warnings: 0
module worklib.Add_full_228:v
```

```
      errors: 0, warnings: 0
module worklib.Add_half_454:v
      errors: 0, warnings: 0
module worklib.Add_half_453:v
      errors: 0, warnings: 0
module worklib.Add_full_227:v
      errors: 0, warnings: 0
module worklib.Add_half_452:v
      errors: 0, warnings: 0
module worklib.Add_half_451:v
      errors: 0, warnings: 0
module worklib.Add_full_226:v
      errors: 0, warnings: 0
module worklib.Add_half_450:v
      errors: 0, warnings: 0
module worklib.Add_half_449:v
      errors: 0, warnings: 0
module worklib.Add_full_225:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_57:v
      errors: 0, warnings: 0
module worklib.Add_rca_0:v
      errors: 0, warnings: 0
module worklib.Add_half_448:v
      errors: 0, warnings: 0
module worklib.Add_half_447:v
      errors: 0, warnings: 0
module worklib.Add_full_224:v
      errors: 0, warnings: 0
module worklib.Add_half_446:v
      errors: 0, warnings: 0
module worklib.Add_half_445:v
      errors: 0, warnings: 0
module worklib.Add_full_223:v
      errors: 0, warnings: 0
module worklib.Add_half_444:v
      errors: 0, warnings: 0
module worklib.Add_half_443:v
      errors: 0, warnings: 0
module worklib.Add_full_222:v
      errors: 0, warnings: 0
module worklib.Add_half_442:v
      errors: 0, warnings: 0
module worklib.Add_half_441:v
      errors: 0, warnings: 0
module worklib.Add_full_221:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_56:v
      errors: 0, warnings: 0
module worklib.Add_half_440:v
      errors: 0, warnings: 0
module worklib.Add_half_439:v
```

```
      errors: 0, warnings: 0
module worklib.Add_full_220:v
      errors: 0, warnings: 0
module worklib.Add_half_438:v
      errors: 0, warnings: 0
module worklib.Add_half_437:v
      errors: 0, warnings: 0
module worklib.Add_full_219:v
      errors: 0, warnings: 0
module worklib.Add_half_436:v
      errors: 0, warnings: 0
module worklib.Add_half_435:v
      errors: 0, warnings: 0
module worklib.Add_full_218:v
      errors: 0, warnings: 0
module worklib.Add_half_434:v
      errors: 0, warnings: 0
module worklib.Add_half_433:v
      errors: 0, warnings: 0
module worklib.Add_full_217:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_55:v
      errors: 0, warnings: 0
module worklib.Add_half_432:v
      errors: 0, warnings: 0
module worklib.Add_half_431:v
      errors: 0, warnings: 0
module worklib.Add_full_216:v
      errors: 0, warnings: 0
module worklib.Add_half_430:v
      errors: 0, warnings: 0
module worklib.Add_half_429:v
      errors: 0, warnings: 0
module worklib.Add_full_215:v
      errors: 0, warnings: 0
module worklib.Add_half_428:v
      errors: 0, warnings: 0
module worklib.Add_half_427:v
      errors: 0, warnings: 0
module worklib.Add_full_214:v
      errors: 0, warnings: 0
module worklib.Add_half_426:v
      errors: 0, warnings: 0
module worklib.Add_half_425:v
      errors: 0, warnings: 0
module worklib.Add_full_213:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_54:v
      errors: 0, warnings: 0
module worklib.Add_half_424:v
      errors: 0, warnings: 0
module worklib.Add_half_423:v
```

```
      errors: 0, warnings: 0
module worklib.Add_full_212:v
      errors: 0, warnings: 0
module worklib.Add_half_422:v
      errors: 0, warnings: 0
module worklib.Add_half_421:v
      errors: 0, warnings: 0
module worklib.Add_full_211:v
      errors: 0, warnings: 0
module worklib.Add_half_420:v
      errors: 0, warnings: 0
module worklib.Add_half_419:v
      errors: 0, warnings: 0
module worklib.Add_full_210:v
      errors: 0, warnings: 0
module worklib.Add_half_418:v
      errors: 0, warnings: 0
module worklib.Add_half_417:v
      errors: 0, warnings: 0
module worklib.Add_full_209:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_53:v
      errors: 0, warnings: 0
module worklib.Add_half_416:v
      errors: 0, warnings: 0
module worklib.Add_half_415:v
      errors: 0, warnings: 0
module worklib.Add_full_208:v
      errors: 0, warnings: 0
module worklib.Add_half_414:v
      errors: 0, warnings: 0
module worklib.Add_half_413:v
      errors: 0, warnings: 0
module worklib.Add_full_207:v
      errors: 0, warnings: 0
module worklib.Add_half_412:v
      errors: 0, warnings: 0
module worklib.Add_half_411:v
      errors: 0, warnings: 0
module worklib.Add_full_206:v
      errors: 0, warnings: 0
module worklib.Add_half_410:v
      errors: 0, warnings: 0
module worklib.Add_half_409:v
      errors: 0, warnings: 0
module worklib.Add_full_205:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_52:v
      errors: 0, warnings: 0
module worklib.Add_half_408:v
      errors: 0, warnings: 0
module worklib.Add_half_407:v
```

```
      errors: 0, warnings: 0
module worklib.Add_full_204:v
      errors: 0, warnings: 0
module worklib.Add_half_406:v
      errors: 0, warnings: 0
module worklib.Add_half_405:v
      errors: 0, warnings: 0
module worklib.Add_full_203:v
      errors: 0, warnings: 0
module worklib.Add_half_404:v
      errors: 0, warnings: 0
module worklib.Add_half_403:v
      errors: 0, warnings: 0
module worklib.Add_full_202:v
      errors: 0, warnings: 0
module worklib.Add_half_402:v
      errors: 0, warnings: 0
module worklib.Add_half_401:v
      errors: 0, warnings: 0
module worklib.Add_full_201:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_51:v
      errors: 0, warnings: 0
module worklib.Add_half_400:v
      errors: 0, warnings: 0
module worklib.Add_half_399:v
      errors: 0, warnings: 0
module worklib.Add_full_200:v
      errors: 0, warnings: 0
module worklib.Add_half_398:v
      errors: 0, warnings: 0
module worklib.Add_half_397:v
      errors: 0, warnings: 0
module worklib.Add_full_199:v
      errors: 0, warnings: 0
module worklib.Add_half_396:v
      errors: 0, warnings: 0
module worklib.Add_half_395:v
      errors: 0, warnings: 0
module worklib.Add_full_198:v
      errors: 0, warnings: 0
module worklib.Add_half_394:v
      errors: 0, warnings: 0
module worklib.Add_half_393:v
      errors: 0, warnings: 0
module worklib.Add_full_197:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_50:v
      errors: 0, warnings: 0
module worklib.Add_half_392:v
      errors: 0, warnings: 0
module worklib.Add_half_391:v
```

```
      errors: 0, warnings: 0
module worklib.Add_full_196:v
      errors: 0, warnings: 0
module worklib.Add_half_390:v
      errors: 0, warnings: 0
module worklib.Add_half_389:v
      errors: 0, warnings: 0
module worklib.Add_full_195:v
      errors: 0, warnings: 0
module worklib.Add_half_388:v
      errors: 0, warnings: 0
module worklib.Add_half_387:v
      errors: 0, warnings: 0
module worklib.Add_full_194:v
      errors: 0, warnings: 0
module worklib.Add_half_386:v
      errors: 0, warnings: 0
module worklib.Add_half_385:v
      errors: 0, warnings: 0
module worklib.Add_full_193:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_49:v
      errors: 0, warnings: 0
module worklib.Add_rca_7:v
      errors: 0, warnings: 0
module worklib.Add_half_256:v
      errors: 0, warnings: 0
module worklib.Add_half_255:v
      errors: 0, warnings: 0
module worklib.Add_full_128:v
      errors: 0, warnings: 0
module worklib.Add_half_254:v
      errors: 0, warnings: 0
module worklib.Add_half_253:v
      errors: 0, warnings: 0
module worklib.Add_full_127:v
      errors: 0, warnings: 0
module worklib.Add_half_252:v
      errors: 0, warnings: 0
module worklib.Add_half_251:v
      errors: 0, warnings: 0
module worklib.Add_full_126:v
      errors: 0, warnings: 0
module worklib.Add_half_250:v
      errors: 0, warnings: 0
module worklib.Add_half_249:v
      errors: 0, warnings: 0
module worklib.Add_full_125:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_32:v
      errors: 0, warnings: 0
module worklib.Add_half_248:v
```

```
      errors: 0, warnings: 0
module worklib.Add_half_247:v
      errors: 0, warnings: 0
module worklib.Add_full_124:v
      errors: 0, warnings: 0
module worklib.Add_half_246:v
      errors: 0, warnings: 0
module worklib.Add_half_245:v
      errors: 0, warnings: 0
module worklib.Add_full_123:v
      errors: 0, warnings: 0
module worklib.Add_half_244:v
      errors: 0, warnings: 0
module worklib.Add_half_243:v
      errors: 0, warnings: 0
module worklib.Add_full_122:v
      errors: 0, warnings: 0
module worklib.Add_half_242:v
      errors: 0, warnings: 0
module worklib.Add_half_241:v
      errors: 0, warnings: 0
module worklib.Add_full_121:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_31:v
      errors: 0, warnings: 0
module worklib.Add_half_240:v
      errors: 0, warnings: 0
module worklib.Add_half_239:v
      errors: 0, warnings: 0
module worklib.Add_full_120:v
      errors: 0, warnings: 0
module worklib.Add_half_238:v
      errors: 0, warnings: 0
module worklib.Add_half_237:v
      errors: 0, warnings: 0
module worklib.Add_full_119:v
      errors: 0, warnings: 0
module worklib.Add_half_236:v
      errors: 0, warnings: 0
module worklib.Add_half_235:v
      errors: 0, warnings: 0
module worklib.Add_full_118:v
      errors: 0, warnings: 0
module worklib.Add_half_234:v
      errors: 0, warnings: 0
module worklib.Add_half_233:v
      errors: 0, warnings: 0
module worklib.Add_full_117:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_30:v
      errors: 0, warnings: 0
module worklib.Add_half_232:v
```

```
      errors: 0, warnings: 0
module worklib.Add_half_231:v
      errors: 0, warnings: 0
module worklib.Add_full_116:v
      errors: 0, warnings: 0
module worklib.Add_half_230:v
      errors: 0, warnings: 0
module worklib.Add_half_229:v
      errors: 0, warnings: 0
module worklib.Add_full_115:v
      errors: 0, warnings: 0
module worklib.Add_half_228:v
      errors: 0, warnings: 0
module worklib.Add_half_227:v
      errors: 0, warnings: 0
module worklib.Add_full_114:v
      errors: 0, warnings: 0
module worklib.Add_half_226:v
      errors: 0, warnings: 0
module worklib.Add_half_225:v
      errors: 0, warnings: 0
module worklib.Add_full_113:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_29:v
      errors: 0, warnings: 0
module worklib.Add_half_224:v
      errors: 0, warnings: 0
module worklib.Add_half_223:v
      errors: 0, warnings: 0
module worklib.Add_full_112:v
      errors: 0, warnings: 0
module worklib.Add_half_222:v
      errors: 0, warnings: 0
module worklib.Add_half_221:v
      errors: 0, warnings: 0
module worklib.Add_full_111:v
      errors: 0, warnings: 0
module worklib.Add_half_220:v
      errors: 0, warnings: 0
module worklib.Add_half_219:v
      errors: 0, warnings: 0
module worklib.Add_full_110:v
      errors: 0, warnings: 0
module worklib.Add_half_218:v
      errors: 0, warnings: 0
module worklib.Add_half_217:v
      errors: 0, warnings: 0
module worklib.Add_full_109:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_28:v
      errors: 0, warnings: 0
module worklib.Add_half_216:v
```

```
      errors: 0, warnings: 0
module worklib.Add_half_215:v
      errors: 0, warnings: 0
module worklib.Add_full_108:v
      errors: 0, warnings: 0
module worklib.Add_half_214:v
      errors: 0, warnings: 0
module worklib.Add_half_213:v
      errors: 0, warnings: 0
module worklib.Add_full_107:v
      errors: 0, warnings: 0
module worklib.Add_half_212:v
      errors: 0, warnings: 0
module worklib.Add_half_211:v
      errors: 0, warnings: 0
module worklib.Add_full_106:v
      errors: 0, warnings: 0
module worklib.Add_half_210:v
      errors: 0, warnings: 0
module worklib.Add_half_209:v
      errors: 0, warnings: 0
module worklib.Add_full_105:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_27:v
      errors: 0, warnings: 0
module worklib.Add_half_208:v
      errors: 0, warnings: 0
module worklib.Add_half_207:v
      errors: 0, warnings: 0
module worklib.Add_full_104:v
      errors: 0, warnings: 0
module worklib.Add_half_206:v
      errors: 0, warnings: 0
module worklib.Add_half_205:v
      errors: 0, warnings: 0
module worklib.Add_full_103:v
      errors: 0, warnings: 0
module worklib.Add_half_204:v
      errors: 0, warnings: 0
module worklib.Add_half_203:v
      errors: 0, warnings: 0
module worklib.Add_full_102:v
      errors: 0, warnings: 0
module worklib.Add_half_202:v
      errors: 0, warnings: 0
module worklib.Add_half_201:v
      errors: 0, warnings: 0
module worklib.Add_full_101:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_26:v
      errors: 0, warnings: 0
module worklib.Add_half_200:v
```

```
      errors: 0, warnings: 0
module worklib.Add_half_199:v
      errors: 0, warnings: 0
module worklib.Add_full_100:v
      errors: 0, warnings: 0
module worklib.Add_half_198:v
      errors: 0, warnings: 0
module worklib.Add_half_197:v
      errors: 0, warnings: 0
module worklib.Add_full_99:v
      errors: 0, warnings: 0
module worklib.Add_half_196:v
      errors: 0, warnings: 0
module worklib.Add_half_195:v
      errors: 0, warnings: 0
module worklib.Add_full_98:v
      errors: 0, warnings: 0
module worklib.Add_half_194:v
      errors: 0, warnings: 0
module worklib.Add_half_193:v
      errors: 0, warnings: 0
module worklib.Add_full_97:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_25:v
      errors: 0, warnings: 0
module worklib.Add_rca_4:v
      errors: 0, warnings: 0
module worklib.Add_half_192:v
      errors: 0, warnings: 0
module worklib.Add_half_191:v
      errors: 0, warnings: 0
module worklib.Add_full_96:v
      errors: 0, warnings: 0
module worklib.Add_half_190:v
      errors: 0, warnings: 0
module worklib.Add_half_189:v
      errors: 0, warnings: 0
module worklib.Add_full_95:v
      errors: 0, warnings: 0
module worklib.Add_half_188:v
      errors: 0, warnings: 0
module worklib.Add_half_187:v
      errors: 0, warnings: 0
module worklib.Add_full_94:v
      errors: 0, warnings: 0
module worklib.Add_half_186:v
      errors: 0, warnings: 0
module worklib.Add_half_185:v
      errors: 0, warnings: 0
module worklib.Add_full_93:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_24:v
```

```
      errors: 0, warnings: 0
module worklib.Add_half_184:v
      errors: 0, warnings: 0
module worklib.Add_half_183:v
      errors: 0, warnings: 0
module worklib.Add_full_92:v
      errors: 0, warnings: 0
module worklib.Add_half_182:v
      errors: 0, warnings: 0
module worklib.Add_half_181:v
      errors: 0, warnings: 0
module worklib.Add_full_91:v
      errors: 0, warnings: 0
module worklib.Add_half_180:v
      errors: 0, warnings: 0
module worklib.Add_half_179:v
      errors: 0, warnings: 0
module worklib.Add_full_90:v
      errors: 0, warnings: 0
module worklib.Add_half_178:v
      errors: 0, warnings: 0
module worklib.Add_half_177:v
      errors: 0, warnings: 0
module worklib.Add_full_89:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_23:v
      errors: 0, warnings: 0
module worklib.Add_half_176:v
      errors: 0, warnings: 0
module worklib.Add_half_175:v
      errors: 0, warnings: 0
module worklib.Add_full_88:v
      errors: 0, warnings: 0
module worklib.Add_half_174:v
      errors: 0, warnings: 0
module worklib.Add_half_173:v
      errors: 0, warnings: 0
module worklib.Add_full_87:v
      errors: 0, warnings: 0
module worklib.Add_half_172:v
      errors: 0, warnings: 0
module worklib.Add_half_171:v
      errors: 0, warnings: 0
module worklib.Add_full_86:v
      errors: 0, warnings: 0
module worklib.Add_half_170:v
      errors: 0, warnings: 0
module worklib.Add_half_169:v
      errors: 0, warnings: 0
module worklib.Add_full_85:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_22:v
```

```
      errors: 0, warnings: 0
module worklib.Add_half_168:v
      errors: 0, warnings: 0
module worklib.Add_half_167:v
      errors: 0, warnings: 0
module worklib.Add_full_84:v
      errors: 0, warnings: 0
module worklib.Add_half_166:v
      errors: 0, warnings: 0
module worklib.Add_half_165:v
      errors: 0, warnings: 0
module worklib.Add_full_83:v
      errors: 0, warnings: 0
module worklib.Add_half_164:v
      errors: 0, warnings: 0
module worklib.Add_half_163:v
      errors: 0, warnings: 0
module worklib.Add_full_82:v
      errors: 0, warnings: 0
module worklib.Add_half_162:v
      errors: 0, warnings: 0
module worklib.Add_half_161:v
      errors: 0, warnings: 0
module worklib.Add_full_81:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_21:v
      errors: 0, warnings: 0
module worklib.Add_half_160:v
      errors: 0, warnings: 0
module worklib.Add_half_159:v
      errors: 0, warnings: 0
module worklib.Add_full_80:v
      errors: 0, warnings: 0
module worklib.Add_half_158:v
      errors: 0, warnings: 0
module worklib.Add_half_157:v
      errors: 0, warnings: 0
module worklib.Add_full_79:v
      errors: 0, warnings: 0
module worklib.Add_half_156:v
      errors: 0, warnings: 0
module worklib.Add_half_155:v
      errors: 0, warnings: 0
module worklib.Add_full_78:v
      errors: 0, warnings: 0
module worklib.Add_half_154:v
      errors: 0, warnings: 0
module worklib.Add_half_153:v
      errors: 0, warnings: 0
module worklib.Add_full_77:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_20:v
```

```
      errors: 0, warnings: 0
module worklib.Add_half_152:v
      errors: 0, warnings: 0
module worklib.Add_half_151:v
      errors: 0, warnings: 0
module worklib.Add_full_76:v
      errors: 0, warnings: 0
module worklib.Add_half_150:v
      errors: 0, warnings: 0
module worklib.Add_half_149:v
      errors: 0, warnings: 0
module worklib.Add_full_75:v
      errors: 0, warnings: 0
module worklib.Add_half_148:v
      errors: 0, warnings: 0
module worklib.Add_half_147:v
      errors: 0, warnings: 0
module worklib.Add_full_74:v
      errors: 0, warnings: 0
module worklib.Add_half_146:v
      errors: 0, warnings: 0
module worklib.Add_half_145:v
      errors: 0, warnings: 0
module worklib.Add_full_73:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_19:v
      errors: 0, warnings: 0
module worklib.Add_half_144:v
      errors: 0, warnings: 0
module worklib.Add_half_143:v
      errors: 0, warnings: 0
module worklib.Add_full_72:v
      errors: 0, warnings: 0
module worklib.Add_half_142:v
      errors: 0, warnings: 0
module worklib.Add_half_141:v
      errors: 0, warnings: 0
module worklib.Add_full_71:v
      errors: 0, warnings: 0
module worklib.Add_half_140:v
      errors: 0, warnings: 0
module worklib.Add_half_139:v
      errors: 0, warnings: 0
module worklib.Add_full_70:v
      errors: 0, warnings: 0
module worklib.Add_half_138:v
      errors: 0, warnings: 0
module worklib.Add_half_137:v
      errors: 0, warnings: 0
module worklib.Add_full_69:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_18:v
```

```
      errors: 0, warnings: 0
module worklib.Add_half_136:v
      errors: 0, warnings: 0
module worklib.Add_half_135:v
      errors: 0, warnings: 0
module worklib.Add_full_68:v
      errors: 0, warnings: 0
module worklib.Add_half_134:v
      errors: 0, warnings: 0
module worklib.Add_half_133:v
      errors: 0, warnings: 0
module worklib.Add_full_67:v
      errors: 0, warnings: 0
module worklib.Add_half_132:v
      errors: 0, warnings: 0
module worklib.Add_half_131:v
      errors: 0, warnings: 0
module worklib.Add_full_66:v
      errors: 0, warnings: 0
module worklib.Add_half_130:v
      errors: 0, warnings: 0
module worklib.Add_half_129:v
      errors: 0, warnings: 0
module worklib.Add_full_65:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_17:v
      errors: 0, warnings: 0
module worklib.Add_rca_3:v
      errors: 0, warnings: 0
module worklib.Add_rca64_0:v
      errors: 0, warnings: 0
module worklib.Add_half_128:v
      errors: 0, warnings: 0
module worklib.Add_half_127:v
      errors: 0, warnings: 0
module worklib.Add_full_64:v
      errors: 0, warnings: 0
module worklib.Add_half_126:v
      errors: 0, warnings: 0
module worklib.Add_half_125:v
      errors: 0, warnings: 0
module worklib.Add_full_63:v
      errors: 0, warnings: 0
module worklib.Add_half_124:v
      errors: 0, warnings: 0
module worklib.Add_half_123:v
      errors: 0, warnings: 0
module worklib.Add_full_62:v
      errors: 0, warnings: 0
module worklib.Add_half_122:v
      errors: 0, warnings: 0
module worklib.Add_half_121:v
```

```
      errors: 0, warnings: 0
module worklib.Add_full_61:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_16:v
      errors: 0, warnings: 0
module worklib.Add_half_120:v
      errors: 0, warnings: 0
module worklib.Add_half_119:v
      errors: 0, warnings: 0
module worklib.Add_full_60:v
      errors: 0, warnings: 0
module worklib.Add_half_118:v
      errors: 0, warnings: 0
module worklib.Add_half_117:v
      errors: 0, warnings: 0
module worklib.Add_full_59:v
      errors: 0, warnings: 0
module worklib.Add_half_116:v
      errors: 0, warnings: 0
module worklib.Add_half_115:v
      errors: 0, warnings: 0
module worklib.Add_full_58:v
      errors: 0, warnings: 0
module worklib.Add_half_114:v
      errors: 0, warnings: 0
module worklib.Add_half_113:v
      errors: 0, warnings: 0
module worklib.Add_full_57:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_15:v
      errors: 0, warnings: 0
module worklib.Add_half_112:v
      errors: 0, warnings: 0
module worklib.Add_half_111:v
      errors: 0, warnings: 0
module worklib.Add_full_56:v
      errors: 0, warnings: 0
module worklib.Add_half_110:v
      errors: 0, warnings: 0
module worklib.Add_half_109:v
      errors: 0, warnings: 0
module worklib.Add_full_55:v
      errors: 0, warnings: 0
module worklib.Add_half_108:v
      errors: 0, warnings: 0
module worklib.Add_half_107:v
      errors: 0, warnings: 0
module worklib.Add_full_54:v
      errors: 0, warnings: 0
module worklib.Add_half_106:v
      errors: 0, warnings: 0
module worklib.Add_half_105:v
```

```
      errors: 0, warnings: 0
module worklib.Add_full_53:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_14:v
      errors: 0, warnings: 0
module worklib.Add_half_104:v
      errors: 0, warnings: 0
module worklib.Add_half_103:v
      errors: 0, warnings: 0
module worklib.Add_full_52:v
      errors: 0, warnings: 0
module worklib.Add_half_102:v
      errors: 0, warnings: 0
module worklib.Add_half_101:v
      errors: 0, warnings: 0
module worklib.Add_full_51:v
      errors: 0, warnings: 0
module worklib.Add_half_100:v
      errors: 0, warnings: 0
module worklib.Add_half_99:v
      errors: 0, warnings: 0
module worklib.Add_full_50:v
      errors: 0, warnings: 0
module worklib.Add_half_98:v
      errors: 0, warnings: 0
module worklib.Add_half_97:v
      errors: 0, warnings: 0
module worklib.Add_full_49:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_13:v
      errors: 0, warnings: 0
module worklib.Add_half_96:v
      errors: 0, warnings: 0
module worklib.Add_half_95:v
      errors: 0, warnings: 0
module worklib.Add_full_48:v
      errors: 0, warnings: 0
module worklib.Add_half_94:v
      errors: 0, warnings: 0
module worklib.Add_half_93:v
      errors: 0, warnings: 0
module worklib.Add_full_47:v
      errors: 0, warnings: 0
module worklib.Add_half_92:v
      errors: 0, warnings: 0
module worklib.Add_half_91:v
      errors: 0, warnings: 0
module worklib.Add_full_46:v
      errors: 0, warnings: 0
module worklib.Add_half_90:v
      errors: 0, warnings: 0
module worklib.Add_half_89:v
```

```
      errors: 0, warnings: 0
module worklib.Add_full_45:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_12:v
      errors: 0, warnings: 0
module worklib.Add_half_88:v
      errors: 0, warnings: 0
module worklib.Add_half_87:v
      errors: 0, warnings: 0
module worklib.Add_full_44:v
      errors: 0, warnings: 0
module worklib.Add_half_86:v
      errors: 0, warnings: 0
module worklib.Add_half_85:v
      errors: 0, warnings: 0
module worklib.Add_full_43:v
      errors: 0, warnings: 0
module worklib.Add_half_84:v
      errors: 0, warnings: 0
module worklib.Add_half_83:v
      errors: 0, warnings: 0
module worklib.Add_full_42:v
      errors: 0, warnings: 0
module worklib.Add_half_82:v
      errors: 0, warnings: 0
module worklib.Add_half_81:v
      errors: 0, warnings: 0
module worklib.Add_full_41:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_11:v
      errors: 0, warnings: 0
module worklib.Add_half_80:v
      errors: 0, warnings: 0
module worklib.Add_half_79:v
      errors: 0, warnings: 0
module worklib.Add_full_40:v
      errors: 0, warnings: 0
module worklib.Add_half_78:v
      errors: 0, warnings: 0
module worklib.Add_half_77:v
      errors: 0, warnings: 0
module worklib.Add_full_39:v
      errors: 0, warnings: 0
module worklib.Add_half_76:v
      errors: 0, warnings: 0
module worklib.Add_half_75:v
      errors: 0, warnings: 0
module worklib.Add_full_38:v
      errors: 0, warnings: 0
module worklib.Add_half_74:v
      errors: 0, warnings: 0
module worklib.Add_half_73:v
```

```
      errors: 0, warnings: 0
module worklib.Add_full_37:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_10:v
      errors: 0, warnings: 0
module worklib.Add_half_72:v
      errors: 0, warnings: 0
module worklib.Add_half_71:v
      errors: 0, warnings: 0
module worklib.Add_full_36:v
      errors: 0, warnings: 0
module worklib.Add_half_70:v
      errors: 0, warnings: 0
module worklib.Add_half_69:v
      errors: 0, warnings: 0
module worklib.Add_full_35:v
      errors: 0, warnings: 0
module worklib.Add_half_68:v
      errors: 0, warnings: 0
module worklib.Add_half_67:v
      errors: 0, warnings: 0
module worklib.Add_full_34:v
      errors: 0, warnings: 0
module worklib.Add_half_66:v
      errors: 0, warnings: 0
module worklib.Add_half_65:v
      errors: 0, warnings: 0
module worklib.Add_full_33:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_9:v
      errors: 0, warnings: 0
module worklib.Add_rca_2:v
      errors: 0, warnings: 0
module worklib.Add_half_64:v
      errors: 0, warnings: 0
module worklib.Add_half_63:v
      errors: 0, warnings: 0
module worklib.Add_full_32:v
      errors: 0, warnings: 0
module worklib.Add_half_62:v
      errors: 0, warnings: 0
module worklib.Add_half_61:v
      errors: 0, warnings: 0
module worklib.Add_full_31:v
      errors: 0, warnings: 0
module worklib.Add_half_60:v
      errors: 0, warnings: 0
module worklib.Add_half_59:v
      errors: 0, warnings: 0
module worklib.Add_full_30:v
      errors: 0, warnings: 0
module worklib.Add_half_58:v
```

```
      errors: 0, warnings: 0
module worklib.Add_half_57:v
      errors: 0, warnings: 0
module worklib.Add_full_29:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_8:v
      errors: 0, warnings: 0
module worklib.Add_half_56:v
      errors: 0, warnings: 0
module worklib.Add_half_55:v
      errors: 0, warnings: 0
module worklib.Add_full_28:v
      errors: 0, warnings: 0
module worklib.Add_half_54:v
      errors: 0, warnings: 0
module worklib.Add_half_53:v
      errors: 0, warnings: 0
module worklib.Add_full_27:v
      errors: 0, warnings: 0
module worklib.Add_half_52:v
      errors: 0, warnings: 0
module worklib.Add_half_51:v
      errors: 0, warnings: 0
module worklib.Add_full_26:v
      errors: 0, warnings: 0
module worklib.Add_half_50:v
      errors: 0, warnings: 0
module worklib.Add_half_49:v
      errors: 0, warnings: 0
module worklib.Add_full_25:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_7:v
      errors: 0, warnings: 0
module worklib.Add_half_48:v
      errors: 0, warnings: 0
module worklib.Add_half_47:v
      errors: 0, warnings: 0
module worklib.Add_full_24:v
      errors: 0, warnings: 0
module worklib.Add_half_46:v
      errors: 0, warnings: 0
module worklib.Add_half_45:v
      errors: 0, warnings: 0
module worklib.Add_full_23:v
      errors: 0, warnings: 0
module worklib.Add_half_44:v
      errors: 0, warnings: 0
module worklib.Add_half_43:v
      errors: 0, warnings: 0
module worklib.Add_full_22:v
      errors: 0, warnings: 0
module worklib.Add_half_42:v
```

```
      errors: 0, warnings: 0
module worklib.Add_half_41:v
      errors: 0, warnings: 0
module worklib.Add_full_21:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_6:v
      errors: 0, warnings: 0
module worklib.Add_half_40:v
      errors: 0, warnings: 0
module worklib.Add_half_39:v
      errors: 0, warnings: 0
module worklib.Add_full_20:v
      errors: 0, warnings: 0
module worklib.Add_half_38:v
      errors: 0, warnings: 0
module worklib.Add_half_37:v
      errors: 0, warnings: 0
module worklib.Add_full_19:v
      errors: 0, warnings: 0
module worklib.Add_half_36:v
      errors: 0, warnings: 0
module worklib.Add_half_35:v
      errors: 0, warnings: 0
module worklib.Add_full_18:v
      errors: 0, warnings: 0
module worklib.Add_half_34:v
      errors: 0, warnings: 0
module worklib.Add_half_33:v
      errors: 0, warnings: 0
module worklib.Add_full_17:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_5:v
      errors: 0, warnings: 0
module worklib.Add_half_32:v
      errors: 0, warnings: 0
module worklib.Add_half_31:v
      errors: 0, warnings: 0
module worklib.Add_full_16:v
      errors: 0, warnings: 0
module worklib.Add_half_30:v
      errors: 0, warnings: 0
module worklib.Add_half_29:v
      errors: 0, warnings: 0
module worklib.Add_full_15:v
      errors: 0, warnings: 0
module worklib.Add_half_28:v
      errors: 0, warnings: 0
module worklib.Add_half_27:v
      errors: 0, warnings: 0
module worklib.Add_full_14:v
      errors: 0, warnings: 0
module worklib.Add_half_26:v
```

```
      errors: 0, warnings: 0
module worklib.Add_half_25:v
      errors: 0, warnings: 0
module worklib.Add_full_13:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_4:v
      errors: 0, warnings: 0
module worklib.Add_half_24:v
      errors: 0, warnings: 0
module worklib.Add_half_23:v
      errors: 0, warnings: 0
module worklib.Add_full_12:v
      errors: 0, warnings: 0
module worklib.Add_half_22:v
      errors: 0, warnings: 0
module worklib.Add_half_21:v
      errors: 0, warnings: 0
module worklib.Add_full_11:v
      errors: 0, warnings: 0
module worklib.Add_half_20:v
      errors: 0, warnings: 0
module worklib.Add_half_19:v
      errors: 0, warnings: 0
module worklib.Add_full_10:v
      errors: 0, warnings: 0
module worklib.Add_half_18:v
      errors: 0, warnings: 0
module worklib.Add_half_17:v
      errors: 0, warnings: 0
module worklib.Add_full_9:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_3:v
      errors: 0, warnings: 0
module worklib.Add_half_16:v
      errors: 0, warnings: 0
module worklib.Add_half_15:v
      errors: 0, warnings: 0
module worklib.Add_full_8:v
      errors: 0, warnings: 0
module worklib.Add_half_14:v
      errors: 0, warnings: 0
module worklib.Add_half_13:v
      errors: 0, warnings: 0
module worklib.Add_full_7:v
      errors: 0, warnings: 0
module worklib.Add_half_12:v
      errors: 0, warnings: 0
module worklib.Add_half_11:v
      errors: 0, warnings: 0
module worklib.Add_full_6:v
      errors: 0, warnings: 0
module worklib.Add_half_10:v
```

```
      errors: 0, warnings: 0
module worklib.Add_half_9:v
      errors: 0, warnings: 0
module worklib.Add_full_5:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_2:v
      errors: 0, warnings: 0
module worklib.Add_half_8:v
      errors: 0, warnings: 0
module worklib.Add_half_7:v
      errors: 0, warnings: 0
module worklib.Add_full_4:v
      errors: 0, warnings: 0
module worklib.Add_half_6:v
      errors: 0, warnings: 0
module worklib.Add_half_5:v
      errors: 0, warnings: 0
module worklib.Add_full_3:v
      errors: 0, warnings: 0
module worklib.Add_half_4:v
      errors: 0, warnings: 0
module worklib.Add_half_3:v
      errors: 0, warnings: 0
module worklib.Add_full_2:v
      errors: 0, warnings: 0
module worklib.Add_half_2:v
      errors: 0, warnings: 0
module worklib.Add_half_1:v
      errors: 0, warnings: 0
module worklib.Add_full_1:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_1:v
      errors: 0, warnings: 0
module worklib.Add_rca_1:v
      errors: 0, warnings: 0
module worklib.Add_rca64_1:v
      errors: 0, warnings: 0
module worklib.Add_half_384:v
      errors: 0, warnings: 0
module worklib.Add_half_383:v
      errors: 0, warnings: 0
module worklib.Add_full_192:v
      errors: 0, warnings: 0
module worklib.Add_half_382:v
      errors: 0, warnings: 0
module worklib.Add_half_381:v
      errors: 0, warnings: 0
module worklib.Add_full_191:v
      errors: 0, warnings: 0
module worklib.Add_half_380:v
      errors: 0, warnings: 0
module worklib.Add_half_379:v
```

```
      errors: 0, warnings: 0
module worklib.Add_full_190:v
      errors: 0, warnings: 0
module worklib.Add_half_378:v
      errors: 0, warnings: 0
module worklib.Add_half_377:v
      errors: 0, warnings: 0
module worklib.Add_full_189:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_48:v
      errors: 0, warnings: 0
module worklib.Add_half_376:v
      errors: 0, warnings: 0
module worklib.Add_half_375:v
      errors: 0, warnings: 0
module worklib.Add_full_188:v
      errors: 0, warnings: 0
module worklib.Add_half_374:v
      errors: 0, warnings: 0
module worklib.Add_half_373:v
      errors: 0, warnings: 0
module worklib.Add_full_187:v
      errors: 0, warnings: 0
module worklib.Add_half_372:v
      errors: 0, warnings: 0
module worklib.Add_half_371:v
      errors: 0, warnings: 0
module worklib.Add_full_186:v
      errors: 0, warnings: 0
module worklib.Add_half_370:v
      errors: 0, warnings: 0
module worklib.Add_half_369:v
      errors: 0, warnings: 0
module worklib.Add_full_185:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_47:v
      errors: 0, warnings: 0
module worklib.Add_half_368:v
      errors: 0, warnings: 0
module worklib.Add_half_367:v
      errors: 0, warnings: 0
module worklib.Add_full_184:v
      errors: 0, warnings: 0
module worklib.Add_half_366:v
      errors: 0, warnings: 0
module worklib.Add_half_365:v
      errors: 0, warnings: 0
module worklib.Add_full_183:v
      errors: 0, warnings: 0
module worklib.Add_half_364:v
      errors: 0, warnings: 0
module worklib.Add_half_363:v
```

```
      errors: 0, warnings: 0
module worklib.Add_full_182:v
      errors: 0, warnings: 0
module worklib.Add_half_362:v
      errors: 0, warnings: 0
module worklib.Add_half_361:v
      errors: 0, warnings: 0
module worklib.Add_full_181:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_46:v
      errors: 0, warnings: 0
module worklib.Add_half_360:v
      errors: 0, warnings: 0
module worklib.Add_half_359:v
      errors: 0, warnings: 0
module worklib.Add_full_180:v
      errors: 0, warnings: 0
module worklib.Add_half_358:v
      errors: 0, warnings: 0
module worklib.Add_half_357:v
      errors: 0, warnings: 0
module worklib.Add_full_179:v
      errors: 0, warnings: 0
module worklib.Add_half_356:v
      errors: 0, warnings: 0
module worklib.Add_half_355:v
      errors: 0, warnings: 0
module worklib.Add_full_178:v
      errors: 0, warnings: 0
module worklib.Add_half_354:v
      errors: 0, warnings: 0
module worklib.Add_half_353:v
      errors: 0, warnings: 0
module worklib.Add_full_177:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_45:v
      errors: 0, warnings: 0
module worklib.Add_half_352:v
      errors: 0, warnings: 0
module worklib.Add_half_351:v
      errors: 0, warnings: 0
module worklib.Add_full_176:v
      errors: 0, warnings: 0
module worklib.Add_half_350:v
      errors: 0, warnings: 0
module worklib.Add_half_349:v
      errors: 0, warnings: 0
module worklib.Add_full_175:v
      errors: 0, warnings: 0
module worklib.Add_half_348:v
      errors: 0, warnings: 0
module worklib.Add_half_347:v
```

```
      errors: 0, warnings: 0
module worklib.Add_full_174:v
      errors: 0, warnings: 0
module worklib.Add_half_346:v
      errors: 0, warnings: 0
module worklib.Add_half_345:v
      errors: 0, warnings: 0
module worklib.Add_full_173:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_44:v
      errors: 0, warnings: 0
module worklib.Add_half_344:v
      errors: 0, warnings: 0
module worklib.Add_half_343:v
      errors: 0, warnings: 0
module worklib.Add_full_172:v
      errors: 0, warnings: 0
module worklib.Add_half_342:v
      errors: 0, warnings: 0
module worklib.Add_half_341:v
      errors: 0, warnings: 0
module worklib.Add_full_171:v
      errors: 0, warnings: 0
module worklib.Add_half_340:v
      errors: 0, warnings: 0
module worklib.Add_half_339:v
      errors: 0, warnings: 0
module worklib.Add_full_170:v
      errors: 0, warnings: 0
module worklib.Add_half_338:v
      errors: 0, warnings: 0
module worklib.Add_half_337:v
      errors: 0, warnings: 0
module worklib.Add_full_169:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_43:v
      errors: 0, warnings: 0
module worklib.Add_half_336:v
      errors: 0, warnings: 0
module worklib.Add_half_335:v
      errors: 0, warnings: 0
module worklib.Add_full_168:v
      errors: 0, warnings: 0
module worklib.Add_half_334:v
      errors: 0, warnings: 0
module worklib.Add_half_333:v
      errors: 0, warnings: 0
module worklib.Add_full_167:v
      errors: 0, warnings: 0
module worklib.Add_half_332:v
      errors: 0, warnings: 0
module worklib.Add_half_331:v
```

```
      errors: 0, warnings: 0
module worklib.Add_full_166:v
      errors: 0, warnings: 0
module worklib.Add_half_330:v
      errors: 0, warnings: 0
module worklib.Add_half_329:v
      errors: 0, warnings: 0
module worklib.Add_full_165:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_42:v
      errors: 0, warnings: 0
module worklib.Add_half_328:v
      errors: 0, warnings: 0
module worklib.Add_half_327:v
      errors: 0, warnings: 0
module worklib.Add_full_164:v
      errors: 0, warnings: 0
module worklib.Add_half_326:v
      errors: 0, warnings: 0
module worklib.Add_half_325:v
      errors: 0, warnings: 0
module worklib.Add_full_163:v
      errors: 0, warnings: 0
module worklib.Add_half_324:v
      errors: 0, warnings: 0
module worklib.Add_half_323:v
      errors: 0, warnings: 0
module worklib.Add_full_162:v
      errors: 0, warnings: 0
module worklib.Add_half_322:v
      errors: 0, warnings: 0
module worklib.Add_half_321:v
      errors: 0, warnings: 0
module worklib.Add_full_161:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_41:v
      errors: 0, warnings: 0
module worklib.Add_rca_6:v
      errors: 0, warnings: 0
module worklib.Add_half_320:v
      errors: 0, warnings: 0
module worklib.Add_half_319:v
      errors: 0, warnings: 0
module worklib.Add_full_160:v
      errors: 0, warnings: 0
module worklib.Add_half_318:v
      errors: 0, warnings: 0
module worklib.Add_half_317:v
      errors: 0, warnings: 0
module worklib.Add_full_159:v
      errors: 0, warnings: 0
module worklib.Add_half_316:v
```

```
      errors: 0, warnings: 0
module worklib.Add_half_315:v
      errors: 0, warnings: 0
module worklib.Add_full_158:v
      errors: 0, warnings: 0
module worklib.Add_half_314:v
      errors: 0, warnings: 0
module worklib.Add_half_313:v
      errors: 0, warnings: 0
module worklib.Add_full_157:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_40:v
      errors: 0, warnings: 0
module worklib.Add_half_312:v
      errors: 0, warnings: 0
module worklib.Add_half_311:v
      errors: 0, warnings: 0
module worklib.Add_full_156:v
      errors: 0, warnings: 0
module worklib.Add_half_310:v
      errors: 0, warnings: 0
module worklib.Add_half_309:v
      errors: 0, warnings: 0
module worklib.Add_full_155:v
      errors: 0, warnings: 0
module worklib.Add_half_308:v
      errors: 0, warnings: 0
module worklib.Add_half_307:v
      errors: 0, warnings: 0
module worklib.Add_full_154:v
      errors: 0, warnings: 0
module worklib.Add_half_306:v
      errors: 0, warnings: 0
module worklib.Add_half_305:v
      errors: 0, warnings: 0
module worklib.Add_full_153:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_39:v
      errors: 0, warnings: 0
module worklib.Add_half_304:v
      errors: 0, warnings: 0
module worklib.Add_half_303:v
      errors: 0, warnings: 0
module worklib.Add_full_152:v
      errors: 0, warnings: 0
module worklib.Add_half_302:v
      errors: 0, warnings: 0
module worklib.Add_half_301:v
      errors: 0, warnings: 0
module worklib.Add_full_151:v
      errors: 0, warnings: 0
module worklib.Add_half_300:v
```

```
      errors: 0, warnings: 0
module worklib.Add_half_299:v
      errors: 0, warnings: 0
module worklib.Add_full_150:v
      errors: 0, warnings: 0
module worklib.Add_half_298:v
      errors: 0, warnings: 0
module worklib.Add_half_297:v
      errors: 0, warnings: 0
module worklib.Add_full_149:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_38:v
      errors: 0, warnings: 0
module worklib.Add_half_296:v
      errors: 0, warnings: 0
module worklib.Add_half_295:v
      errors: 0, warnings: 0
module worklib.Add_full_148:v
      errors: 0, warnings: 0
module worklib.Add_half_294:v
      errors: 0, warnings: 0
module worklib.Add_half_293:v
      errors: 0, warnings: 0
module worklib.Add_full_147:v
      errors: 0, warnings: 0
module worklib.Add_half_292:v
      errors: 0, warnings: 0
module worklib.Add_half_291:v
      errors: 0, warnings: 0
module worklib.Add_full_146:v
      errors: 0, warnings: 0
module worklib.Add_half_290:v
      errors: 0, warnings: 0
module worklib.Add_half_289:v
      errors: 0, warnings: 0
module worklib.Add_full_145:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_37:v
      errors: 0, warnings: 0
module worklib.Add_half_288:v
      errors: 0, warnings: 0
module worklib.Add_half_287:v
      errors: 0, warnings: 0
module worklib.Add_full_144:v
      errors: 0, warnings: 0
module worklib.Add_half_286:v
      errors: 0, warnings: 0
module worklib.Add_half_285:v
      errors: 0, warnings: 0
module worklib.Add_full_143:v
      errors: 0, warnings: 0
module worklib.Add_half_284:v
```

```
      errors: 0, warnings: 0
module worklib.Add_half_283:v
      errors: 0, warnings: 0
module worklib.Add_full_142:v
      errors: 0, warnings: 0
module worklib.Add_half_282:v
      errors: 0, warnings: 0
module worklib.Add_half_281:v
      errors: 0, warnings: 0
module worklib.Add_full_141:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_36:v
      errors: 0, warnings: 0
module worklib.Add_half_280:v
      errors: 0, warnings: 0
module worklib.Add_half_279:v
      errors: 0, warnings: 0
module worklib.Add_full_140:v
      errors: 0, warnings: 0
module worklib.Add_half_278:v
      errors: 0, warnings: 0
module worklib.Add_half_277:v
      errors: 0, warnings: 0
module worklib.Add_full_139:v
      errors: 0, warnings: 0
module worklib.Add_half_276:v
      errors: 0, warnings: 0
module worklib.Add_half_275:v
      errors: 0, warnings: 0
module worklib.Add_full_138:v
      errors: 0, warnings: 0
module worklib.Add_half_274:v
      errors: 0, warnings: 0
module worklib.Add_half_273:v
      errors: 0, warnings: 0
module worklib.Add_full_137:v
      errors: 0, warnings: 0
module worklib.Add_rca_4_35:v
      errors: 0, warnings: 0
module worklib.Add_half_272:v
      errors: 0, warnings: 0
module worklib.Add_half_271:v
      errors: 0, warnings: 0
module worklib.Add_full_136:v
      errors: 0, warnings: 0
module worklib.Add_half_270:v
      errors: 0, warnings: 0
module worklib.Add_half_269:v
      errors: 0, warnings: 0
module worklib.Add_full_135:v
      errors: 0, warnings: 0
module worklib.Add_half_268:v
```

```
            errors: 0, warnings: 0
      module worklib.Add_half_267:v
            errors: 0, warnings: 0
      module worklib.Add_full_134:v
            errors: 0, warnings: 0
      module worklib.Add_half_266:v
            errors: 0, warnings: 0
      module worklib.Add_half_265:v
            errors: 0, warnings: 0
      module worklib.Add_full_133:v
            errors: 0, warnings: 0
      module worklib.Add_rca_4_34:v
            errors: 0, warnings: 0
      module worklib.Add_half_264:v
            errors: 0, warnings: 0
      module worklib.Add_half_263:v
            errors: 0, warnings: 0
      module worklib.Add_full_132:v
            errors: 0, warnings: 0
      module worklib.Add_half_262:v
            errors: 0, warnings: 0
      module worklib.Add_half_261:v
            errors: 0, warnings: 0
      module worklib.Add_full_131:v
            errors: 0, warnings: 0
      module worklib.Add_half_260:v
            errors: 0, warnings: 0
      module worklib.Add_half_259:v
            errors: 0, warnings: 0
      module worklib.Add_full_130:v
            errors: 0, warnings: 0
      module worklib.Add_half_258:v
            errors: 0, warnings: 0
      module worklib.Add_half_257:v
            errors: 0, warnings: 0
      module worklib.Add_full_129:v
            errors: 0, warnings: 0
      module worklib.Add_rca_4_33:v
            errors: 0, warnings: 0
      module worklib.Add_rca_5:v
            errors: 0, warnings: 0
      module worklib.div_DW01_inc_0:v
            errors: 0, warnings: 0
      module worklib.div:v
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CEOX1.tsbvlibp
      module tc240c.CEOX1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CAN2X1.tsbvlibp
      module tc240c.CAN2X1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/COR2X1.tsbvlibp
```

```
      module tc240c.COR2X1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CAN2XL.tsbvlibp
      module tc240c.CAN2XL:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CIVX2.tsbvlibp
      module tc240c.CIVX2:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CENX1.tsbvlibp
      module tc240c.CENX1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CEOXL.tsbvlibp
      module tc240c.CEOXL:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CND2IX1.tsbvlibp
      module tc240c.CND2IX1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CND2XL.tsbvlibp
      module tc240c.CND2XL:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CND2X1.tsbvlibp
      module tc240c.CND2X1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CIVXL.tsbvlibp
      module tc240c.CIVXL:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CIVX1.tsbvlibp
      module tc240c.CIVX1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CNR2X1.tsbvlibp
      module tc240c.CNR2X1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CNR2XL.tsbvlibp
      module tc240c.CNR2XL:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CHA1X1.tsbvlibp
      module tc240c.CHA1X1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CTSX2.tsbvlibp
      module tc240c.CTSX2:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CAOR1X1.tsbvlibp
      module tc240c.CAOR1X1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CAOR2X1.tsbvlibp
      module tc240c.CAOR2X1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CNR8X1.tsbvlibp
      module tc240c.CNR8X1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CFD1QXL.tsbvlibp
      module tc240c.CFD1QXL:tsbvlibp
```

```
           errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CFD1XL.tsbvlibp
     module tc240c.CFD1XL:tsbvlibp
           errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CFD2QXL.tsbvlibp
     module tc240c.CFD2QXL:tsbvlibp
           errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CFD1X1.tsbvlibp
     module tc240c.CFD1X1:tsbvlibp
           errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CFD1QX1.tsbvlibp
     module tc240c.CFD1QX1:tsbvlibp
           errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CAOR1X4.tsbvlibp
     module tc240c.CAOR1X4:tsbvlibp
           errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/COR3X2.tsbvlibp
     module tc240c.COR3X2:tsbvlibp
           errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CAN3X2.tsbvlibp
     module tc240c.CAN3X2:tsbvlibp
           errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/COND1X1.tsbvlibp
     module tc240c.COND1X1:tsbvlibp
           errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CIVDX1.tsbvlibp
     module tc240c.CIVDX1:tsbvlibp
           errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/COAN1X1.tsbvlibp
     module tc240c.COAN1X1:tsbvlibp
           errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CIVDXL.tsbvlibp
     module tc240c.CIVDXL:tsbvlibp
           errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/COND1XL.tsbvlibp
     module tc240c.COND1XL:tsbvlibp
           errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CNR2X2.tsbvlibp
     module tc240c.CNR2X2:tsbvlibp
           errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CDLY1XL.tsbvlibp
     module tc240c.CDLY1XL:tsbvlibp
           errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CNIVX1.tsbvlibp
     module tc240c.CNIVX1:tsbvlibp
           errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CAOR2XL.tsbvlibp
     module tc240c.CAOR2XL:tsbvlibp
           errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CANR2X1.tsbvlibp
     module tc240c.CANR2X1:tsbvlibp
           errors: 0, warnings: 0
```

```
file: /apps/toshiba/sjsu/verilog/tc240c/CND3XL.tsbvlibp
      module tc240c.CND3XL:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/COND4CX1.tsbvlibp
      module tc240c.COND4CX1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/COR3X1.tsbvlibp
      module tc240c.COR3X1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/COND2X1.tsbvlibp
      module tc240c.COND2X1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CNR2IX1.tsbvlibp
      module tc240c.CNR2IX1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/COND3X1.tsbvlibp
      module tc240c.COND3X1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CANR1XL.tsbvlibp
      module tc240c.CANR1XL:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CANR3X1.tsbvlibp
      module tc240c.CANR3X1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CNR3XL.tsbvlibp
      module tc240c.CNR3XL:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CND4X1.tsbvlibp
      module tc240c.CND4X1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/CMXI2X1.tsbvlibp
      module tc240c.CMXI2X1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/COR6X1.tsbvlibp
      module tc240c.COR6X1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/tsbCFD1QXL.tsbvlibp
      module tc240c.tsbCFD1QXL:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/tsbCFD1XL.tsbvlibp
      module tc240c.tsbCFD1XL:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/tsbCFD2QXL.tsbvlibp
      module tc240c.tsbCFD2QXL:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/tsbCFD1X1.tsbvlibp
      module tc240c.tsbCFD1X1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/tsbCFD1QX1.tsbvlibp
      module tc240c.tsbCFD1QX1:tsbvlibp
            errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/TMUX21INVprim.tsbvlibp
```

```
      primitive tc240c.TMUX21INVprim:tsbvlibp
           errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/TFDPNOprim.tsbvlibp
      primitive tc240c.TFDPNOprim:tsbvlibp
           errors: 0, warnings: 0
file: /apps/toshiba/sjsu/verilog/tc240c/TFDPRBNOprim.tsbvlibp
      primitive tc240c.TFDPRBNOprim:tsbvlibp
           errors: 0, warnings: 0
           Caching library 'tc240c' ....... Done
           Caching library 'worklib' ....... Done
      Elaborating the design hierarchy:
  Add_rca_0 M1 ( .sum(w10), .a({1'b0, opera1_not[30:0]}), .b({1'b0,
1'b0, 1'b0,
              |
ncelab: *W,CUVWSP (./div_netlist.v,9807|13): 1 output port was not
connected:
ncelab: (./div_netlist.v,1149): c_out

  Add_rca_7 M6 ( .sum(w13), .a({1'b1, n1293, n1295, n1296, n1297,
n1298, n1299,
              |
ncelab: *W,CUVWSP (./div_netlist.v,9811|13): 1 output port was not
connected:
ncelab: (./div_netlist.v,2323): c_out

  Add_rca64_0 M2 ( .sum(w11), .a({1'b0, n1216, n1215, n1214, n1213,
n1212,
               |
ncelab: *W,CUVWSP (./div_netlist.v,9818|15): 1 output port was not
connected:
ncelab: (./div_netlist.v,4698): c_out

  Add_rca64_1 M4 ( .sum(w12), .a(result_not), .b({1'b0, 1'b0, 1'b0,
1'b0, 1'b0,
               |
ncelab: *W,CUVWSP (./div_netlist.v,9831|15): 1 output port was not
connected:
ncelab: (./div_netlist.v,7051): c_out

  Add_rca_6 M3 ( .sum(w1), .a(opera1_copy), .b({n1142, D[30:0]}),
.c_in(1'b0)
              |
ncelab: *W,CUVWSP (./div_netlist.v,9838|13): 1 output port was not
connected:
ncelab: (./div_netlist.v,8211): c_out

  Add_rca_5 M5 ( .sum(w9), .a(opera1_copydiv), .b({n1142, D[30:0]}),
.c_in(
              |
ncelab: *W,CUVWSP (./div_netlist.v,9840|13): 1 output port was not
connected:
ncelab: (./div_netlist.v,9381): c_out
```

```
  CFD1XL \nest_reg[1]  ( .D(n777), .CP(clock), .QN(n1322) );
                       |
ncelab: *W,CUVWSP (./div_netlist.v,9910|21): 1 output port was not
connected:
ncelab: (/apps/toshiba/sjsu/verilog/tc240c/CFD1XL.tsbvlibp,7): Q

  CFD1XL \nest_reg[2]  ( .D(n776), .CP(clock), .QN(n1323) );
                       |
ncelab: *W,CUVWSP (./div_netlist.v,9911|21): 1 output port was not
connected:
ncelab: (/apps/toshiba/sjsu/verilog/tc240c/CFD1XL.tsbvlibp,7): Q

  CFD1XL \result_copy_reg[31]  ( .D(n710), .CP(clock), .QN(n1355) );
                               |
ncelab: *W,CUVWSP (./div_netlist.v,9944|29): 1 output port was not
connected:
ncelab: (/apps/toshiba/sjsu/verilog/tc240c/CFD1XL.tsbvlibp,7): Q

  CFD1XL \result_copy_reg[63]  ( .D(n743), .CP(clock), .Q(n1142) );
                               |
ncelab: *W,CUVWSP (./div_netlist.v,10162|29): 1 output port was not
connected:
ncelab: (/apps/toshiba/sjsu/verilog/tc240c/CFD1XL.tsbvlibp,7): QN

      Building instance overlay tables: ..................... Done
      Generating native compiled code:
            tc240c.CANR1XL:tsbvlibp <0x5b3d9c36>
                  streams:   0, words:     0
            tc240c.CANR2X1:tsbvlibp <0x759f56f5>
                  streams:   0, words:     0
            tc240c.CANR3X1:tsbvlibp <0x7323d4f3>
                  streams:   0, words:     0
            tc240c.CAOR1X1:tsbvlibp <0x108972c0>
                  streams:   0, words:     0
            tc240c.CAOR1X4:tsbvlibp <0x7b66be3c>
                  streams:   0, words:     0
            tc240c.CAOR2X1:tsbvlibp <0x638225ab>
                  streams:   0, words:     0
            tc240c.CAOR2XL:tsbvlibp <0x79bd3f40>
                  streams:   0, words:     0
            tc240c.CENX1:tsbvlibp <0x0fa8523d>
                  streams:   0, words:     0
            tc240c.CEOX1:tsbvlibp <0x4400a8d7>
                  streams:   0, words:     0
            tc240c.CEOXL:tsbvlibp <0x098af818>
                  streams:   0, words:     0
            tc240c.CHA1X1:tsbvlibp <0x30760590>
                  streams:   0, words:     0
            tc240c.CMXI2X1:tsbvlibp <0x21a930df>
                  streams:   0, words:     0
            tc240c.COAN1X1:tsbvlibp <0x456fa7fe>
```

```
                streams:   0, words:     0
              tc240c.COND1X1:tsbvlibp <0x69c0ce76>
                streams:   0, words:     0
              tc240c.COND1XL:tsbvlibp <0x36ede661>
                streams:   0, words:     0
              tc240c.COND2X1:tsbvlibp <0x71b9bf6b>
                streams:   0, words:     0
              tc240c.COND3X1:tsbvlibp <0x3c28d710>
                streams:   0, words:     0
              tc240c.COND4CX1:tsbvlibp <0x460c0bc5>
                streams:   0, words:     0
              tc240c.tsbCFD1QX1:tsbvlibp <0x1f1b900c>
                streams:   0, words:     0
              tc240c.tsbCFD1QXL:tsbvlibp <0x0755e884>
                streams:   0, words:     0
              tc240c.tsbCFD1X1:tsbvlibp <0x277249fa>
                streams:   0, words:     0
              tc240c.tsbCFD1XL:tsbvlibp <0x355406e0>
                streams:   0, words:     0
              tc240c.tsbCFD2QXL:tsbvlibp <0x5e553f7b>
                streams:   0, words:     0
              worklib.Add_rca64_0:v <0x73760c11>
                streams:   2, words:   409
              worklib.Add_rca64_1:v <0x78f25dd2>
                streams:   2, words:   409
              worklib.div:v <0x641238cc>
                streams:   2, words:   324
              worklib.test_div:v <0x467a758f>
                streams:  11, words: 12219
        Building instance specific data structures.
        Loading native compiled code:     ..................... Done
        Design hierarchy summary:
                               Instances  Unique
              Modules:              3801     899
              UDPs:                  298       3
              Primitives:           9643      10
              Timing outputs:       2730      29
              Registers:             303      13
              Scalar wires:         3049       -
              Expanded wires:        288       8
              Vectored wires:          2       -
              Initial blocks:          4       4
              Pseudo assignments:     12      12
              Timing checks:        1791     602
              Simulation timescale:  10ps
        Writing initial simulation snapshot: worklib.test_div:v
Loading snapshot worklib.test_div:v ..................... Done
ncsim> source /apps/cadence/INCISIV141/tools/inca/files/ncsimrc
ncsim> run
                    0 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxxx,
start=x, clock=0, muordi=1, reset=x, valid=x, result=xxxxxxxxxxxxxxxx
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                  10 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxxx,
start=x, clock=1, muordi=1, reset=x, valid=x, result=xxxxxxxxxxxxxxxx
                  20 opera1=xxxxxxxx, opera2=xxxxxxxxxxxxxxxx,
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Warning!  Timing violation
            $hold( posedge CP &&& D_CD_low:3110 NS, CD:3110100 PS,
0.52 : 520 PS );
             File:
/apps/toshiba/sjsu/verilog/tc240c/tsbCFD2QXL.tsbvlibp, line = 32
            Scope: test_div.M1.\cust_reg[2] .tsbCFD2QXL_1
             Time: 3110100 PS

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                8210 opera1=cbcbcbcc, opera2=ebcdebcdebdcebdd,
start=0, clock=1, muordi=1, reset=0, valid=1, result=2a572a576309457f
                8220 opera1=cbcbcbcc, opera2=ebcdebcdebdcebdd,
start=0, clock=0, muordi=1, reset=0, valid=1, result=2a572a576309457f
                8230 opera1=cbcbcbcc, opera2=ebcdebcdebdcebdd,
start=0, clock=1, muordi=1, reset=0, valid=1, result=2a572a576309457f
                8240 opera1=cbcbcbcc, opera2=ebcdebcdebdcebdd,
start=0, clock=0, muordi=1, reset=0, valid=1, result=2a572a576309457f
                8250 opera1=cbcbcbcc, opera2=ebcdebcdebdcebdd,
start=0, clock=1, muordi=1, reset=0, valid=1, result=2a572a576309457f
Simulation complete via $finish(1) at time 8260 NS + 0
./testdiv.v:86 #2000 $finish;
ncsim> exit
```

C.3 Contents of Selected Reports from Synthesis (Design Compiler)

For Multiplier:

```
Inferred memory devices in process
      in routine mul line 70 in file
            './mul.v'.
===============================================================================
==
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST
|
===============================================================================
==
|      cust_reg       | Flip-flop |   3   |  Y  | N  | Y  | N  | N  | N  | N
|
===============================================================================
==

Inferred memory devices in process
      in routine mul line 92 in file
            './mul.v'.
===============================================================================
==
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST
|
===============================================================================
==
|        i_reg        | Flip-flop |  32   |  Y  | N  | N  | N  | N  | N  | N
|
|   opera1_copy_reg   | Flip-flop |  32   |  Y  | N  | N  | N  | N  | N  | N
|
|       w4_reg        | Flip-flop |   1   |  N  | N  | N  | N  | N  | N  | N
|
|     result_reg      | Flip-flop |  64   |  Y  | N  | N  | N  | N  | N  | N
|
|   result_copy_reg   | Flip-flop |  64   |  N  | N  | N  | N  | N  | N  | N
|
|   result_not_reg    | Flip-flop |  64   |  Y  | N  | N  | N  | N  | N  | N
|
|      valid_reg      | Flip-flop |   1   |  N  | N  | N  | N  | N  | N  | N
|
|      nest_reg       | Flip-flop |   3   |  N  | N  | N  | N  | N  | N  | N
|
===============================================================================
==

Inferred tri-state devices in process
      in routine mul line 30 in file
            './mul.v'.
================================================
| Register Name |       Type       | Width | MB |
================================================
|      A1       | Tri-State Buffer |   1   | N  |
================================================
```

```
Inferred tri-state devices in process
      in routine mul line 32 in file
            './mul.v'.
===============================================
| Register Name |       Type       | Width | MB |
===============================================
|      A5       | Tri-State Buffer |   1   | N  |
===============================================

Inferred tri-state devices in process
      in routine mul line 34 in file
            './mul.v'.
===============================================
| Register Name |       Type       | Width | MB |
===============================================
|      A7       | Tri-State Buffer |   1   | N  |
===============================================

Inferred tri-state devices in process
      in routine mul line 31 in file
            './mul.v'.
===============================================
| Register Name |       Type       | Width | MB |
===============================================
|      A2       | Tri-State Buffer |   1   | N  |
===============================================

Inferred tri-state devices in process
      in routine mul line 33 in file
            './mul.v'.
===============================================
| Register Name |       Type       | Width | MB |
===============================================
|      A6       | Tri-State Buffer |   1   | N  |
===============================================

Inferred tri-state devices in process
      in routine mul line 35 in file
            './mul.v'.
===============================================
| Register Name |       Type       | Width | MB |
===============================================
|      A8       | Tri-State Buffer |   1   | N  |
===============================================
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : mul
Version: C-2009.06-SP5
Date   : Sun Dec 11 06:21:51 2016
****************************************

Operating Conditions: WCCOM25   Library: tc240c
Wire Load Model Mode: top
```

```
Startpoint: w4_reg (rising edge-triggered flip-flop clocked by clock)
Endpoint: result_reg[63]
          (rising edge-triggered flip-flop clocked by clock)
Path Group: clock
Path Type: max

Point                                          Incr       Path
-----------------------------------------------------------------
clock clock (rise edge)                        0.00       0.00
clock network delay (propagated)               0.00       0.00
w4_reg/CP (CFD1QX2)                            0.00       0.00 r
w4_reg/Q (CFD1QX2)                             0.42       0.42 f
U1066/Z (CIVX2)                                0.07       0.50 r
A8/Z (CTSX2)                                   0.27       0.77 f
M4/c_in (Add_rca64_1)                          0.00       0.77 f
M4/M1/c_in (Add_rca_2)                         0.00       0.77 f
M4/M1/M1/c_in (Add_rca_4_16)                   0.00       0.77 f
M4/M1/M1/M1/c_in (Add_full_64)                 0.00       0.77 f
M4/M1/M1/M1/M2/b (Add_half_127)                0.00       0.77 f
M4/M1/M1/M1/M2/U3/Z (CIVX2)                    0.05       0.82 r
M4/M1/M1/M1/M2/U2/Z (CNR2X1)                   0.07       0.89 f
M4/M1/M1/M1/M2/c_out (Add_half_127)            0.00       0.89 f
M4/M1/M1/M1/U2/Z (CND2IX1)                     0.19       1.08 f
M4/M1/M1/M1/c_out (Add_full_64)                0.00       1.08 f
M4/M1/M1/M2/c_in (Add_full_63)                 0.00       1.08 f
M4/M1/M1/M2/M2/b (Add_half_125)                0.00       1.08 f
M4/M1/M1/M2/M2/U2/Z (CAN2X1)                   0.18       1.25 f
M4/M1/M1/M2/M2/c_out (Add_half_125)            0.00       1.25 f
M4/M1/M1/M2/U2/Z (CND2IX1)                     0.19       1.44 f
M4/M1/M1/M2/c_out (Add_full_63)                0.00       1.44 f
M4/M1/M1/M3/c_in (Add_full_62)                 0.00       1.44 f
M4/M1/M1/M3/M2/b (Add_half_123)                0.00       1.44 f
M4/M1/M1/M3/M2/U2/Z (CAN2X1)                   0.18       1.62 f
M4/M1/M1/M3/M2/c_out (Add_half_123)            0.00       1.62 f
M4/M1/M1/M3/U2/Z (CND2IX1)                     0.19       1.80 f
M4/M1/M1/M3/c_out (Add_full_62)                0.00       1.80 f
M4/M1/M1/M4/c_in (Add_full_61)                 0.00       1.80 f
M4/M1/M1/M4/M2/b (Add_half_121)                0.00       1.80 f
M4/M1/M1/M4/M2/U2/Z (CAN2X1)                   0.18       1.98 f
M4/M1/M1/M4/M2/c_out (Add_half_121)            0.00       1.98 f
M4/M1/M1/M4/U2/Z (CND2IX1)                     0.19       2.16 f
M4/M1/M1/M4/c_out (Add_full_61)                0.00       2.16 f
M4/M1/M1/c_out (Add_rca_4_16)                  0.00       2.16 f
M4/M1/M2/c_in (Add_rca_4_15)                   0.00       2.16 f
M4/M1/M2/M1/c_in (Add_full_60)                 0.00       2.16 f
M4/M1/M2/M1/M2/b (Add_half_119)                0.00       2.16 f
M4/M1/M2/M1/M2/U2/Z (CAN2X1)                   0.18       2.34 f
M4/M1/M2/M1/M2/c_out (Add_half_119)            0.00       2.34 f
M4/M1/M2/M1/U2/Z (CND2IX1)                     0.19       2.52 f
M4/M1/M2/M1/c_out (Add_full_60)                0.00       2.52 f
M4/M1/M2/M2/c_in (Add_full_59)                 0.00       2.52 f
M4/M1/M2/M2/M2/b (Add_half_117)                0.00       2.52 f
M4/M1/M2/M2/M2/U2/Z (CAN2X1)                   0.18       2.70 f
M4/M1/M2/M2/M2/c_out (Add_half_117)            0.00       2.70 f
M4/M1/M2/M2/U2/Z (CND2IX1)                     0.19       2.88 f
M4/M1/M2/M2/c_out (Add_full_59)                0.00       2.88 f
M4/M1/M2/M3/c_in (Add_full_58)                 0.00       2.88 f
```

```
M4/M1/M2/M3/M2/b (Add_half_115)          0.00       2.88 f
M4/M1/M2/M3/M2/U2/Z (CAN2X1)             0.18       3.06 f
M4/M1/M2/M3/M2/c_out (Add_half_115)      0.00       3.06 f
M4/M1/M2/M3/U2/Z (CND2IX1)               0.19       3.25 f
M4/M1/M2/M3/c_out (Add_full_58)          0.00       3.25 f
M4/M1/M2/M4/c_in (Add_full_57)           0.00       3.25 f
M4/M1/M2/M4/M2/b (Add_half_113)          0.00       3.25 f
M4/M1/M2/M4/M2/U2/Z (CAN2X1)             0.18       3.42 f
M4/M1/M2/M4/M2/c_out (Add_half_113)      0.00       3.42 f
M4/M1/M2/M4/U2/Z (CND2IX1)               0.19       3.61 f
M4/M1/M2/M4/c_out (Add_full_57)          0.00       3.61 f
M4/M1/M2/c_out (Add_rca_4_15)            0.00       3.61 f
M4/M1/M3/c_in (Add_rca_4_14)             0.00       3.61 f
M4/M1/M3/M1/c_in (Add_full_56)           0.00       3.61 f
M4/M1/M3/M1/M2/b (Add_half_111)          0.00       3.61 f
M4/M1/M3/M1/M2/U2/Z (CAN2X1)             0.18       3.78 f
M4/M1/M3/M1/M2/c_out (Add_half_111)      0.00       3.78 f
M4/M1/M3/M1/U2/Z (CND2IX1)               0.19       3.97 f
M4/M1/M3/M1/c_out (Add_full_56)          0.00       3.97 f
M4/M1/M3/M2/c_in (Add_full_55)           0.00       3.97 f
M4/M1/M3/M2/M2/b (Add_half_109)          0.00       3.97 f
M4/M1/M3/M2/M2/U2/Z (CAN2X1)             0.18       4.15 f
M4/M1/M3/M2/M2/c_out (Add_half_109)      0.00       4.15 f
M4/M1/M3/M2/U2/Z (CND2IX1)               0.19       4.33 f
M4/M1/M3/M2/c_out (Add_full_55)          0.00       4.33 f
M4/M1/M3/M3/c_in (Add_full_54)           0.00       4.33 f
M4/M1/M3/M3/M2/b (Add_half_107)          0.00       4.33 f
M4/M1/M3/M3/M2/U2/Z (CAN2X1)             0.18       4.51 f
M4/M1/M3/M3/M2/c_out (Add_half_107)      0.00       4.51 f
M4/M1/M3/M3/U2/Z (CND2IX1)               0.19       4.69 f
M4/M1/M3/M3/c_out (Add_full_54)          0.00       4.69 f
M4/M1/M3/M4/c_in (Add_full_53)           0.00       4.69 f
M4/M1/M3/M4/M2/b (Add_half_105)          0.00       4.69 f
M4/M1/M3/M4/M2/U2/Z (CAN2X1)             0.18       4.87 f
M4/M1/M3/M4/M2/c_out (Add_half_105)      0.00       4.87 f
M4/M1/M3/M4/U1/Z (COR2X1)                0.26       5.13 f
M4/M1/M3/M4/c_out (Add_full_53)          0.00       5.13 f
M4/M1/M3/c_out (Add_rca_4_14)            0.00       5.13 f
M4/M1/M4/c_in (Add_rca_4_13)             0.00       5.13 f
M4/M1/M4/M1/c_in (Add_full_52)           0.00       5.13 f
M4/M1/M4/M1/M2/b (Add_half_103)          0.00       5.13 f
M4/M1/M4/M1/M2/U2/Z (CAN2X1)             0.18       5.31 f
M4/M1/M4/M1/M2/c_out (Add_half_103)      0.00       5.31 f
M4/M1/M4/M1/U1/Z (COR2X1)                0.26       5.57 f
M4/M1/M4/M1/c_out (Add_full_52)          0.00       5.57 f
M4/M1/M4/M2/c_in (Add_full_51)           0.00       5.57 f
M4/M1/M4/M2/M2/b (Add_half_101)          0.00       5.57 f
M4/M1/M4/M2/M2/U2/Z (CAN2X1)             0.18       5.75 f
M4/M1/M4/M2/M2/c_out (Add_half_101)      0.00       5.75 f
M4/M1/M4/M2/U1/Z (COR2X1)                0.26       6.01 f
M4/M1/M4/M2/c_out (Add_full_51)          0.00       6.01 f
M4/M1/M4/M3/c_in (Add_full_50)           0.00       6.01 f
M4/M1/M4/M3/M2/b (Add_half_99)           0.00       6.01 f
M4/M1/M4/M3/M2/U2/Z (CAN2X1)             0.18       6.18 f
M4/M1/M4/M3/M2/c_out (Add_half_99)       0.00       6.18 f
M4/M1/M4/M3/U1/Z (COR2X1)                0.26       6.45 f
M4/M1/M4/M3/c_out (Add_full_50)          0.00       6.45 f
```

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M4/M1/M4/M4/c_in (Add_full_49)           0.00       6.45 f
M4/M1/M4/M4/M2/b (Add_half_97)           0.00       6.45 f
M4/M1/M4/M4/M2/U2/Z (CAN2X1)             0.18       6.62 f
M4/M1/M4/M4/M2/c_out (Add_half_97)       0.00       6.62 f
M4/M1/M4/M4/U1/Z (COR2X1)                0.26       6.89 f
M4/M1/M4/M4/c_out (Add_full_49)          0.00       6.89 f
M4/M1/M4/c_out (Add_rca_4_13)            0.00       6.89 f
M4/M1/M5/c_in (Add_rca_4_12)             0.00       6.89 f
M4/M1/M5/M1/c_in (Add_full_48)           0.00       6.89 f
M4/M1/M5/M1/M2/b (Add_half_95)           0.00       6.89 f
M4/M1/M5/M1/M2/U2/Z (CAN2X1)             0.18       7.06 f
M4/M1/M5/M1/M2/c_out (Add_half_95)       0.00       7.06 f
M4/M1/M5/M1/U1/Z (COR2X1)                0.26       7.32 f
M4/M1/M5/M1/c_out (Add_full_48)          0.00       7.32 f
M4/M1/M5/M2/c_in (Add_full_47)           0.00       7.32 f
M4/M1/M5/M2/M2/b (Add_half_93)           0.00       7.32 f
M4/M1/M5/M2/M2/U2/Z (CAN2X1)             0.18       7.50 f
M4/M1/M5/M2/M2/c_out (Add_half_93)       0.00       7.50 f
M4/M1/M5/M2/U1/Z (COR2X1)                0.26       7.76 f
M4/M1/M5/M2/c_out (Add_full_47)          0.00       7.76 f
M4/M1/M5/M3/c_in (Add_full_46)           0.00       7.76 f
M4/M1/M5/M3/M2/b (Add_half_91)           0.00       7.76 f
M4/M1/M5/M3/M2/U2/Z (CAN2X1)             0.18       7.94 f
M4/M1/M5/M3/M2/c_out (Add_half_91)       0.00       7.94 f
M4/M1/M5/M3/U1/Z (COR2X1)                0.26       8.20 f
M4/M1/M5/M3/c_out (Add_full_46)          0.00       8.20 f
M4/M1/M5/M4/c_in (Add_full_45)           0.00       8.20 f
M4/M1/M5/M4/M2/b (Add_half_89)           0.00       8.20 f
M4/M1/M5/M4/M2/U2/Z (CAN2X1)             0.18       8.38 f
M4/M1/M5/M4/M2/c_out (Add_half_89)       0.00       8.38 f
M4/M1/M5/M4/U1/Z (COR2X1)                0.26       8.64 f
M4/M1/M5/M4/c_out (Add_full_45)          0.00       8.64 f
M4/M1/M5/c_out (Add_rca_4_12)            0.00       8.64 f
M4/M1/M6/c_in (Add_rca_4_11)             0.00       8.64 f
M4/M1/M6/M1/c_in (Add_full_44)           0.00       8.64 f
M4/M1/M6/M1/M2/b (Add_half_87)           0.00       8.64 f
M4/M1/M6/M1/M2/U2/Z (CAN2X1)             0.18       8.82 f
M4/M1/M6/M1/M2/c_out (Add_half_87)       0.00       8.82 f
M4/M1/M6/M1/U1/Z (COR2X1)                0.26       9.08 f
M4/M1/M6/M1/c_out (Add_full_44)          0.00       9.08 f
M4/M1/M6/M2/c_in (Add_full_43)           0.00       9.08 f
M4/M1/M6/M2/M2/b (Add_half_85)           0.00       9.08 f
M4/M1/M6/M2/M2/U2/Z (CAN2X1)             0.18       9.25 f
M4/M1/M6/M2/M2/c_out (Add_half_85)       0.00       9.25 f
M4/M1/M6/M2/U1/Z (COR2X1)                0.26       9.52 f
M4/M1/M6/M2/c_out (Add_full_43)          0.00       9.52 f
M4/M1/M6/M3/c_in (Add_full_42)           0.00       9.52 f
M4/M1/M6/M3/M2/b (Add_half_83)           0.00       9.52 f
M4/M1/M6/M3/M2/U2/Z (CAN2X1)             0.18       9.69 f
M4/M1/M6/M3/M2/c_out (Add_half_83)       0.00       9.69 f
M4/M1/M6/M3/U1/Z (COR2X1)                0.26       9.96 f
M4/M1/M6/M3/c_out (Add_full_42)          0.00       9.96 f
M4/M1/M6/M4/c_in (Add_full_41)           0.00       9.96 f
M4/M1/M6/M4/M2/b (Add_half_81)           0.00       9.96 f
M4/M1/M6/M4/M2/U2/Z (CAN2X1)             0.18      10.13 f
M4/M1/M6/M4/M2/c_out (Add_half_81)       0.00      10.13 f
M4/M1/M6/M4/U1/Z (COR2X1)                0.26      10.39 f
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```
M4/M1/M6/M4/c_out (Add_full_41)          0.00      10.39 f
M4/M1/M6/c_out (Add_rca_4_11)            0.00      10.39 f
M4/M1/M7/c_in (Add_rca_4_10)             0.00      10.39 f
M4/M1/M7/M1/c_in (Add_full_40)           0.00      10.39 f
M4/M1/M7/M1/M2/b (Add_half_79)           0.00      10.39 f
M4/M1/M7/M1/M2/U2/Z (CAN2X1)             0.18      10.57 f
M4/M1/M7/M1/M2/c_out (Add_half_79)       0.00      10.57 f
M4/M1/M7/M1/U1/Z (COR2X1)                0.26      10.83 f
M4/M1/M7/M1/c_out (Add_full_40)          0.00      10.83 f
M4/M1/M7/M2/c_in (Add_full_39)           0.00      10.83 f
M4/M1/M7/M2/M2/b (Add_half_77)           0.00      10.83 f
M4/M1/M7/M2/M2/U2/Z (CAN2X1)             0.18      11.01 f
M4/M1/M7/M2/M2/c_out (Add_half_77)       0.00      11.01 f
M4/M1/M7/M2/U1/Z (COR2X1)                0.26      11.27 f
M4/M1/M7/M2/c_out (Add_full_39)          0.00      11.27 f
M4/M1/M7/M3/c_in (Add_full_38)           0.00      11.27 f
M4/M1/M7/M3/M2/b (Add_half_75)           0.00      11.27 f
M4/M1/M7/M3/M2/U2/Z (CAN2X1)             0.18      11.45 f
M4/M1/M7/M3/M2/c_out (Add_half_75)       0.00      11.45 f
M4/M1/M7/M3/U1/Z (COR2X1)                0.26      11.71 f
M4/M1/M7/M3/c_out (Add_full_38)          0.00      11.71 f
M4/M1/M7/M4/c_in (Add_full_37)           0.00      11.71 f
M4/M1/M7/M4/M2/b (Add_half_73)           0.00      11.71 f
M4/M1/M7/M4/M2/U2/Z (CAN2X1)             0.18      11.89 f
M4/M1/M7/M4/M2/c_out (Add_half_73)       0.00      11.89 f
M4/M1/M7/M4/U1/Z (COR2X1)                0.26      12.15 f
M4/M1/M7/M4/c_out (Add_full_37)          0.00      12.15 f
M4/M1/M7/c_out (Add_rca_4_10)            0.00      12.15 f
M4/M1/M8/c_in (Add_rca_4_9)              0.00      12.15 f
M4/M1/M8/M1/c_in (Add_full_36)           0.00      12.15 f
M4/M1/M8/M1/M2/b (Add_half_71)           0.00      12.15 f
M4/M1/M8/M1/M2/U2/Z (CAN2X1)             0.18      12.32 f
M4/M1/M8/M1/M2/c_out (Add_half_71)       0.00      12.32 f
M4/M1/M8/M1/U1/Z (COR2X1)                0.26      12.59 f
M4/M1/M8/M1/c_out (Add_full_36)          0.00      12.59 f
M4/M1/M8/M2/c_in (Add_full_35)           0.00      12.59 f
M4/M1/M8/M2/M2/b (Add_half_69)           0.00      12.59 f
M4/M1/M8/M2/M2/U2/Z (CAN2X1)             0.18      12.76 f
M4/M1/M8/M2/M2/c_out (Add_half_69)       0.00      12.76 f
M4/M1/M8/M2/U1/Z (COR2X1)                0.26      13.03 f
M4/M1/M8/M2/c_out (Add_full_35)          0.00      13.03 f
M4/M1/M8/M3/c_in (Add_full_34)           0.00      13.03 f
M4/M1/M8/M3/M2/b (Add_half_67)           0.00      13.03 f
M4/M1/M8/M3/M2/U2/Z (CAN2X1)             0.18      13.20 f
M4/M1/M8/M3/M2/c_out (Add_half_67)       0.00      13.20 f
M4/M1/M8/M3/U1/Z (COR2X1)                0.26      13.46 f
M4/M1/M8/M3/c_out (Add_full_34)          0.00      13.46 f
M4/M1/M8/M4/c_in (Add_full_33)           0.00      13.46 f
M4/M1/M8/M4/M2/b (Add_half_65)           0.00      13.46 f
M4/M1/M8/M4/M2/U2/Z (CAN2X1)             0.18      13.64 f
M4/M1/M8/M4/M2/c_out (Add_half_65)       0.00      13.64 f
M4/M1/M8/M4/U1/Z (COR2X1)                0.26      13.90 f
M4/M1/M8/M4/c_out (Add_full_33)          0.00      13.90 f
M4/M1/M8/c_out (Add_rca_4_9)             0.00      13.90 f
M4/M1/c_out (Add_rca_2)                  0.00      13.90 f
M4/M2/c_in (Add_rca_1)                   0.00      13.90 f
M4/M2/M1/c_in (Add_rca_4_8)              0.00      13.90 f
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M4/M2/M1/M1/c_in (Add_full_32)           0.00      13.90 f
M4/M2/M1/M1/M2/b (Add_half_63)           0.00      13.90 f
M4/M2/M1/M1/M2/U2/Z (CAN2X1)             0.18      14.08 f
M4/M2/M1/M1/M2/c_out (Add_half_63)       0.00      14.08 f
M4/M2/M1/M1/U1/Z (COR2X1)                0.26      14.34 f
M4/M2/M1/M1/c_out (Add_full_32)          0.00      14.34 f
M4/M2/M1/M2/c_in (Add_full_31)           0.00      14.34 f
M4/M2/M1/M2/M2/b (Add_half_61)           0.00      14.34 f
M4/M2/M1/M2/M2/U2/Z (CAN2X1)             0.18      14.52 f
M4/M2/M1/M2/M2/c_out (Add_half_61)       0.00      14.52 f
M4/M2/M1/M2/U1/Z (COR2X1)                0.26      14.78 f
M4/M2/M1/M2/c_out (Add_full_31)          0.00      14.78 f
M4/M2/M1/M3/c_in (Add_full_30)           0.00      14.78 f
M4/M2/M1/M3/M2/b (Add_half_59)           0.00      14.78 f
M4/M2/M1/M3/M2/U2/Z (CAN2X1)             0.18      14.96 f
M4/M2/M1/M3/M2/c_out (Add_half_59)       0.00      14.96 f
M4/M2/M1/M3/U1/Z (COR2X1)                0.26      15.22 f
M4/M2/M1/M3/c_out (Add_full_30)          0.00      15.22 f
M4/M2/M1/M4/c_in (Add_full_29)           0.00      15.22 f
M4/M2/M1/M4/M2/b (Add_half_57)           0.00      15.22 f
M4/M2/M1/M4/M2/U2/Z (CAN2X1)             0.18      15.39 f
M4/M2/M1/M4/M2/c_out (Add_half_57)       0.00      15.39 f
M4/M2/M1/M4/U1/Z (COR2X1)                0.26      15.66 f
M4/M2/M1/M4/c_out (Add_full_29)          0.00      15.66 f
M4/M2/M1/c_out (Add_rca_4_8)             0.00      15.66 f
M4/M2/M2/c_in (Add_rca_4_7)              0.00      15.66 f
M4/M2/M2/M1/c_in (Add_full_28)           0.00      15.66 f
M4/M2/M2/M1/M2/b (Add_half_55)           0.00      15.66 f
M4/M2/M2/M1/M2/U2/Z (CAN2X1)             0.18      15.83 f
M4/M2/M2/M1/M2/c_out (Add_half_55)       0.00      15.83 f
M4/M2/M2/M1/U1/Z (COR2X1)                0.26      16.10 f
M4/M2/M2/M1/c_out (Add_full_28)          0.00      16.10 f
M4/M2/M2/M2/c_in (Add_full_27)           0.00      16.10 f
M4/M2/M2/M2/M2/b (Add_half_53)           0.00      16.10 f
M4/M2/M2/M2/M2/U2/Z (CAN2X1)             0.18      16.27 f
M4/M2/M2/M2/M2/c_out (Add_half_53)       0.00      16.27 f
M4/M2/M2/M2/U1/Z (COR2X1)                0.26      16.53 f
M4/M2/M2/M2/c_out (Add_full_27)          0.00      16.53 f
M4/M2/M2/M3/c_in (Add_full_26)           0.00      16.53 f
M4/M2/M2/M3/M2/b (Add_half_51)           0.00      16.53 f
M4/M2/M2/M3/M2/U2/Z (CAN2X1)             0.18      16.71 f
M4/M2/M2/M3/M2/c_out (Add_half_51)       0.00      16.71 f
M4/M2/M2/M3/U1/Z (COR2X1)                0.26      16.97 f
M4/M2/M2/M3/c_out (Add_full_26)          0.00      16.97 f
M4/M2/M2/M4/c_in (Add_full_25)           0.00      16.97 f
M4/M2/M2/M4/M2/b (Add_half_49)           0.00      16.97 f
M4/M2/M2/M4/M2/U2/Z (CAN2X1)             0.18      17.15 f
M4/M2/M2/M4/M2/c_out (Add_half_49)       0.00      17.15 f
M4/M2/M2/M4/U1/Z (COR2X1)                0.26      17.41 f
M4/M2/M2/M4/c_out (Add_full_25)          0.00      17.41 f
M4/M2/M2/c_out (Add_rca_4_7)             0.00      17.41 f
M4/M2/M3/c_in (Add_rca_4_6)              0.00      17.41 f
M4/M2/M3/M1/c_in (Add_full_24)           0.00      17.41 f
M4/M2/M3/M1/M2/b (Add_half_47)           0.00      17.41 f
M4/M2/M3/M1/M2/U2/Z (CAN2X1)             0.18      17.59 f
M4/M2/M3/M1/M2/c_out (Add_half_47)       0.00      17.59 f
M4/M2/M3/M1/U1/Z (COR2X1)                0.26      17.85 f
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M4/M2/M3/M1/c_out (Add_full_24)          0.00      17.85 f
M4/M2/M3/M2/c_in (Add_full_23)           0.00      17.85 f
M4/M2/M3/M2/M2/b (Add_half_45)           0.00      17.85 f
M4/M2/M3/M2/M2/U2/Z (CAN2X1)             0.18      18.03 f
M4/M2/M3/M2/M2/c_out (Add_half_45)       0.00      18.03 f
M4/M2/M3/M2/U1/Z (COR2X1)                0.26      18.29 f
M4/M2/M3/M2/c_out (Add_full_23)          0.00      18.29 f
M4/M2/M3/M3/c_in (Add_full_22)           0.00      18.29 f
M4/M2/M3/M3/M2/b (Add_half_43)           0.00      18.29 f
M4/M2/M3/M3/M2/U2/Z (CAN2X1)             0.18      18.46 f
M4/M2/M3/M3/M2/c_out (Add_half_43)       0.00      18.46 f
M4/M2/M3/M3/U1/Z (COR2X1)                0.26      18.73 f
M4/M2/M3/M3/c_out (Add_full_22)          0.00      18.73 f
M4/M2/M3/M4/c_in (Add_full_21)           0.00      18.73 f
M4/M2/M3/M4/M2/b (Add_half_41)           0.00      18.73 f
M4/M2/M3/M4/M2/U2/Z (CAN2X1)             0.18      18.90 f
M4/M2/M3/M4/M2/c_out (Add_half_41)       0.00      18.90 f
M4/M2/M3/M4/U1/Z (COR2X1)                0.26      19.17 f
M4/M2/M3/M4/c_out (Add_full_21)          0.00      19.17 f
M4/M2/M3/c_out (Add_rca_4_6)             0.00      19.17 f
M4/M2/M4/c_in (Add_rca_4_5)              0.00      19.17 f
M4/M2/M4/M1/c_in (Add_full_20)           0.00      19.17 f
M4/M2/M4/M1/M2/b (Add_half_39)           0.00      19.17 f
M4/M2/M4/M1/M2/U2/Z (CAN2X1)             0.18      19.34 f
M4/M2/M4/M1/M2/c_out (Add_half_39)       0.00      19.34 f
M4/M2/M4/M1/U1/Z (COR2X1)                0.26      19.60 f
M4/M2/M4/M1/c_out (Add_full_20)          0.00      19.60 f
M4/M2/M4/M2/c_in (Add_full_19)           0.00      19.60 f
M4/M2/M4/M2/M2/b (Add_half_37)           0.00      19.60 f
M4/M2/M4/M2/M2/U2/Z (CAN2X1)             0.18      19.78 f
M4/M2/M4/M2/M2/c_out (Add_half_37)       0.00      19.78 f
M4/M2/M4/M2/U1/Z (COR2X1)                0.26      20.04 f
M4/M2/M4/M2/c_out (Add_full_19)          0.00      20.04 f
M4/M2/M4/M3/c_in (Add_full_18)           0.00      20.04 f
M4/M2/M4/M3/M2/b (Add_half_35)           0.00      20.04 f
M4/M2/M4/M3/M2/U2/Z (CAN2X1)             0.18      20.22 f
M4/M2/M4/M3/M2/c_out (Add_half_35)       0.00      20.22 f
M4/M2/M4/M3/U1/Z (COR2X1)                0.26      20.48 f
M4/M2/M4/M3/c_out (Add_full_18)          0.00      20.48 f
M4/M2/M4/M4/c_in (Add_full_17)           0.00      20.48 f
M4/M2/M4/M4/M2/b (Add_half_33)           0.00      20.48 f
M4/M2/M4/M4/M2/U2/Z (CAN2X1)             0.18      20.66 f
M4/M2/M4/M4/M2/c_out (Add_half_33)       0.00      20.66 f
M4/M2/M4/M4/U1/Z (COR2X1)                0.26      20.92 f
M4/M2/M4/M4/c_out (Add_full_17)          0.00      20.92 f
M4/M2/M4/c_out (Add_rca_4_5)             0.00      20.92 f
M4/M2/M5/c_in (Add_rca_4_4)              0.00      20.92 f
M4/M2/M5/M1/c_in (Add_full_16)           0.00      20.92 f
M4/M2/M5/M1/M2/b (Add_half_31)           0.00      20.92 f
M4/M2/M5/M1/M2/U2/Z (CAN2X1)             0.18      21.10 f
M4/M2/M5/M1/M2/c_out (Add_half_31)       0.00      21.10 f
M4/M2/M5/M1/U1/Z (COR2X1)                0.26      21.36 f
M4/M2/M5/M1/c_out (Add_full_16)          0.00      21.36 f
M4/M2/M5/M2/c_in (Add_full_15)           0.00      21.36 f
M4/M2/M5/M2/M2/b (Add_half_29)           0.00      21.36 f
M4/M2/M5/M2/M2/U2/Z (CAN2X1)             0.18      21.53 f
M4/M2/M5/M2/M2/c_out (Add_half_29)       0.00      21.53 f
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M4/M2/M5/M2/U1/Z (COR2X1)                0.26      21.80 f
M4/M2/M5/M2/c_out (Add_full_15)          0.00      21.80 f
M4/M2/M5/M3/c_in (Add_full_14)           0.00      21.80 f
M4/M2/M5/M3/M2/b (Add_half_27)           0.00      21.80 f
M4/M2/M5/M3/M2/U2/Z (CAN2X1)             0.18      21.97 f
M4/M2/M5/M3/M2/c_out (Add_half_27)       0.00      21.97 f
M4/M2/M5/M3/U1/Z (COR2X1)                0.26      22.24 f
M4/M2/M5/M3/c_out (Add_full_14)          0.00      22.24 f
M4/M2/M5/M4/c_in (Add_full_13)           0.00      22.24 f
M4/M2/M5/M4/M2/b (Add_half_25)           0.00      22.24 f
M4/M2/M5/M4/M2/U2/Z (CAN2X1)             0.18      22.41 f
M4/M2/M5/M4/M2/c_out (Add_half_25)       0.00      22.41 f
M4/M2/M5/M4/U1/Z (COR2X1)                0.26      22.68 f
M4/M2/M5/M4/c_out (Add_full_13)          0.00      22.68 f
M4/M2/M5/c_out (Add_rca_4_4)             0.00      22.68 f
M4/M2/M6/c_in (Add_rca_4_3)              0.00      22.68 f
M4/M2/M6/M1/c_in (Add_full_12)           0.00      22.68 f
M4/M2/M6/M1/M2/b (Add_half_23)           0.00      22.68 f
M4/M2/M6/M1/M2/U2/Z (CAN2X1)             0.18      22.85 f
M4/M2/M6/M1/M2/c_out (Add_half_23)       0.00      22.85 f
M4/M2/M6/M1/U2/Z (CND2IX1)               0.19      23.04 f
M4/M2/M6/M1/c_out (Add_full_12)          0.00      23.04 f
M4/M2/M6/M2/c_in (Add_full_11)           0.00      23.04 f
M4/M2/M6/M2/M2/b (Add_half_21)           0.00      23.04 f
M4/M2/M6/M2/M2/U2/Z (CAN2X1)             0.18      23.21 f
M4/M2/M6/M2/M2/c_out (Add_half_21)       0.00      23.21 f
M4/M2/M6/M2/U1/Z (COR2X1)                0.26      23.48 f
M4/M2/M6/M2/c_out (Add_full_11)          0.00      23.48 f
M4/M2/M6/M3/c_in (Add_full_10)           0.00      23.48 f
M4/M2/M6/M3/M2/b (Add_half_19)           0.00      23.48 f
M4/M2/M6/M3/M2/U2/Z (CAN2X1)             0.18      23.65 f
M4/M2/M6/M3/M2/c_out (Add_half_19)       0.00      23.65 f
M4/M2/M6/M3/U2/Z (CND2IX1)               0.19      23.84 f
M4/M2/M6/M3/c_out (Add_full_10)          0.00      23.84 f
M4/M2/M6/M4/c_in (Add_full_9)            0.00      23.84 f
M4/M2/M6/M4/M2/b (Add_half_17)           0.00      23.84 f
M4/M2/M6/M4/M2/U2/Z (CAN2X1)             0.18      24.01 f
M4/M2/M6/M4/M2/c_out (Add_half_17)       0.00      24.01 f
M4/M2/M6/M4/U2/Z (CND2IX1)               0.19      24.20 f
M4/M2/M6/M4/c_out (Add_full_9)           0.00      24.20 f
M4/M2/M6/c_out (Add_rca_4_3)             0.00      24.20 f
M4/M2/M7/c_in (Add_rca_4_2)              0.00      24.20 f
M4/M2/M7/M1/c_in (Add_full_8)            0.00      24.20 f
M4/M2/M7/M1/M2/b (Add_half_15)           0.00      24.20 f
M4/M2/M7/M1/M2/U2/Z (CAN2X1)             0.18      24.37 f
M4/M2/M7/M1/M2/c_out (Add_half_15)       0.00      24.37 f
M4/M2/M7/M1/U2/Z (CND2IX1)               0.19      24.56 f
M4/M2/M7/M1/c_out (Add_full_8)           0.00      24.56 f
M4/M2/M7/M2/c_in (Add_full_7)            0.00      24.56 f
M4/M2/M7/M2/M2/b (Add_half_13)           0.00      24.56 f
M4/M2/M7/M2/M2/U2/Z (CAN2X1)             0.18      24.74 f
M4/M2/M7/M2/M2/c_out (Add_half_13)       0.00      24.74 f
M4/M2/M7/M2/U2/Z (CND2IX1)               0.19      24.92 f
M4/M2/M7/M2/c_out (Add_full_7)           0.00      24.92 f
M4/M2/M7/M3/c_in (Add_full_6)            0.00      24.92 f
M4/M2/M7/M3/M2/b (Add_half_11)           0.00      24.92 f
M4/M2/M7/M3/M2/U2/Z (CAN2X1)             0.18      25.10 f
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  M4/M2/M7/M3/M2/c_out (Add_half_11)       0.00      25.10 f
  M4/M2/M7/M3/U2/Z (CND2IX1)               0.19      25.28 f
  M4/M2/M7/M3/c_out (Add_full_6)           0.00      25.28 f
  M4/M2/M7/M4/c_in (Add_full_5)            0.00      25.28 f
  M4/M2/M7/M4/M2/b (Add_half_9)            0.00      25.28 f
  M4/M2/M7/M4/M2/U2/Z (CAN2X1)             0.18      25.46 f
  M4/M2/M7/M4/M2/c_out (Add_half_9)        0.00      25.46 f
  M4/M2/M7/M4/U1/Z (COR2X1)                0.26      25.72 f
  M4/M2/M7/M4/c_out (Add_full_5)           0.00      25.72 f
  M4/M2/M7/c_out (Add_rca_4_2)             0.00      25.72 f
  M4/M2/M8/c_in (Add_rca_4_1)              0.00      25.72 f
  M4/M2/M8/M1/c_in (Add_full_4)            0.00      25.72 f
  M4/M2/M8/M1/M2/b (Add_half_7)            0.00      25.72 f
  M4/M2/M8/M1/M2/U6/Z (CAN2X1)             0.18      25.89 f
  M4/M2/M8/M1/M2/c_out (Add_half_7)        0.00      25.89 f
  M4/M2/M8/M1/U2/Z (CND2IX1)               0.21      26.10 f
  M4/M2/M8/M1/c_out (Add_full_4)           0.00      26.10 f
  M4/M2/M8/M2/c_in (Add_full_3)            0.00      26.10 f
  M4/M2/M8/M2/M2/b (Add_half_5)            0.00      26.10 f
  M4/M2/M8/M2/M2/U2/Z (CAN2X1)             0.18      26.28 f
  M4/M2/M8/M2/M2/c_out (Add_half_5)        0.00      26.28 f
  M4/M2/M8/M2/U1/Z (COR2X1)                0.26      26.54 f
  M4/M2/M8/M2/c_out (Add_full_3)           0.00      26.54 f
  M4/M2/M8/M3/c_in (Add_full_2)            0.00      26.54 f
  M4/M2/M8/M3/M2/b (Add_half_3)            0.00      26.54 f
  M4/M2/M8/M3/M2/U5/Z (CAN2X1)             0.18      26.72 f
  M4/M2/M8/M3/M2/c_out (Add_half_3)        0.00      26.72 f
  M4/M2/M8/M3/U1/Z (CND2IX1)               0.21      26.93 f
  M4/M2/M8/M3/c_out (Add_full_2)           0.00      26.93 f
  M4/M2/M8/M4/c_in (Add_full_1)            0.00      26.93 f
  M4/M2/M8/M4/M2/b (Add_half_1)            0.00      26.93 f
  M4/M2/M8/M4/M2/U1/Z (CND2X1)             0.08      27.01 r
  M4/M2/M8/M4/M2/U3/Z (CND2X1)             0.11      27.12 f
  M4/M2/M8/M4/M2/sum (Add_half_1)          0.00      27.12 f
  M4/M2/M8/M4/sum (Add_full_1)             0.00      27.12 f
  M4/M2/M8/sum[3] (Add_rca_4_1)            0.00      27.12 f
  M4/M2/sum[31] (Add_rca_1)                0.00      27.12 f
  M4/sum[63] (Add_rca64_1)                 0.00      27.12 f
  U1471/Z (CND2IX1)                        0.07      27.19 r
  U1472/Z (CND2IX1)                        0.08      27.28 f
  result_reg[63]/D (CFD1QXL)               0.00      27.28 f
  data arrival time                                  27.28

  clock clock (rise edge)                 28.00      28.00
  clock network delay (propagated)         0.00      28.00
  clock uncertainty                       -0.25      27.75
  result_reg[63]/CP (CFD1QXL)              0.00      27.75 r
  library setup time                      -0.46      27.29
  data required time                                 27.29
  ---------------------------------------------------------
  data required time                                 27.29
  data arrival time                                 -27.28
  ---------------------------------------------------------
  slack (MET)                                        0.01
**************************************
Report : area
Design : mul
```

```
Version: C-2009.06-SP5
Date   : Sun Dec 11 06:21:51 2016
****************************************

Library(s) Used:

    tc240c (File: /apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25)

Number of ports:              165
Number of nets:              1545
Number of cells:             1247
Number of references:          54

Combinational area:       3346.500000
Noncombinational area:     947.500000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:          4294.000000
Total area:                 undefined

Loading db file '/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_BCCOM25'
Loading db file '/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25'
Warning: Main library 'tc240c' does not specify the following unit required
for power: 'Leakage Power'. (PWR-424)
Information: Propagating switching activity (low effort zero delay
simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

****************************************
Report : power
        -analysis_effort low
Design : mul
Version: C-2009.06-SP5
Date   : Sun Dec 11 06:21:52 2016
****************************************

Library(s) Used:

    tc240c (File: /apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25)

Operating Conditions: WCCOM25   Library: tc240c
Wire Load Model Mode: top

Global Operating Voltage = 2.3
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = Unitless

  Cell Internal Power  =   1.6938 mW   (90%)
  Net Switching Power  = 187.4021 uW   (10%)
                         ---------
Total Dynamic Power    =   1.8812 mW  (100%)
Cell Leakage Power     =   0.0000
```

For Divider:

```
Inferred memory devices in process
      in routine div line 76 in file
            './div.v'.
==========================================================================
==
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST
|
==========================================================================
==
|      cust_reg       | Flip-flop |   3   |  Y  | N  | Y  | N  | N  | N  | N
|
==========================================================================
==

Inferred memory devices in process
      in routine div line 98 in file
            './div.v'.
==========================================================================
==
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST
|
==========================================================================
==
|   opera1_copy_reg   | Flip-flop |  32   |  Y  | N  | N  | N  | N  | N  | N
|
|       w4_reg        | Flip-flop |   1   |  N  | N  | N  | N  | N  | N  | N
|
|     result_reg      | Flip-flop |  64   |  Y  | N  | N  | N  | N  | N  | N
|
|        i_reg        | Flip-flop |  32   |  Y  | N  | N  | N  | N  | N  | N
|
|   result_not_reg    | Flip-flop |  64   |  Y  | N  | N  | N  | N  | N  | N
|
|   result_copy_reg   | Flip-flop |  32   |  Y  | N  | N  | N  | N  | N  | N
|
|   result_copy_reg   | Flip-flop |  32   |  N  | N  | N  | N  | N  | N  | N
|
|       OPE_reg       | Flip-flop |   1   |  N  | N  | N  | N  | N  | N  | N
|
| opera1_copydiv_reg  | Flip-flop |  32   |  Y  | N  | N  | N  | N  | N  | N
|
|      valid_reg      | Flip-flop |   1   |  N  | N  | N  | N  | N  | N  | N
|
|      nest_reg       | Flip-flop |   3   |  N  | N  | N  | N  | N  | N  | N
|
==========================================================================
==

Inferred tri-state devices in process
      in routine div line 32 in file
            './div.v'.
================================================
| Register Name |       Type       | Width | MB |
================================================
```

```
|      A1       | Tri-State Buffer |   1   | N  |
=================================================

Inferred tri-state devices in process
      in routine div line 33 in file
            './div.v'.
=================================================
| Register Name |       Type       | Width | MB |
=================================================
|      A2       | Tri-State Buffer |   1   | N  |
=================================================

Inferred tri-state devices in process
      in routine div line 37 in file
            './div.v'.
=================================================
| Register Name |       Type       | Width | MB |
=================================================
|      A4       | Tri-State Buffer |   1   | N  |
=================================================

Inferred tri-state devices in process
      in routine div line 35 in file
            './div.v'.
=================================================
| Register Name |       Type       | Width | MB |
=================================================
|      A6       | Tri-State Buffer |   1   | N  |
=================================================

Inferred tri-state devices in process
      in routine div line 39 in file
            './div.v'.
=================================================
| Register Name |       Type       | Width | MB |
=================================================
|      A8       | Tri-State Buffer |   1   | N  |
=================================================

Inferred tri-state devices in process
      in routine div line 34 in file
            './div.v'.
=================================================
| Register Name |       Type       | Width | MB |
=================================================
|      A5       | Tri-State Buffer |   1   | N  |
=================================================

Inferred tri-state devices in process
      in routine div line 36 in file
            './div.v'.
=================================================
| Register Name |       Type       | Width | MB |
=================================================
|      A3       | Tri-State Buffer |   1   | N  |
=================================================
```

```
Inferred tri-state devices in process
      in routine div line 38 in file
            './div.v'.
===============================================
| Register Name |       Type       | Width | MB |
===============================================
|      A7       | Tri-State Buffer |   1   | N  |
===============================================

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : div
Version: C-2009.06-SP5
Date   : Sun Dec 11 05:36:55 2016
****************************************

Operating Conditions: WCCOM25   Library: tc240c
Wire Load Model Mode: top

  Startpoint: opera2[63] (input port)
  Endpoint: result_copy_reg[63]
            (rising edge-triggered flip-flop clocked by clock)
  Path Group: clock
  Path Type: max

  Point                                          Incr       Path
  -----------------------------------------------------------------
  clock (input port clock) (rise edge)        0.00       0.00
  input external delay                        0.00       0.00 r
  opera2[63] (in)                             0.00       0.00 r
  U898/Z0 (CIVDX1)                            0.06       0.06 f
  U974/Z (CND2X1)                             0.08       0.14 r
  U899/Z (CND2X1)                             0.14       0.28 f
  M2/a[0] (Add_rca64_0)                       0.00       0.28 f
  M2/M1/a[0] (Add_rca_4)                      0.00       0.28 f
  M2/M1/M1/a[0] (Add_rca_4_32)                0.00       0.28 f
  M2/M1/M1/M1/a (Add_full_128)                0.00       0.28 f
  M2/M1/M1/M1/M1/a (Add_half_256)             0.00       0.28 f
  M2/M1/M1/M1/M1/U3/Z (CENX1)                 0.22       0.50 f
  M2/M1/M1/M1/M1/sum (Add_half_256)           0.00       0.50 f
  M2/M1/M1/M1/M2/a (Add_half_255)             0.00       0.50 f
  M2/M1/M1/M1/M2/U2/Z (CAN2X1)                0.17       0.67 f
  M2/M1/M1/M1/M2/c_out (Add_half_255)         0.00       0.67 f
  M2/M1/M1/M1/U1/Z (COR2X1)                   0.26       0.93 f
  M2/M1/M1/M1/c_out (Add_full_128)            0.00       0.93 f
  M2/M1/M1/M2/c_in (Add_full_127)             0.00       0.93 f
  M2/M1/M1/M2/M2/b (Add_half_253)             0.00       0.93 f
  M2/M1/M1/M2/M2/U2/Z (CAN2X1)                0.18       1.10 f
  M2/M1/M1/M2/M2/c_out (Add_half_253)         0.00       1.10 f
  M2/M1/M1/M2/U1/Z (COR2X1)                   0.26       1.37 f
  M2/M1/M1/M2/c_out (Add_full_127)            0.00       1.37 f
  M2/M1/M1/M3/c_in (Add_full_126)             0.00       1.37 f
  M2/M1/M1/M3/M2/b (Add_half_251)             0.00       1.37 f
  M2/M1/M1/M3/M2/U2/Z (CAN2X1)                0.18       1.54 f
```

```
M2/M1/M1/M3/M2/c_out (Add_half_251)      0.00       1.54 f
M2/M1/M1/M3/U1/Z (COR2X1)                0.26       1.81 f
M2/M1/M1/M3/c_out (Add_full_126)         0.00       1.81 f
M2/M1/M1/M4/c_in (Add_full_125)          0.00       1.81 f
M2/M1/M1/M4/M2/b (Add_half_249)          0.00       1.81 f
M2/M1/M1/M4/M2/U2/Z (CAN2X1)             0.18       1.98 f
M2/M1/M1/M4/M2/c_out (Add_half_249)      0.00       1.98 f
M2/M1/M1/M4/U1/Z (COR2X1)                0.26       2.24 f
M2/M1/M1/M4/c_out (Add_full_125)         0.00       2.24 f
M2/M1/M1/c_out (Add_rca_4_32)            0.00       2.24 f
M2/M1/M2/c_in (Add_rca_4_31)             0.00       2.24 f
M2/M1/M2/M1/c_in (Add_full_124)          0.00       2.24 f
M2/M1/M2/M1/M2/b (Add_half_247)          0.00       2.24 f
M2/M1/M2/M1/M2/U2/Z (CAN2X1)             0.18       2.42 f
M2/M1/M2/M1/M2/c_out (Add_half_247)      0.00       2.42 f
M2/M1/M2/M1/U1/Z (COR2X1)                0.26       2.68 f
M2/M1/M2/M1/c_out (Add_full_124)         0.00       2.68 f
M2/M1/M2/M2/c_in (Add_full_123)          0.00       2.68 f
M2/M1/M2/M2/M2/b (Add_half_245)          0.00       2.68 f
M2/M1/M2/M2/M2/U2/Z (CAN2X1)             0.18       2.86 f
M2/M1/M2/M2/M2/c_out (Add_half_245)      0.00       2.86 f
M2/M1/M2/M2/U1/Z (COR2X1)                0.26       3.12 f
M2/M1/M2/M2/c_out (Add_full_123)         0.00       3.12 f
M2/M1/M2/M3/c_in (Add_full_122)          0.00       3.12 f
M2/M1/M2/M3/M2/b (Add_half_243)          0.00       3.12 f
M2/M1/M2/M3/M2/U2/Z (CAN2X1)             0.18       3.30 f
M2/M1/M2/M3/M2/c_out (Add_half_243)      0.00       3.30 f
M2/M1/M2/M3/U1/Z (COR2X1)                0.26       3.56 f
M2/M1/M2/M3/c_out (Add_full_122)         0.00       3.56 f
M2/M1/M2/M4/c_in (Add_full_121)          0.00       3.56 f
M2/M1/M2/M4/M2/b (Add_half_241)          0.00       3.56 f
M2/M1/M2/M4/M2/U2/Z (CAN2X1)             0.18       3.74 f
M2/M1/M2/M4/M2/c_out (Add_half_241)      0.00       3.74 f
M2/M1/M2/M4/U1/Z (COR2X1)                0.26       4.00 f
M2/M1/M2/M4/c_out (Add_full_121)         0.00       4.00 f
M2/M1/M2/c_out (Add_rca_4_31)            0.00       4.00 f
M2/M1/M3/c_in (Add_rca_4_30)             0.00       4.00 f
M2/M1/M3/M1/c_in (Add_full_120)          0.00       4.00 f
M2/M1/M3/M1/M2/b (Add_half_239)          0.00       4.00 f
M2/M1/M3/M1/M2/U2/Z (CAN2X1)             0.18       4.17 f
M2/M1/M3/M1/M2/c_out (Add_half_239)      0.00       4.17 f
M2/M1/M3/M1/U1/Z (COR2X1)                0.26       4.44 f
M2/M1/M3/M1/c_out (Add_full_120)         0.00       4.44 f
M2/M1/M3/M2/c_in (Add_full_119)          0.00       4.44 f
M2/M1/M3/M2/M2/b (Add_half_237)          0.00       4.44 f
M2/M1/M3/M2/M2/U2/Z (CAN2X1)             0.18       4.61 f
M2/M1/M3/M2/M2/c_out (Add_half_237)      0.00       4.61 f
M2/M1/M3/M2/U1/Z (COR2X1)                0.26       4.88 f
M2/M1/M3/M2/c_out (Add_full_119)         0.00       4.88 f
M2/M1/M3/M3/c_in (Add_full_118)          0.00       4.88 f
M2/M1/M3/M3/M2/b (Add_half_235)          0.00       4.88 f
M2/M1/M3/M3/M2/U2/Z (CAN2X1)             0.18       5.05 f
M2/M1/M3/M3/M2/c_out (Add_half_235)      0.00       5.05 f
M2/M1/M3/M3/U1/Z (COR2X1)                0.26       5.31 f
M2/M1/M3/M3/c_out (Add_full_118)         0.00       5.31 f
M2/M1/M3/M4/c_in (Add_full_117)          0.00       5.31 f
M2/M1/M3/M4/M2/b (Add_half_233)          0.00       5.31 f
```

```
M2/M1/M3/M4/M2/U2/Z (CAN2X1)              0.18       5.49 f
M2/M1/M3/M4/M2/c_out (Add_half_233)       0.00       5.49 f
M2/M1/M3/M4/U1/Z (COR2X1)                 0.26       5.75 f
M2/M1/M3/M4/c_out (Add_full_117)          0.00       5.75 f
M2/M1/M3/c_out (Add_rca_4_30)             0.00       5.75 f
M2/M1/M4/c_in (Add_rca_4_29)              0.00       5.75 f
M2/M1/M4/M1/c_in (Add_full_116)           0.00       5.75 f
M2/M1/M4/M1/M2/b (Add_half_231)           0.00       5.75 f
M2/M1/M4/M1/M2/U2/Z (CAN2X1)              0.18       5.93 f
M2/M1/M4/M1/M2/c_out (Add_half_231)       0.00       5.93 f
M2/M1/M4/M1/U1/Z (COR2X1)                 0.26       6.19 f
M2/M1/M4/M1/c_out (Add_full_116)          0.00       6.19 f
M2/M1/M4/M2/c_in (Add_full_115)           0.00       6.19 f
M2/M1/M4/M2/M2/b (Add_half_229)           0.00       6.19 f
M2/M1/M4/M2/M2/U2/Z (CAN2X1)              0.18       6.37 f
M2/M1/M4/M2/M2/c_out (Add_half_229)       0.00       6.37 f
M2/M1/M4/M2/U1/Z (COR2X1)                 0.26       6.63 f
M2/M1/M4/M2/c_out (Add_full_115)          0.00       6.63 f
M2/M1/M4/M3/c_in (Add_full_114)           0.00       6.63 f
M2/M1/M4/M3/M2/b (Add_half_227)           0.00       6.63 f
M2/M1/M4/M3/M2/U2/Z (CAN2X1)              0.18       6.81 f
M2/M1/M4/M3/M2/c_out (Add_half_227)       0.00       6.81 f
M2/M1/M4/M3/U1/Z (COR2X1)                 0.26       7.07 f
M2/M1/M4/M3/c_out (Add_full_114)          0.00       7.07 f
M2/M1/M4/M4/c_in (Add_full_113)           0.00       7.07 f
M2/M1/M4/M4/M2/b (Add_half_225)           0.00       7.07 f
M2/M1/M4/M4/M2/U2/Z (CAN2X1)              0.18       7.24 f
M2/M1/M4/M4/M2/c_out (Add_half_225)       0.00       7.24 f
M2/M1/M4/M4/U1/Z (COR2X1)                 0.26       7.51 f
M2/M1/M4/M4/c_out (Add_full_113)          0.00       7.51 f
M2/M1/M4/c_out (Add_rca_4_29)             0.00       7.51 f
M2/M1/M5/c_in (Add_rca_4_28)              0.00       7.51 f
M2/M1/M5/M1/c_in (Add_full_112)           0.00       7.51 f
M2/M1/M5/M1/M2/b (Add_half_223)           0.00       7.51 f
M2/M1/M5/M1/M2/U2/Z (CAN2X1)              0.18       7.68 f
M2/M1/M5/M1/M2/c_out (Add_half_223)       0.00       7.68 f
M2/M1/M5/M1/U1/Z (COR2X1)                 0.26       7.95 f
M2/M1/M5/M1/c_out (Add_full_112)          0.00       7.95 f
M2/M1/M5/M2/c_in (Add_full_111)           0.00       7.95 f
M2/M1/M5/M2/M2/b (Add_half_221)           0.00       7.95 f
M2/M1/M5/M2/M2/U2/Z (CAN2X1)              0.18       8.12 f
M2/M1/M5/M2/M2/c_out (Add_half_221)       0.00       8.12 f
M2/M1/M5/M2/U1/Z (COR2X1)                 0.26       8.38 f
M2/M1/M5/M2/c_out (Add_full_111)          0.00       8.38 f
M2/M1/M5/M3/c_in (Add_full_110)           0.00       8.38 f
M2/M1/M5/M3/M2/b (Add_half_219)           0.00       8.38 f
M2/M1/M5/M3/M2/U2/Z (CAN2X1)              0.18       8.56 f
M2/M1/M5/M3/M2/c_out (Add_half_219)       0.00       8.56 f
M2/M1/M5/M3/U1/Z (COR2X1)                 0.26       8.82 f
M2/M1/M5/M3/c_out (Add_full_110)          0.00       8.82 f
M2/M1/M5/M4/c_in (Add_full_109)           0.00       8.82 f
M2/M1/M5/M4/M2/b (Add_half_217)           0.00       8.82 f
M2/M1/M5/M4/M2/U2/Z (CAN2X1)              0.18       9.00 f
M2/M1/M5/M4/M2/c_out (Add_half_217)       0.00       9.00 f
M2/M1/M5/M4/U1/Z (COR2X1)                 0.26       9.26 f
M2/M1/M5/M4/c_out (Add_full_109)          0.00       9.26 f
M2/M1/M5/c_out (Add_rca_4_28)             0.00       9.26 f
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M2/M1/M6/c_in (Add_rca_4_27)              0.00       9.26 f
M2/M1/M6/M1/c_in (Add_full_108)           0.00       9.26 f
M2/M1/M6/M1/M2/b (Add_half_215)           0.00       9.26 f
M2/M1/M6/M1/M2/U2/Z (CAN2X1)              0.18       9.44 f
M2/M1/M6/M1/M2/c_out (Add_half_215)       0.00       9.44 f
M2/M1/M6/M1/U1/Z (COR2X1)                 0.26       9.70 f
M2/M1/M6/M1/c_out (Add_full_108)          0.00       9.70 f
M2/M1/M6/M2/c_in (Add_full_107)           0.00       9.70 f
M2/M1/M6/M2/M2/b (Add_half_213)           0.00       9.70 f
M2/M1/M6/M2/M2/U2/Z (CAN2X1)              0.18       9.88 f
M2/M1/M6/M2/M2/c_out (Add_half_213)       0.00       9.88 f
M2/M1/M6/M2/U1/Z (COR2X1)                 0.26      10.14 f
M2/M1/M6/M2/c_out (Add_full_107)          0.00      10.14 f
M2/M1/M6/M3/c_in (Add_full_106)           0.00      10.14 f
M2/M1/M6/M3/M2/b (Add_half_211)           0.00      10.14 f
M2/M1/M6/M3/M2/U2/Z (CAN2X1)              0.18      10.32 f
M2/M1/M6/M3/M2/c_out (Add_half_211)       0.00      10.32 f
M2/M1/M6/M3/U1/Z (COR2X1)                 0.26      10.58 f
M2/M1/M6/M3/c_out (Add_full_106)          0.00      10.58 f
M2/M1/M6/M4/c_in (Add_full_105)           0.00      10.58 f
M2/M1/M6/M4/M2/b (Add_half_209)           0.00      10.58 f
M2/M1/M6/M4/M2/U2/Z (CAN2X1)              0.18      10.75 f
M2/M1/M6/M4/M2/c_out (Add_half_209)       0.00      10.75 f
M2/M1/M6/M4/U1/Z (COR2X1)                 0.26      11.02 f
M2/M1/M6/M4/c_out (Add_full_105)          0.00      11.02 f
M2/M1/M6/c_out (Add_rca_4_27)             0.00      11.02 f
M2/M1/M7/c_in (Add_rca_4_26)              0.00      11.02 f
M2/M1/M7/M1/c_in (Add_full_104)           0.00      11.02 f
M2/M1/M7/M1/M2/b (Add_half_207)           0.00      11.02 f
M2/M1/M7/M1/M2/U2/Z (CAN2X1)              0.18      11.19 f
M2/M1/M7/M1/M2/c_out (Add_half_207)       0.00      11.19 f
M2/M1/M7/M1/U1/Z (COR2X1)                 0.26      11.46 f
M2/M1/M7/M1/c_out (Add_full_104)          0.00      11.46 f
M2/M1/M7/M2/c_in (Add_full_103)           0.00      11.46 f
M2/M1/M7/M2/M2/b (Add_half_205)           0.00      11.46 f
M2/M1/M7/M2/M2/U2/Z (CAN2X1)              0.18      11.63 f
M2/M1/M7/M2/M2/c_out (Add_half_205)       0.00      11.63 f
M2/M1/M7/M2/U1/Z (COR2X1)                 0.26      11.89 f
M2/M1/M7/M2/c_out (Add_full_103)          0.00      11.89 f
M2/M1/M7/M3/c_in (Add_full_102)           0.00      11.89 f
M2/M1/M7/M3/M2/b (Add_half_203)           0.00      11.89 f
M2/M1/M7/M3/M2/U2/Z (CAN2X1)              0.18      12.07 f
M2/M1/M7/M3/M2/c_out (Add_half_203)       0.00      12.07 f
M2/M1/M7/M3/U1/Z (COR2X1)                 0.26      12.33 f
M2/M1/M7/M3/c_out (Add_full_102)          0.00      12.33 f
M2/M1/M7/M4/c_in (Add_full_101)           0.00      12.33 f
M2/M1/M7/M4/M2/b (Add_half_201)           0.00      12.33 f
M2/M1/M7/M4/M2/U2/Z (CAN2X1)              0.18      12.51 f
M2/M1/M7/M4/M2/c_out (Add_half_201)       0.00      12.51 f
M2/M1/M7/M4/U1/Z (COR2X1)                 0.26      12.77 f
M2/M1/M7/M4/c_out (Add_full_101)          0.00      12.77 f
M2/M1/M7/c_out (Add_rca_4_26)             0.00      12.77 f
M2/M1/M8/c_in (Add_rca_4_25)              0.00      12.77 f
M2/M1/M8/M1/c_in (Add_full_100)           0.00      12.77 f
M2/M1/M8/M1/M2/b (Add_half_199)           0.00      12.77 f
M2/M1/M8/M1/M2/U2/Z (CAN2X1)              0.18      12.95 f
M2/M1/M8/M1/M2/c_out (Add_half_199)       0.00      12.95 f
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M2/M1/M8/M1/U1/Z (COR2X1)                0.26      13.21 f
M2/M1/M8/M1/c_out (Add_full_100)         0.00      13.21 f
M2/M1/M8/M2/c_in (Add_full_99)           0.00      13.21 f
M2/M1/M8/M2/M2/b (Add_half_197)          0.00      13.21 f
M2/M1/M8/M2/M2/U2/Z (CAN2X1)             0.18      13.39 f
M2/M1/M8/M2/M2/c_out (Add_half_197)      0.00      13.39 f
M2/M1/M8/M2/U1/Z (COR2X1)                0.26      13.65 f
M2/M1/M8/M2/c_out (Add_full_99)          0.00      13.65 f
M2/M1/M8/M3/c_in (Add_full_98)           0.00      13.65 f
M2/M1/M8/M3/M2/b (Add_half_195)          0.00      13.65 f
M2/M1/M8/M3/M2/U2/Z (CAN2X1)             0.18      13.82 f
M2/M1/M8/M3/M2/c_out (Add_half_195)      0.00      13.82 f
M2/M1/M8/M3/U1/Z (COR2X1)                0.26      14.09 f
M2/M1/M8/M3/c_out (Add_full_98)          0.00      14.09 f
M2/M1/M8/M4/c_in (Add_full_97)           0.00      14.09 f
M2/M1/M8/M4/M2/b (Add_half_193)          0.00      14.09 f
M2/M1/M8/M4/M2/U2/Z (CAN2X1)             0.18      14.26 f
M2/M1/M8/M4/M2/c_out (Add_half_193)      0.00      14.26 f
M2/M1/M8/M4/U1/Z (COR2X1)                0.26      14.53 f
M2/M1/M8/M4/c_out (Add_full_97)          0.00      14.53 f
M2/M1/M8/c_out (Add_rca_4_25)            0.00      14.53 f
M2/M1/c_out (Add_rca_4)                  0.00      14.53 f
M2/M2/c_in (Add_rca_3)                   0.00      14.53 f
M2/M2/M1/c_in (Add_rca_4_24)             0.00      14.53 f
M2/M2/M1/M1/c_in (Add_full_96)           0.00      14.53 f
M2/M2/M1/M1/M2/b (Add_half_191)          0.00      14.53 f
M2/M2/M1/M1/M2/U2/Z (CAN2X1)             0.18      14.70 f
M2/M2/M1/M1/M2/c_out (Add_half_191)      0.00      14.70 f
M2/M2/M1/M1/U1/Z (COR2X1)                0.26      14.96 f
M2/M2/M1/M1/c_out (Add_full_96)          0.00      14.96 f
M2/M2/M1/M2/c_in (Add_full_95)           0.00      14.96 f
M2/M2/M1/M2/M2/b (Add_half_189)          0.00      14.96 f
M2/M2/M1/M2/M2/U2/Z (CAN2X1)             0.18      15.14 f
M2/M2/M1/M2/M2/c_out (Add_half_189)      0.00      15.14 f
M2/M2/M1/M2/U1/Z (COR2X1)                0.26      15.40 f
M2/M2/M1/M2/c_out (Add_full_95)          0.00      15.40 f
M2/M2/M1/M3/c_in (Add_full_94)           0.00      15.40 f
M2/M2/M1/M3/M2/b (Add_half_187)          0.00      15.40 f
M2/M2/M1/M3/M2/U2/Z (CAN2X1)             0.18      15.58 f
M2/M2/M1/M3/M2/c_out (Add_half_187)      0.00      15.58 f
M2/M2/M1/M3/U1/Z (COR2X1)                0.26      15.84 f
M2/M2/M1/M3/c_out (Add_full_94)          0.00      15.84 f
M2/M2/M1/M4/c_in (Add_full_93)           0.00      15.84 f
M2/M2/M1/M4/M2/b (Add_half_185)          0.00      15.84 f
M2/M2/M1/M4/M2/U2/Z (CAN2X1)             0.18      16.02 f
M2/M2/M1/M4/M2/c_out (Add_half_185)      0.00      16.02 f
M2/M2/M1/M4/U1/Z (COR2X1)                0.26      16.28 f
M2/M2/M1/M4/c_out (Add_full_93)          0.00      16.28 f
M2/M2/M1/c_out (Add_rca_4_24)            0.00      16.28 f
M2/M2/M2/c_in (Add_rca_4_23)             0.00      16.28 f
M2/M2/M2/M1/c_in (Add_full_92)           0.00      16.28 f
M2/M2/M2/M1/M2/b (Add_half_183)          0.00      16.28 f
M2/M2/M2/M1/M2/U2/Z (CAN2X1)             0.18      16.46 f
M2/M2/M2/M1/M2/c_out (Add_half_183)      0.00      16.46 f
M2/M2/M2/M1/U1/Z (COR2X1)                0.26      16.72 f
M2/M2/M2/M1/c_out (Add_full_92)          0.00      16.72 f
M2/M2/M2/M2/c_in (Add_full_91)           0.00      16.72 f
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M2/M2/M2/M2/M2/b (Add_half_181)          0.00      16.72 f
M2/M2/M2/M2/M2/U2/Z (CAN2X1)             0.18      16.89 f
M2/M2/M2/M2/M2/c_out (Add_half_181)      0.00      16.89 f
M2/M2/M2/M2/U1/Z (COR2X1)                0.26      17.16 f
M2/M2/M2/M2/c_out (Add_full_91)          0.00      17.16 f
M2/M2/M2/M3/c_in (Add_full_90)           0.00      17.16 f
M2/M2/M2/M3/M2/b (Add_half_179)          0.00      17.16 f
M2/M2/M2/M3/M2/U2/Z (CAN2X1)             0.18      17.33 f
M2/M2/M2/M3/M2/c_out (Add_half_179)      0.00      17.33 f
M2/M2/M2/M3/U1/Z (COR2X1)                0.26      17.60 f
M2/M2/M2/M3/c_out (Add_full_90)          0.00      17.60 f
M2/M2/M2/M4/c_in (Add_full_89)           0.00      17.60 f
M2/M2/M2/M4/M2/b (Add_half_177)          0.00      17.60 f
M2/M2/M2/M4/M2/U2/Z (CAN2X1)             0.18      17.77 f
M2/M2/M2/M4/M2/c_out (Add_half_177)      0.00      17.77 f
M2/M2/M2/M4/U1/Z (COR2X1)                0.26      18.03 f
M2/M2/M2/M4/c_out (Add_full_89)          0.00      18.03 f
M2/M2/M2/c_out (Add_rca_4_23)            0.00      18.03 f
M2/M2/M3/c_in (Add_rca_4_22)             0.00      18.03 f
M2/M2/M3/M1/c_in (Add_full_88)           0.00      18.03 f
M2/M2/M3/M1/M2/b (Add_half_175)          0.00      18.03 f
M2/M2/M3/M1/M2/U2/Z (CAN2X1)             0.18      18.21 f
M2/M2/M3/M1/M2/c_out (Add_half_175)      0.00      18.21 f
M2/M2/M3/M1/U1/Z (COR2X1)                0.26      18.47 f
M2/M2/M3/M1/c_out (Add_full_88)          0.00      18.47 f
M2/M2/M3/M2/c_in (Add_full_87)           0.00      18.47 f
M2/M2/M3/M2/M2/b (Add_half_173)          0.00      18.47 f
M2/M2/M3/M2/M2/U2/Z (CAN2X1)             0.18      18.65 f
M2/M2/M3/M2/M2/c_out (Add_half_173)      0.00      18.65 f
M2/M2/M3/M2/U1/Z (COR2X1)                0.26      18.91 f
M2/M2/M3/M2/c_out (Add_full_87)          0.00      18.91 f
M2/M2/M3/M3/c_in (Add_full_86)           0.00      18.91 f
M2/M2/M3/M3/M2/b (Add_half_171)          0.00      18.91 f
M2/M2/M3/M3/M2/U2/Z (CAN2X1)             0.18      19.09 f
M2/M2/M3/M3/M2/c_out (Add_half_171)      0.00      19.09 f
M2/M2/M3/M3/U1/Z (COR2X1)                0.26      19.35 f
M2/M2/M3/M3/c_out (Add_full_86)          0.00      19.35 f
M2/M2/M3/M4/c_in (Add_full_85)           0.00      19.35 f
M2/M2/M3/M4/M2/b (Add_half_169)          0.00      19.35 f
M2/M2/M3/M4/M2/U2/Z (CAN2X1)             0.18      19.53 f
M2/M2/M3/M4/M2/c_out (Add_half_169)      0.00      19.53 f
M2/M2/M3/M4/U1/Z (COR2X1)                0.26      19.79 f
M2/M2/M3/M4/c_out (Add_full_85)          0.00      19.79 f
M2/M2/M3/c_out (Add_rca_4_22)            0.00      19.79 f
M2/M2/M4/c_in (Add_rca_4_21)             0.00      19.79 f
M2/M2/M4/M1/c_in (Add_full_84)           0.00      19.79 f
M2/M2/M4/M1/M2/b (Add_half_167)          0.00      19.79 f
M2/M2/M4/M1/M2/U2/Z (CAN2X1)             0.18      19.96 f
M2/M2/M4/M1/M2/c_out (Add_half_167)      0.00      19.96 f
M2/M2/M4/M1/U1/Z (COR2X1)                0.26      20.23 f
M2/M2/M4/M1/c_out (Add_full_84)          0.00      20.23 f
M2/M2/M4/M2/c_in (Add_full_83)           0.00      20.23 f
M2/M2/M4/M2/M2/b (Add_half_165)          0.00      20.23 f
M2/M2/M4/M2/M2/U2/Z (CAN2X1)             0.18      20.40 f
M2/M2/M4/M2/M2/c_out (Add_half_165)      0.00      20.40 f
M2/M2/M4/M2/U1/Z (COR2X1)                0.26      20.67 f
M2/M2/M4/M2/c_out (Add_full_83)          0.00      20.67 f
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M2/M2/M4/M3/c_in (Add_full_82)           0.00      20.67 f
M2/M2/M4/M3/M2/b (Add_half_163)          0.00      20.67 f
M2/M2/M4/M3/M2/U2/Z (CAN2X1)             0.18      20.84 f
M2/M2/M4/M3/M2/c_out (Add_half_163)      0.00      20.84 f
M2/M2/M4/M3/U1/Z (COR2X1)                0.26      21.10 f
M2/M2/M4/M3/c_out (Add_full_82)          0.00      21.10 f
M2/M2/M4/M4/c_in (Add_full_81)           0.00      21.10 f
M2/M2/M4/M4/M2/b (Add_half_161)          0.00      21.10 f
M2/M2/M4/M4/M2/U2/Z (CAN2X1)             0.18      21.28 f
M2/M2/M4/M4/M2/c_out (Add_half_161)      0.00      21.28 f
M2/M2/M4/M4/U1/Z (COR2X1)                0.26      21.54 f
M2/M2/M4/M4/c_out (Add_full_81)          0.00      21.54 f
M2/M2/M4/c_out (Add_rca_4_21)            0.00      21.54 f
M2/M2/M5/c_in (Add_rca_4_20)             0.00      21.54 f
M2/M2/M5/M1/c_in (Add_full_80)           0.00      21.54 f
M2/M2/M5/M1/M2/b (Add_half_159)          0.00      21.54 f
M2/M2/M5/M1/M2/U2/Z (CAN2X1)             0.18      21.72 f
M2/M2/M5/M1/M2/c_out (Add_half_159)      0.00      21.72 f
M2/M2/M5/M1/U1/Z (COR2X1)                0.26      21.98 f
M2/M2/M5/M1/c_out (Add_full_80)          0.00      21.98 f
M2/M2/M5/M2/c_in (Add_full_79)           0.00      21.98 f
M2/M2/M5/M2/M2/b (Add_half_157)          0.00      21.98 f
M2/M2/M5/M2/M2/U2/Z (CAN2X1)             0.18      22.16 f
M2/M2/M5/M2/M2/c_out (Add_half_157)      0.00      22.16 f
M2/M2/M5/M2/U1/Z (COR2X1)                0.26      22.42 f
M2/M2/M5/M2/c_out (Add_full_79)          0.00      22.42 f
M2/M2/M5/M3/c_in (Add_full_78)           0.00      22.42 f
M2/M2/M5/M3/M2/b (Add_half_155)          0.00      22.42 f
M2/M2/M5/M3/M2/U2/Z (CAN2X1)             0.18      22.60 f
M2/M2/M5/M3/M2/c_out (Add_half_155)      0.00      22.60 f
M2/M2/M5/M3/U1/Z (COR2X1)                0.26      22.86 f
M2/M2/M5/M3/c_out (Add_full_78)          0.00      22.86 f
M2/M2/M5/M4/c_in (Add_full_77)           0.00      22.86 f
M2/M2/M5/M4/M2/b (Add_half_153)          0.00      22.86 f
M2/M2/M5/M4/M2/U2/Z (CAN2X1)             0.18      23.03 f
M2/M2/M5/M4/M2/c_out (Add_half_153)      0.00      23.03 f
M2/M2/M5/M4/U1/Z (COR2X1)                0.26      23.30 f
M2/M2/M5/M4/c_out (Add_full_77)          0.00      23.30 f
M2/M2/M5/c_out (Add_rca_4_20)            0.00      23.30 f
M2/M2/M6/c_in (Add_rca_4_19)             0.00      23.30 f
M2/M2/M6/M1/c_in (Add_full_76)           0.00      23.30 f
M2/M2/M6/M1/M2/b (Add_half_151)          0.00      23.30 f
M2/M2/M6/M1/M2/U2/Z (CAN2X1)             0.18      23.47 f
M2/M2/M6/M1/M2/c_out (Add_half_151)      0.00      23.47 f
M2/M2/M6/M1/U1/Z (COR2X1)                0.26      23.74 f
M2/M2/M6/M1/c_out (Add_full_76)          0.00      23.74 f
M2/M2/M6/M2/c_in (Add_full_75)           0.00      23.74 f
M2/M2/M6/M2/M2/b (Add_half_149)          0.00      23.74 f
M2/M2/M6/M2/M2/U2/Z (CAN2X1)             0.18      23.91 f
M2/M2/M6/M2/M2/c_out (Add_half_149)      0.00      23.91 f
M2/M2/M6/M2/U1/Z (COR2X1)                0.26      24.17 f
M2/M2/M6/M2/c_out (Add_full_75)          0.00      24.17 f
M2/M2/M6/M3/c_in (Add_full_74)           0.00      24.17 f
M2/M2/M6/M3/M2/b (Add_half_147)          0.00      24.17 f
M2/M2/M6/M3/M2/U2/Z (CAN2X1)             0.18      24.35 f
M2/M2/M6/M3/M2/c_out (Add_half_147)      0.00      24.35 f
M2/M2/M6/M3/U1/Z (COR2X1)                0.26      24.61 f
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M2/M2/M6/M3/c_out (Add_full_74)          0.00      24.61 f
M2/M2/M6/M4/c_in (Add_full_73)           0.00      24.61 f
M2/M2/M6/M4/M2/b (Add_half_145)          0.00      24.61 f
M2/M2/M6/M4/M2/U2/Z (CAN2X1)             0.18      24.79 f
M2/M2/M6/M4/M2/c_out (Add_half_145)      0.00      24.79 f
M2/M2/M6/M4/U1/Z (COR2X1)                0.26      25.05 f
M2/M2/M6/M4/c_out (Add_full_73)          0.00      25.05 f
M2/M2/M6/c_out (Add_rca_4_19)            0.00      25.05 f
M2/M2/M7/c_in (Add_rca_4_18)             0.00      25.05 f
M2/M2/M7/M1/c_in (Add_full_72)           0.00      25.05 f
M2/M2/M7/M1/M2/b (Add_half_143)          0.00      25.05 f
M2/M2/M7/M1/M2/U2/Z (CAN2X1)             0.18      25.23 f
M2/M2/M7/M1/M2/c_out (Add_half_143)      0.00      25.23 f
M2/M2/M7/M1/U1/Z (COR2X1)                0.26      25.49 f
M2/M2/M7/M1/c_out (Add_full_72)          0.00      25.49 f
M2/M2/M7/M2/c_in (Add_full_71)           0.00      25.49 f
M2/M2/M7/M2/M2/b (Add_half_141)          0.00      25.49 f
M2/M2/M7/M2/M2/U2/Z (CAN2X1)             0.18      25.67 f
M2/M2/M7/M2/M2/c_out (Add_half_141)      0.00      25.67 f
M2/M2/M7/M2/U1/Z (COR2X1)                0.26      25.93 f
M2/M2/M7/M2/c_out (Add_full_71)          0.00      25.93 f
M2/M2/M7/M3/c_in (Add_full_70)           0.00      25.93 f
M2/M2/M7/M3/M2/b (Add_half_139)          0.00      25.93 f
M2/M2/M7/M3/M2/U2/Z (CAN2X1)             0.18      26.10 f
M2/M2/M7/M3/M2/c_out (Add_half_139)      0.00      26.10 f
M2/M2/M7/M3/U1/Z (COR2X1)                0.26      26.37 f
M2/M2/M7/M3/c_out (Add_full_70)          0.00      26.37 f
M2/M2/M7/M4/c_in (Add_full_69)           0.00      26.37 f
M2/M2/M7/M4/M2/b (Add_half_137)          0.00      26.37 f
M2/M2/M7/M4/M2/U2/Z (CAN2X1)             0.18      26.54 f
M2/M2/M7/M4/M2/c_out (Add_half_137)      0.00      26.54 f
M2/M2/M7/M4/U1/Z (COR2X1)                0.26      26.81 f
M2/M2/M7/M4/c_out (Add_full_69)          0.00      26.81 f
M2/M2/M7/c_out (Add_rca_4_18)            0.00      26.81 f
M2/M2/M8/c_in (Add_rca_4_17)             0.00      26.81 f
M2/M2/M8/M1/c_in (Add_full_68)           0.00      26.81 f
M2/M2/M8/M1/M2/b (Add_half_135)          0.00      26.81 f
M2/M2/M8/M1/M2/U2/Z (CAN2X1)             0.18      26.98 f
M2/M2/M8/M1/M2/c_out (Add_half_135)      0.00      26.98 f
M2/M2/M8/M1/U2/Z (CND2IX1)               0.19      27.17 f
M2/M2/M8/M1/c_out (Add_full_68)          0.00      27.17 f
M2/M2/M8/M2/c_in (Add_full_67)           0.00      27.17 f
M2/M2/M8/M2/M2/b (Add_half_133)          0.00      27.17 f
M2/M2/M8/M2/M2/U2/Z (CAN2X1)             0.18      27.34 f
M2/M2/M8/M2/M2/c_out (Add_half_133)      0.00      27.34 f
M2/M2/M8/M2/U2/Z (CND2IX1)               0.18      27.53 f
M2/M2/M8/M2/c_out (Add_full_67)          0.00      27.53 f
M2/M2/M8/M3/c_in (Add_full_66)           0.00      27.53 f
M2/M2/M8/M3/M2/b (Add_half_131)          0.00      27.53 f
M2/M2/M8/M3/M2/U6/Z (CAN2X1)             0.18      27.70 f
M2/M2/M8/M3/M2/c_out (Add_half_131)      0.00      27.70 f
M2/M2/M8/M3/U2/Z (CND2IX1)               0.20      27.90 f
M2/M2/M8/M3/c_out (Add_full_66)          0.00      27.90 f
M2/M2/M8/M4/c_in (Add_full_65)           0.00      27.90 f
M2/M2/M8/M4/M2/b (Add_half_129)          0.00      27.90 f
M2/M2/M8/M4/M2/U2/Z (CND2X1)             0.08      27.98 r
M2/M2/M8/M4/M2/U4/Z (CND2X1)             0.11      28.09 f
```

```
  M2/M2/M8/M4/M2/sum (Add_half_129)        0.00      28.09 f
  M2/M2/M8/M4/sum (Add_full_65)            0.00      28.09 f
  M2/M2/M8/sum[3] (Add_rca_4_17)           0.00      28.09 f
  M2/M2/sum[31] (Add_rca_3)                0.00      28.09 f
  M2/sum[63] (Add_rca64_0)                 0.00      28.09 f
  U973/Z (CND2IX1)                         0.07      28.16 r
  U972/Z (CND2X1)                          0.09      28.25 f
  result_copy_reg[63]/D (CFD1XL)           0.00      28.25 f
  data arrival time                                  28.25

  clock clock (rise edge)                 29.00      29.00
  clock network delay (propagated)         0.00      29.00
  clock uncertainty                       -0.25      28.75
  result_copy_reg[63]/CP (CFD1XL)          0.00      28.75 r
  library setup time                      -0.47      28.28
  data required time                                 28.28
  ---------------------------------------------------------
  data required time                                 28.28
  data arrival time                                 -28.25
  ---------------------------------------------------------
  slack (MET)                                         0.03


****************************************
Report : area
Design : div
Version: C-2009.06-SP5
Date   : Sun Dec 11 05:36:55 2016
****************************************

Library(s) Used:

    tc240c (File: /apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25)

Number of ports:              165
Number of nets:              1745
Number of cells:             1326
Number of references:          48

Combinational area:       4012.000000
Noncombinational area:    1090.500000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:          5102.500000
Total area:                 undefined

Loading db file '/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_BCCOM25'
Loading db file '/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25'
Warning: Main library 'tc240c' does not specify the following unit required
for power: 'Leakage Power'. (PWR-424)
Information: Propagating switching activity (low effort zero delay
simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)
```

```
****************************************
Report : power
        -analysis_effort low
Design : div
Version: C-2009.06-SP5
Date   : Sun Dec 11 05:36:56 2016
****************************************


Library(s) Used:

    tc240c (File: /apps/toshiba/sjsu/synopsys/tc240c/tc240c.db_WCCOM25)


Operating Conditions: WCCOM25   Library: tc240c
Wire Load Model Mode: top

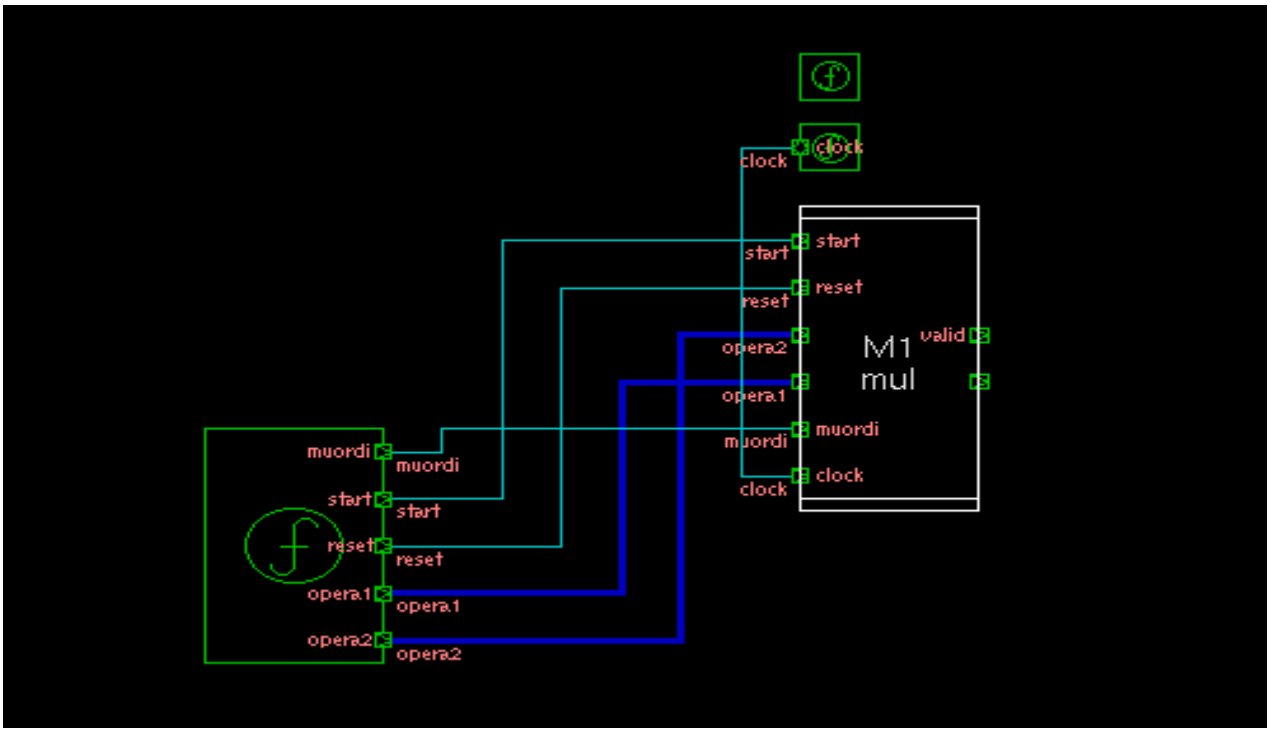

Global Operating Voltage = 2.3
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = Unitless

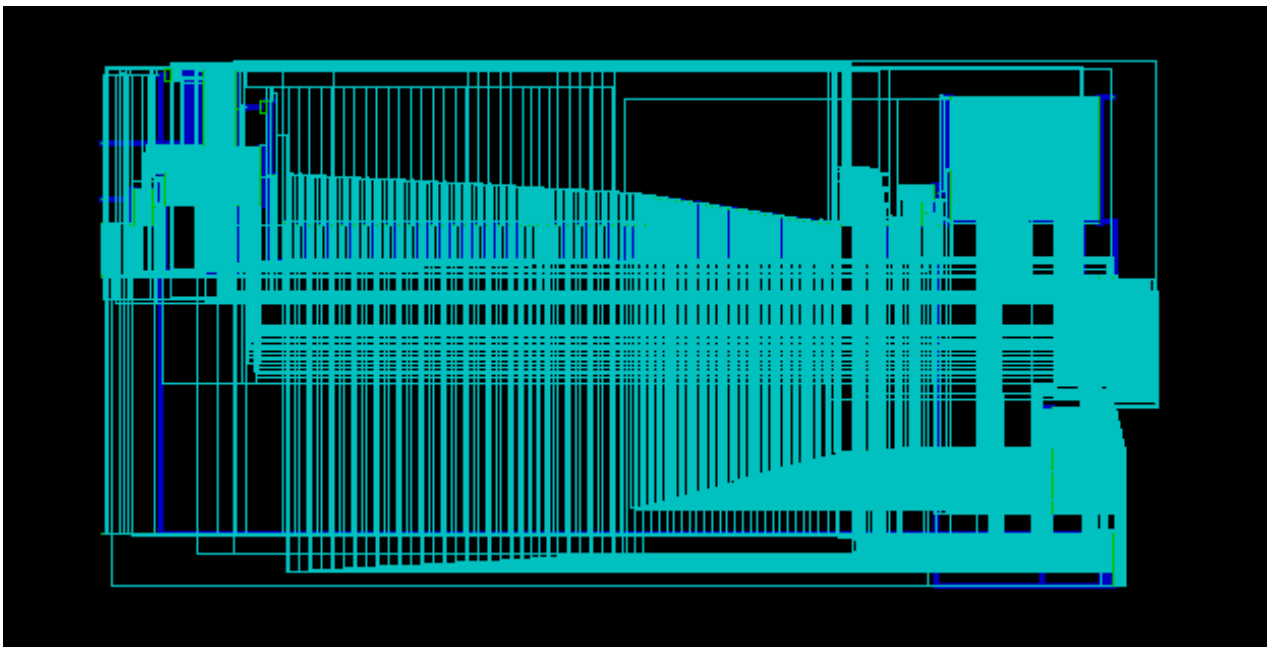

  Cell Internal Power  =   2.0386 mW   (88%)
  Net Switching Power  = 271.2307 uW   (12%)
                         ---------
Total Dynamic Power    =   2.3098 mW  (100%)

Cell Leakage Power     =   0.0000
```

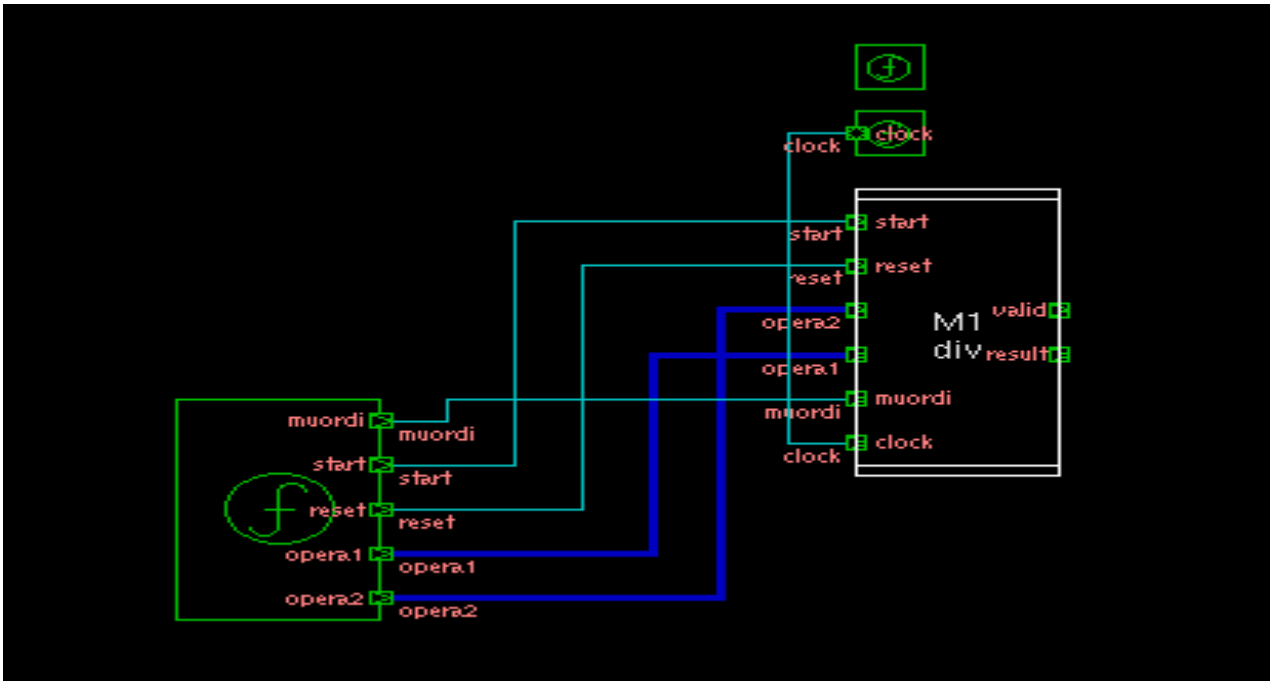
C.4 Selected Screenshot Circuits from Synthesis (Design Compiler)

For Multiplier:





For Divider:


clock
clock
start
reset
opera2
opera1
muordi
clock
start
reset
valid
result
M1
div
muordi
muordi
start
start
reset
reset
opera1
opera1
opera2
opera2


test_div.M11.vv4