KAZAKH BRITISH TECHNICAL UNIVERSITY

School of Information Technology and Engineering

Laboratory work 5 week7
FOUR-BIT BINARY PARALLEL ADDER.

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Aims:
investigate 4-bit binary parallel adder operation; make an addition according to the task. Compare the results of the addition with ones, made by theoretical way.

Practice task:
Preparation to lab work

Answers to Questions

Learn the information about adders.

Draw look-ahead carry generator scheme with application of Scheme Design System.

Consider experiment's scheme and analyze its operation. Draw it using Scheme Design System.

Draw the scheme of 8-bit binary parallel adder on the basis of 7483 chip with application of Scheme Design System. It will be the scheme for experiment 5B.

Answer the questions below in written form.

What is a half-(full-) adder?

A half-adder is a basic digital circuit used in computing to add two binary numbers. It can add two single-bit binary numbers (A and B) and outputs the sum (S) of the two bits and a carry-out (Cout) bit representing whether there's a carry to the next higher bit position.

Show the truth table for half-(full-) adder.

A	B	$Cout$	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Show the algebraic expressions for sum and carry for half-(full-) adder.

$$S = A \oplus B$$
$$\text{Cout} = A \cdot B$$

$$S = A \oplus B \oplus \text{Cin}$$
$$\text{Cout} = (A \cdot B) + (\text{Cin} \cdot (A \oplus B))$$

What is a binary parallel adder?

A binary parallel adder is a digital circuit that adds two binary numbers in parallel, meaning that all corresponding bits (same bit position) of the two numbers are added simultaneously. This is in contrast to a serial adder, where bits are added sequentially.

What is a serial adder?

A serial adder is a digital circuit that adds two binary numbers serially, meaning that the bits are added sequentially, one after the other, starting from the least significant bit (LSB) to the most significant bit (MSB).

How many adders are needed to construct 7-bit parallel adder?

To construct a 7-bit parallel adder, you would need seven full-adders. Each full-adder would be responsible for adding one bit from each of the two 7-bit numbers, along with any carry from the previous less significant bit addition. This arrangement allows you to add the two 7-bit numbers in parallel, completing the addition in a single step.

How many bits have typical full-adders ICs got?

Typical full-adder ICs usually have 3 bits.

How to connect IC's full-adders if one package is not enough?

To connect multiple full-adder ICs for a larger adder:

1. Connect the carry-out (Cout) of one IC to the carry-in (Cin) of the next.
2. Connect the sum (S) outputs of all the full-adder ICs together.
3. Provide inputs (A, B, and Cin for the first IC) to the appropriate inputs.
4. The carry-out (Cout) of the last IC is the final carry-out of the adder.

What is a look-ahead carry generator?

A look-ahead carry generator is a circuit used in digital electronics to speed up the carry propagation in binary addition. In a typical binary adder, the carry out from each bit addition depends on the carry in and the two bits being added, which causes a ripple effect where each carry bit depends on the carry bit from the previous less significant bit.

What functions can look-ahead carry generator produce?

A look-ahead carry generator produces the carry-out (Cout) for each bit position in binary addition. It uses the generate (G) and propagate (P) functions.

LAB WORK PERFORMANCE

1.Demonstrate presence of your home preparation for lab work to your instructor.

2.Pass test of 10 questions.

3.Get a permission to begin the work.

4.Mount the scheme of experiment 5A on the breadboard and perform it.

5.Make a conclusion about functionality of the scheme. Compare your results with theoretical ones.

6.Demonstrate your results to your instructor. If your results are correct you may dismount your scheme, if no – find the mistake.

7.Repeat steps 4 to 6 for experiment 5B.

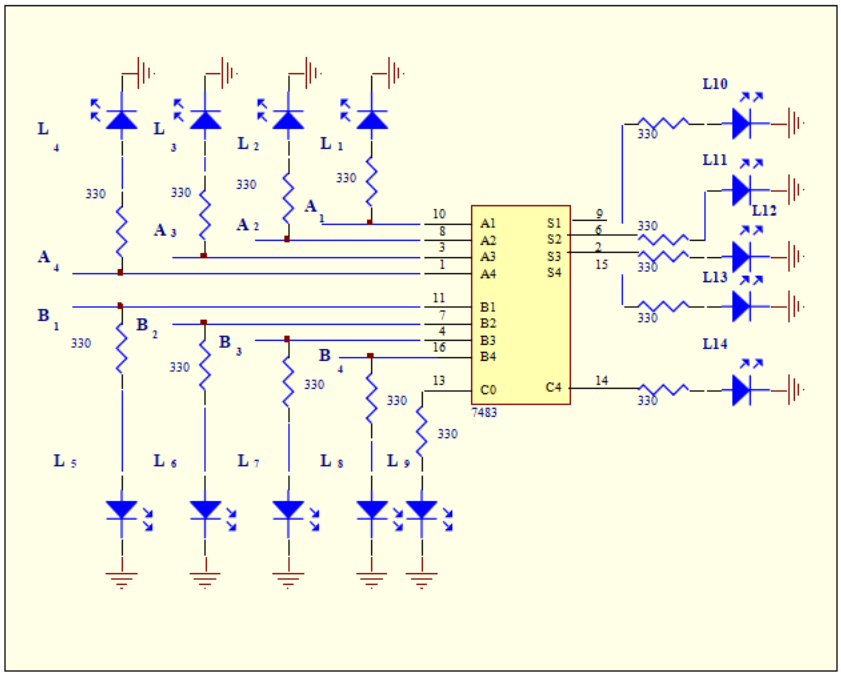
8.Be ready to answer your instructor's questions in process of work.

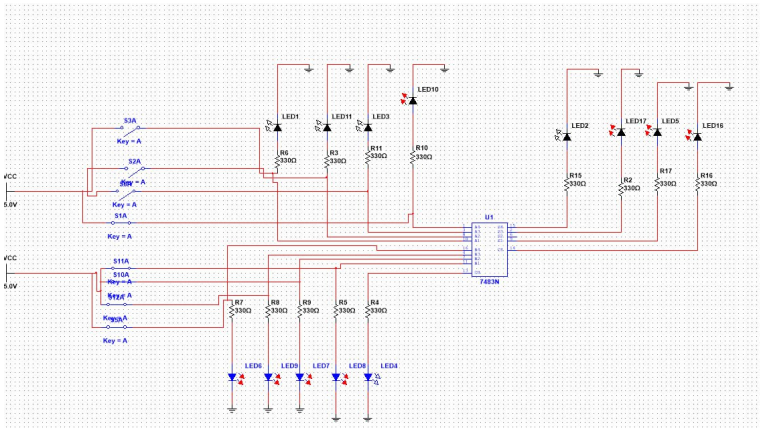
9.Complete your work, dismount your schemes, clean your working place.

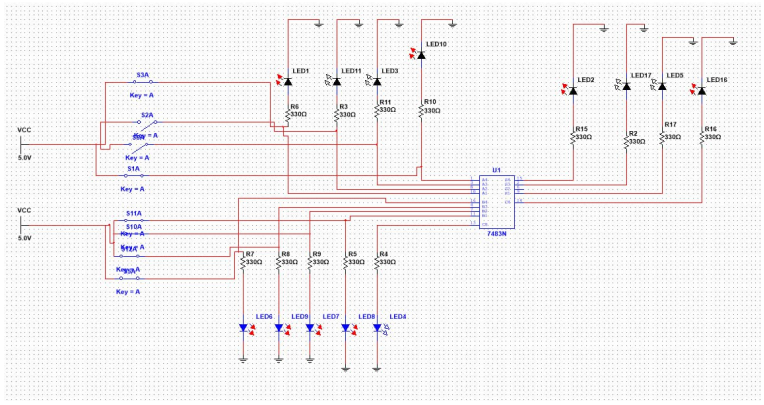
10.Answer your instructor's final questions, obtain your mark.

11.Ask your instructor's permission to leave.

Experiment 5A. Realize the following circuit on a breadboard. Connecting A and B inputs to either GND (for 0) or VCC (for 1) based on the following table, fill in the blanks. Connect pin 5 of 7483 to VCC and pin 12 to GND. Write ON or OFF for LEDs.




VCC
5.0V
S3A
S2A
S1A
S11A
S10A
S12A
S13A
Key = A
U1
7483N
LED1
LED11
LED3
LED10
LED2
LED17
LED5
LED16
LED6
LED9
LED7
LED8
LED4
R6 330Ω
R3 330Ω
R11 330Ω
R10 330Ω
R15 330Ω
R2 330Ω
R17 330Ω
R16 330Ω
R7 330Ω
R8 330Ω
R9 330Ω
R5 330Ω
R4 330Ω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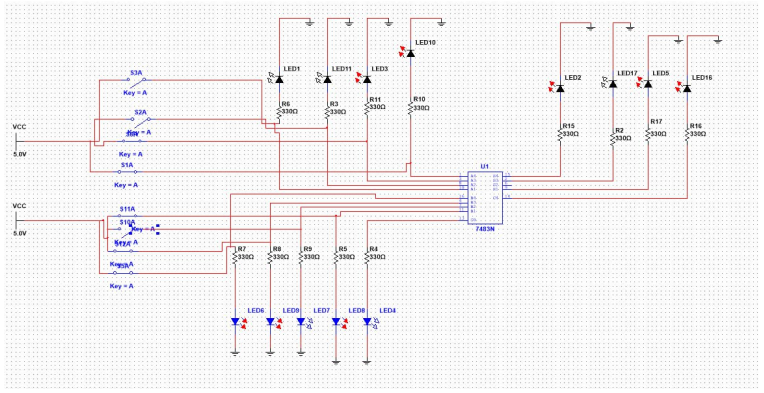
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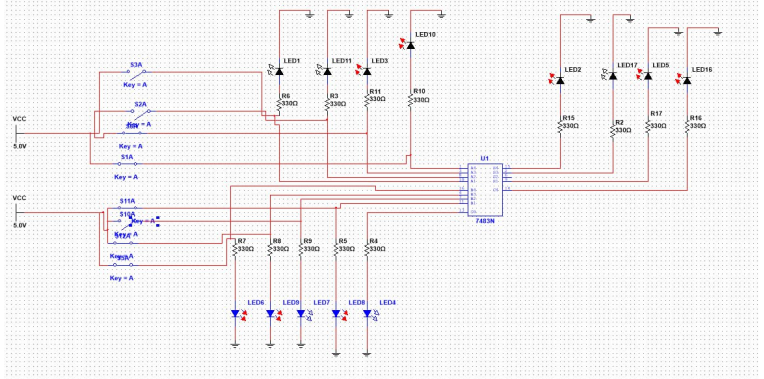
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R9 330Ω
R5 330Ω
R4 330Ω

Numbers for addition								inputs									outputs				
A1	A2	A3	A4	B1	B2	B3	B4	L1	L2	L3	L4	L5	L6	L7	L8	L9	L 10	L 11	L 12	L 13	L 14
1	1	0	0	1	1	0	1	0	0	1	1	1	1	0	1	0	0	0	0	0	1
0	0	0	1	1	1	1	1	0	0	1	1	1	1	1	1	0	0	0	0	0	1
1	0	0	1	0	1	1	0	1	0	0	1	1	0	0	1	0	0	0	1	0	1

TEST QUESTIONS

1. Name the inputs_____and outputs_____of a half-adder.
   A. A_0,B_0, C_{in}, $\sum_0$ B. A_0,B_0, C_{out}, $\sum_0$ C. C_{in}, $\sum_0$ A_0,B_0 D. C_{out}, $\sum_0$ A_0,B_0,
   E. $\sum_0$ A_0,B_0

2. The first strip to obtain resistance 220 Ω must be
   A. white B. Green C. Brown D. Yellow E. red

3. What statement is wrong?
   A. (X+Y)(X+Z)=X+YZ B. X(Y+Z)=XY+XZ C. X+XY=X
   D. (X+Y)′=X′Y′ E. X(X+Y)=X+Y

4. A Boolean function is an expression, formed with
   A. binary numbers
   B. binary variables
   C. binary variables and operators
   D. binary variables, the two binary operators OR and AND, the unary operator NOT, parentheses, and equal sign.
   E. binary variables, the binary operators OR, AND, and NOT, parentheses, and equal sign.

5. 7483 is
   A. 3*8 decoder B. 4-bit magnitude comparator C. Code converter
   D. 4-bit full adder E. priority encoder

6. What factor is, as a rule, more important for the circuit?
   A. number of gates B. Types of gates C. Propagation delay
   D. number of levels of implementation D. None of above mentioned

7. Serial binary adder consists of
   A. n full adders, connected in cascade, where n-number of digits for addition
   B. n half adders, connected in cascade, where n-number of digits for addition
   C. n full adders and a storage device, where n-number of digits for addition
   D. n half adders and a storage device, where n-number of digits for addition
   E. one full adder and a storage device

8. A half-subtractor is a_____circuit, that subtracts_____bits and produces their difference.
   A. sequential; three
   B. sequential; two
   C. combinational; two
   D. combinational; three
   E. sequential or combinational; three

9. Make addition of binary numbers: 1001 and 1010. Result is
   A. 10011 B.1001 C. 1100 D. 11001 E. 10101

10. To construct 6-bit parallel adder we must use cascade of such full-adders IC s as
    A. two 2-bit and one 1-bit B. one 2-bit and one 3-bit C.one 4-bit and one 1-bit
    D. five 1-bit E. none of above mentioned, because 5-bit parallel adder IC exists itself