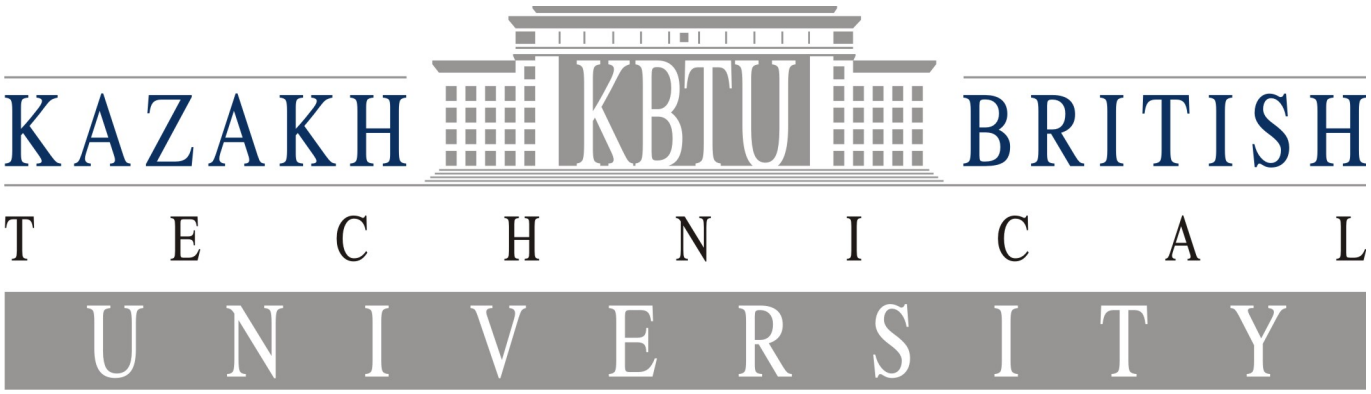


School of Information Technology and Engineering

**Laboratory work 10 week11**
**D flip- lop**

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**PREPARATION TO LAB WORK.**

1. Learn the information about flip-flops.
2. Consider the scheme of experiment 11A and define the results theoretically. Draw the circuit with application of Scheme Design System.
3. Draw the D-flip-flop implemented with NAND gates (using Scheme Design System) for the experiment 11B.
4. Answer the question below in written form.
   - 4.1. What circuit is called sequential?
   - 4.2. What sequential circuit is called synchronous?
   - 4.3. What sequential circuit is called asynchronous?
   - 4.4. What is a master-clock generator?
   - 4.5. What circuits are called clocked sequential circuits?
   - 4.6. What is a flip-flop?
   - 4.7. What types of flip-flops do you know?
   - 4.8. Show truth tables for all types of flip-flops.
   - 4.9. Show the typical schemes of RS, D, T, JK-flip-flops and describe their operation. (Use Scheme Design System).
   - 4.10. What is a master-slave flip-flop?
   - 4.11. What is setup time and hold time for flip-flop?
   - 4.12. Show excitation tables for all types of flip-flops.
   - 4.13. What types of flip-flops' triggering do you know?

**LAB WORK PERFORMANCE.**

1. Demonstrate presence of your home preparation for lab work to your instructor.
2. Pass test of 10 questions.
3. Get a permission to begin the work.
4. Mount the scheme of experiment 11A on the breadboard and perform it. Fill in the table.
5. Make a conclusion about functionality of the scheme. Compare your results with theoretical ones.
6. Demonstrate your results to your instructor. If your results are correct you may dismount your scheme, if no – find the mistake.
7. Repeat steps 4-6 for experiment 11B.
8. Be ready to answer your instructor's questions in process of work.
9. Complete your work, dismount your schemes, clean your working place.
10. Answer your instructor's final questions, obtain your mark.
11. Ask your instructor's permission to leave.

Figure 1: Preparation for lab

**Answers of questions**

# 1 Learn about Flip-Flops:

Start by understanding the basics of flip-flops, their types, operation, and applications. Flip-flops are fundamental building blocks in digital electronics used for storing binary information.

# 2 Consider Experiment 11A

Review the schematic and theoretical outcomes of Experiment 11A. Understand how the D-flip-flop operates in theory before proceeding with the practical aspect.

# 3 Draw D-flip-flop with NAND gates:

Use a Scheme Design System to draw the circuit of a D-flip-flop implemented with NAND gates. This involves creating the circuit diagram using NAND gates to represent the functionality of a D-flip-flop.

# 4 Answer Theoretical Questions:

- 4.1. **Sequential Circuit:** A circuit is called sequential if its output depends not only on the present input but also on the previous inputs.
- 4.2 **Synchronous Sequential Circuit:**In a synchronous sequential circuit, all flip-flops are clocked simultaneously.
- 4.3. **Asynchronous Sequential Circuit:** In an asynchronous sequential circuit, the outputs depend on both the present inputs and the previous state of the circuit.
- 4.4. **Master-clock generator:** It's a circuit that generates the clock signal used to synchronize the operation of synchronous sequential circuits.
- 4.5. **Clocked Sequential Circuits:** These are sequential circuits that use a clock signal to synchronize their operation.
- 4.6. **Flip-Flop:** A flip-flop is a digital circuit element capable of storing one bit of information.
- 4.7. **Types of Flip-Flops:** Common types include SR, D, JK, and T flip-flops.
- 4.8. **Truth Tables:** Provide truth tables for each type of flip-flop, showing the relationship between inputs and outputs.
- 4.9. **Schemes and Operation:** Draw typical schemes for RS, D, T, and JK flip-flops and describe their operation.
- 4.10. **Master-Slave Flip-Flop:** It's a type of flip-flop where two flip-flops are connected in series, and the second flip-flop only changes state when the clock signal changes.
- 4.11. **Setup and Hold Time:** Setup time is the minimum time before the clock transition during which the data must be stable, while hold time is the minimum time after the clock transition during which the data must be stable.
- 4.12. **Excitation Tables:** Show the excitation tables for each type of flip-flop, indicating the inputs required to transition between states.
- 4.13. **Triggering Types:** Flip-flops can be edge-triggered or level-triggered.

# 5 Lab Work Performance:

Follow the steps outlined for the lab work, including demonstrating your preparation, passing a test, obtaining permission to start, performing experiments 11A and 11B, comparing results with theory, and answering any questions from your instructor.

# 6 Conclusion and Clean-up:

Conclude your work, clean your workspace, and answer any final questions from your instructor before obtaining your mark and leaving.

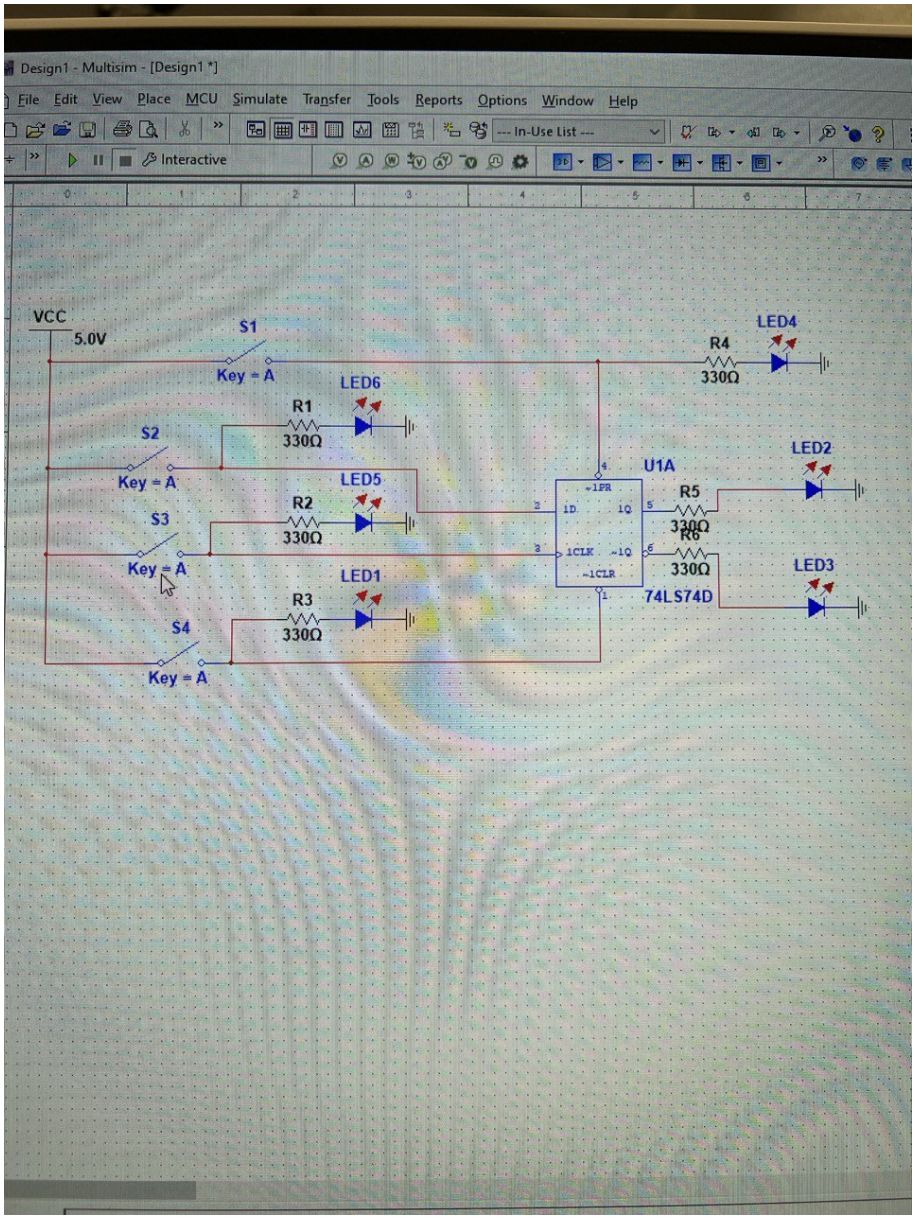


Figure 2: D flip flop on Multisim

**TEST QUESTIONS**

1. _____ flip-flop gives us uncertainty if set and reset inputs have value 1 at the same time.
A. RS and clocked RS B.RS or clocked RS C. D D. JK E. T

2. This is characteristic table of _____ flip-flop.

| | Q (t+1) |
|---|---|
| 0 | 0 |
| 1 | 1 |

A. RS B. Clocked RS C. D D. JK E. T

3. This is excitation table of _____ flip-flop.

| Q(t) | Q (t+1) | | |
|---|---|---|---|
| 0 | 0 | 0 | X |
| 0 | 1 | 1 | X |
| 1 | 0 | X | 1 |
| 1 | 1 | X | 0 |

A. RS B. Clocked RS C. D D. JK E. T

4. What state sequence for Q(t+1) is correct?

| J | K | Q (t+1) |
|---|---|---|
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

A. 1, 0, Q(t), ? B. 1, 0,?, Q(t) C. Q(t), 0,1,Q´(t) D. Q(t), 0,1, 1 E. Q(t), 0,1, 0

5. Set-dominate flip-flop has got _____ input(s).
A. 1 B. 2 C. 1 or 2 D. 3 E. 2 or 3

6. D flip-flop characteristic equation is _____
A. Q(t+1)=DQ B. Q(t+1)=D+Q C. Q(t+1)=D
D. Q(t+1)=D´Q E. Q(t+1)=D´

7. A state equation of the sequential circuit is
A. an expression to describe next state of the circuit
B. an expression to describe present state of the circuit
C. a Boolean function that specifies the present state conditions
D. a Boolean function that specifies the present state conditions that make the next state equal to 1
E. a Boolean function that specifies the next state conditions that make the present state equal to 1

8. How many options to gain state 10 will the circuit with the state table below have?

| Present state | | Next state | | | |
|---|---|---|---|---|---|
| | | X=0 | | X=1 | |
| A | B | A | B | A | B |
| 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 |

A. 1 B. 2 C. 3 D. 4 E. 5

Figure 3: Quiz 1

| | A | B | C | D | E | F | G | H | I | J | K |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | | **D** | **CLK** | **CD** | **SD** | **LED1** | **LED2** | **LED3** | **LED4** | **LED5** | **LED6** |
| 2 | **1** | 0 | 0 | 5 | 5 | OFF | OFF | ON | ON | OFF | ON |
| 3 | **2** | 0 | 5 | 5 | 5 | OFF | ON | ON | ON | OFF | ON |
| 4 | **3** | 0 | 0 | 5 | 5 | OFF | OFF | ON | ON | OFF | ON |
| 5 | **4** | 5 | 0 | 5 | 5 | ON | OFF | ON | ON | OFF | ON |
| 6 | **5** | 5 | 5 | 5 | 5 | ON | ON | ON | ON | ON | OFF |
| 7 | **6** | 5 | 0 | 5 | 5 | ON | OFF | ON | ON | ON | OFF |
| 8 | **7** | 5 | 0 | 0 | 5 | ON | OFF | OFF | ON | OFF | ON |
| 9 | **8** | 5 | 0 | 5 | 5 | ON | OFF | ON | ON | OFF | ON |
| 10 | **9** | 5 | 0 | 5 | 0 | ON | OFF | ON | OFF | ON | OFF |
| 11 | **10** | 5 | 0 | 5 | 5 | ON | OFF | ON | ON | ON | OFF |
| 12 | **11** | 5 | 0 | 0 | 5 | ON | OFF | OFF | ON | OFF | ON |
| 13 | **12** | 5 | 0 | 5 | 5 | ON | OFF | ON | ON | OFF | ON |
| 14 | **13** | 5 | 0 | 5 | 0 | ON | OFF | ON | OFF | OFF | ON |
| 15 | **14** | 5 | 0 | 5 | 5 | ON | OFF | ON | ON | OFF | ON |
| 16 | **15** | 0 | 0 | 5 | 5 | OFF | OFF | ON | ON | OFF | ON |
| 17 | **16** | 0 | 0 | 0 | 5 | OFF | OFF | OFF | ON | OFF | ON |
| 18 | **17** | 0 | 0 | 5 | 5 | OFF | OFF | ON | ON | OFF | ON |
| 19 | **18** | 0 | 0 | 5 | 0 | OFF | OFF | ON | OFF | ON | OFF |
| 20 | **19** | 0 | 0 | 5 | 5 | OFF | OFF | ON | ON | ON | OFF |
| 21 | **20** | 0 | 5 | 5 | 5 | OFF | ON | ON | ON | ON | OFF |
| 22 | **21** | 0 | 0 | 5 | 5 | OFF | OFF | ON | ON | ON | OFF |
| 23 | **22** | 0 | 0 | 0 | 5 | OFF | OFF | OFF | ON | OFF | ON |
| 24 | **23*** | 0 | 0 | 0 | 0 | OFF | OFF | OFF | OFF | OFF | ON |
| 25 | **24** | 0 | 0 | 5 | 0 | OFF | OFF | ON | OFF | ON | OFF |
| 26 | **25** | 0 | 0 | 5 | 5 | OFF | OFF | ON | ON | ON | OFF |



Figure 4: Quiz 1

- D
- C
- D
- C
- C
- C
- A
- B
- C
- B