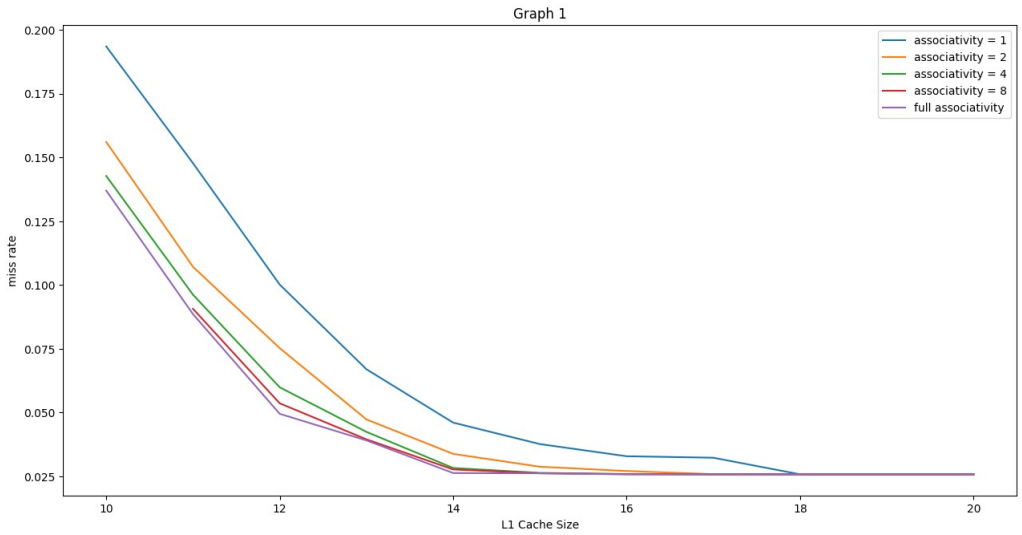
GRAPH 1

(total number of simulations: 55)



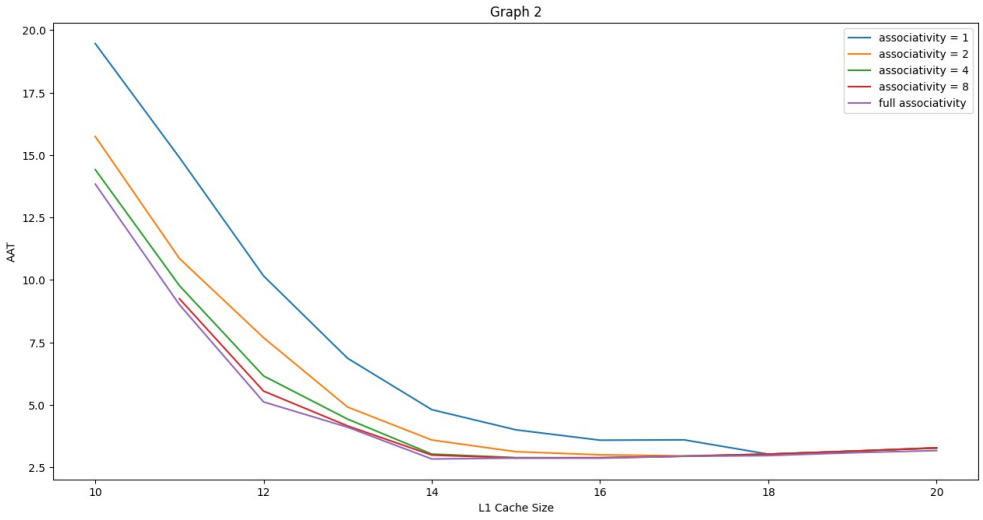
L1 cache size: 2^{10} - 2^{20}
BLOCKSIZE = 32.
L2 cache: None.
Replacement policy: LRU
Inclusion property: non-inclusive

Discussion:

1. The graph shows that for a fixed associativity, the miss rate decreases, as the L1 cache size increases. Actually larger caches can hold more data which plays major role in reducing cache misses.
   And for a fixed cache size, the miss rate decreases as associativity increases. This might be due to the reduced number of conflict misses, as a higher associativity allows more blocks to share the same index.
2. From the graph, we can see that the compulsory miss rate is **0.025**. Cause after this point the miss rate does not change even if the cache size increases.
3. The average miss rate for associativity 1, 2, 4, 8, and full associativity is 0.06681, 0.052632, 0.047751, 0.036704, and 0.045083. So, the conflict miss rate is,
   a. 0.066809 – 0.045083 = **0.021726**, for associativity = 1
   b. 0.052632 – 0.045083 = **0.007548**, for associativity = 2
   c. 0.047751 – 0.045083 = **0.002668**, for associativity = 4
   d. 0.036704 – 0.035895 = **0.000809**, for associativity = 8

GRAPH 2

(total number of simulations: 55)



L1 cache size: 2^{10} - 2^{20}
L1 Associativity: [1, 2, 4, 8, FA]
BLOCKSIZE = 32.
L2 cache: None.
Replacement policy: LRU
Inclusion property: non-inclusive

Discussion:

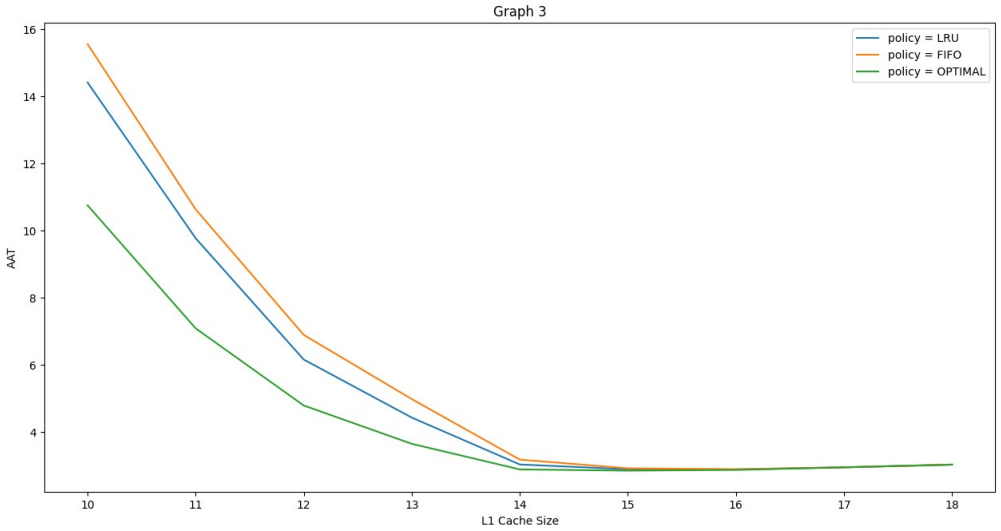
1. As the cache size increases, the Average Access Time (AAT) decreases up to a certain point because larger caches reduce miss rate which improves AAT.

2. From the graph, we can see that for a memory hierarchy with only an L1 cache and BLOCKSIZE = 32, **Full associativity** at a cache size of **2^{14} bytes** yields the lowest AAT which is approximately 2.83473.

Sample cover page for MP1.

GRAPH 3

(total number of simulations: 27)



L1 cache size: $2^{10} – 2^{18}$
L1 Associativity: 4
BLOCKSIZE = 32.
L2 cache: None.
Replacement policy: [LRU, FIFO, OPTIMAL]
Inclusion property: non-inclusive

Discussion:

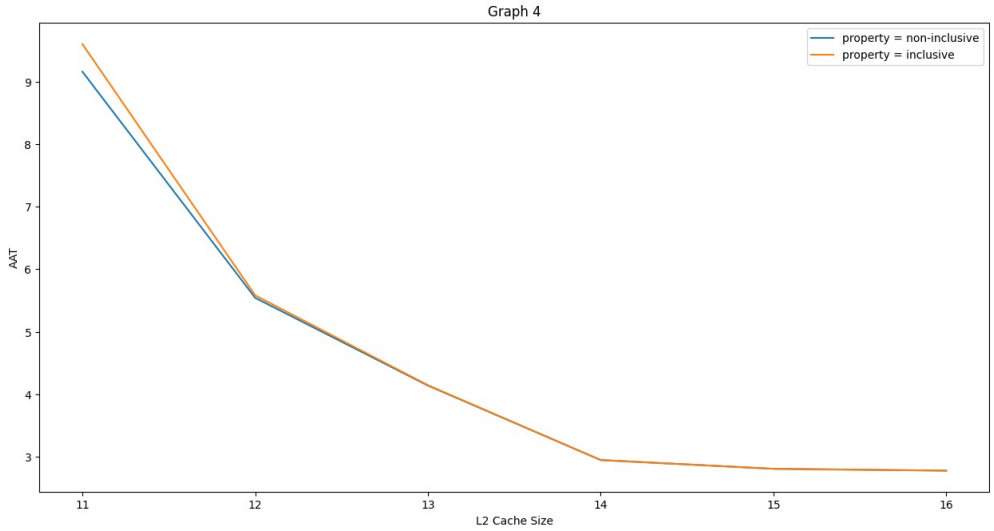
1. Discuss trends in the graph. Which replacement policy yields the best (*i.e.*, lowest) AAT?

1. For all three replacement policies (LRU, FIFO, and OPTIMAL), the Average Access Time (AAT) generally decreases as the cache size increases because larger caches reduce miss rate which improves AAT.

2. From the graph, we can see that the **OPTIMAL policy** yields the lowest AAT for all cache sizes which is also expected.

GRAPH 4

(total number of simulations: 12)



L1 cache: 1024
L1 Associativity: 4
L2 cache size: 2^{11} - 2^{16}
L2 Associativity: 8
BLOCKSIZE = 32
Replacement policy: LRU
Inclusion property: [non-inclusive, inclusive]

Discussion:

1. For both non-inclusive and inclusive properties, the AAT decreases as the L2 cache size increases. A larger L2 cache helps to reduce the AAT by providing more capacity to hold data, thus reducing the cache misses as well as decreasing AAT
2. The **non-inclusive** property consistently yields a slightly lower AAT than the inclusive property across all L2 cache sizes.