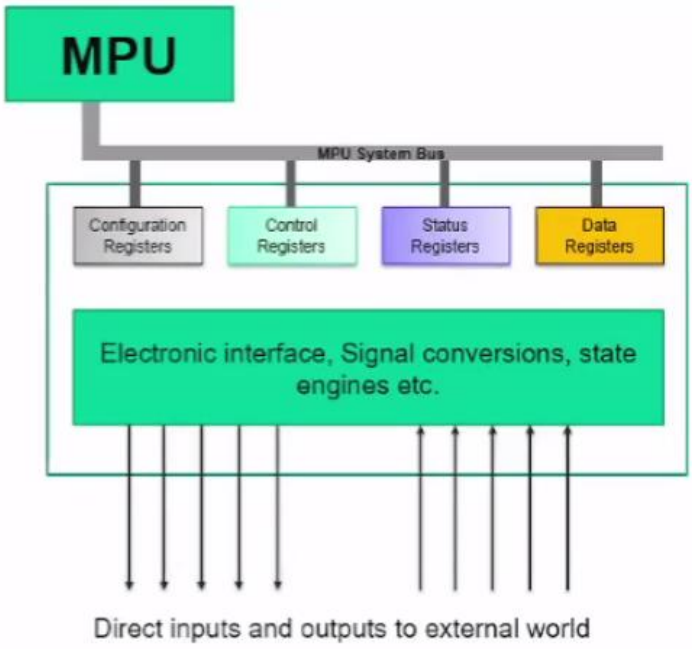
IoT - Week 8

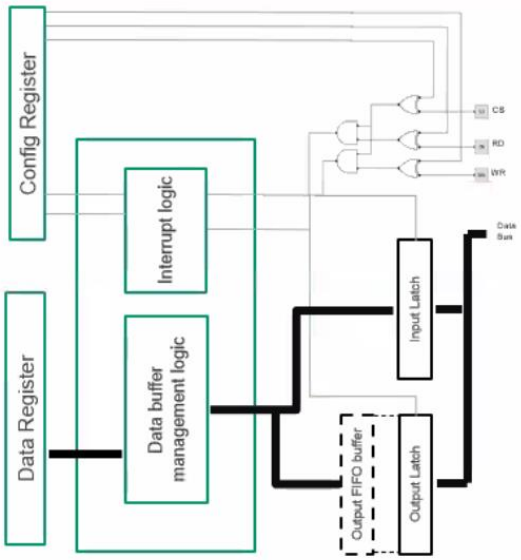
Pheriperal interfaces: The general structure



Direct inputs and outputs to external world

- *A peripheral module in general communicate with the MPU via a set of registers*
  - *These registers are mapped onto specific IO port addresses of the MPU bus*
- *Four main types of registers*
  - *Configuration registers*
    - *Typically used to provide initial configuration of the peripheral interface*
  - *Control (Command) registers*
    - *Used to send instruction on specific tasks and initiate functional operations*
  - *Status registers*
    - *Read operational status of the peripheral device including any error conditions*
  - *Data registers*
    - *Used to transfer data between the MPU and peripheral device*

Parallel Slave Port

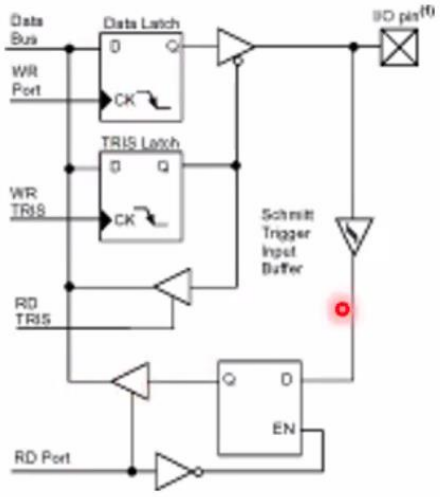


- *Used to interface with a microprocessor / system bus of an external device*
- *Compatible with control and data protocols of the external bus*
- *Configuration register provides initial setup such as enabling interrupts, polarity selection of the data latch, etc.*
- *Data output is through the write buffer register (which is usually a FIFO buffer), while read register provides the data input path*
- *Status register shows the condition of the read and write buffers*

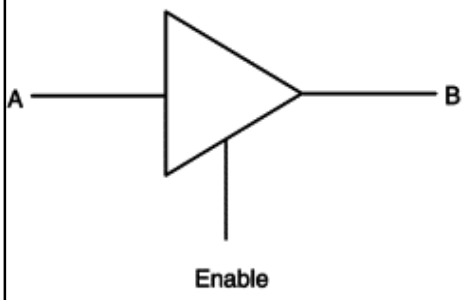
Bit Addressable Digital IO Ports

- *Bit addressable IO ports provide direct access to individual pins of the microcontroller via their respective control / data registers*
- *At hardware level these pins can provide different functions and capabilities, often controlled by the configuration register*
  - *Simple digital input / output with data latching*
  - *Combined analog / digital IO*
  - *Additional physical layer properties such as*
    - *Resister Pull-up / Pull-down*
    - *Open collector (drain) with tri-state outputs*
    - *Schematic trigger (hysteresis) inputs*

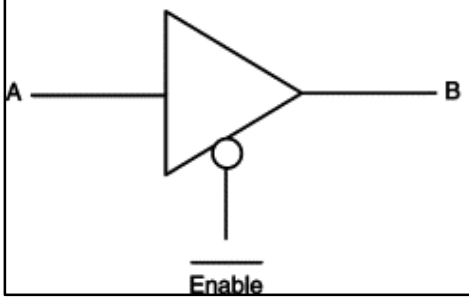
Bit Addressable Digital IO Ports



- *Simple Bit-addressable digital IO port in PIC16XXX series*
- *Configured via TRIS register that determine whether the individual bit act as an Input pin or as a latched output pin*
  - *Input pin when TRIS is true*
- *Has Schmitt trigger buffers that implement a hysteresis band to support noisy inputs*
- *Input can be latched or in transparent mode via an external **RDPort** signal*
- *The same configuration is repeated for all 8 bits in the IO port (PORTD)*

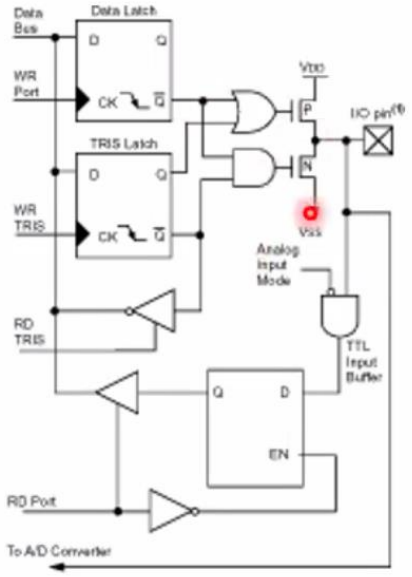


Enable	A	B
0	0	Z
0	1	Z
1	0	0
1	1	1



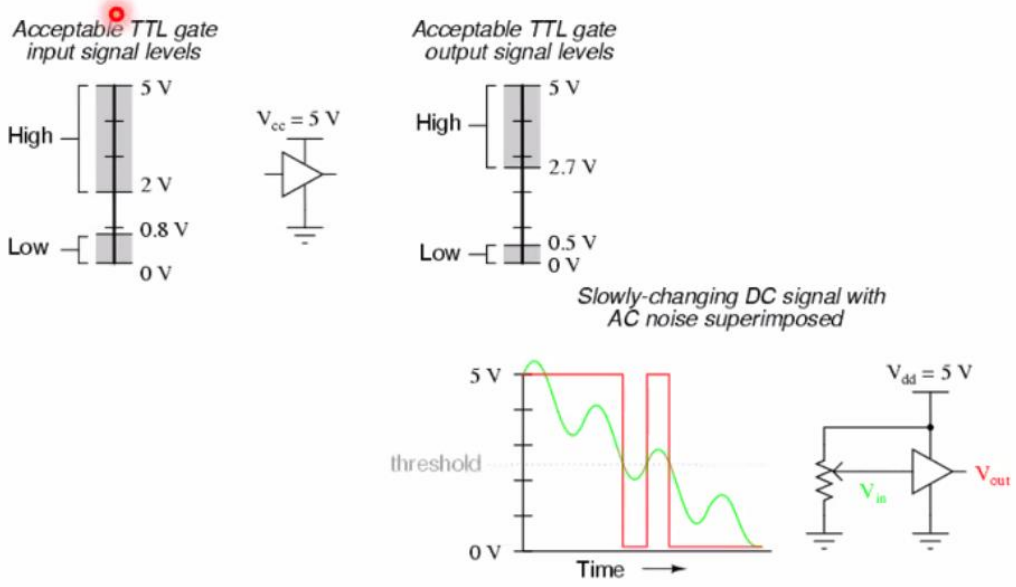
$\overline{\text{Enable}}$	A	B
0	0	0
0	1	1
1	0	Z
1	1	Z

Bit Addressable Digital IO Ports

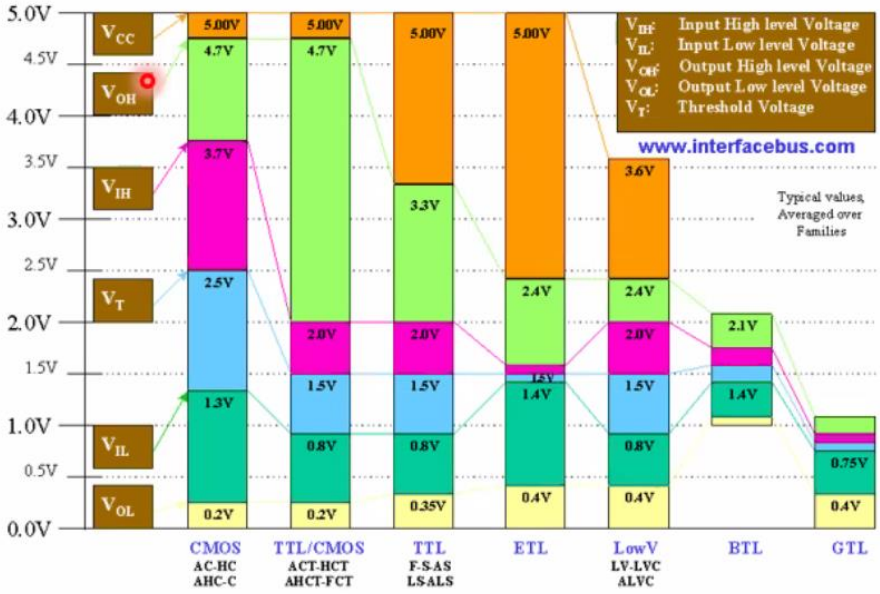


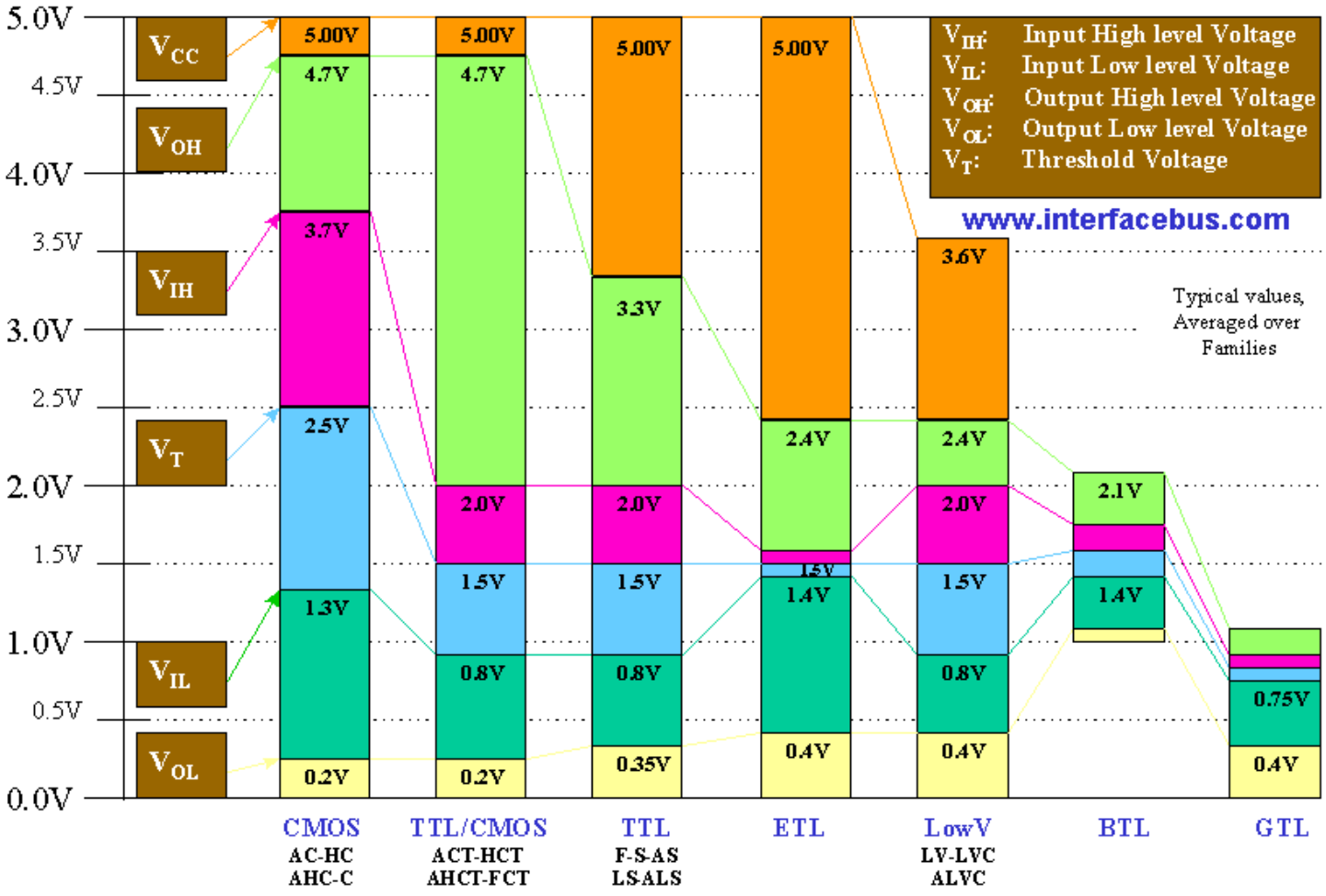
- *Digital bit addressable port with high-current capability and analog input support (PORTA in PIC16XXX)*
- *Configured via two registers*
  - *TRIS for direction control*
  - *Analog Input Mode – enable analog input*
- *Two MOSFET at the output stage allow high current driving and sinking*
- *Selecting Analog input mode disable digital reading*
  - *Pin must be in input mode to support analog input mode*
  - *Separate AtoD converter (not shown in the schematic) is required*

Digital IO – Practical voltage levels

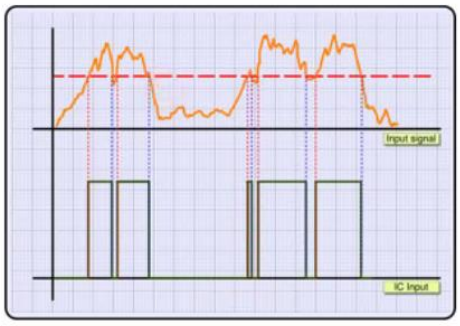


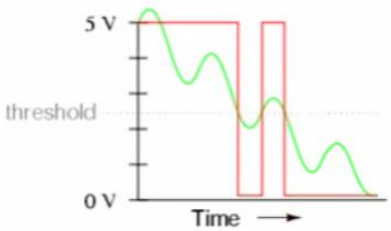
Logic Levels – Different families





Schmitt Trigger Inputs

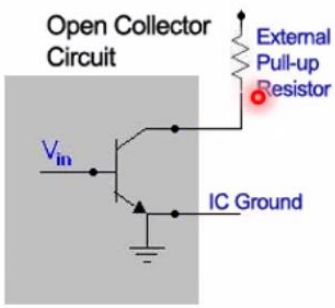


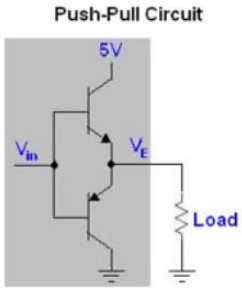


- *Use of single threshold is problematic*
  - *Threshold may not be consistent*
  - *Signal may cross threshold due to noise*
- ***Solution**: Use different thresholds for Low -> High and High - > Low transitions*

Gates with Schmitt Trigger Inputs

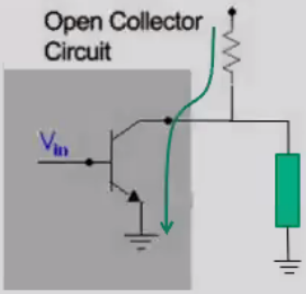
Digital IO – Push-Pull Vs Open outputs



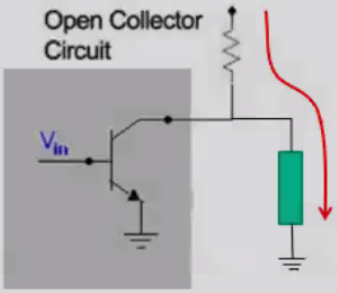


- *An open (collector / drain) configuration provides active driving only on one logic state*
- *External pull-up resisters are needed to drive the load when the device output is on "Open" state*
  - *Loading on the resister must be carefully considered to ensure correct logic state at the output*

Digital IO – Push-Pull Vs Open outputs

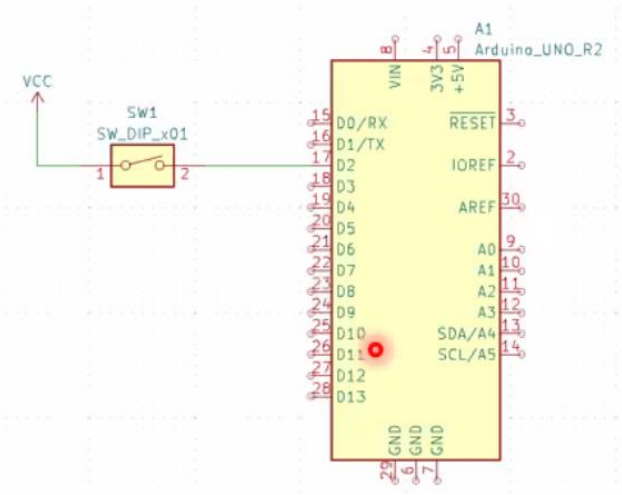


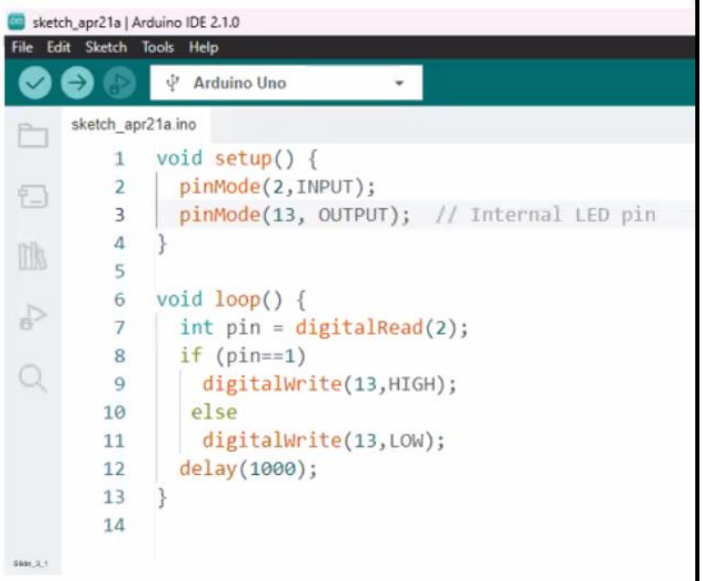
When the output is at Logic –Low state the load voltage is clamped at Vce of the output transistor. The external pull-up resister act as a current limiter



When the output is at Logic–High state current flows through the load. Output voltage is determined by potential division between the load and the external pull-up resister. Care must be taken to maintain output voltage at logic high level.

Reading one bit input





- *How would you expect the output to be?*
- *Does it behaves as expected?*