Sahana Prabhu
www.linkedin.com/in/p-sahana ● sahana.prabhu@mail.utoronto.ca

PROFESSIONAL SUMMARY

Computer Engineering student (graduating June 2026) with proven expertise in **digital verification** and **embedded systems development**. Delivered measurable impact at **Synopsys** through **UVM testbench development** and **verification automation**, while leading technical projects from concept to execution, including designing a new leadership program and developing production-ready **ML systems**. Combines strong technical skills in **SystemVerilog**, **Python**, and **hardware design** with demonstrated ability to drive **cross-functional initiatives**, influence **stakeholders**, and translate complex requirements into actionable solutions.

SKILLS

- **Programming**: Python, C/C++, MATLAB, SystemVerilog/Verilog, TCL, Perl
- **Electrical & Hardware**: Protocol Compliance (PCIe, UART, Bluetooth), Embedded Firmware (STM32, Arduino), UVM Testbench Development, RTL Debugging, FPGA Design, Sensor Integration, CMOS Layout, DRC/LVS, Parasitic Extraction, SRAM Design
- **Project Management**: Schedule & Cost Management, Stakeholder Coordination, Risk Mitigation, Cross-Functional Team Leadership, Technical Documentation (Confluence/Jira), Process Optimization
- **Tools**: Synopsys Verdi, Git/Perforce, ModelSim, Quartus Prime, Microsoft Office 365, Linux

EDUCATION

Faculty of Applied Science and Engineering, University of Toronto **Expected June 2026**
BASc Computer Engineering, Minor: Artificial Intelligence, Sustainable Energy

- **Honors & Awards:** Engineering International Scholarship Awardee | Dean's Honour List (4/6 semesters)
- **Leadership:** EDI Chair & Leadership Training Coordinator, Frosh Week | Choreographer, Skule Nite

EXPERIENCE

Emerging Leaders Program Co-Designer (https://tinyurl.com/ELSahana) | UofT Jul. 2025 - Present

- Identified gap in leadership development offerings and **built compelling business case** to secure funding for entirely new program, demonstrating strategic thinking and ability to influence stakeholders
- **Led cross-functional program design** by facilitating workshops with student leaders, administrators, and faculty to gather requirements and co-create curriculum aligned with organizational goals
- Defined success metrics and **evaluation framework to measure program impact** on leadership pipeline development and student engagement outcomes
- Secured ongoing work-study position to **facilitate program delivery**, demonstrating self-starter mentality and commitment to driving initiatives from concept through execution

CMOS Integrated Circuit Design & Layout | University of Toronto Sept. 2025 – Dec. 2025

- Designed full-custom **CMOS layouts (inverter, NAND)** from schematics using **Micromagic MAX**, implementing poly, diffusion, and metal layers in compliance with 0.25 µm design rules.
- Completed **full physical verification flows (DRC, LVS), achieving zero violations** and schematic-layout netlist consistency.
- Designed a **6T SRAM memory cell in Micromagic SUE**, optimizing transistor width ratios ($W\_PD/W\_PG \geq 2.7$) for **read stability and writeability** under area constraints.
- Performed **parasitic extraction and back-annotated HSPICE simulations** to analyze interconnect capacitance effects on delay and transient response.

Digital Verification Engineering Intern, Synopsys | Mississauga, Canada May 2024 - Aug. 2025

- Developed and maintained **constrained-random SystemVerilog UVM testbenches** for **PMA** and **PMD verification**, enhancing **regression** results by identifying critical corner cases previously missed.

- Integrated **SRM matching** to improve testing and validation of **CTLE**, increasing coverage of critical analog-digital interactions in **PCIe PHY IP**.
- Participated in **peer code reviews** and design discussions, providing **feedback on verification strategies** and implementation approaches.
- Authored comprehensive **test plans and decomposed functional requirements** into well-defined verification tasks tracked through Jira.
- Developed **TCL scripts** for **coverage exclusion files** and edited **Perl scripts** to streamline **regression flows** at block level, eliminating manual processes and improving verification automation efficiency.
- Collaborated with the design team to analyze **RTL implementation** for **corner cases**, ensuring compliance with **PCIe protocol specifications** and optimizing logic for performance and reliability.

Laidlaw Scholar (https://tinyurl.com/laidlawSP) & Reach Alliance Researcher | UofT Jun. 2022 - Sept. 2025

- Conducted comprehensive **literature review on blockchain-backed NFC technology** for humanitarian aid, **identifying key research gaps** and **translating technical capabilities into business value** for disaster-prone communities.
- **Designed and executed qualitative research methodology**, leading 20+ stakeholder interviews with community leaders, aid organizations, and technology providers in **disaster-prone communities (Vanuatu)**, gathering qualitative insights on challenges and opportunities for the aid distribution system
- **Developed data analysis framework using** Python and created visualizations, presenting research at Reach Conference '23 in Mexico to 50+ researchers, faculty mentors, and industry leaders **with actionable policy recommendations**

Sensor-Driven Smart Mirror for Dementia Care Support | University of Toronto Jan. 2024 - May 2024

- Developed **UART-based firmware on STM32** for **real-time sensor data transmission via Bluetooth** to **Raspberry Pi**, enabling seamless device communication for cognitive stimulation features including timed photo displays and medication reminders.
- Engineered dynamic **UI controls with sensor-triggered mode switching** and optimized power management through **PIR-based motion detection firmware**, reducing energy consumption by automatically disabling display during inactivity.
- Programmed **touch screen interaction using IR sensors** to toggle between display modes (photos, reminders, weather) and interfaced with phone data via **Bluetooth** to display synchronized medication reminders for dementia care support.

Bird Species Classification using Deep Learning | University of Toronto, Canada Jan. 2024 - May 2024

- Developed a scalable **ML deployment pipeline** using Python, YOLOv8, and TensorFlow, processing 11,788+ images and implementing transfer learning with ResNet-101, **achieving 8x improvement over baseline and demonstrating production ML engineering best practices**
- Architected a custom classifier with dropout regularization and average pooling layers, making solution architecture decisions to combat overfitting while achieving 82.41% test accuracy **for conservation applications**
- **Implemented automated model monitoring** with early stopping and learning rate scheduling, optimizing convergence and achieving 81.06% validation accuracy and 97% training accuracy **across 200 species classes**

Community Outreach Director & ECE Class Representative, EngSoc | UofT Sep. 2023 - May 2024

- Managed **multi-channel outreach campaign reaching 400+ ECE students**, planning and executing 15+ events that increased participation by 40%
- **Led advocacy projects** negotiating with university administration on exam schedules, accommodations, professor assignments, and budget allocation

- **Coordinated cross-functional initiatives** between student government, faculty administration, and external vendors while balancing competing priorities and meeting all deadlines
- **Built and maintained stakeholder relationships** through regular communication, follow-up, and consultative approach

Geometry Dash VGA Game Development | University of Toronto Mar. 2023 - May 2023

Project Link: https://github.com/hannahlila04/geometry-dash-vga-project

- Built multi-level **rhythm-based game in C** for **DE1-SOC FPGA's VGA display using ARM A9** Processor, featuring collision detection algorithms, dynamic scoring mechanics, and adjustable difficulty through speed incrementation.
- Configured **PS/2 keyboard and DE1-SOC button interface**s for player controls, establishing **polling** systems for spacebar-activated jumps and KEY-based difficulty selection.

Team Lead, Simple Processor (Digital System Design)| UofT, Canada Feb. 2023 - Mar. 2023

- Designed **16-bit processor architecture** using **Verilog** with integrated **ALU**, **FSM controller**, **memory interface**, and **LED output connectivity**, ensuring compatibility with **DE1-SoC** development boards.
- Developed **dynamic loading algorithm** for **compiler software**, enabling arbitrary memory address execution and creating a flexible **program execution framework** that enhanced processor modularity and performance.
- Extended **processor instruction set architecture (ISA)** by implementing four custom instructions (**ld, st, and, b{cond}**), enabling **external memory access**, **bitwise operations**, and **conditional branching** for enhanced computational capabilities.

Team Lead, Digital Demodulator | University of Toronto (UofT), Canada Dec. 2022 - May 2023

- Led cross-functional team of 3 engineers in developing **digital demodulator** for **software-defined transceiver** using **Verilog**, achieving 30% improvement in **signal extraction accuracy** through innovative **filtering algorithms**.
- Designed comprehensive **quality control framework** across 3 design stages, implementing systematic **testing procedures** that reduced **defects** by 20% and ensured reliable **hardware performance**.
- Implemented **Git version control workflow**, establishing **branching strategies** and **code review processes** that reduced collaboration errors by 40% and improved **project delivery efficiency**.

Researcher, High-Performance Computing Center Stuttgart | Stuttgart, Germany Jun. 2023 - Aug. 2023

- Engineered **C++ plugins** for **COVISE** and **OpenCover** visualization platforms, creating custom **algorithms** for **traffic trajectory data extraction** and **3D rendering**, enhancing **intersection analysis** capabilities.
- Built automated **data ingestion pipeline** in **C++**, converting diverse trajectory data formats into structured datasets and reducing **data processing time** by 30% through optimized **parsing algorithms**.
- Implemented computational methods in **C++** to analyze **pedestrian-vehicle interactions** at intersections, developing novel **analytical approaches** for safer **intersection design optimization**.

Project Management Intern, Soap Cycling Singapore | Singapore Apr. 2020 - Jul. 2020

- Analyzed collection data to develop **COVID-19 scenario projections** for recycling expansion, forecasting **savings of 1,400+ bottles and 72+ liters of soap** to inform strategic decisions
- **Assessed warehouse capacity constraints and optimized inventory systems**, providing data-driven recommendations to improve operational efficiency
- Created **comprehensive business proposal with partner criteria and cost-benefit analysis**, presenting recommendations that balanced technical feasibility with **strategic objectives to executive leadership**