EEE3027 Integrated Circuit Design

Semester 1 Report

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Contents

Abstract

This is a placeholder for the abstract of the report.

Introduction

1.1 Background and Key Concepts

1.1.1 Transistors

A transistor is a semiconductor device used to amplify or switch electronic signals and electrical power. It is composed of semiconductor material, usually with at least three terminals for connection to an external circuit. A voltage or current applied to one pair of the transistor's terminals controls the current through another pair of terminals.

Transistor Structure:

- **Source (S):** The terminal through which carriers enter the channel.
- **Drain (D):** The terminal through which carriers leave the channel.
- **Gate (G):** The terminal that modulates the conductivity of the channel.
- **Body (B):** The substrate on which the transistor is built, often connected to the source.
- **Channel:** The region between the source and drain where current flows when the transistor is on.
- **Oxide Layer:** An insulating layer between the gate and the channel, typically made of silicon dioxide (SiO2).

Figure 1: Basic structure of an NMOS and PMOS transistor.

1.1.2 MOSFET Types

- **N-channel (NMOS):** electrons are charge carriers.
- **P-channel (PMOS):** holes are charge carriers.

1.1.3 Operating Regions of a MOSFET

Region	Condition (N-channel)	Description
Cutoff	$V_{GS} < V_{th}$	OFF (no current)
Triode (Linear)	$V_{GS} > V_{th}$, $V_{DS} < V_{GS} - V_{th}$	Acts as variable resistor
Saturation (Active)	$V_{GS} > V_{th}$, $V_{DS} \geq V_{GS} - V_{th}$	Current source (amplifier region)

1.2 Importance of MOSFET Physical Parameters

The physical dimensions of a MOSFET determine its performance in terms of speed, power, and reliability.

1.2.1 Key Parameters and Effects

Parameter	Symbol	Importance
Gate Length	L	Controls speed/gain; shorter L, more speed but causes leakage.
Gate Width	W	Controls current; wider W, more current and capacitance.
Oxide Thickness	t_{ox}	Thinner ox - improves gate control but increases tunneling.
Channel Depth	–	Affects channel formation and conductivity.
Threshold Voltage	V_{th}	Determines switching voltage.
Junction Depth	–	Impacts short-channel effects and capacitance.

1.2.2 Significance

- **Speed:** shorter channel $\Rightarrow$ faster switching.
- **Power Efficiency:** optimized V_{th} and t_{ox} reduce power loss.
- **Current Drive:** larger W gives more drive capability.
- **Reliability:** careful balance of parameters prevents breakdown and leakage.

1.3 Gain

1.3.1 Definition

Gain is the ratio of output signal to input signal, as shown by *Equations 1 and 2*:

$$\text{Gain} = \frac{\text{Output}}{\text{Input}} \tag{1}$$

Types include:

$$A_v = \frac{V_{out}}{V_{in}}, \quad A_i = \frac{I_{out}}{I_{in}}, \quad A_p = \frac{P_{out}}{P_{in}} \tag{2}$$

1.3.2 Gain in BJTs and MOSFETs

Equations 3 and 4 show gain definitions for BJTs and MOSFETs:

$$\text{BJT current gain}\beta = \frac{I_C}{I_B} \tag{3}$$

$$\text{MOSFET transconductance}g_m = \frac{\partial I_D}{\partial V_{GS}} = \beta(V_{GS} - V_{th}) \tag{4}$$

1.3.3 Gain in Decibels

Gain in decibels (dB) is given by *Equation 5*

$$\text{Voltage Gain (dB)} = 20\log_{10}\left(\frac{V_{out}}{V_{in}}\right) \tag{5}$$

:

1.3.4 Importance

- Determines amplification strength.
- Critical in analogue amplifiers, control systems, and logic gates.

1.4 Gate Length vs. Channel Length

- **Gate Length (L_G):** physical distance between source and drain under the gate.
- **Channel Length (L_{CH}):** effective electrical distance current travels.

They are related by *Equation 6*:

$$L_{CH} = L_G - \Delta L \tag{6}$$

where ΔL is due to lateral diffusion of dopants.

1.4.1 Difference and Importance

Shorter effective channel length causes:

- Increased leakage and short-channel effects.
- Lower threshold voltage.
- Reduced control by the gate.

1.5 Beta (β) Equations for MOSFETs

Shown by *Equations 7 and 8*:

1.5.1 Definition

$$I_D = \frac{1}{2}\beta(V_{GS} - V_{th})^2 \quad \text{(saturation region)} \tag{7}$$

$$I_D = \beta\left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right] \quad \text{(linear region)} \tag{8}$$

1.5.2 Beta Expression

Beta can also be expressed by *Equation 9*:

$$\boxed{\beta = \mu_n C_{ox} \frac{W}{L}} \tag{9}$$

where:

- μ_n = carrier mobility
- $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$ = oxide capacitance per unit area
- W = gate width
- L = gate length

1.5.3 Related Terms

$$k' = \mu_n C_{ox}, \quad \beta = k' \frac{W}{L}$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \beta(V_{GS} - V_{th})$$

1.5.4 Importance

- Determines how strongly a MOSFET amplifies a signal.
- Affects gain, speed, and current drive.
- Critical for matching and biasing in analogue ICs.

Formative Assessment 1 Report

A MOS transistor operates in two main regions depending on the drain-source voltage (V_{DS}) and the gate-source voltage (V_{GS}). In *Figure 2*, we can see the NMOS Sweep for a few specified V_{GS} values. The explanation of the code will be explained below

2.1 NMOS I-V Characteristics (First Task - Lab 1 Part 1)

Linear Region

This occurs when:

$$V_{DS} < V_{GS} - V_T \tag{10}$$

In this region, the transistor behaves like a voltage-controlled resistor. The drain current is given by *Equation 11*:

$$I_D = \beta \left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2 \right] \tag{11}$$

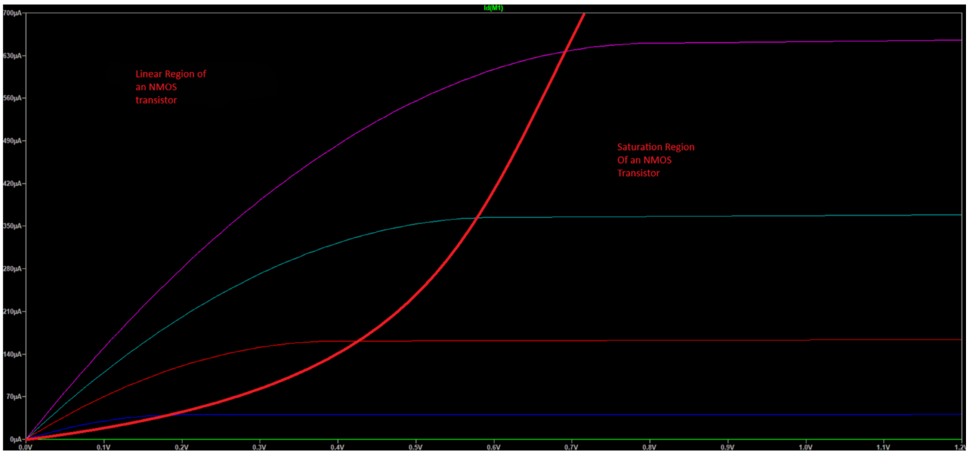

Figure 2: NMOS I-V Characteristics showing Linear and Saturation regions for different V_{GS} values.

where, if we refer to *Equation 10* again:

$$\beta = \frac{W}{L}\mu_n C_{ox} = \frac{W}{L}K_P$$

Initially, the current I_D increases approximately linearly with V_{DS}.

Saturation Region

This occurs when:

$$V_{DS} \geq V_{GS} - V_T \tag{12}$$

In this region, the channel is *pinched off* near the drain, and the drain current becomes almost independent of V_{DS}:

$$I_D = \frac{\beta}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \tag{13}$$

The slight upward slope in the I_D–V_{DS} characteristics is due to **channel-length modulation**, represented by the parameter λ (typically $\lambda = 0.02$). Parameters have been defined below and in the Background section. *Listing 1* shows the code used to generate the graph (next page).

```
* Task 1 Extended: Sweep VDS and VGS (multiple curves)
* nmos_DC_sweep.cir is a netlist.

* Sets the VGS value to 1.2V (can be changed to sweep different values)
.param VGSVAL=1.2

* Tells us the voltages that we will use and the connections (so V_GS is a DC source and it has a gate connection (0V DC), same with the Drain)
VGS G 0 DC {VGSVAL}
VDS D 0 DC 0
* Tells us the transistor dimensions (gate width (W), channel length (L)) along with source and body voltage.
M1 D G 0 0 NLEVEL1 W=10u L=1u

.model NLEVEL1 NMOS LEVEL=1 VTO=0.4 KP=200u LAMBDA=0.02
* VTO is V_th, KP = transconductance parameter, LAMBDA is the channel-length modulation factor.

.dc VDS 0 1.2 0.01 VGS 0.4 1.2 0.2
* plots the drain current (I(M1)s) against VDS for different VGS values from 0.4V to 1.2V in steps of 0.2V
.plot DC I(M1)s
.end

* Comments start with asterisk
* First line is title (can be anything)
* Last line must be .END (or .end as SPICE is case insensitive)
* Node names: numbers or alphanumeric
* Node 0 is always ground
* Component values: scientific notation (1e-12) or units (1p, 1n, 1u, 1m, 1k, 1meg)
```

Listing 1: NMOS Sweep Simulation Code

Parameter Definitions

- I_D : Drain current
- V_{GS} : Gate-to-source voltage
- V_T : Threshold voltage
- V_{DS} : Drain-to-source voltage
- μ_n : Electron mobility
- C_{ox} : Oxide capacitance per unit area
- W : Channel width
- L : Channel length
- $\beta = \frac{W}{L}\mu_n C_{ox}$: Process transconductance parameter
- λ : Channel-length modulation parameter (typically $\lambda = 0.02$)

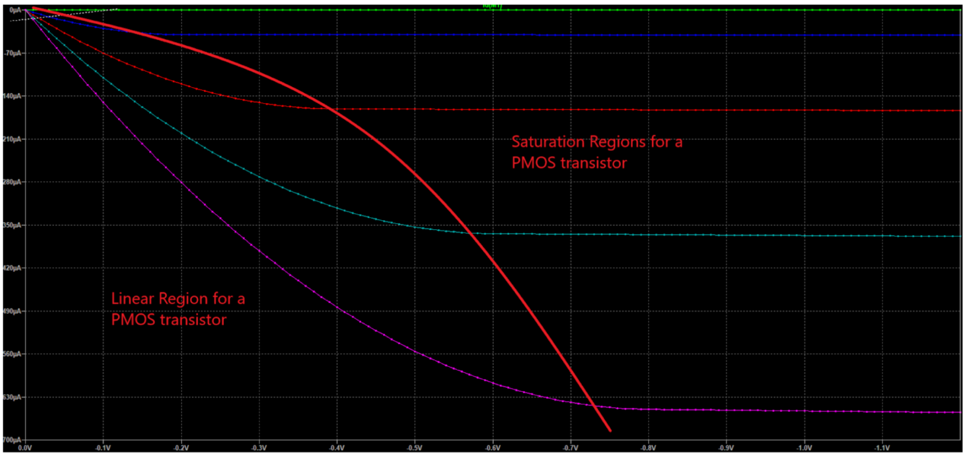

Figure 3: PMOS I-V Characteristics showing Linear and Saturation regions for different V_{SG} values.

2.2 PMOS I-V Characteristics (Second Task - Lab 1 Part 1)

We can see the PMOS Sweep for a few specified V_{SG} values in *Figure 3*. The explanation of the code will be shown below:

For a PMOS transistor, all voltages are **negative** relative to the NMOS device. The key differences are:

- V_{SG} (source-to-gate voltage) replaces V_{GS}
- V_{SD} (source-to-drain voltage) replaces V_{DS}
- The drain current I_D flows from the **source to the drain**, opposite to that of the NMOS

Linear Region

This occurs when:

$$V_{SD} < V_{SG} - |V_T|$$

The transistor behaves like a voltage-controlled resistor. The drain current is given by:

$$I_D = \beta \left[(V_{SG} - |V_T|)V_{SD} - \frac{1}{2}V_{SD}^2 \right]$$

where:

$$\beta = \frac{W}{L}\mu_p C_{ox} = \frac{W}{L}K_P$$

Initially, I_D increases approximately linearly with V_{SD}.

Saturation Region

This occurs when:

$$V_{SD} \geq V_{SG} - |V_T|$$

In this region, the channel is *pinched off* near the drain, and the current becomes almost independent of V_{SD}:

$$I_D = \frac{\beta}{2}(V_{SG} - |V_T|)^2(1 + \lambda V_{SD})$$

The small increase in I_D with V_{SD} is due to **channel-length modulation**, represented by λ.

Calculation with Example Values from PMOS Sweep

For a PMOS transistor with:

$$V_{SG} = 1.2 \text{ V}, \quad |V_T| = 0.4 \text{ V}$$

the boundary between the linear and saturation regions occurs at:

$$V_{SD} = V_{SG} - |V_T| = 1.2 - 0.4 = 0.8 \text{ V}$$

On an I_D–V_{DS} plot, this corresponds to:

$$V_{DS} = -0.8 \text{ V}$$

indicating the same boundary but with reversed voltage polarity compared to NMOS operation.

For $V_{GS} = -1.2\,\text{V}$:

$$\begin{gathered}
\text{Saturation occurs when } V_{DS} \leq -0.8\,\text{V} \\
\text{Linear region: } -0.8\,\text{V} < V_{DS} < 0\,\text{V} \\
\text{Saturation region: } V_{DS} \leq -0.8\,\text{V}
\end{gathered}$$

$$\begin{gathered}
\text{Linear Region } (V_{SD} < V_{SG} - |V_T|): \\
I_D = -\beta\left[(V_{SG} - |V_T|)V_{SD} - \tfrac{1}{2}V_{SD}^2\right]
\end{gathered}$$

$$\text{Note: Current is negative (flows from source to drain)}$$

$$\begin{gathered}
\text{Example calculation for } V_{SG} = 1.2\,\text{V},\ V_{SD} = 0.4\,\text{V}: \\
\beta = \frac{W}{L} \cdot K_P = \frac{10}{1} \cdot 200\,\mu = 2\,\text{mA/V}^2 \\
I_D = -2\,\text{mA/V}^2 \times \left[(1.2 - 0.4) \times 0.4 - 0.5 \times 0.4^2\right] \\
I_D = -2\,\text{mA/V}^2 \times [0.32 - 0.08] \\
I_D = -2\,\text{mA/V}^2 \times 0.24 \\
I_D = -0.48\,\text{mA} = -480\,\mu\text{A}
\end{gathered}$$

$$\text{Saturation Region } (V_{SD} \geq V_{SG} - |V_T|):$$
$$I_D = -\frac{\beta}{2}(V_{SG} - |V_T|)^2(1 + \lambda V_{SD})$$

$$\text{Example for } V_{SG} = 1.2\,\text{V},\ V_{SD} = 1.2\,\text{V}:$$
$$I_D = -\left(\frac{2\,\text{mA/V}^2}{2}\right)(0.8)^2(1.024)$$
$$I_D = -1\,\text{mA/V}^2 \times 0.64 \times 1.024$$
$$I_D = -0.655\,\text{mA} = -655\,\mu\text{A}$$

Current is negative (opposite polarity to NMOS) and the curves mirror NMOS behavior, with saturation boundaries at $V_{DS} = -(V_{SG} - |V_T|)$. This is shown in *Figure 3*.

```
* TASK 2: PMOS I-V DC Sweep with Multiple VSG Curves

* Define gate-source voltage as parameter (negative for PMOS)
.param VGSVAL=-1.2

* Gate voltage source: negative voltage for PMOS operation
* Connected between gate (G) and ground (0)
VGS G 0 DC {VGSVAL}

* Drain voltage source: starts at 0V, swept negative
VDS D 0 DC 0

* PMOS transistor M1:
* Connections: Drain=D, Gate=G, Source=0(GND), Bulk=0(GND)
* In normal PMOS, bulk connects to highest potential (VDD)
* Here, 0V used  as reference for ease of simulation, refer to source
  in report.
* Geometry: Width=10um (same as NMOS), Length=1um
M1 D G 0 0 PLEVEL1 W=10u L=1u

* Level 1 PMOS model parameters:
* VTO    = -0.4V   : Threshold voltage (negative for PMOS)
* KP     = 200uA/V^2: Transconductance (typically half of NMOS in
  reality)
* LAMBDA= 0.02V^-1: Channel-length modulation (same as NMOS)
.model PLEVEL1 PMOS LEVEL=1 VTO=-0.4 KP=200u LAMBDA=0.02

* DC Sweep Analysis:
* Primary sweep: VDS from 0V to -1.2V in -0.01V steps (negative
  direction)
* Secondary sweep: VGS from -0.4V to -1.2V in -0.2V steps
* This generates 5 curves (VGS = -0.4, -0.6, -0.8, -1.0, -1.2V)
.dc VDS 0 -1.2 -0.01 VGS -0.4 -1.2 -0.2

* Plot drain current (will be negative for PMOS)
.plot DC I(M1)

* End of netlist
.end
```

Listing 2: PMOS Sweep Simulation Code

2.3 Beta Sweep

2.3.1 Question 1: Identification

- VGS = 1.2V (from .param VGSVAL=1.2)
- VDS = 1.2V (from .param VDSVAL=1.2)
- L = 1um (from M1 line: L=1u)

2.3.2 Question 2A Model Parameter Definitions

VTO (Threshold Voltage): Symbol: V_T or V_{th}. Units: Volts (V).

Zero-bias threshold voltage - the minimum gate-source voltage required to form a conducting inversion channel. Below this voltage, the transistor is in cutoff. Determined by gate material work function, oxide thickness, substrate doping, and interface charges. In our simulation: VTO = 0.4V (NMOS), -0.4V (PMOS).

KP (Transconductance Parameter): Symbol: k' or μC_{ox}. Units: A/V^2.

Intrinsic transconductance parameter representing the product of carrier mobility (μ) and gate oxide capacitance per unit area (C_{ox}):

$$KP = \mu \cdot C_{ox} = \mu \cdot \frac{\varepsilon_{ox}}{t_{ox}} \tag{14}$$

Determines current drive capability. The gain factor is $\beta = (W/L) \cdot KP$, so $I_D \propto KP$. NMOS typically has 2-3× higher KP than PMOS due to higher electron mobility. In our simulation: KP = 200μA/V^2 for both types.

LAMBDA (Channel-Length Modulation): Symbol: λ. Units: V^{-1}. Default: 0.0.

Channel-length modulation coefficient accounting for effective channel shortening as V_{DS} increases in saturation. Without LAMBDA, saturation curves would be perfectly flat (infinite output resistance). With LAMBDA:

$$I_D(sat) = \frac{\beta}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \tag{15}$$

Output resistance: $r_o = 1/(\lambda I_D)$. Inversely proportional to channel length: $\lambda \propto 1/L$. Analogous to inverse Early voltage in BJTs. In our simulation: $\lambda = 0.02$ V^{-1}, causing ∼2.4% current increase across 1.2V V_{DS} range.

2.3.3 Question 2B Model Assumptions

The standard textbook equation for saturation current is:

$$I_D = \frac{\beta}{2}(V_{GS} - V_T)^2 \quad \text{where } \beta = \frac{W}{L} \cdot \mu_n C_{ox} \tag{16}$$

The complete SPICE Level 1 equation is:

$$I_D = \frac{KP}{2} \cdot \frac{W_{eff}}{L_{eff}} \cdot (V_{GS} - VTO)^2 \cdot (1 + LAMBDA \cdot V_{DS}) \tag{17}$$

To simplify the SPICE model to match textbook equations, the following assumptions are made:

1. LAMBDA = 0 (or very small): The term $(1 + \lambda V_{DS})$ is set to 1, neglecting channel-length modulation. This assumes perfectly flat I-V curves in saturation with infinite output resistance. In our simulation, $\lambda = 0.02$ causes only a ∼2.4% variation, which is small but non-zero.

2. No body effect ($\gamma = 0$ or $V_{SB} = 0$): The body effect modifies threshold voltage as:

$$V_T = V_{T0} + \gamma(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}) \tag{18}$$

When bulk and source are both at ground ($V_{SB} = 0$), this term vanishes and $V_T = V_{T0}$, which is our case.

3. Long-channel approximation: Velocity saturation is neglected, assuming drift velocity remains proportional to electric field. Valid for $L \geq 1\mu$m. Short-channel effects (DIBL, threshold roll-off) are ignored.

4. No mobility degradation: Carrier mobility μ is assumed constant, independent of V_{GS}. In reality, high vertical electric fields reduce mobility, but Level 1 ignores this.

5. Ideal effective dimensions: $W_{eff} = W$ and $L_{eff} = L$ (no parasitic effects). When $LD = WD = XL = XW = DEL = 0$, drawn and effective dimensions are equal.

6. Subthreshold conduction ignored: For $V_{GS} < V_T$, Level 1 assumes $I_D = 0$. In reality, exponential subthreshold current exists: $I_D \propto \exp(V_{GS}/nV_t)$.

Verification of equivalence: If $KP = \mu_n C_{ox}$, then:

$$\beta_{textbook} = \frac{W}{L} \cdot \mu_n C_{ox} = \frac{W}{L} \cdot KP = \beta_{SPICE} \tag{19}$$

With $LAMBDA = 0$, $V_{SB} = 0$, and ideal geometry, the equations become identical.

2.3.4 Simulation Verification

VTO verification: DC sweep shows $I_D \approx 0$ at $V_{GS} = 0.4$V, confirming threshold. Current increases dramatically for $V_{GS} > 0.4$V.

KP verification: From beta_w_sweep.cir:

$$\frac{dI_D}{dW} = 65.54\,\mu\text{A}/\mu\text{m (measured)} = \frac{KP}{2L}(V_{GS} - VTO)^2(1+\lambda V_{DS}) = 65.54\,\mu\text{A}/\mu\text{m (theory)} \tag{20}$$

Perfect agreement validates KP = 200 μA/V^2.

LAMBDA verification: In saturation at $V_{GS} = 1.2$V:

- $V_{DS} = 0.8$V: $I_D = 642\ \mu$A, $(1 + 0.02 \times 0.8) = 1.016 \rightarrow +1.6\%$
- $V_{DS} = 1.2$V: $I_D = 656\ \mu$A, $(1 + 0.02 \times 1.2) = 1.024 \rightarrow +2.4\%$

Measured current increase: $(656 - 642)/642 = 2.2\% \approx 2.4\%$ predicted. Slight upward slope in saturation curves confirms $\lambda = 0.02\text{V}^{-1}$.

Body effect assumption: $V_{SB} = 0$ throughout (source and bulk both grounded), so $V_T = VTO = 0.4$V constant. Confirmed by consistent threshold across all simulations.

Subthreshold assumption: Setting $V_{GS} = 0.3\text{V} < V_T$ yields $I_D \approx 0$ as Level 1 predicts, though real devices show exponential subthreshold current ($\sim$pA range).

Report Checklist

- Lab 1 Part 1
- N-Type characteristics
- P-Type characteristics

- MOSFET operation
- Parts that constitute a MOSFET and what altering them does to the operation of the MOSFET.
- Explanation of the PMOS and NMOS operation regions.
- What measurements were taken and how they were taken.
- Explanation of the graphs plotted and what they signify.
- Include code snippets of the simulation code used.
- Include graphs plotted.
- Analysis of the results.
    1. DC Analysis of NMOS and PMOS and explanation of what DC analysis is.
    2. Task 1: NMOS DC I-V sweep with annotations.
    3. Task 2: PMOS DC I-V sweep with annotations.
    4. Gain factor calculation and explanation.
    5. Beta explanation with Python example.
    6. Task 4 Iterative solution
- Lab 1 Part 2
- Explain what static analysis is.
- Draw an annotated schematic of the inverter circuit.
- Explain the operation of the inverter circuit.
- 1B, Annotate the file (All 7 lines)
- TASK 1C: DC Modes You have simulated the DC transfer characteristic of a CMOS inverter by sweeping the input voltage Vin from 0 V to 5 V. Plot the output voltage Vout against Vin. On your plot of Vout vs. Vin, clearly mark and label the following five operating points: A: Vin=0, B: Vin=1, C: Vin=2.5, D: Vin=4, E: Vin=5, For each point (A–E), identify the operating region of both the NMOS and PMOS transistors: Cutoff Triode (Linear) or Saturation, showing it as a table, and approximate Vout at each point.
- TASK 1D, NMOS pull up example, show the sweep as well, then answer these 5 questions:
- Q1. (1 mark) What is the highest output voltage reached in the NMOS pull-up version? Why does it not reach 5 V?
- Q2. (1 mark) Explain what happens to the NMOS pull-up transistor when Vin=0. Is it conducting?
- Q3. (1 mark) Describe what would happen if this NMOS-only inverter drove another CMOS logic gate. What are the risks?

- Q4. (1 mark) Why does a PMOS transistor avoid this issue? How does it behave differently from NMOS in pull-up?
- Q5. (2 marks) On your NMOS-only inverter plot, annotate the output voltage limit and mark the region where a 1 cannot be produced.
- TASK 2: TASK 2: CMOS Inverter Design for Delay Specification Use LTspice and theoretical models to design an inverter that meets timing specifications. Analyze performance using simulation and transistor-level delay theory (including propagation delay, rise/fall time, capacitive loading).
- TASK 2 Question 1 Transient Simulation and Analysis.
- TASK 2 Question 2 RC Delay Model.
- TASK 2 Question 3 Design and New Alternatives for performance.
- TASK 2 Question 4 Selection of questions to be answered.