EEE3027 Integrated Circuit Design

Semester 1 Report

Sahas Talasila *230057896*

Contents

Abstract

This is a placeholder for the abstract of the report.

Introduction

1.1 Background

This is a placeholder for the background information.

- Lab 1 Part 1
- N-Type characteristics
- P-Type characteristics
- MOSFET operation
- Parts that constitute a MOSFET and what altering them does to the operation of the MOSFET.
- Explanation of the PMOS and NMOS operation regions.
- What measurements were taken and how they were taken.
- Explanation of the graphs plotted and what they signify.
- Include code snippets of the simulation code used.
- Include graphs plotted.
- Analysis of the results.
    1. DC Analysis of NMOS and PMOS and explanation of what DC analysis is.
    2. Task 1: NMOS DC I-V sweep with annotations.
    3. Task 2: PMOS DC I-V sweep with annotations.
    4. Gain factor calculation and explanation.
    5. Beta explanation with Python example.
    6. Task 4 Iterative solution
- Lab 1 Part 2
- Explain what static analysis is.
- Draw an annotated schematic of the inverter circuit.
- Explain the operation of the inverter circuit.
- 1B, Annotate the file (All 7 lines)
- TASK 1C: DC Modes You have simulated the DC transfer characteristic of a CMOS inverter by sweeping the input voltage Vin from 0 V to 5 V. Plot the output voltage Vout against Vin. On your plot of Vout vs. Vin, clearly mark and label the following five operating points: A: Vin=0, B: Vin=1, C: Vin=2.5, D: Vin=4, E: Vin=5, For each point (A–E), identify the operating region of both the NMOS and

PMOS transistors: Cutoff Triode (Linear) or Saturation, showing it as a table, and approximate Vout at each point.

- TASK 1D, NMOS pull up example, show the sweep as well, then answer these 5 questions:
- Q1. (1 mark) What is the highest output voltage reached in the NMOS pull-up version? Why does it not reach 5 V?
- Q2. (1 mark) Explain what happens to the NMOS pull-up transistor when Vin=0. Is it conducting?
- Q3. (1 mark) Describe what would happen if this NMOS-only inverter drove another CMOS logic gate. What are the risks?
- Q4. (1 mark) Why does a PMOS transistor avoid this issue? How does it behave differently from NMOS in pull-up?
- Q5. (2 marks) On your NMOS-only inverter plot, annotate the output voltage limit and mark the region where a 1 cannot be produced.
- TASK 2: TASK 2: CMOS Inverter Design for Delay Specification Use LTspice and theoretical models to design an inverter that meets timing specifications. Analyze performance using simulation and transistor-level delay theory (including propagation delay, rise/fall time, capacitive loading).
- TASK 2 Question 1 Transient Simulation and Analysis.
- TASK 2 Question 2 RC Delay Model.
- TASK 2 Question 3 Design and New Alternatives for performance.
- TASK 2 Question 4 Selection of questions to be answered.