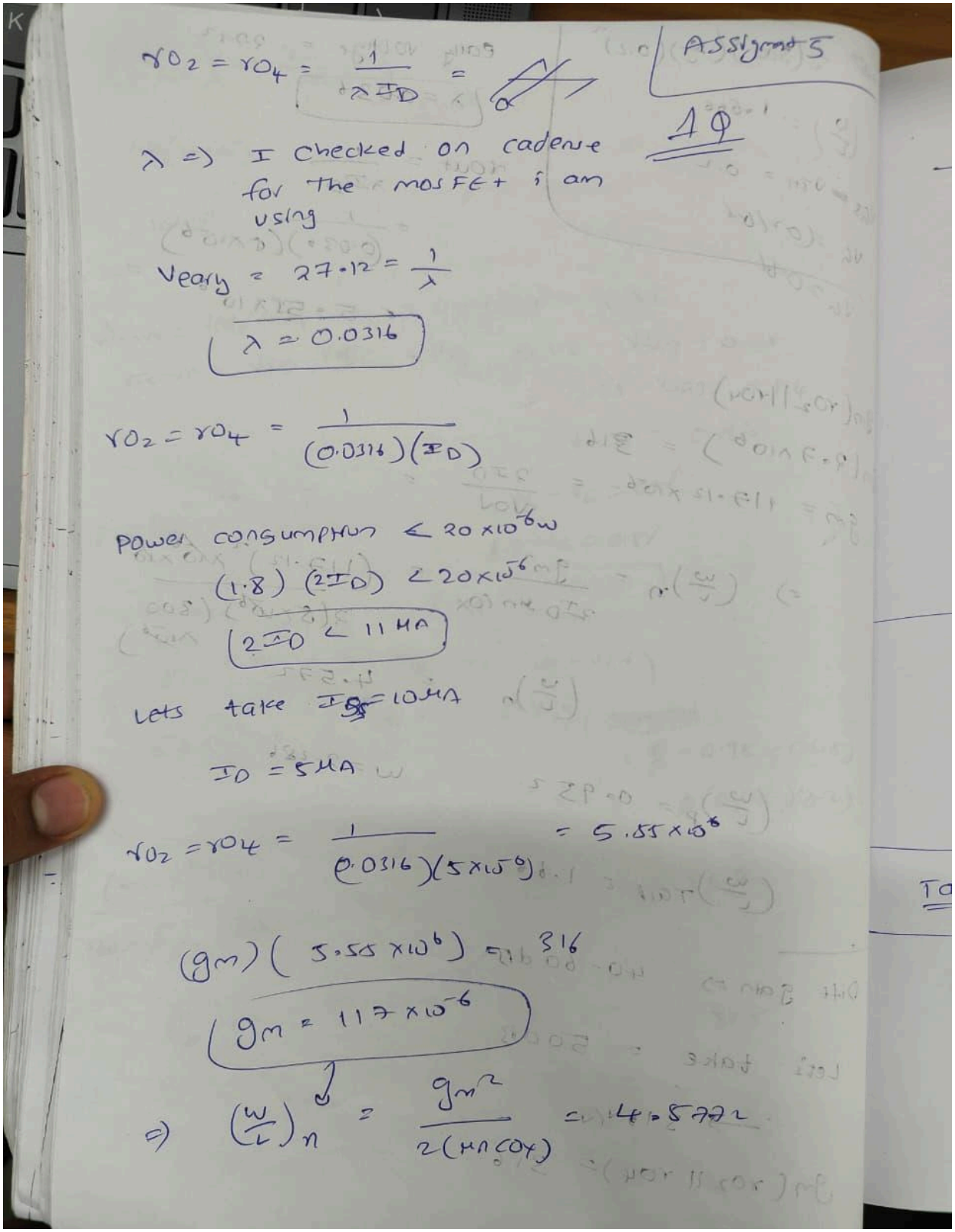
Analog CMOS IC Design (EE651)

23110064

CALCULATIONS (analytical)



ICMR = 0.8 − 1.4

$V_{ICMR1} = V_{OV5} + V_{OV1} + V_{T1} = 0.4 + 0.45$
$= 0.85$ ✓

$V_{ICmax} = V_{DD} - V_{SG} + V_{T1}$

$= 1.8 - V_{SG3} + 0.45 = 1.4$

$V_{SG} = 0.85 \Rightarrow 1.8 - V_G = 0.85$

$V_{G3} = 0.95$

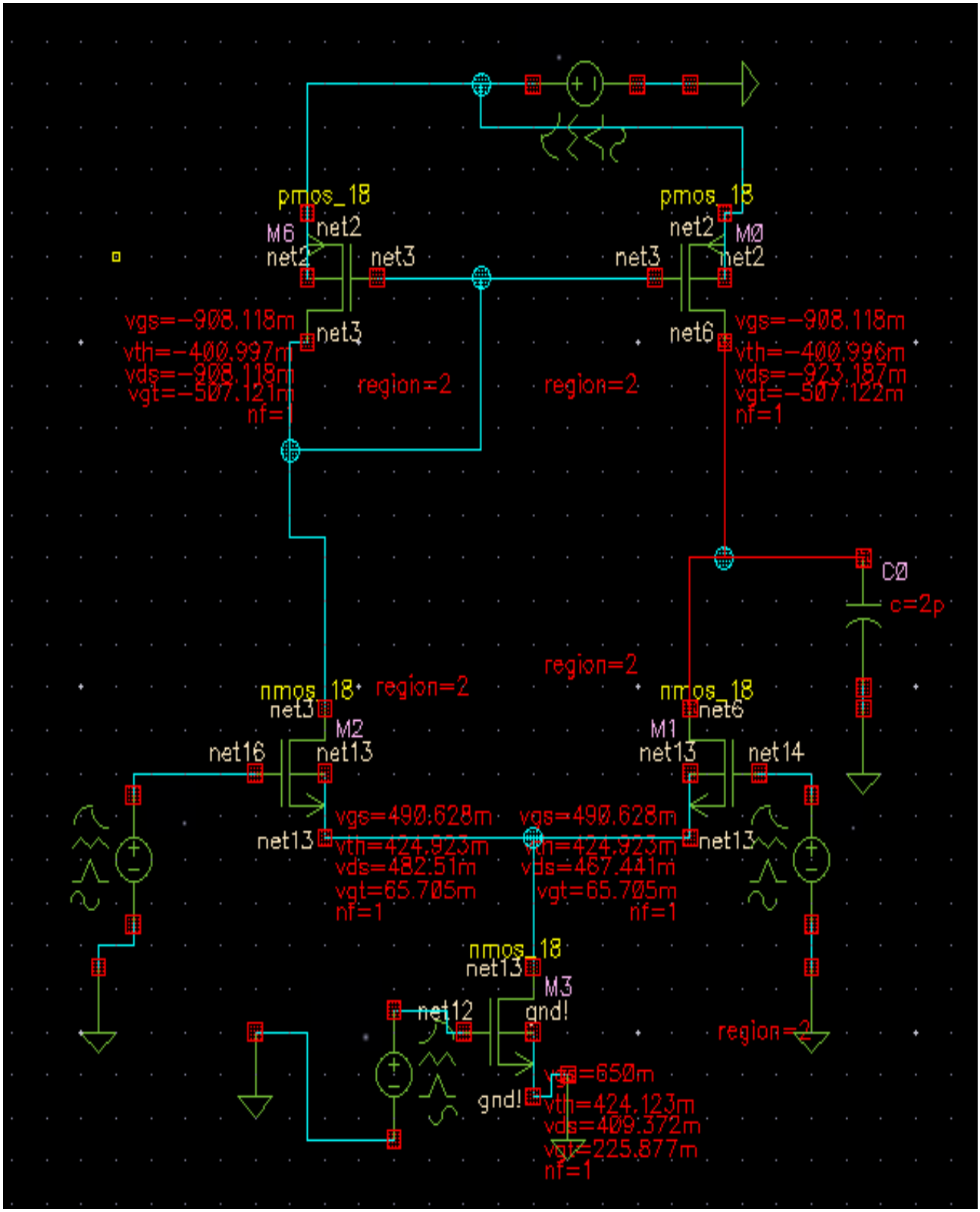
FOV PMOS

$5 \times 10^{-6} = \frac{1}{2}(65 \times 10^{-6})\left(\frac{W}{L}\right)\frac{(1.8 - 0.95 - 0.4)}{(1 + (0.036)(0.2))}$

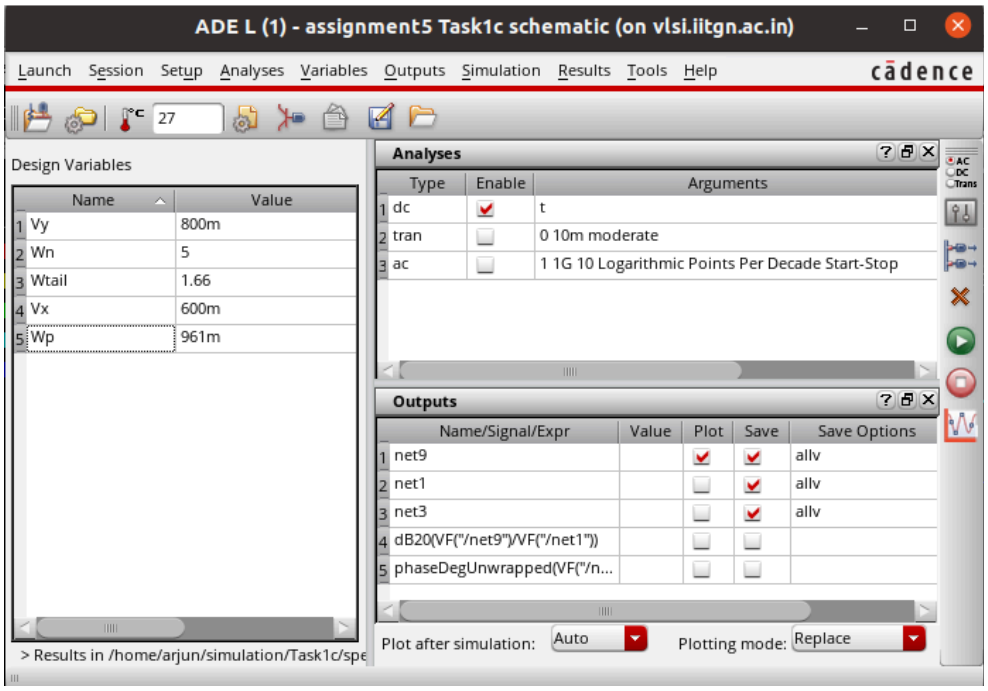
$\left(\frac{W}{L}\right)_P = 0.952$

Tail $\Rightarrow$ $\left(\frac{W}{L}\right) = 1.6663$

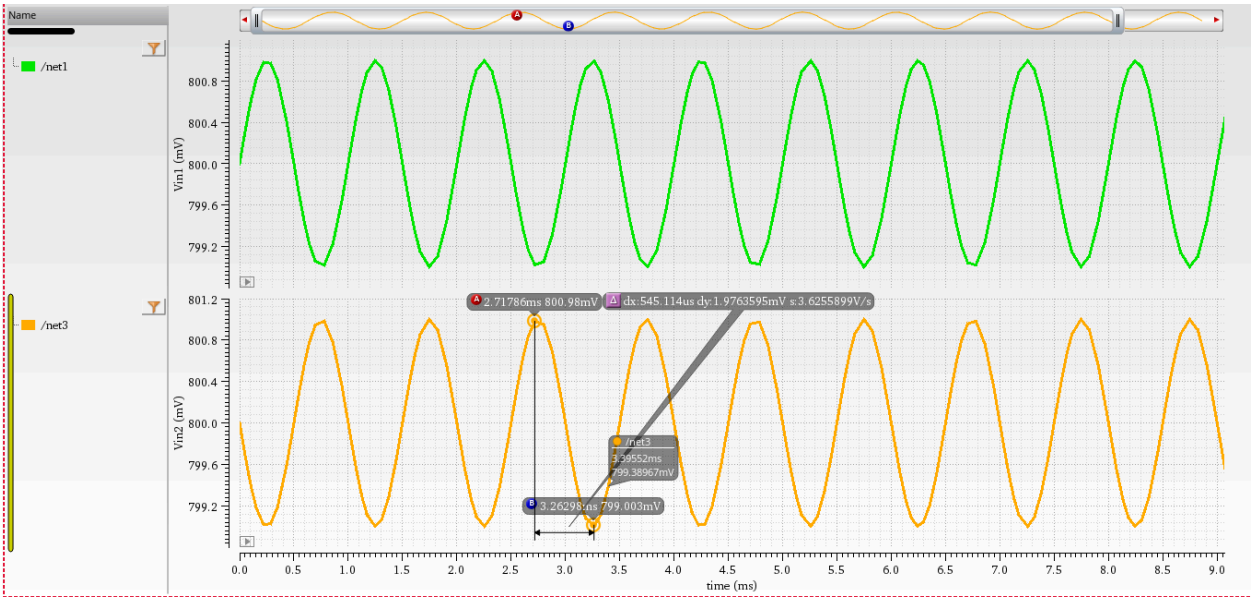
Schematic


pmos_18
M6
net2
net3
vgs=-908.118m
vth=-400.997m
vds=-908.118m
vgt=-507.121m
nf=1
region=2
pmos_18
M0
net2
net3
net6
vgs=-908.118m
vth=-400.996m
vds=-923.187m
vgt=-507.122m
nf=1
region=2
C0
c=2p
nmos_18
M2
net3
net16
net13
region=2
nmos_18
M1
net6
net13
net14
region=2
vgs=490.628m
vth=424.923m
vds=482.51m
vgt=65.705m
nf=1
vgs=490.628m
vth=424.923m
vds=467.441m
vgt=65.705m
nf=1
nmos_18
M3
net13
net12
gnd!
gnd!
vgs=650m
vth=424.123m
vds=409.372m
vgt=225.877m
nf=1
region=2

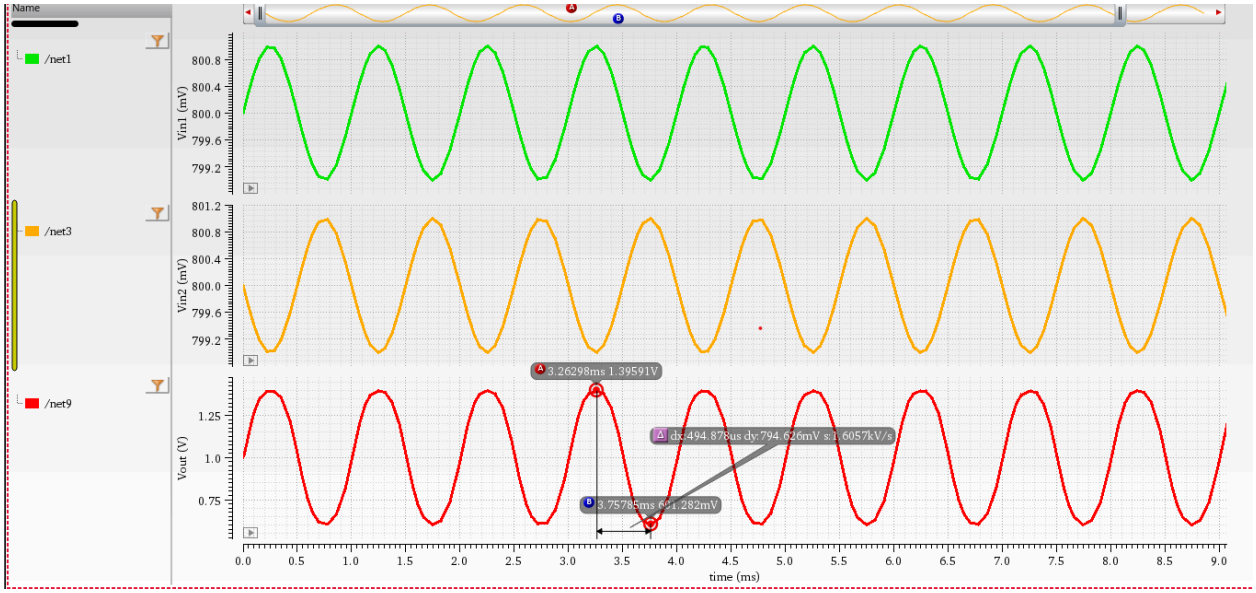
ADE L

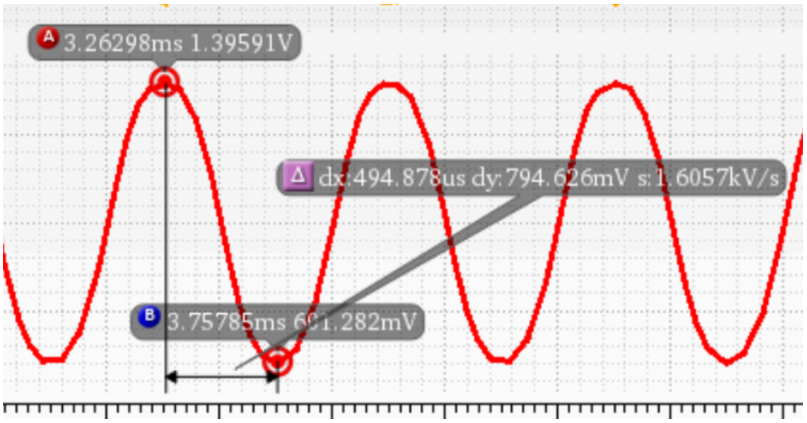


Below graphs are voltage input *V+* and *V-*



1.Plot of output voltage

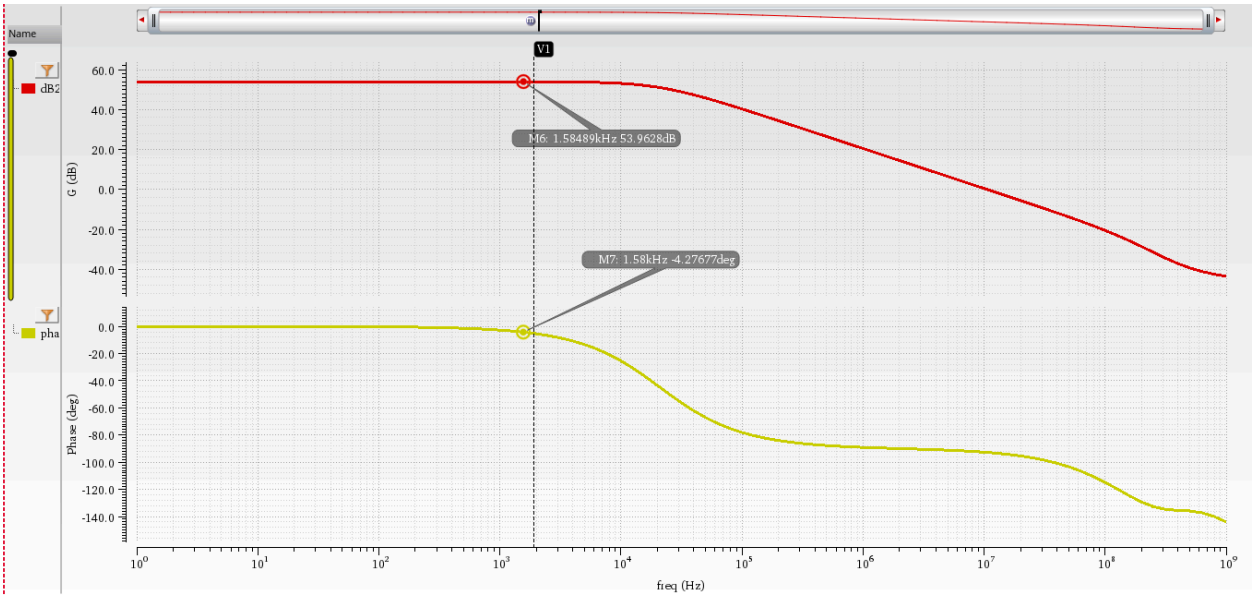




Swing is 794.626mV

Gain at 1kHz = $20\log(\frac{794.626}{2}) = 51.97\text{dB} > 40\text{ dB}$

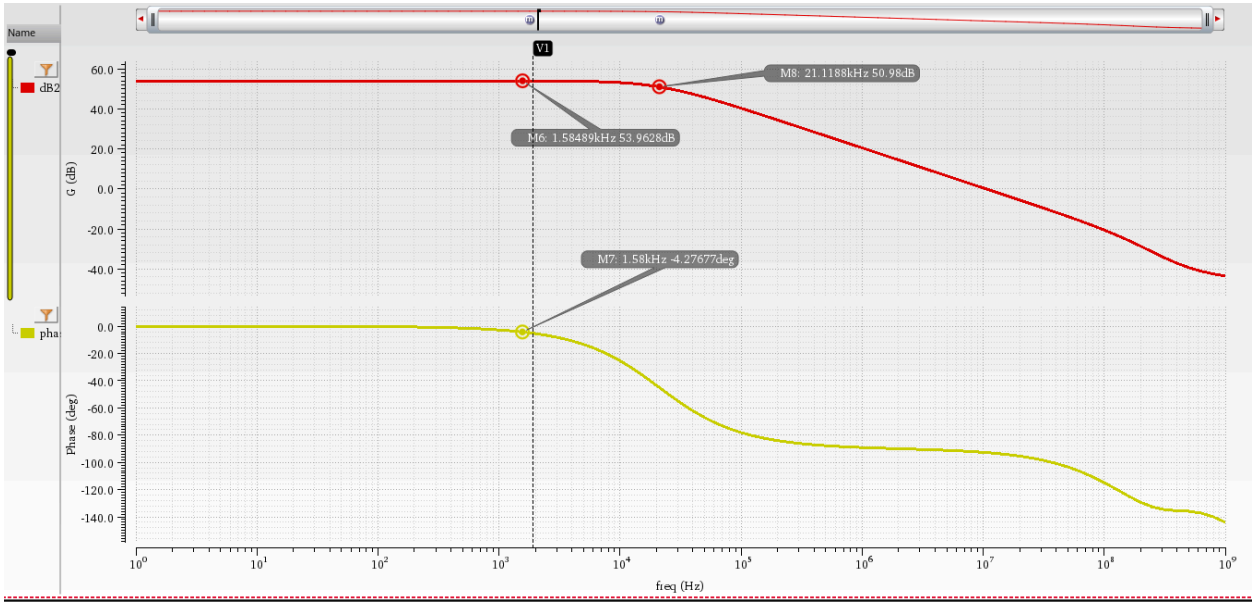
Bode plot

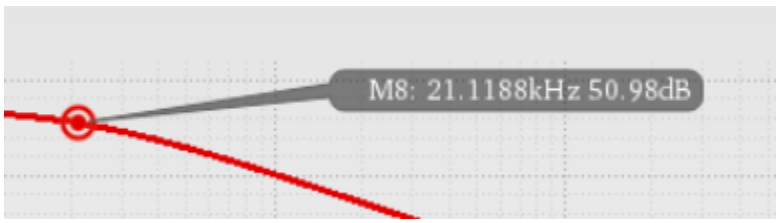


NOW WE ARE CALCULATION BANDWIDTH FOR THIS BLOT

Peak = 53.98dB

Peak – 3dB = 50.98dB





Bandwidth = 21.116kHz

Design an Operational **Transconductance Amplifier (OTA)** for the following specifications.

- Differential Gain = 40 - 60 dB (Gain should vary between 40 to 60 dB by changing Vcont)

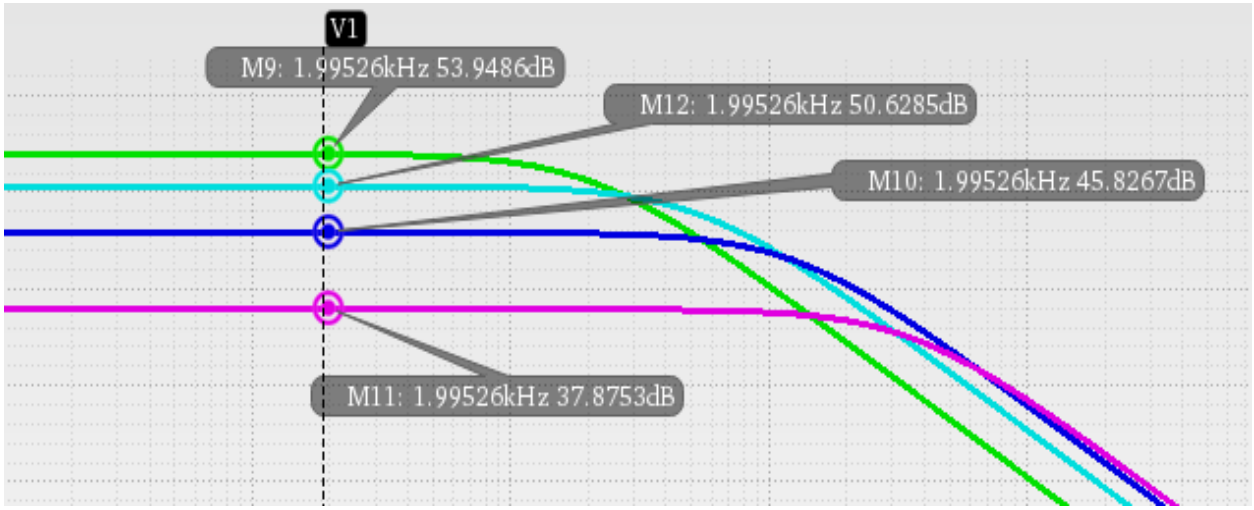
Now we are going to change Vcont and observe the gain (whether it is in 40-60dB)

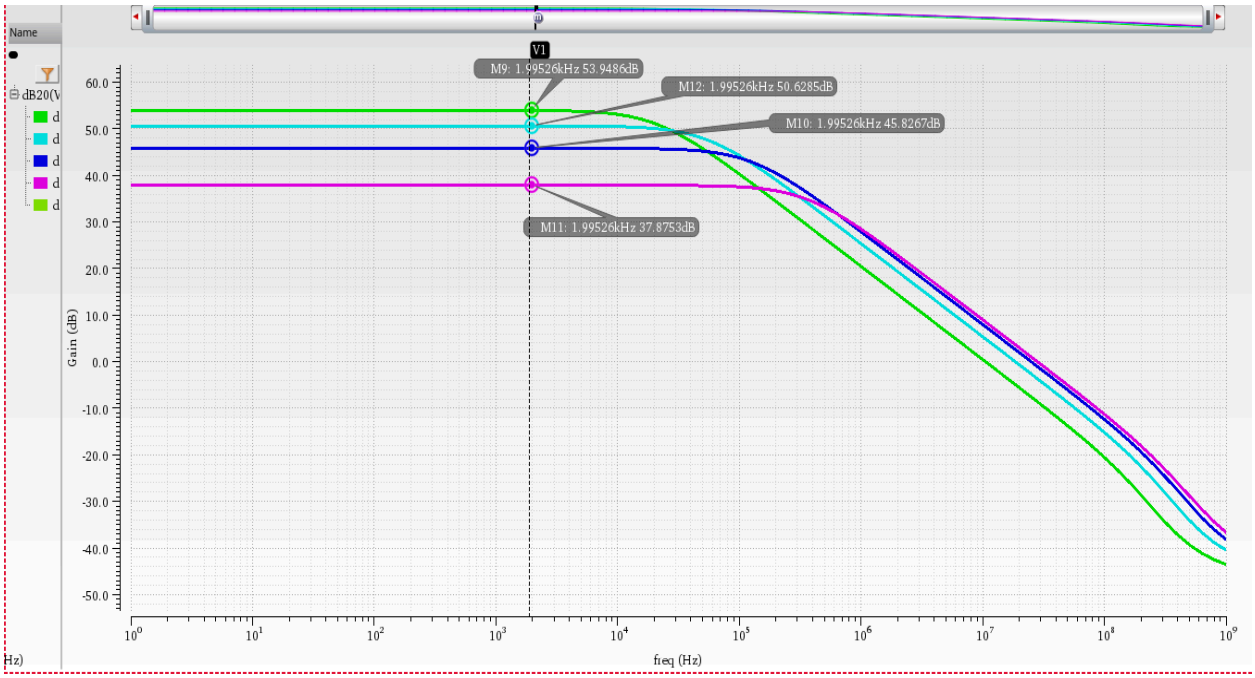
Green = 0.8

Light blue = 0.8667

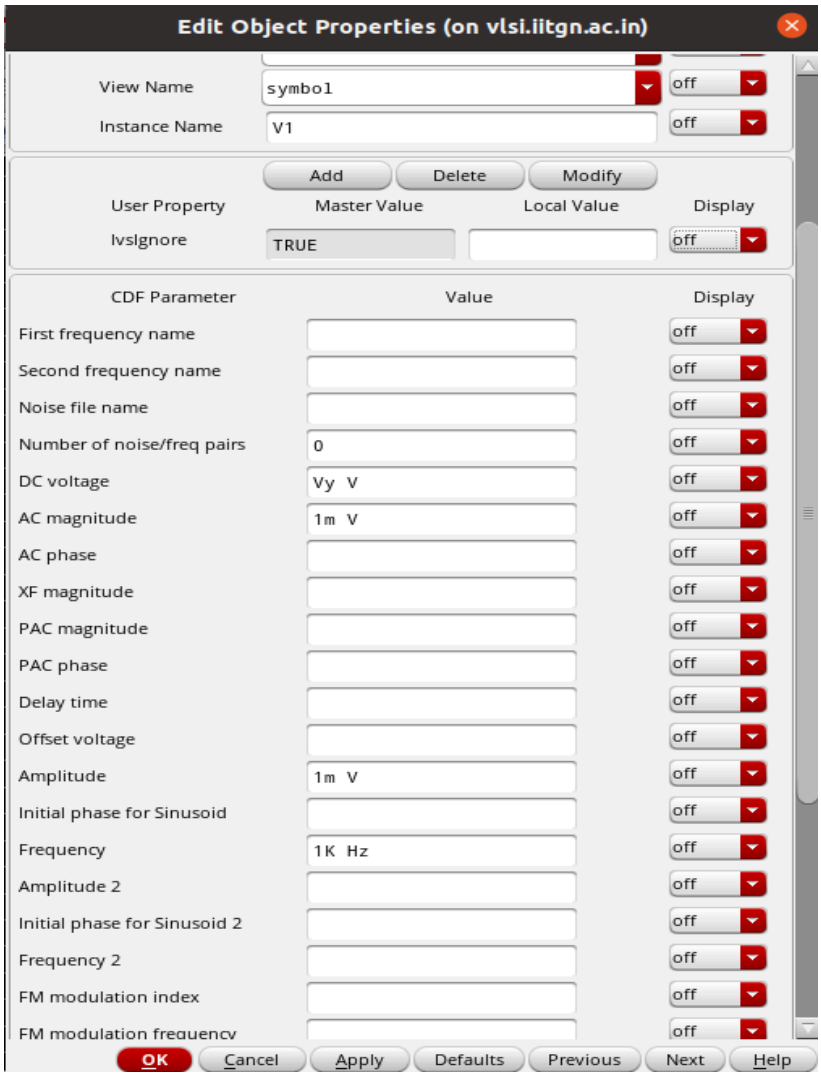
Blue = 0.9333

Pink = 1

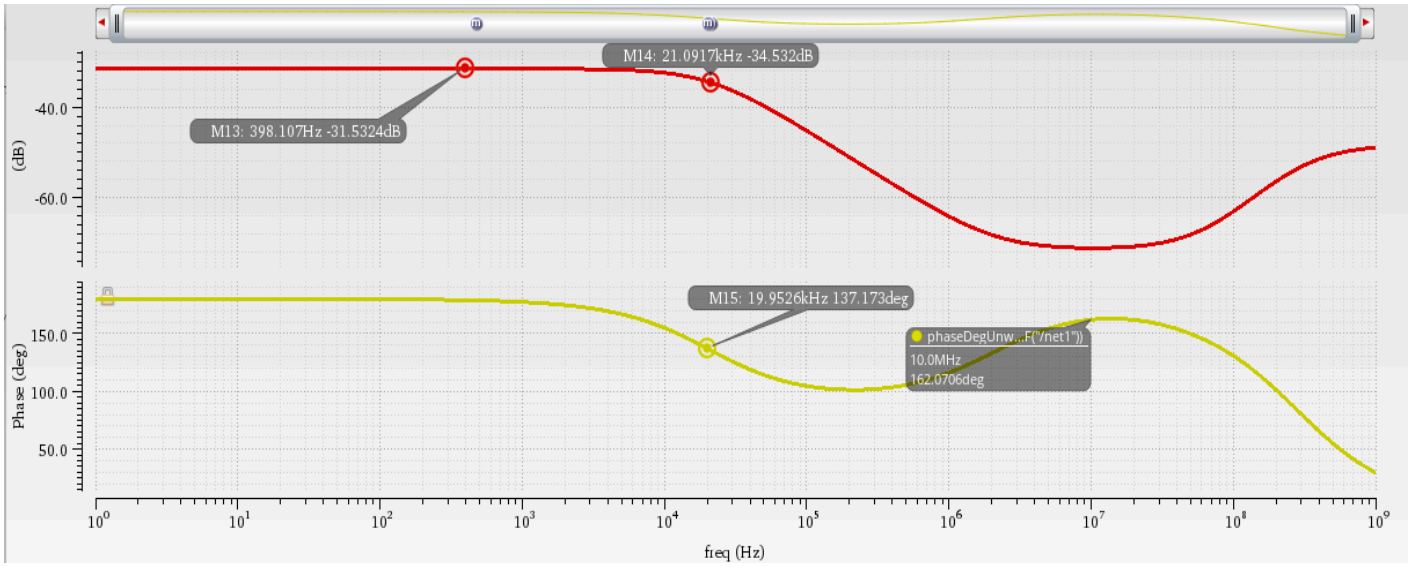




2.NOW WE ARE CHECKING CMRR CONDITION

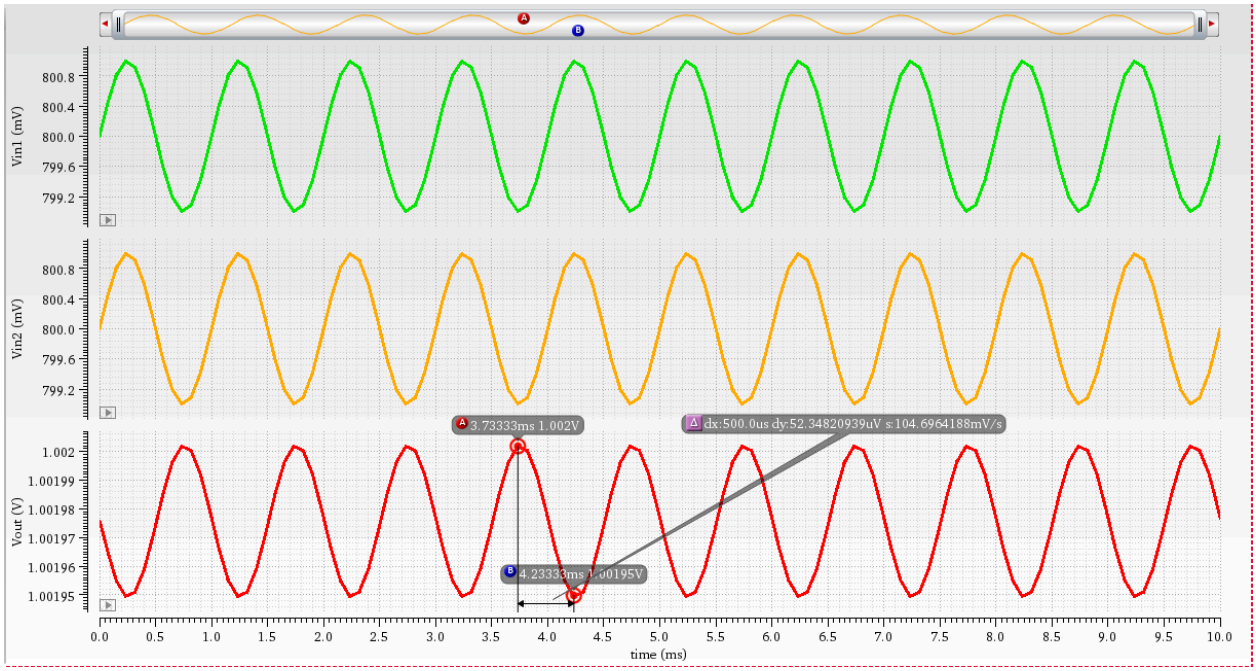


Bode plot



$$\text{CMRR} = \frac{diff\ gain}{common\ mode\ gain}$$

We have differential gain now we are calculating common mode gain



From the above plot at 1kHz freq

Common mode gain = $20\log(\frac{52.34}{2})$ = 28.299dB

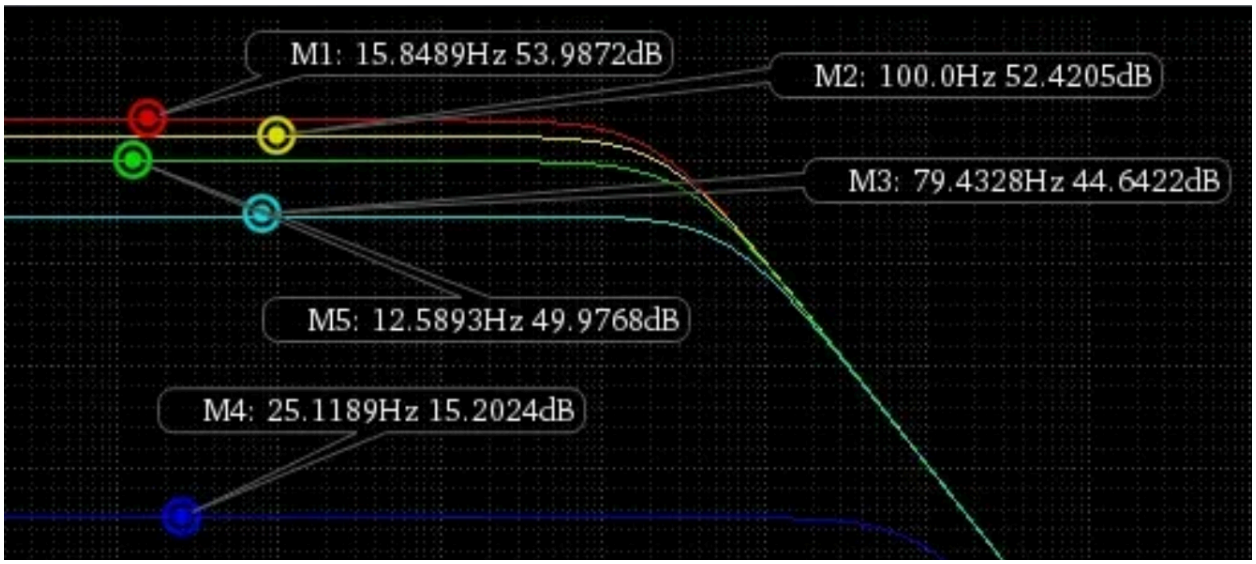
Calculating CMRR

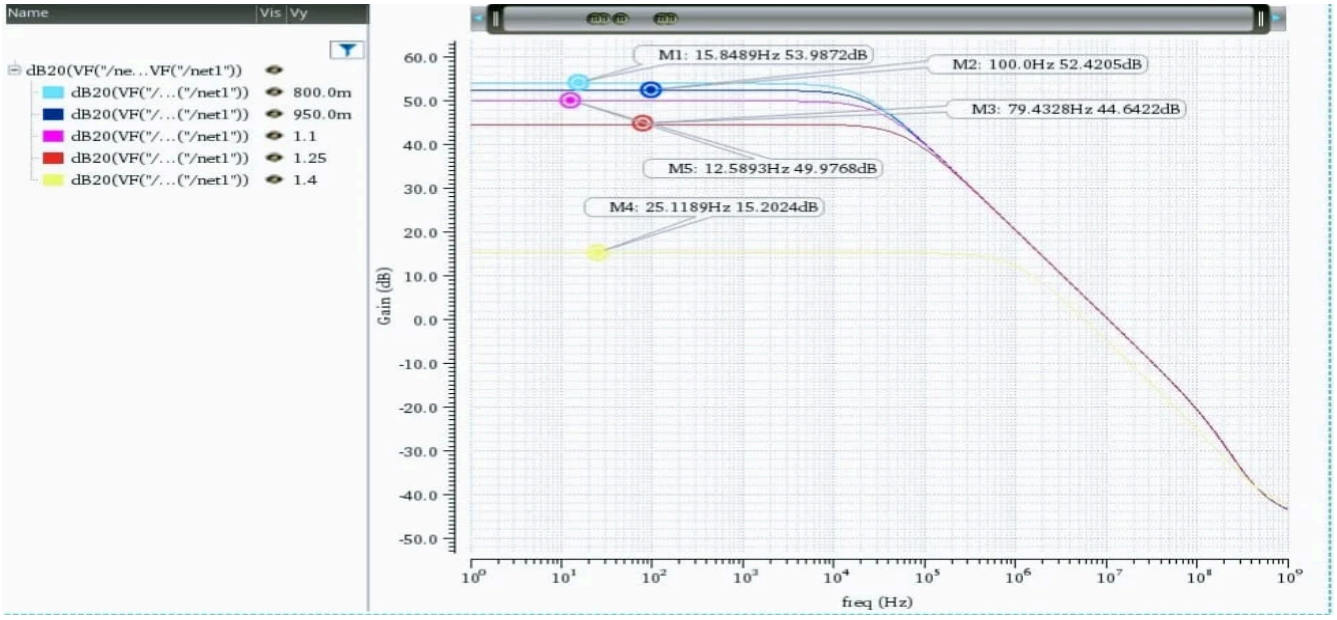
=> **CMRR(dB) = diff gain(dB) – common mode gain(dB)**

= 51.97dB – (28.299dB) = 79.299dB > 70dB

Condition satisfied

3.NOW WE ARE CHECKING ICMR CONDITION





From the plot, we observe that varying the input DC voltage from 0.8 V to 1.4 V *(parametric analysis)* does not significantly affect the gain, which remains consistently between 40 dB and 50 dB. However, at 1.4 V, the gain drops sharply to approximately 15 dB => our ICMR is around 0.8V to ~1.3V