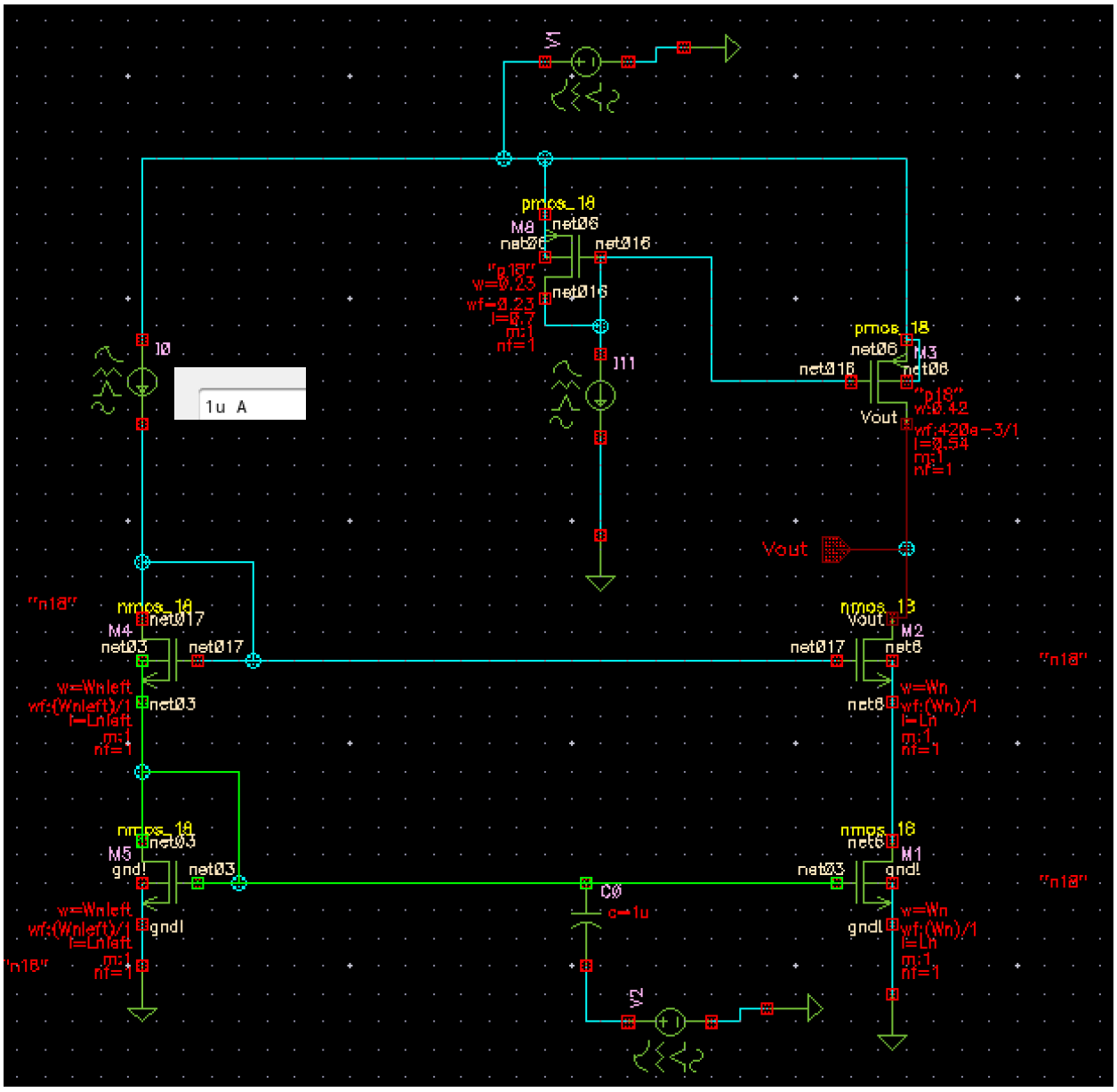
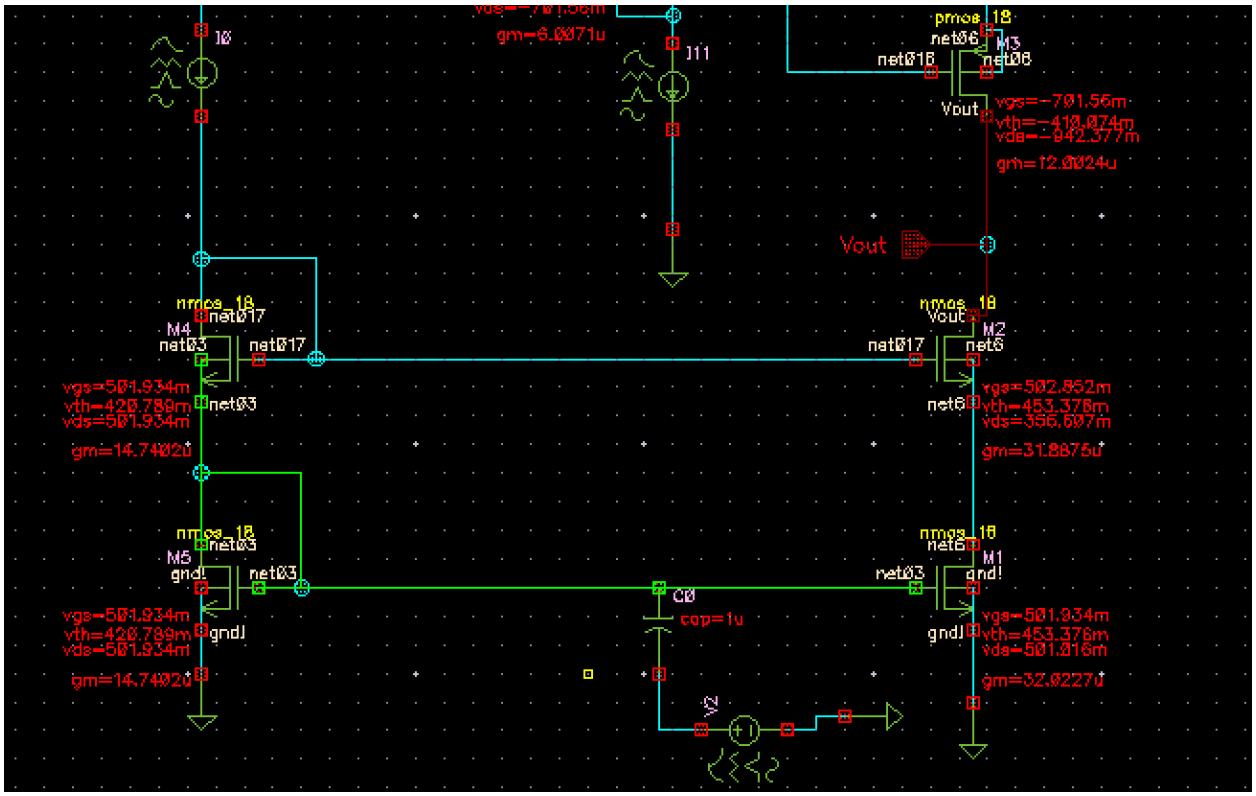
1st question:

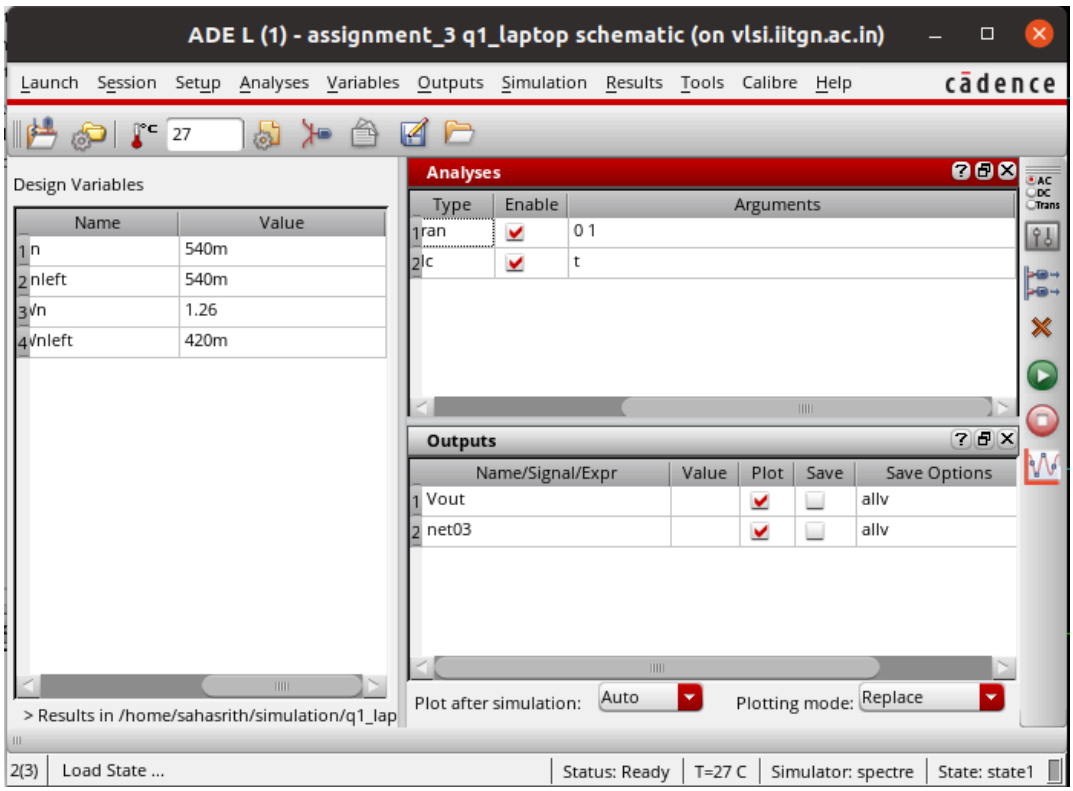


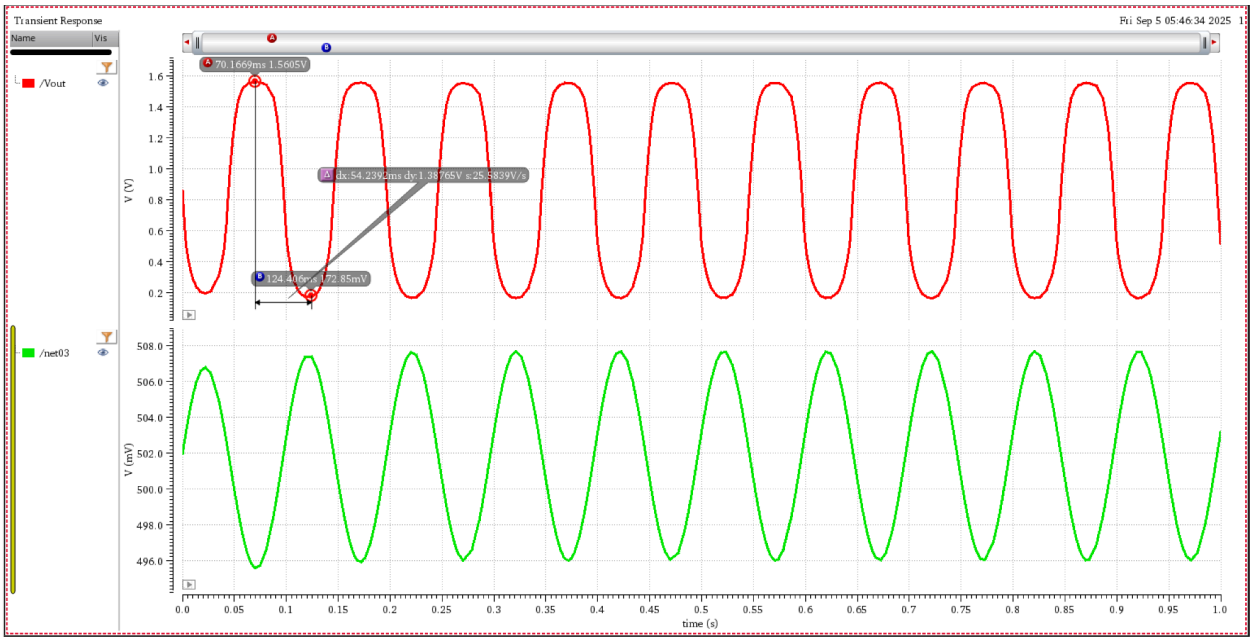
- Here i used cascode CS amplifier to increase the output impedance (which increases gain)
- Used pmos (in saturation) as resistor connecting VDD to Vout
- For biasing the above pmos i used I to V converterwhich is diode connected Pmos

Dc operating point:



ADL

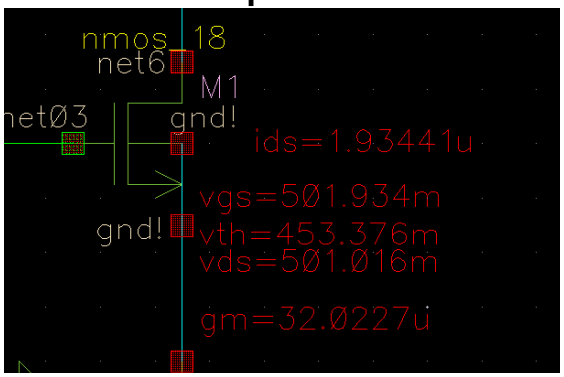




$$\frac{1.387\,65}{0.012} = 115.637\,5$$

Gain = 1.38765/0.012 = 115.637 > 200V/V

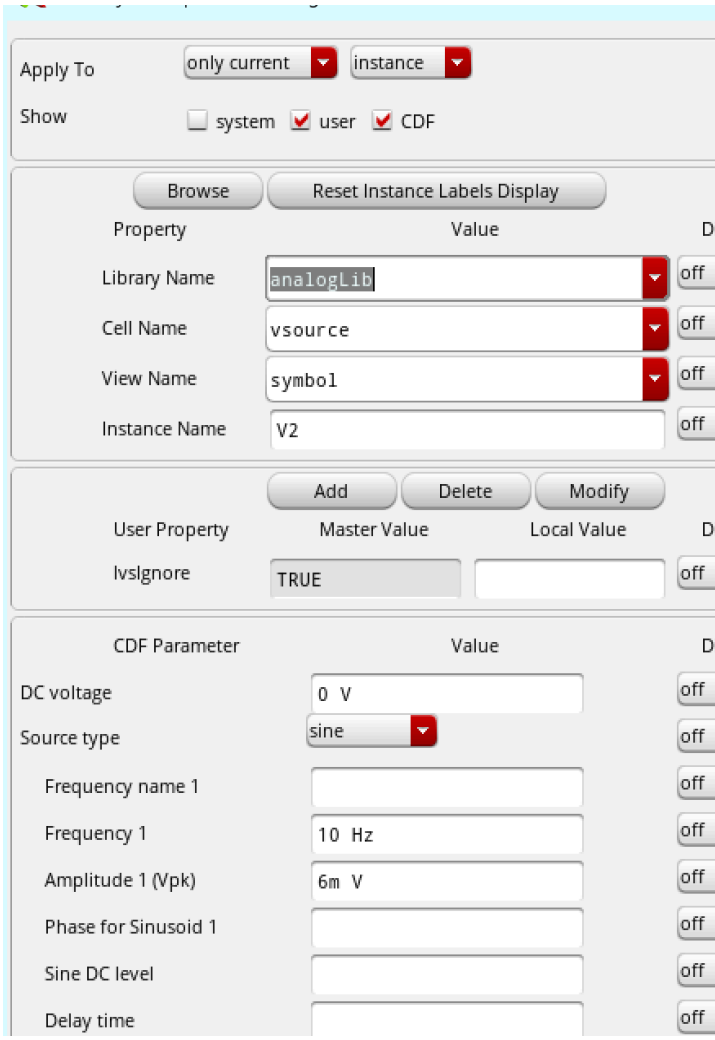
Power consumption



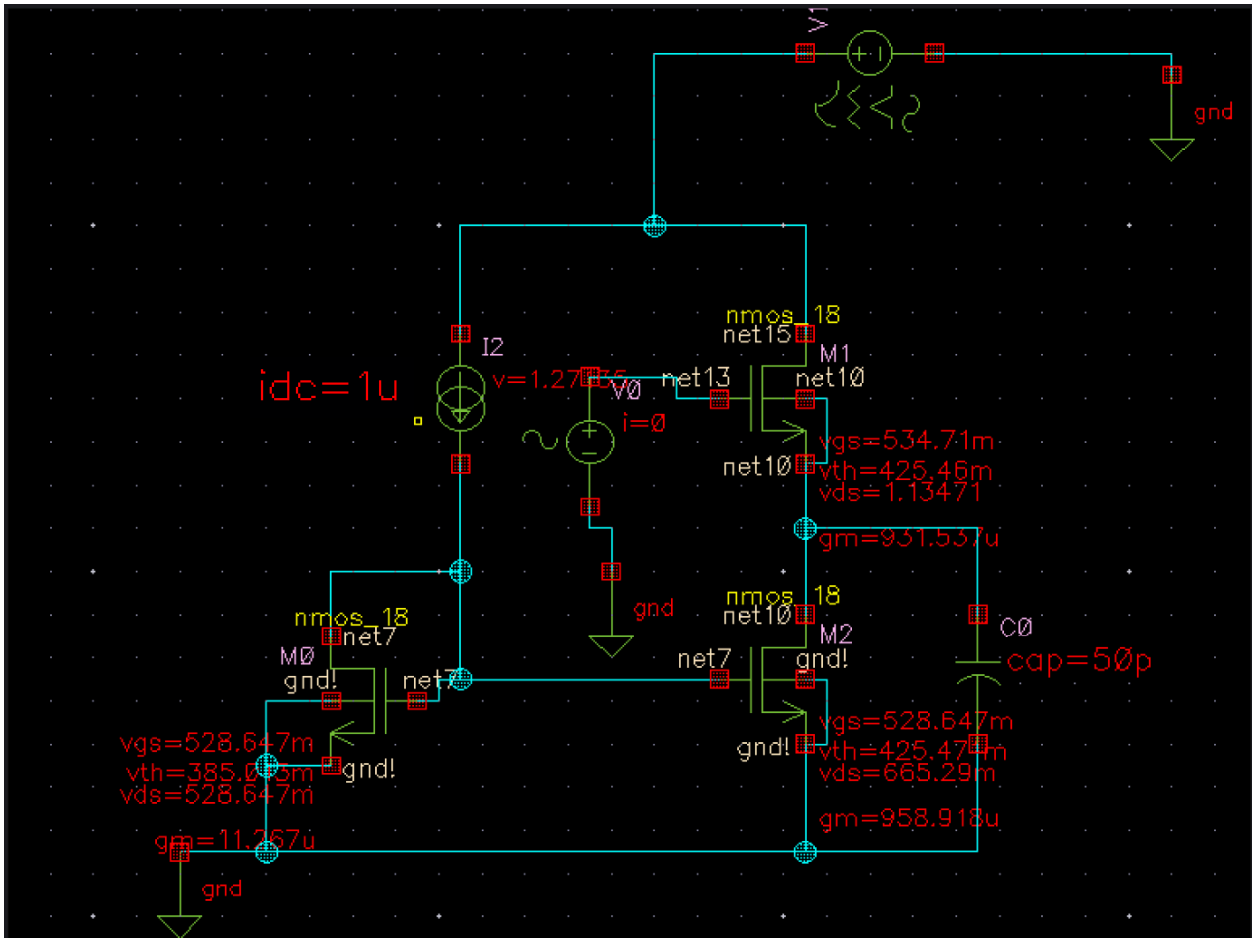
$$(1\times10^{-6}+1.93\times10^{-6})(1.8) = 0.000\,005\,274$$

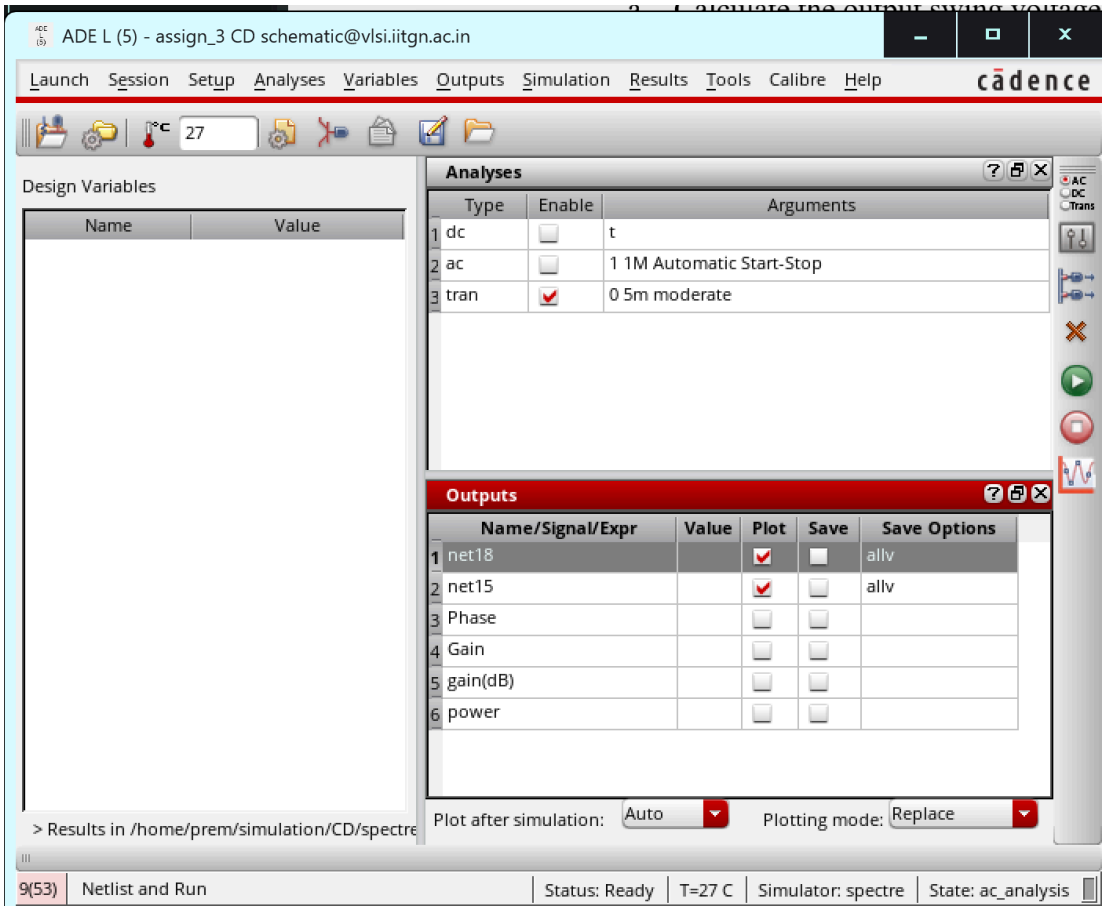
~ Which is less than 10uW

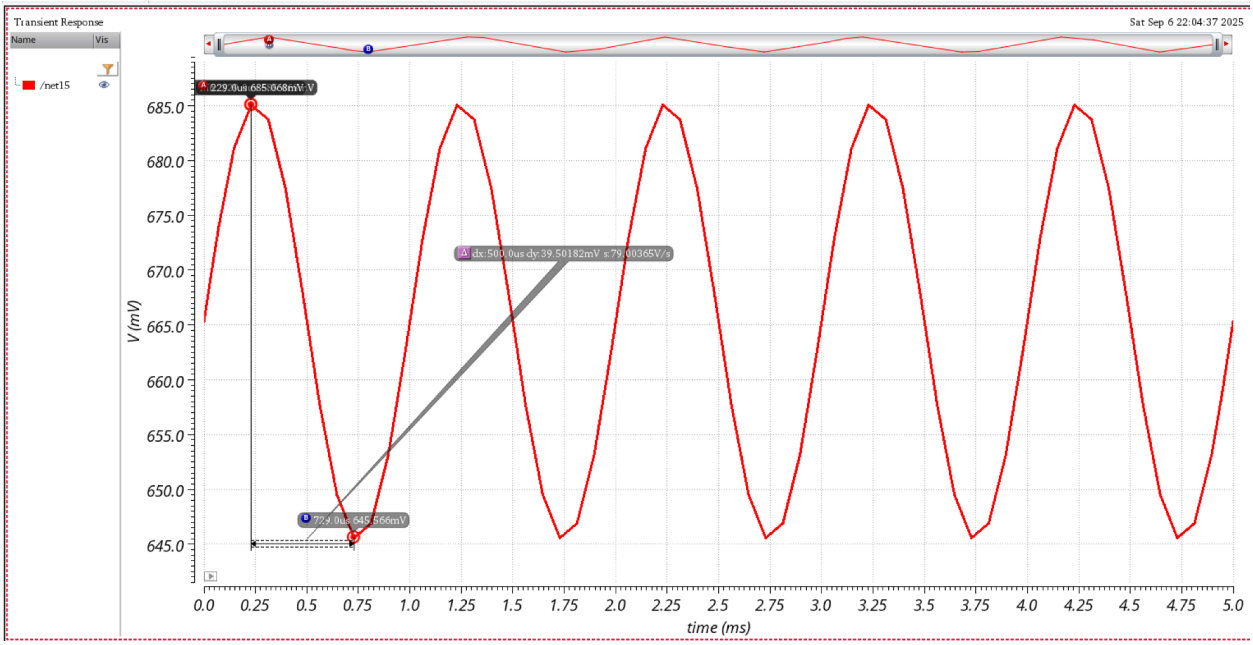
2nd question

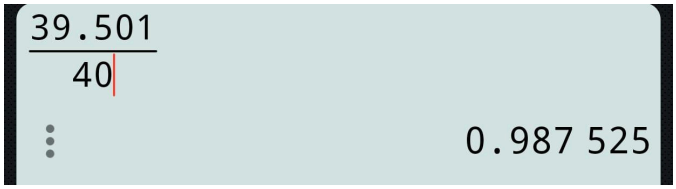


2nd question: Schematic



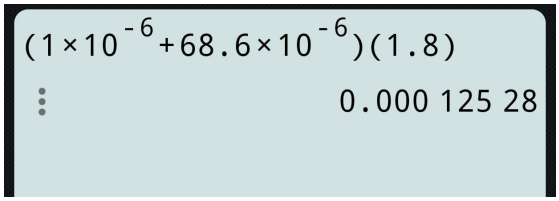




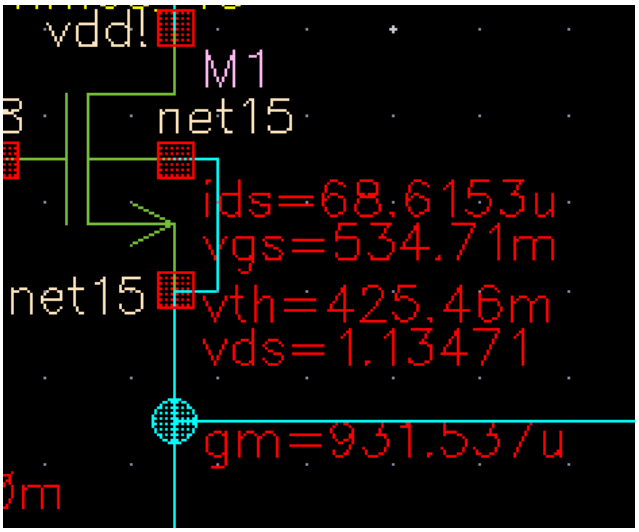


Gain = 39.501/40 = 0.987 > 0.95V/V

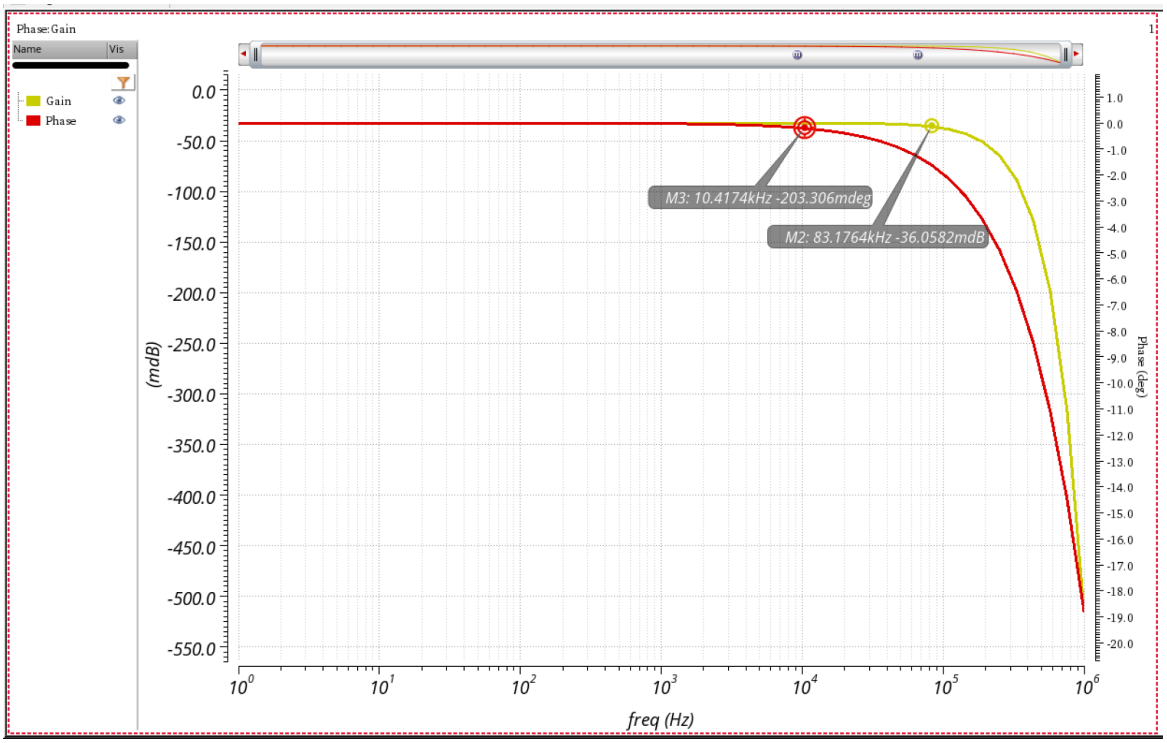
Power consumption



~ Which is less than 2mW



Gain and phase plot:



Freq response