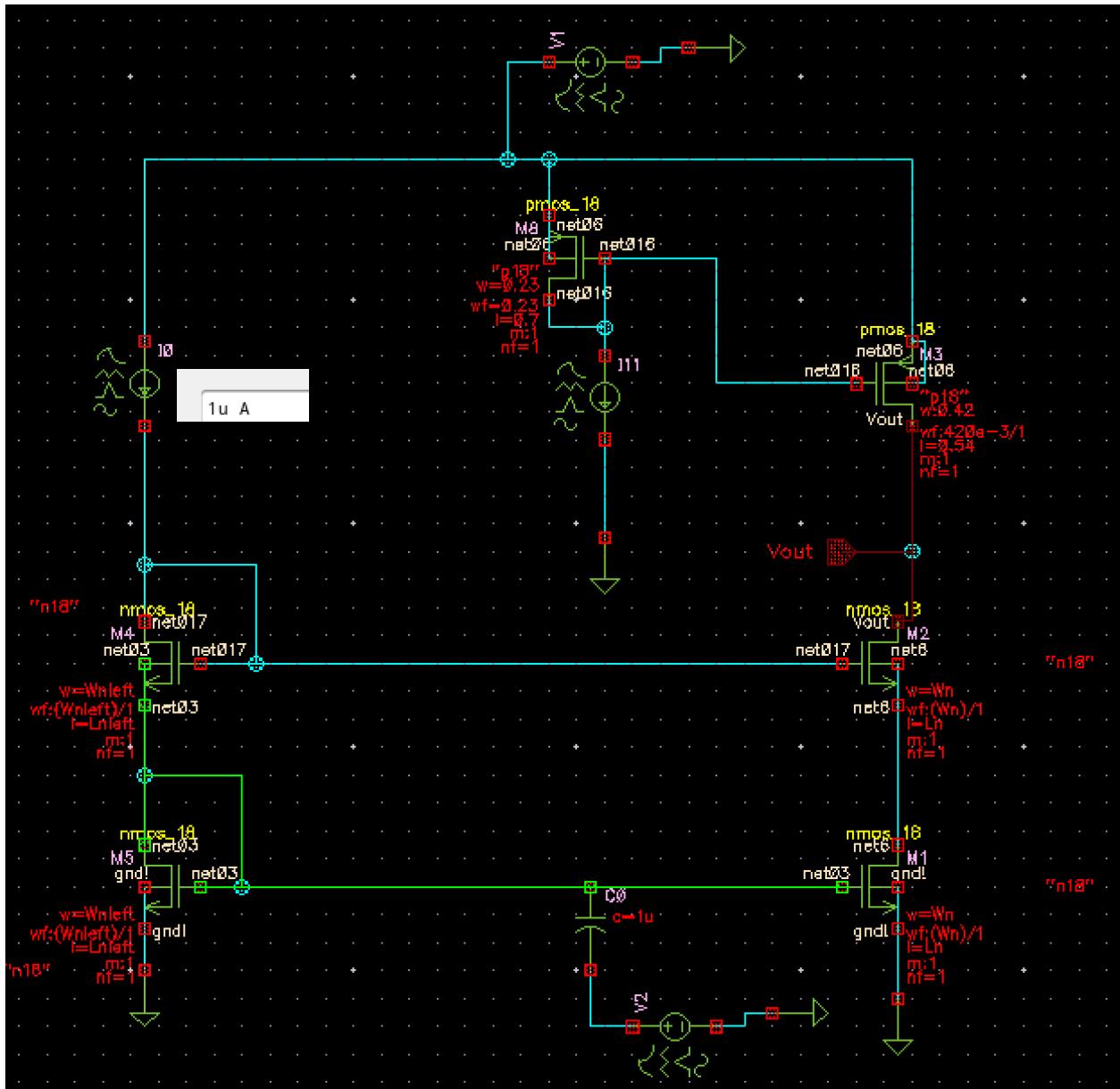
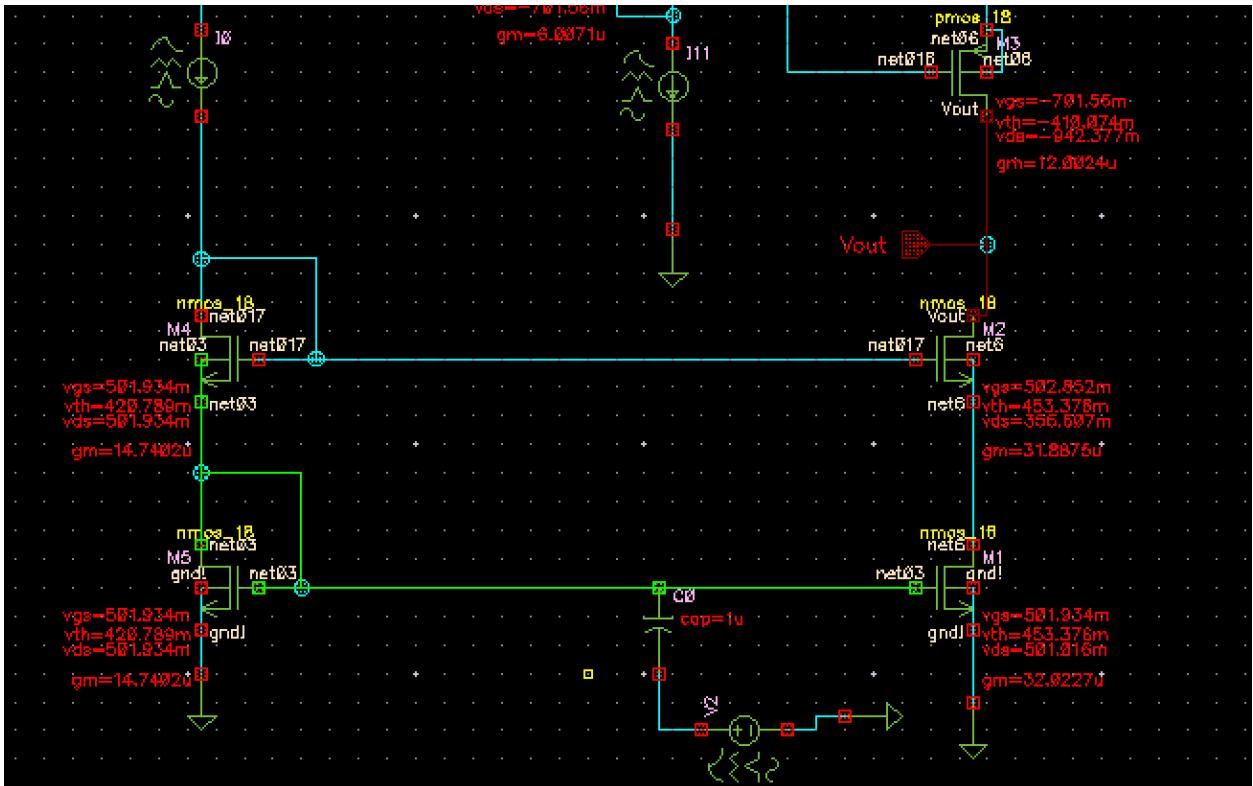


## 1st question:

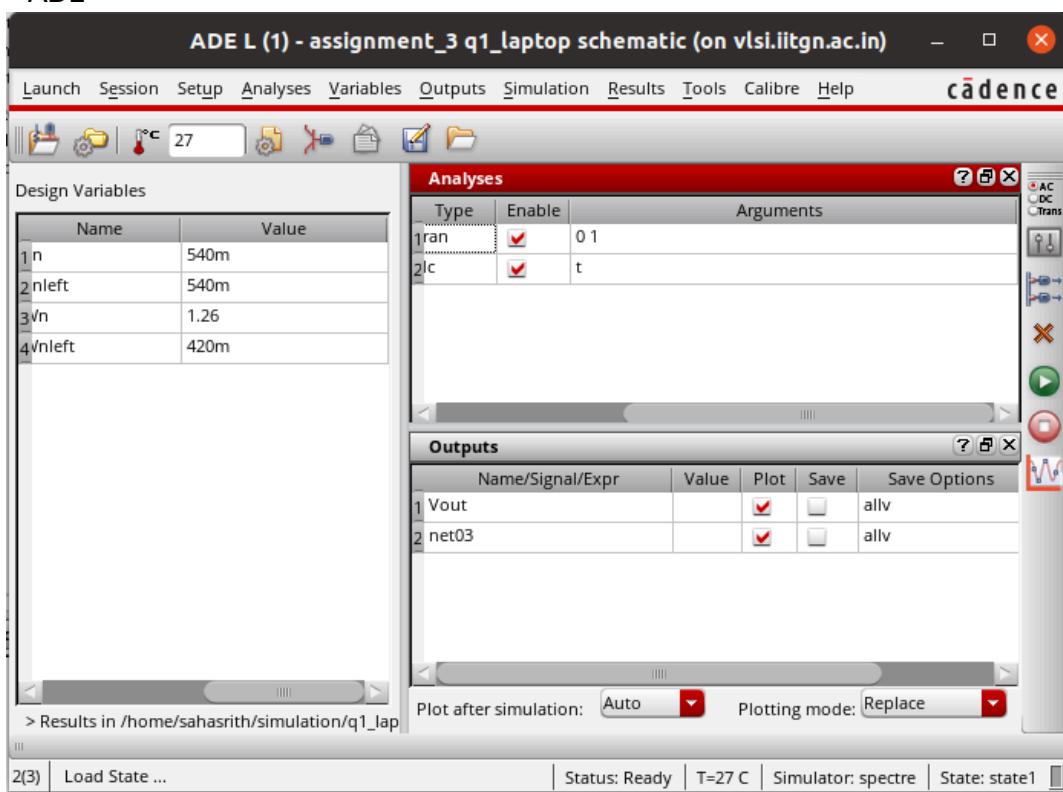


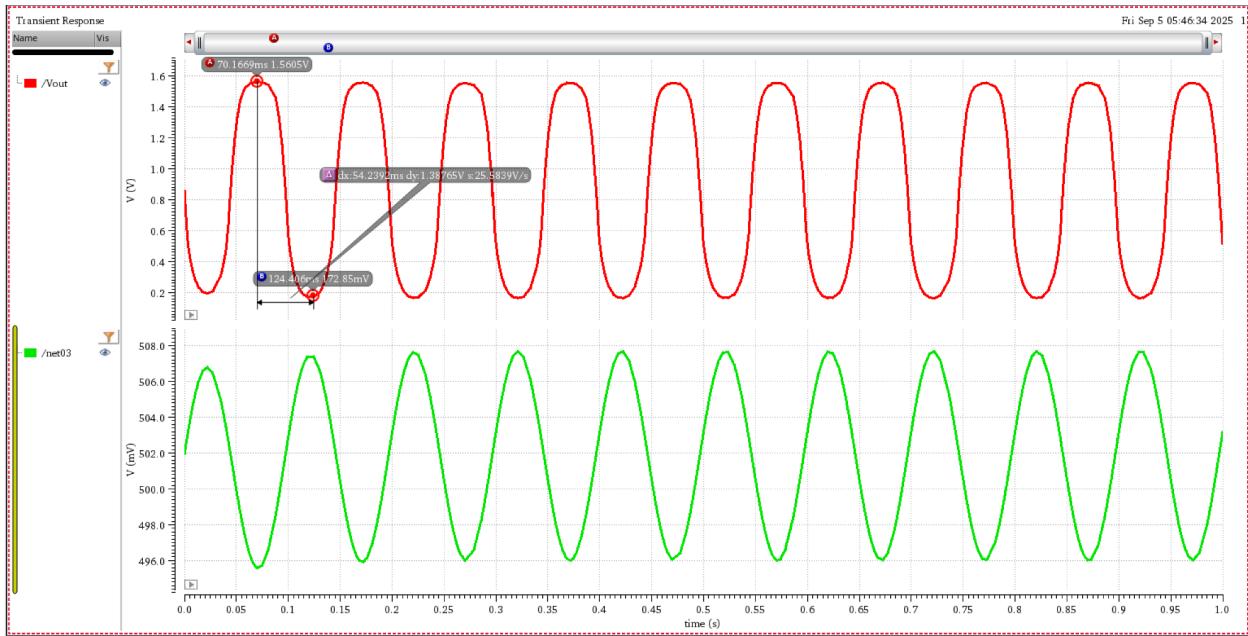
- Here i used cascode CS amplifier to increase the output impedance (which increases gain)
  - Used pmos (in saturation) as resistor connecting VDD to Vout
  - For biasing the above pmos i used I to V converter which is diode connected Pmos

Dc operating point:



ADL

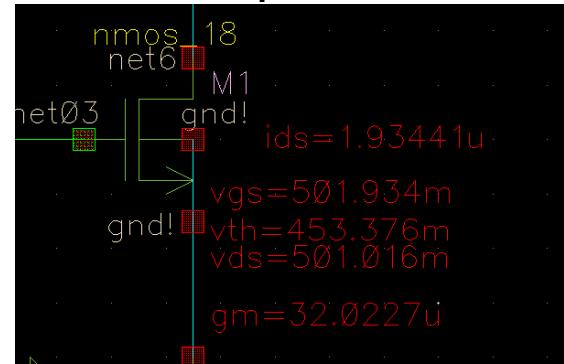




$$\frac{1.38765}{0.012} = 115.6375$$

$$\text{Gain} = 1.38765/0.012 = 115.637 > 200\text{V/V}$$

### Power consumption



$$(1 \times 10^{-6} + 1.93 \times 10^{-6})(1.8)$$

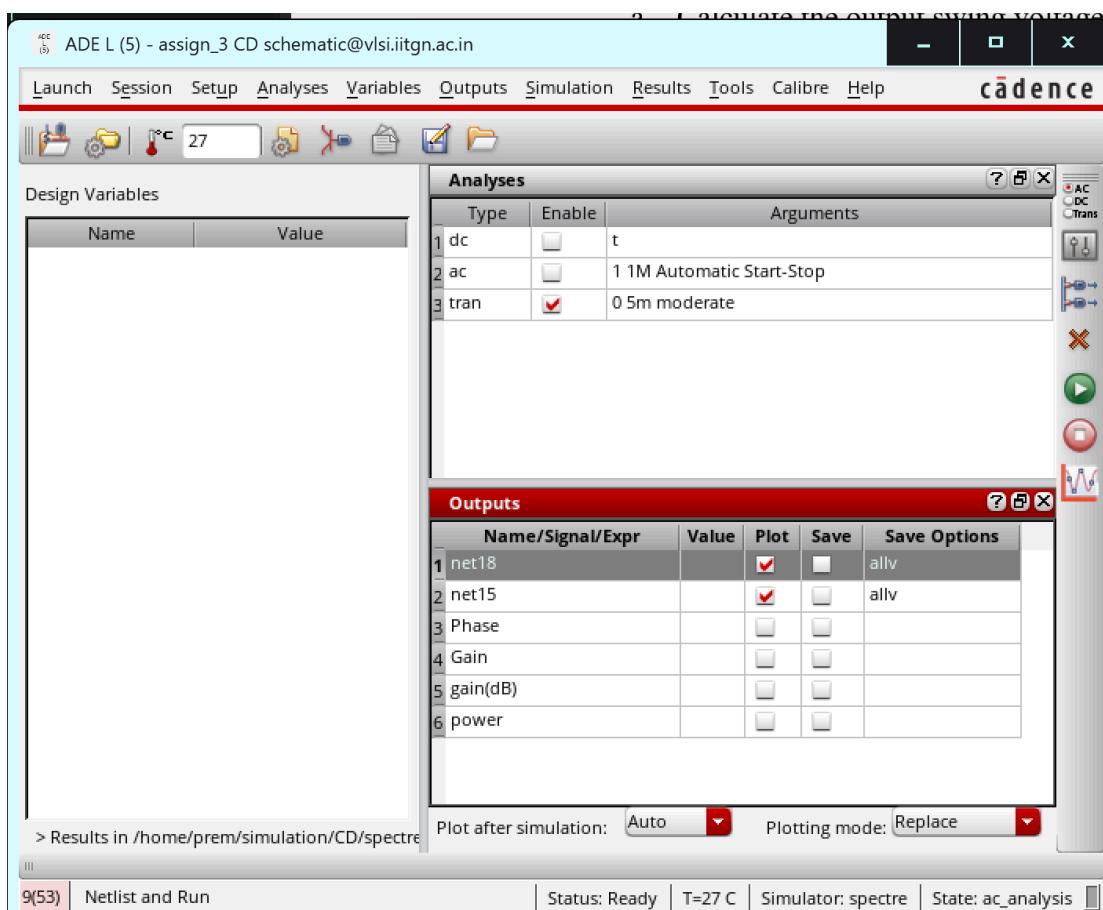
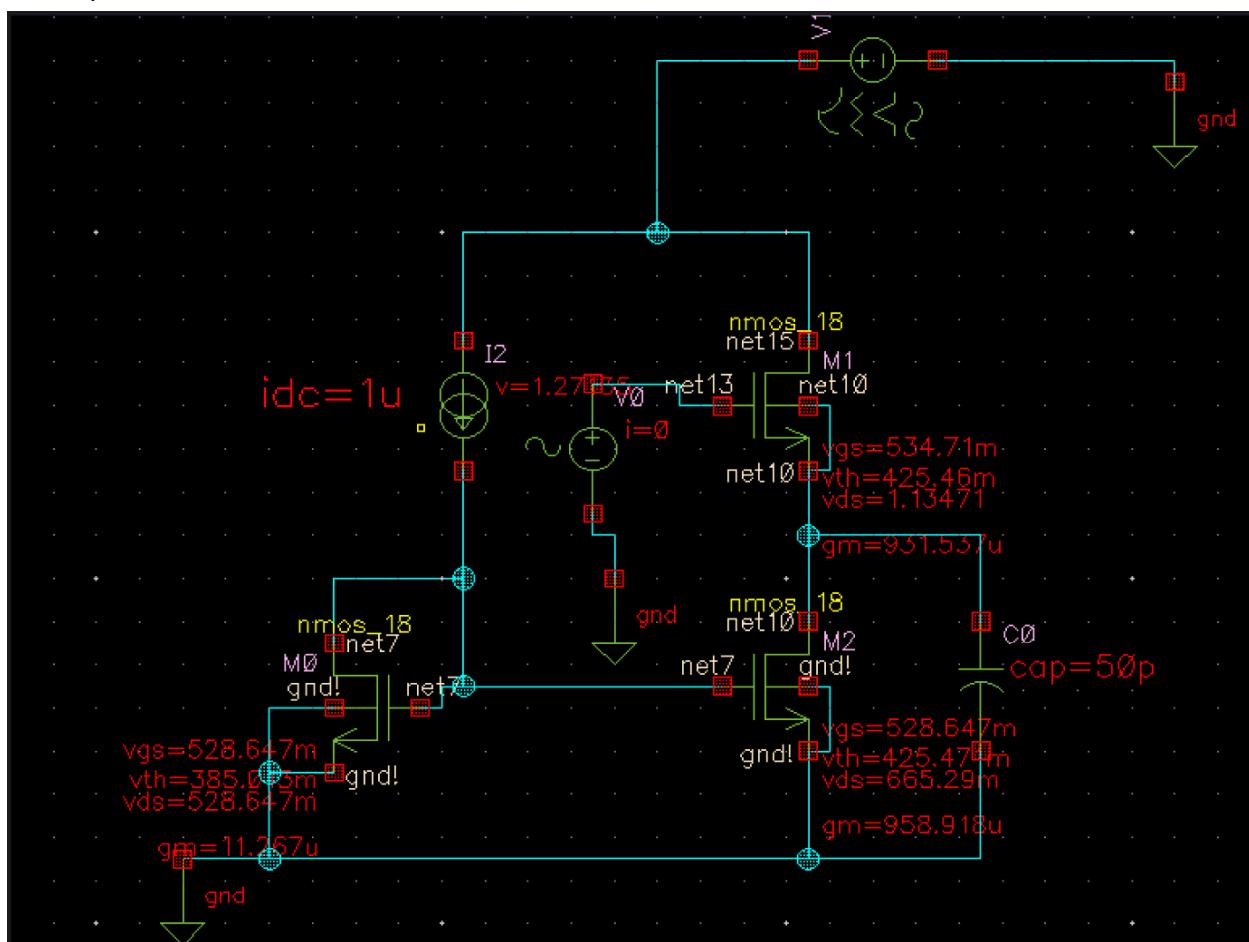
$$0.000\ 005\ 274$$

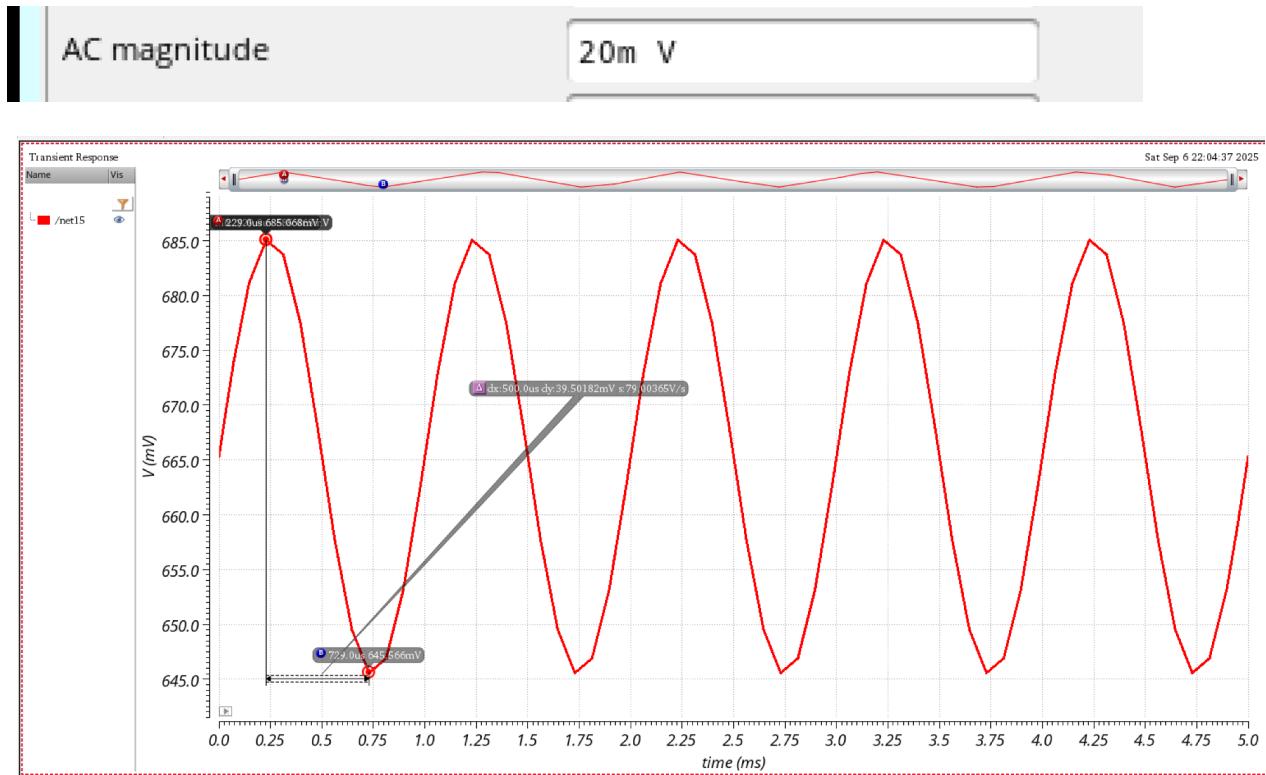
**~ Which is less than 10uW**

2nd question

Apply To		Reset Instance Labels Display	
Property	Value		
Library Name	analogLib	off	
Cell Name	vsource	off	
View Name	symbol	off	
Instance Name	V2	off	
User Property		Master Value	Local Value
IvsIgnore	TRUE	off	
CDF Parameter		Value	
DC voltage	0 V	off	
Source type	sine	off	
Frequency name 1		off	
Frequency 1	10 Hz	off	
Amplitude 1 (Vpk)	6m V	off	
Phase for Sinusoid 1		off	
Sine DC level		off	
Delay time		off	

2nd question: Schematic





$$\frac{39.501}{40}$$

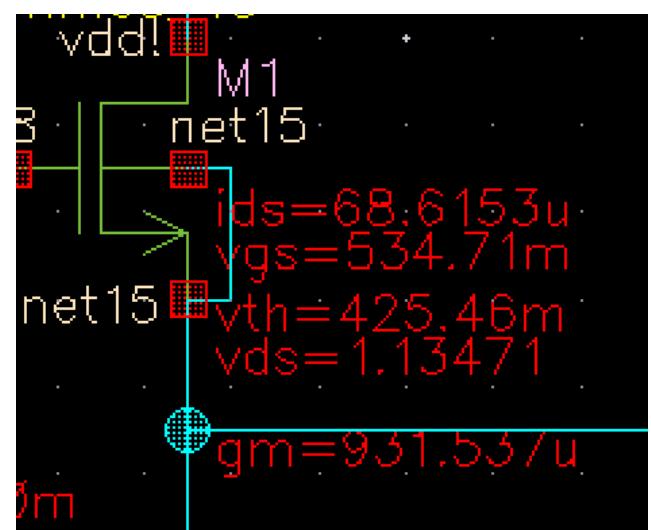
$$0.987 \ 525$$

$$\text{Gain} = 39.501/40 = 0.987 > 0.95\text{V/V}$$

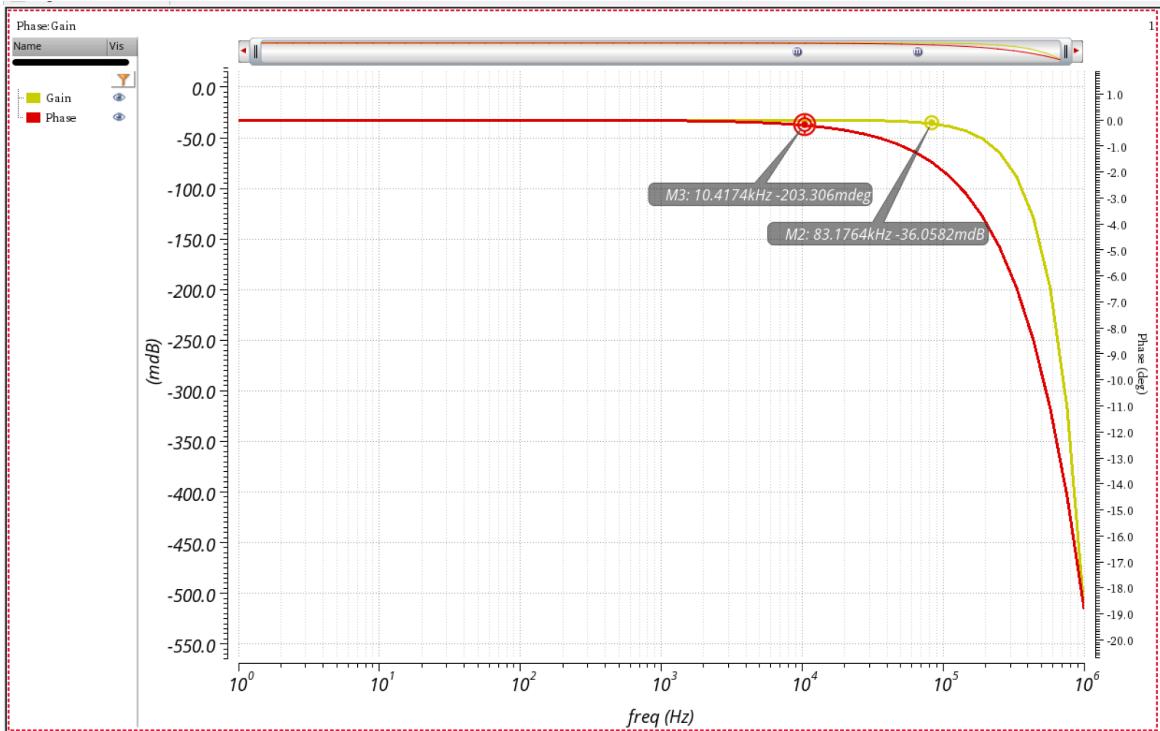
Power consumption

$$(1 \times 10^{-6} + 68.6 \times 10^{-6})(1.8) \\ \vdots \quad 0.000 \ 125 \ 28$$

**~ Which is less than 2mW**



## Gain and phase plot:



Freq response

