

# Analog CMOS IC Design (EE651)

## 23110064

2nd Question

2a)

Q)  $V_{OV} > 150mV$

①                          ②

$$V_{AS1} = V_{AS2}$$

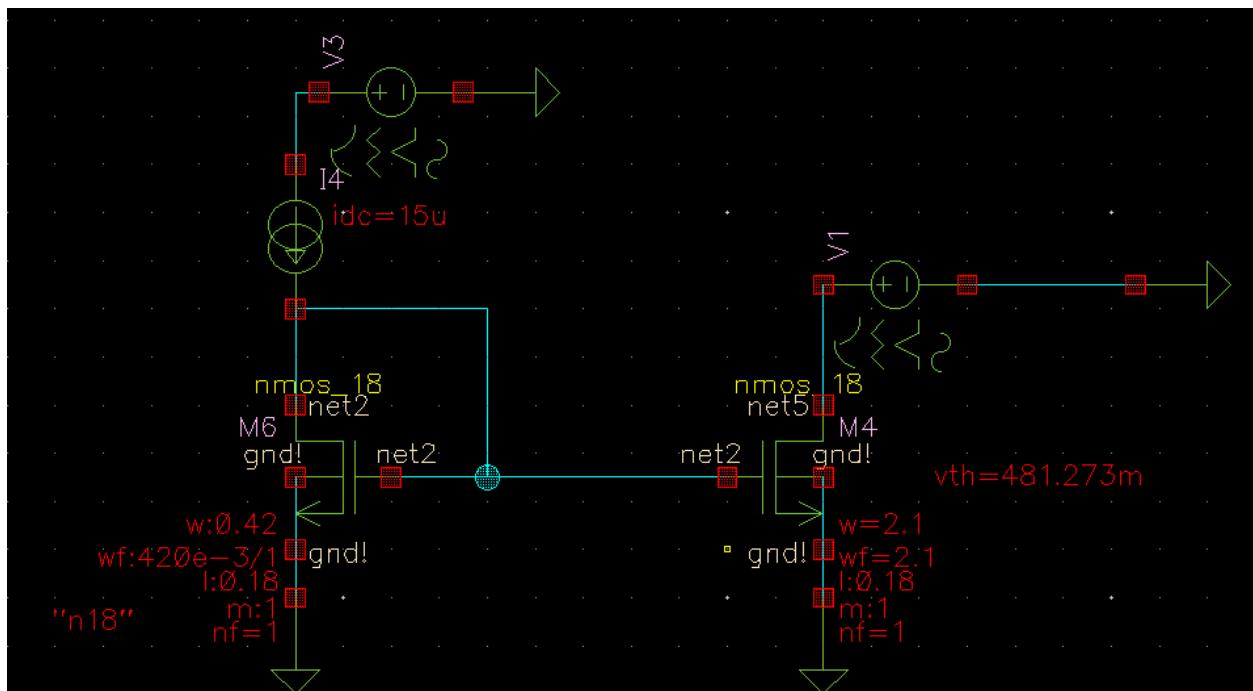
$I_{REF}$                       (5) ( $I_{REF}$ )

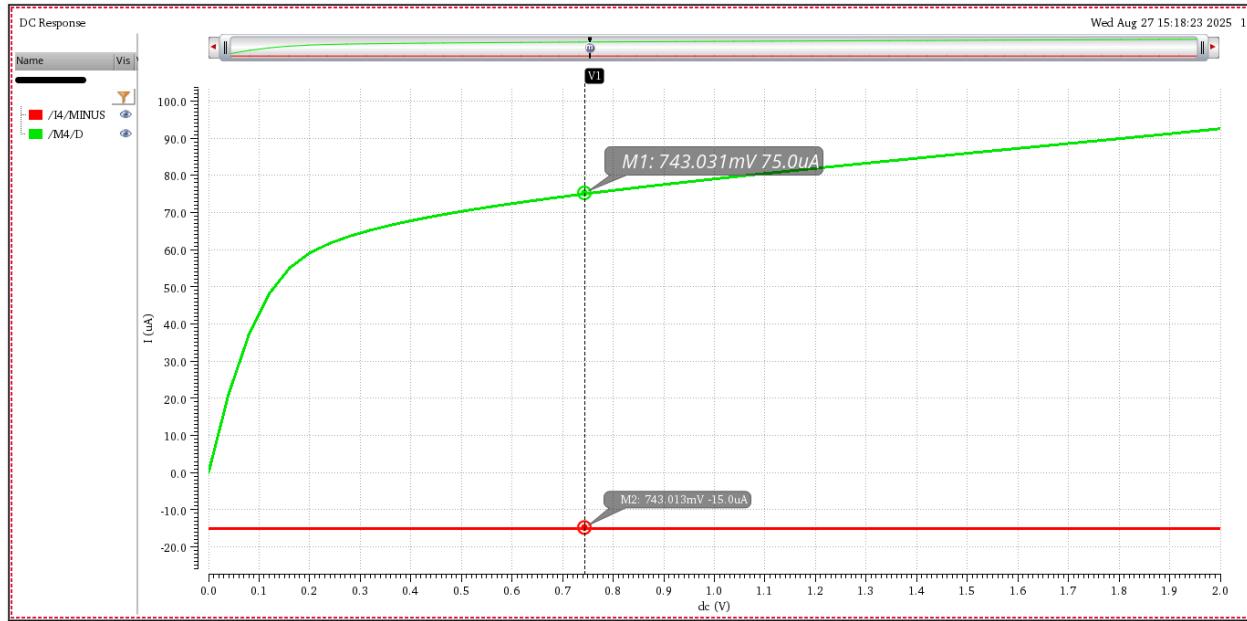
$$I_{D1} = \frac{1}{2} (\mu_n C_{ox}) \left( \frac{w_1}{L_1} \right) (V_{AS} - V_{TH})^2$$

$$I_{D2} = \frac{1}{2} (\mu_n C_{ox}) \left( \frac{w_2}{L_2} \right)_2 (V_{AS} - V_{TH})^2$$

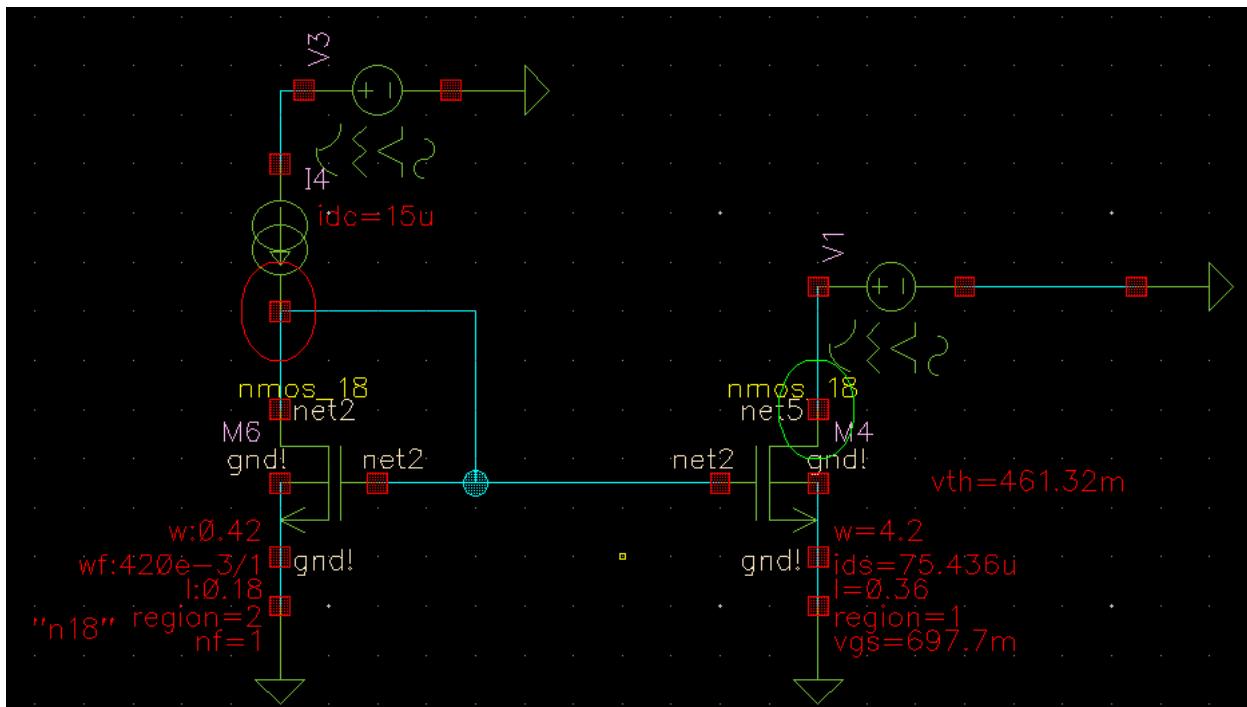
$$\frac{I_{D2}}{I_{D1}} = 5 = \frac{(w_2/L_2)_2}{(w_1/L_1)_1}$$

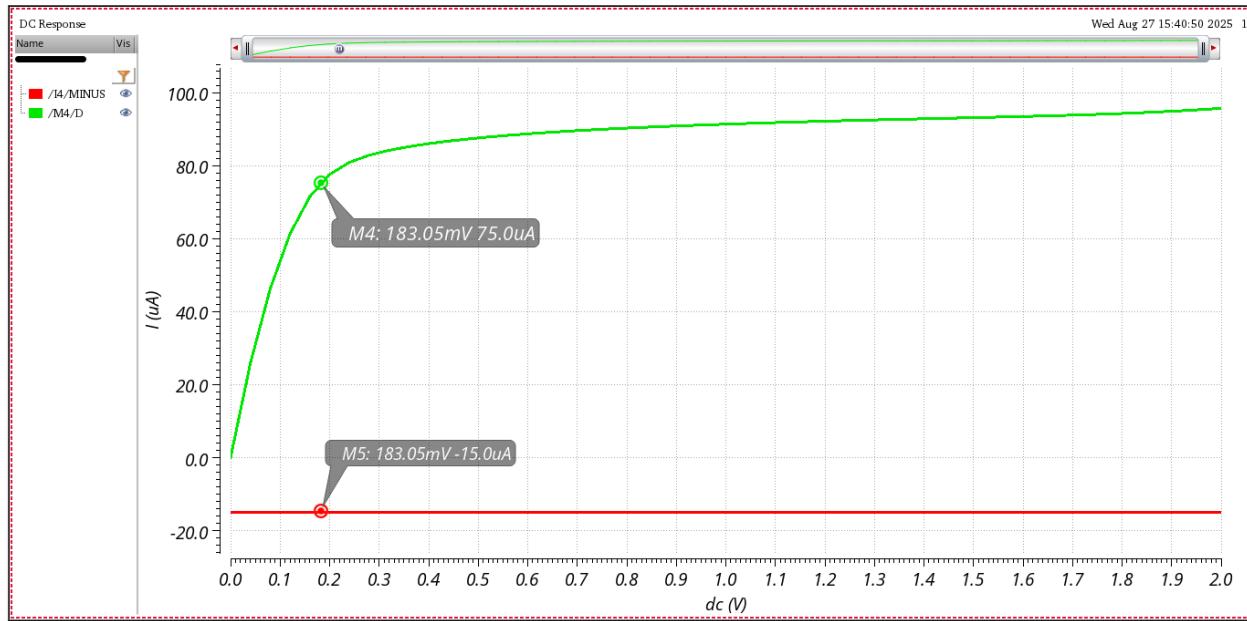
1st iteration of changing L and W of right mosfet so that the ratio of w/l right mosfet is 5 times w/l of left mosfet



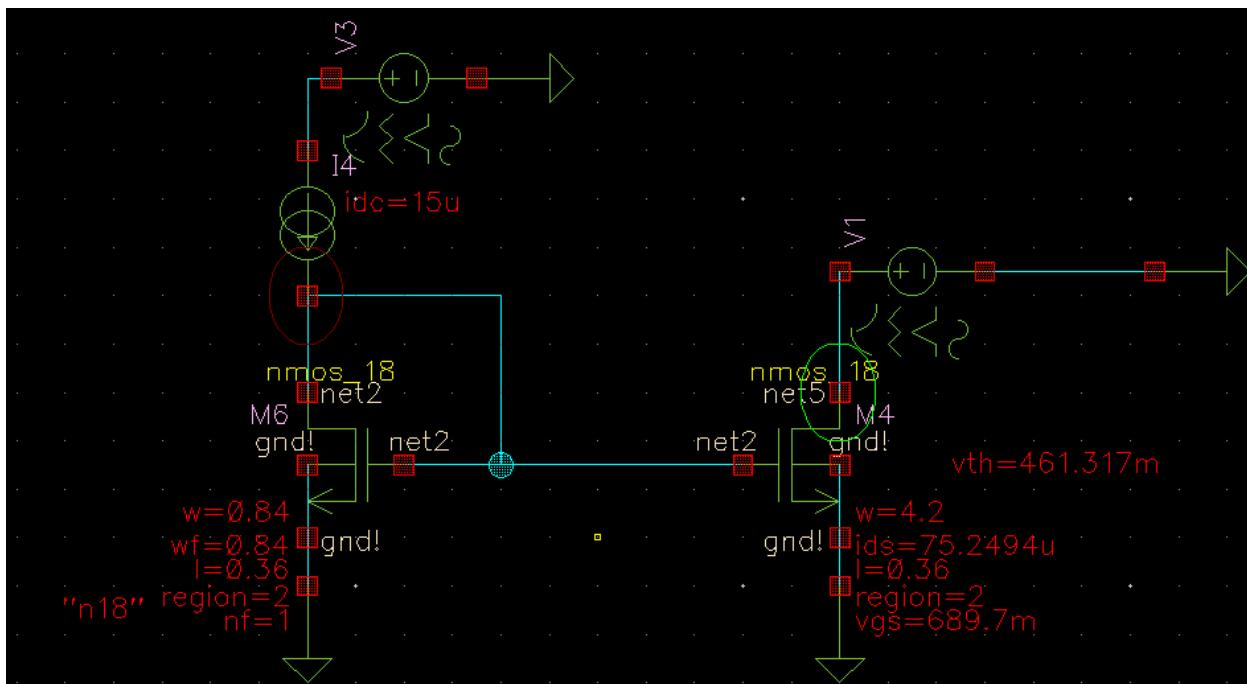


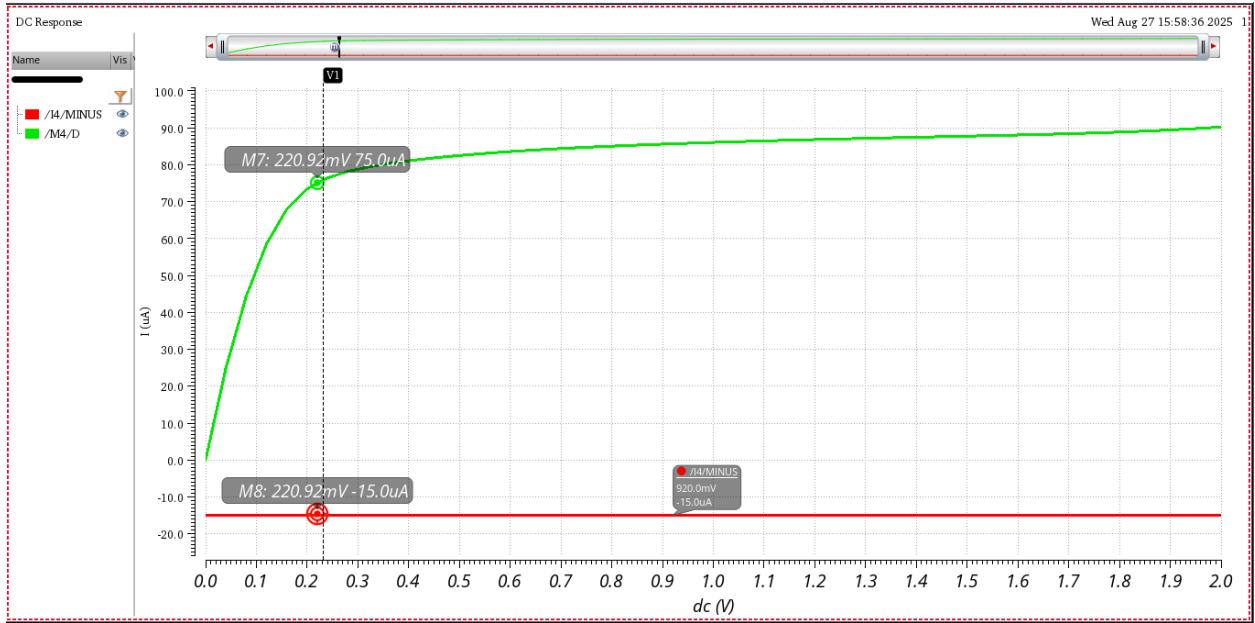
2nd iteration (increasing the length to minimize channel length modulation keeping the ratio of w/l right mosfet is 5 times w/l of left mosfet)



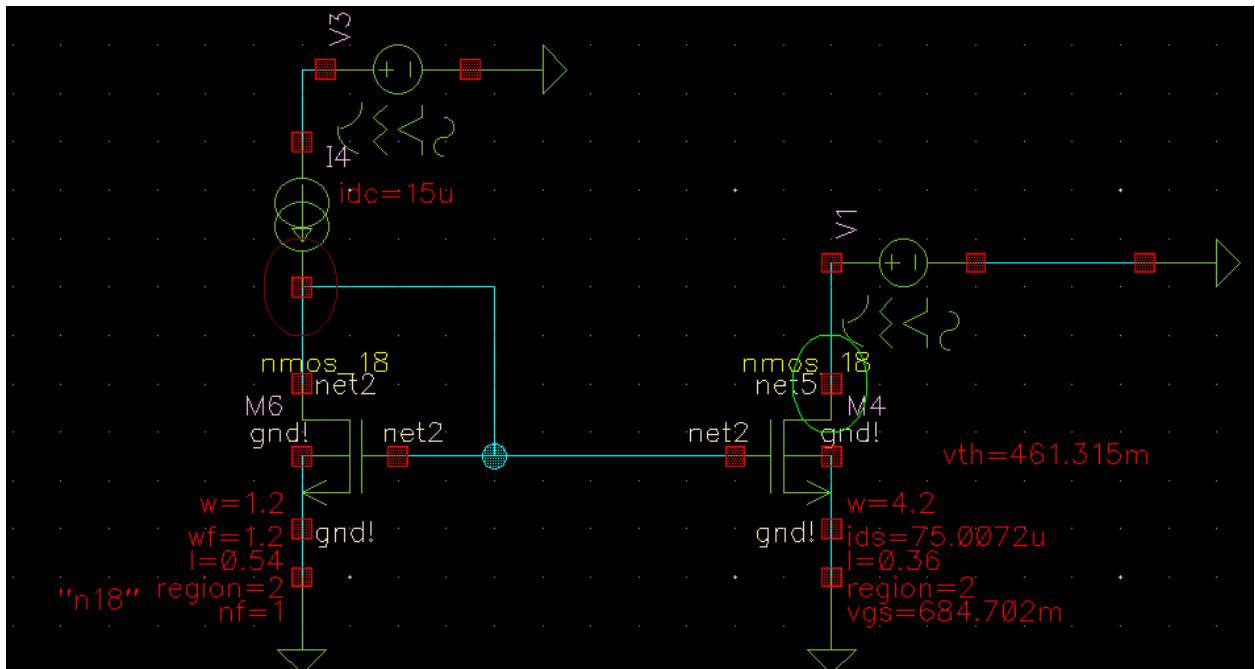


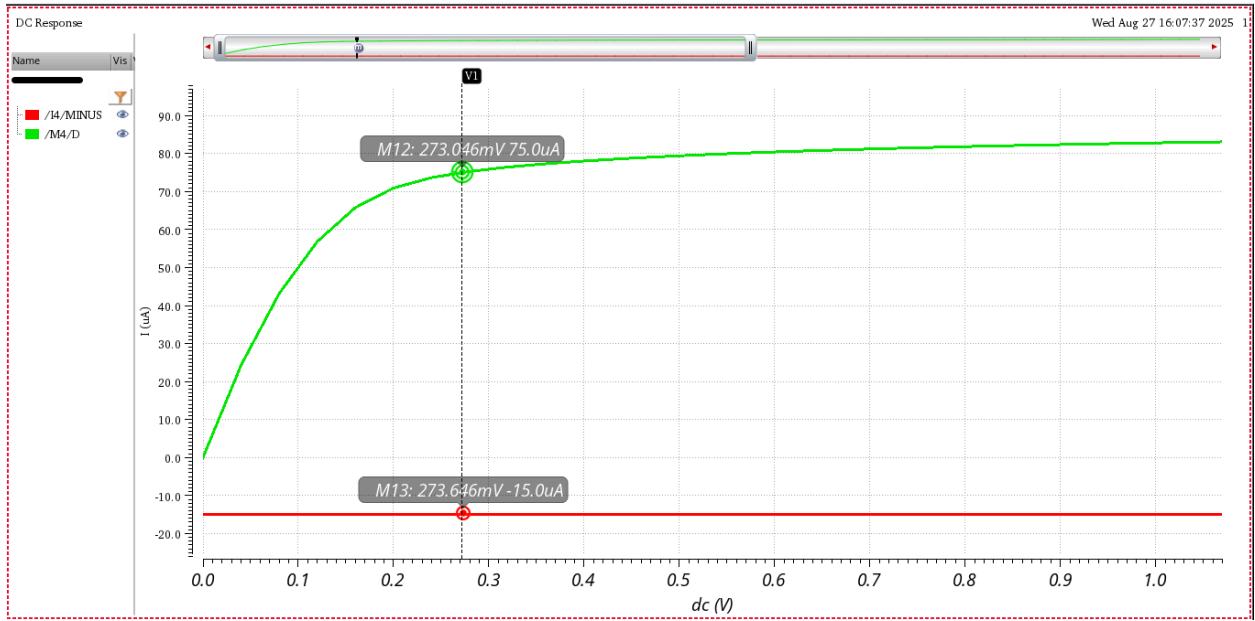
3rd iteration of changing l(increasing to minimize channel length modulation) and w of left mosfet keeping right w,l same as 2nd iteration





4th iteration of changing l and w of left mosfet keeping right w,l same as 2nd iteration

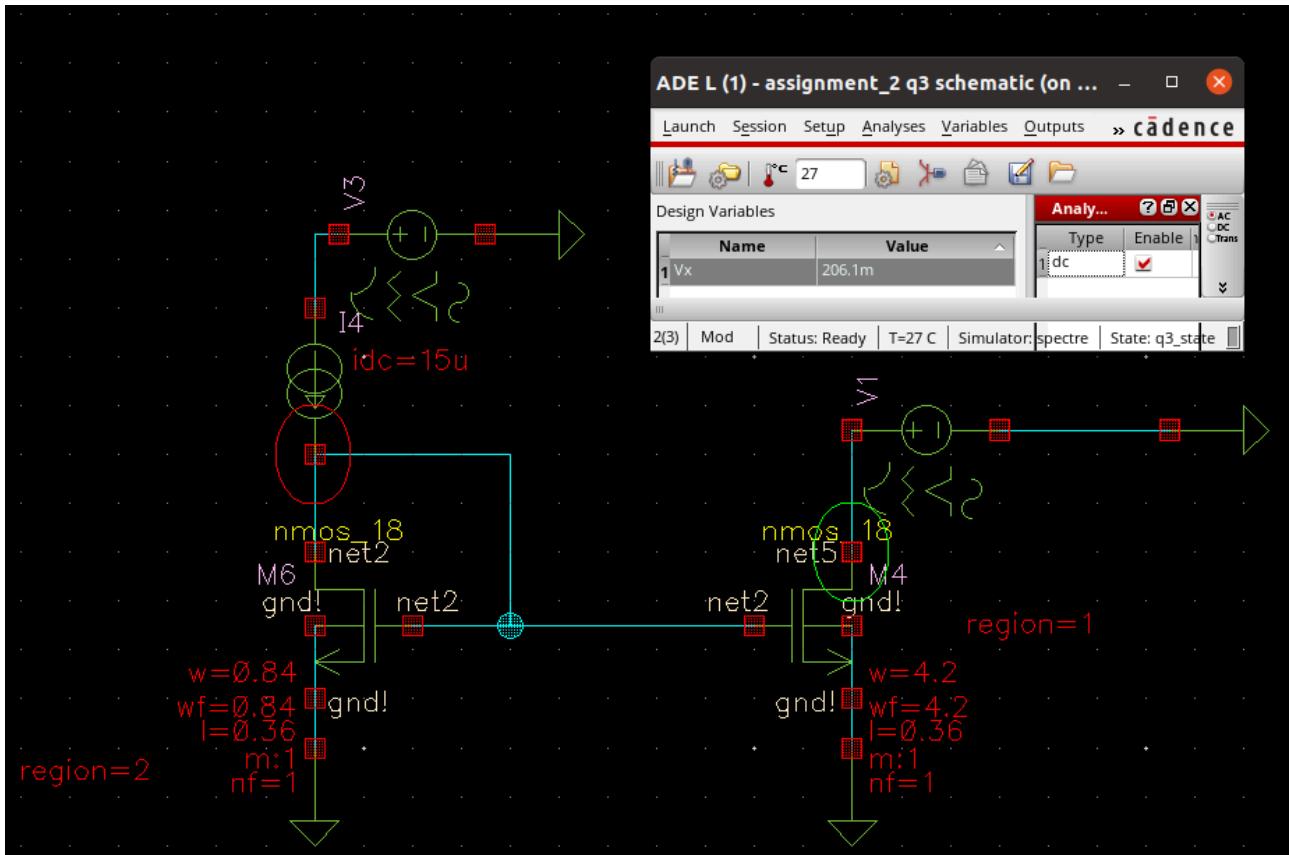




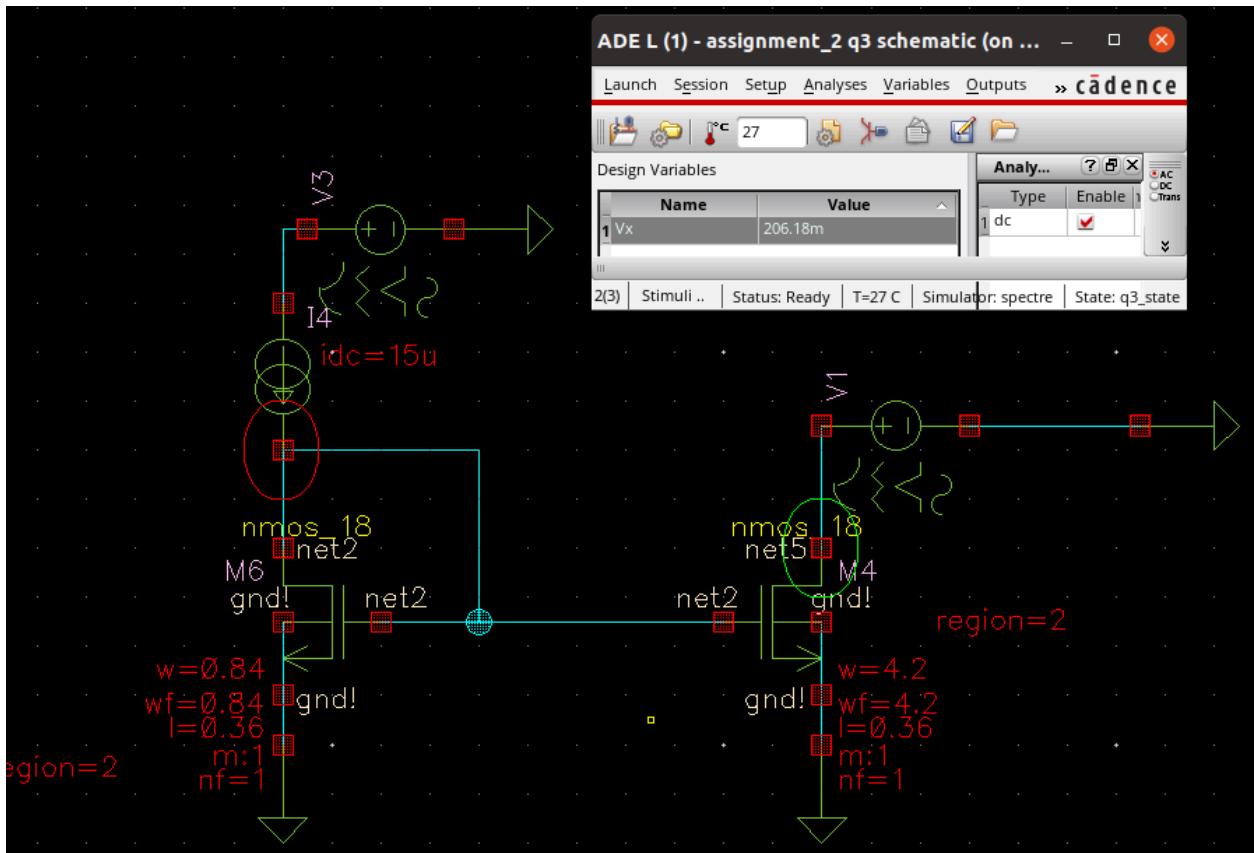
Finally i choosen the 3rd iteration

## 2b) calculating the saturation point

1st plot

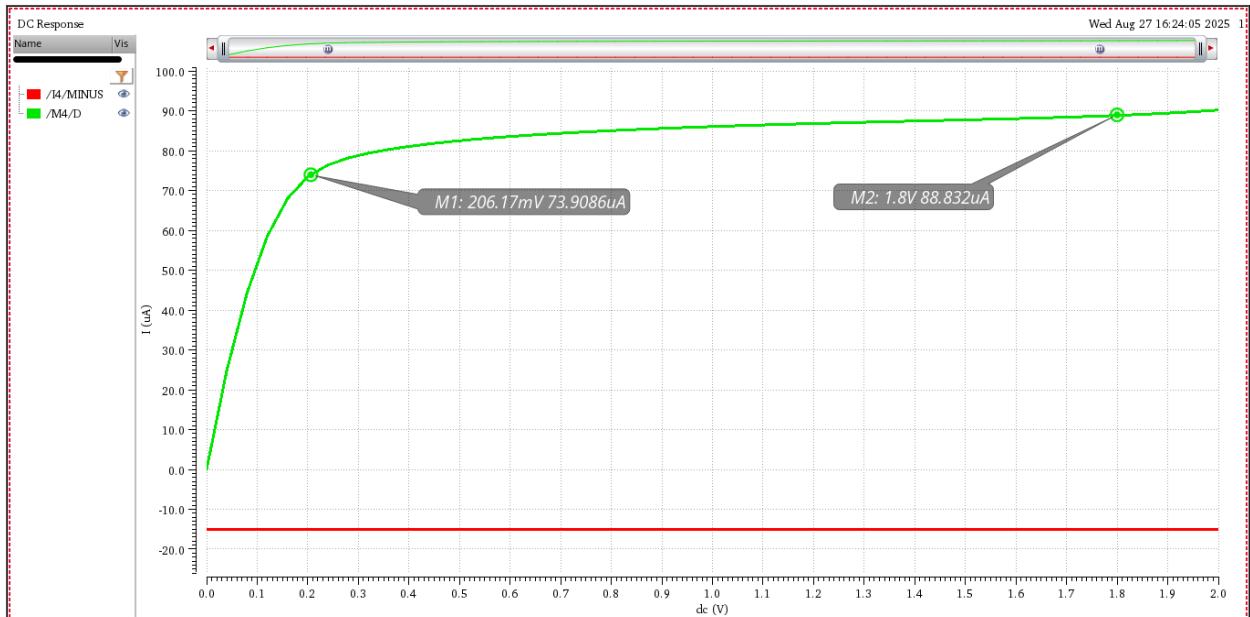


2nd plot



By the above two plots we can understand that we get Saturation point around 206.17mv(Vx)

## Determining percentage error

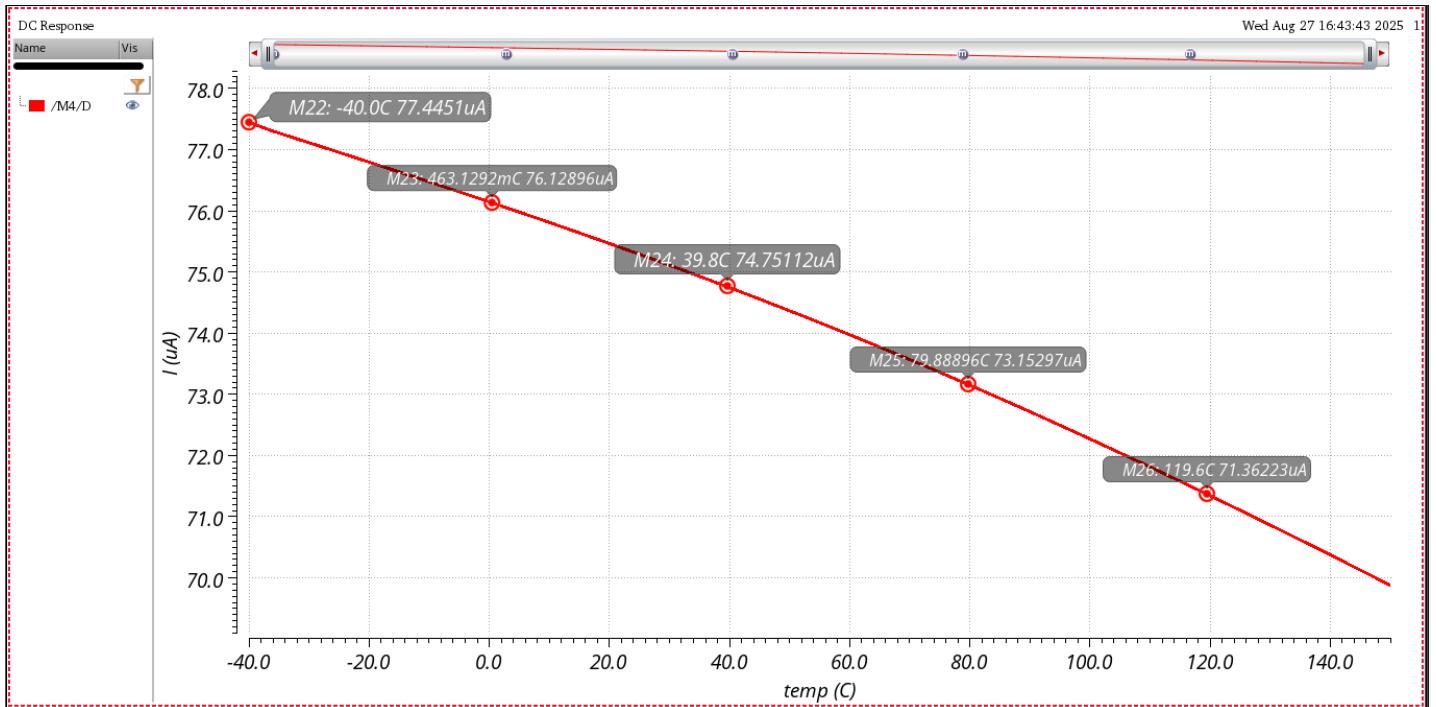


Voltage	Current(I)
0.206 V	73.9uA
1.8 V	88.83uA

$$\begin{aligned}\% \text{error} &= \frac{|I(1.8v) - I(\text{end of sat})|}{I(1.8v)} \times 100 \\ &= \frac{|88.83 - 73.9|}{88.83} \times 100 = 16.9\%\end{aligned}$$

## 2c) Temperature variation

Now i am fixing the Vx as 220.92mv (as you can see the 3rd iteration at voltage where we are getting 75uA)



$$ID \propto \mu(T)(VGS - VTH(T))^2$$

=> Mobility ( $\mu$ ) decreases with temperature (due to phonon scattering), which reduces current as temperature increases.

- Mobility and Temperature Relationship

The mobility ( $\mu$ ) of carriers (electrons/holes) in a MOSFET channel depends strongly on temperature (T) due to scattering mechanisms.

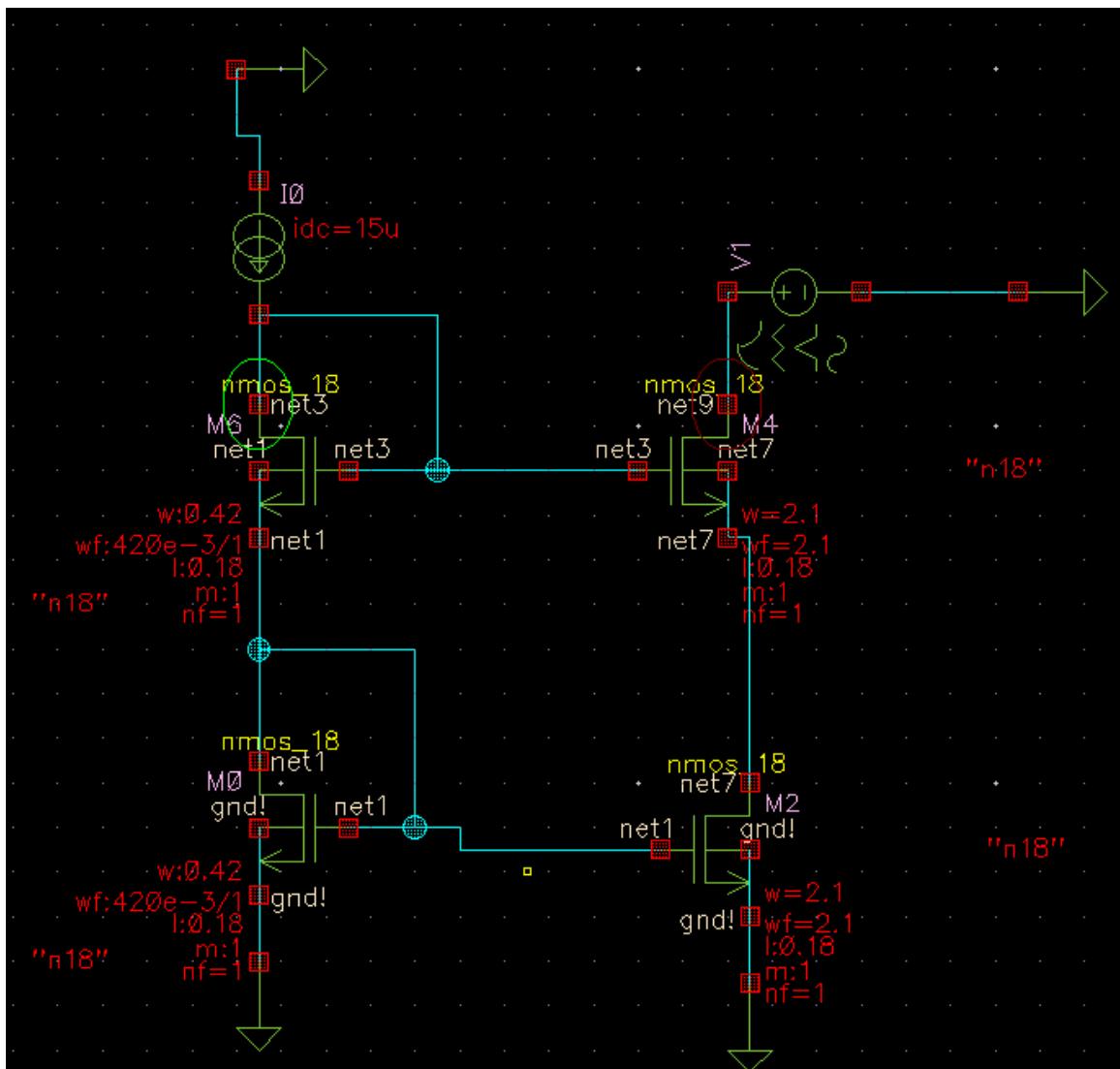
$$\mu(T) \propto T^{-m}$$

$m$  is a constant which is different for elec, holes

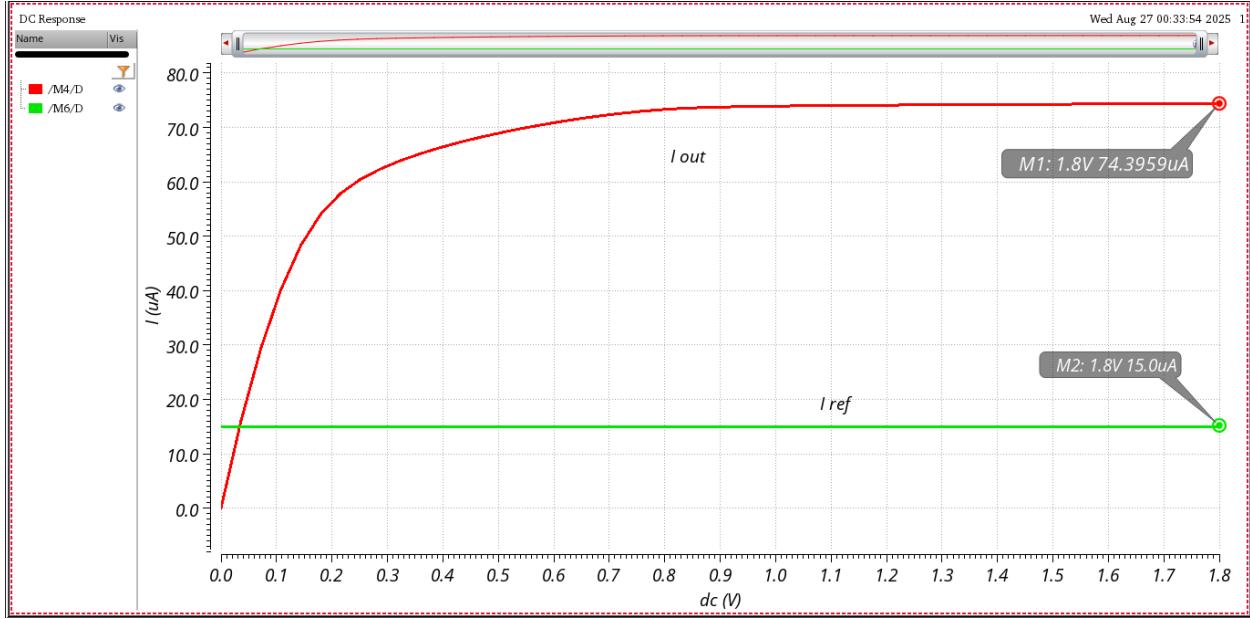
=> This might be one factor in reducing the current

### 3rd Question

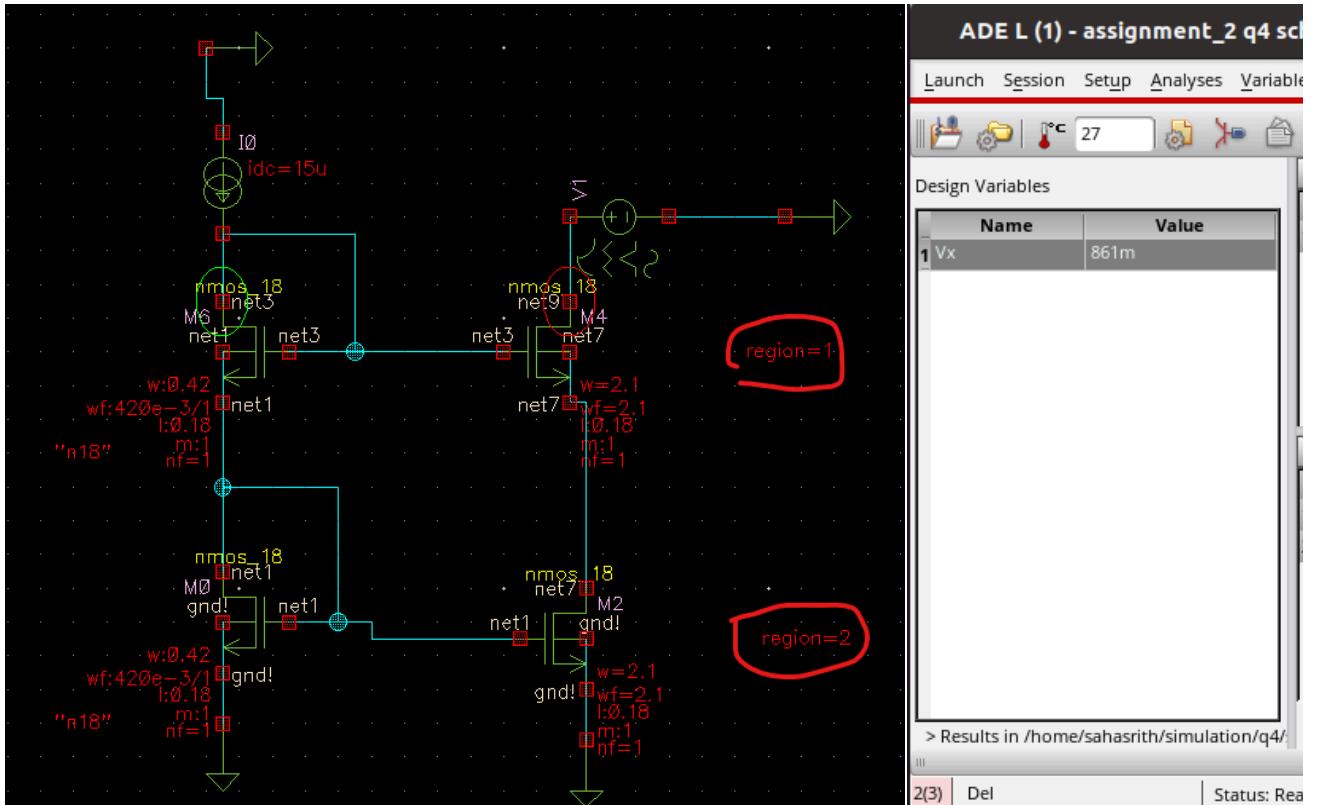
3a)

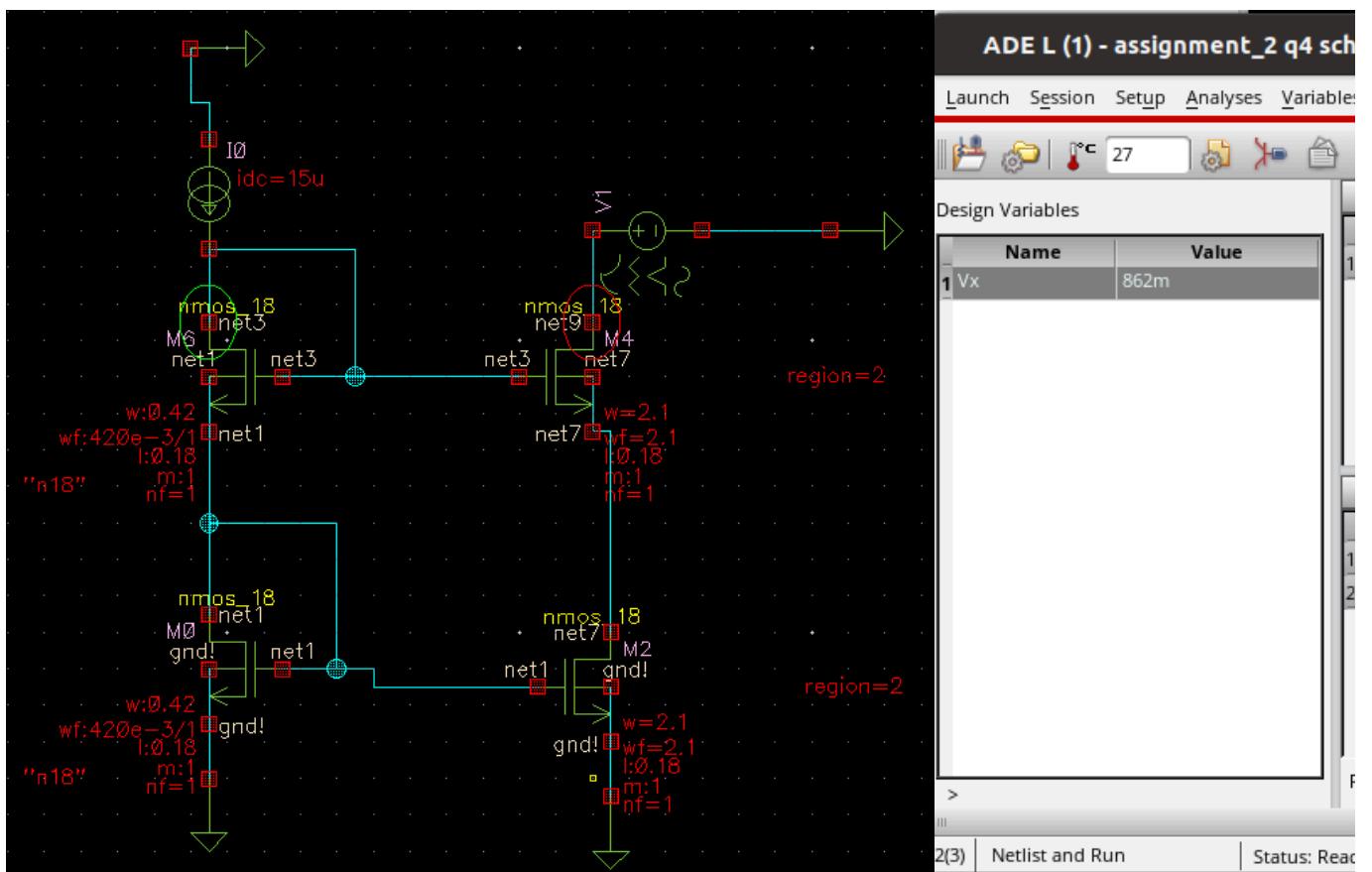


Vary the voltage at the drain of M3 from 0 to VDD (DC Sweep Simulation) and plotting the current vs Vx:



3b) Find the minimum voltage at the drain of M3 to ensure both M3 and M2 remain in saturation.



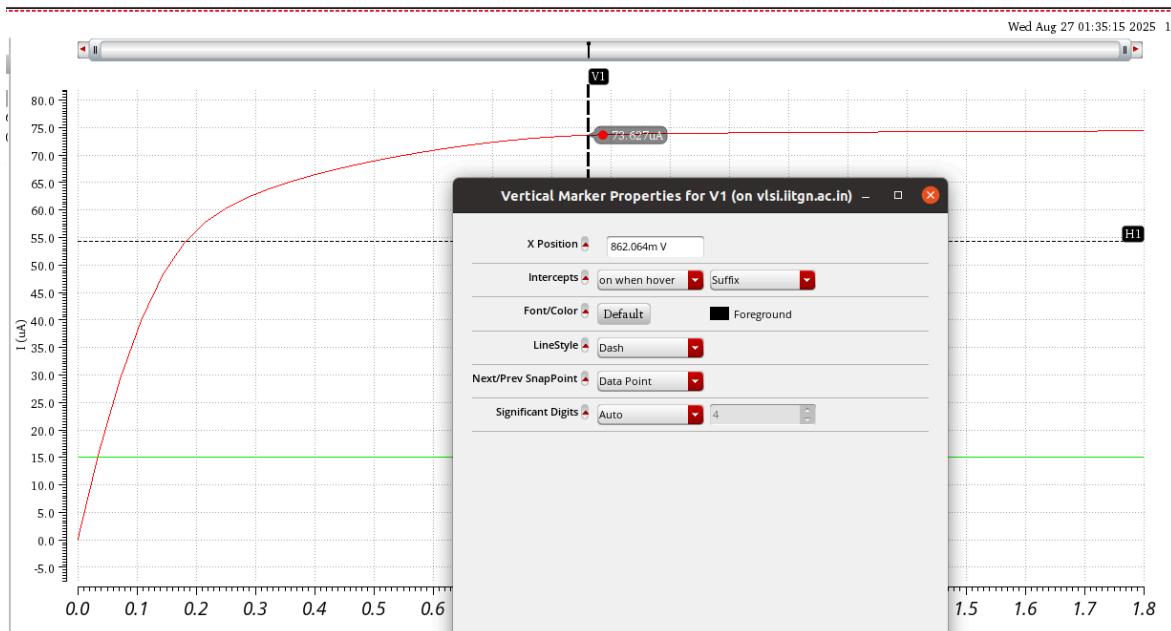


By the above two plots we can understand that we get Saturation point around 0.862mv( $V_x$ )  
This is the minimum voltage to keep both in saturation

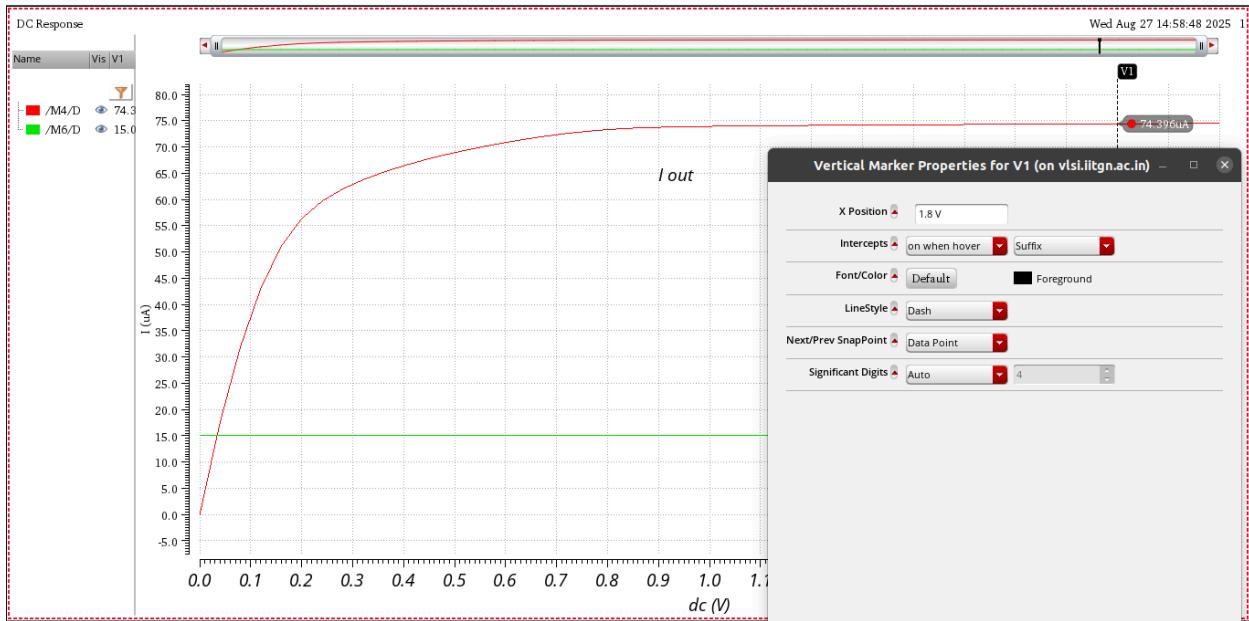
### 3c) Determine the percentage error in $I_{out}$ with $I$ at edge of saturation

Now i am fixing the  $V_x$  as 0.862mv

Current at 0.862v = 73.627



Current at 1.8v = 74.396

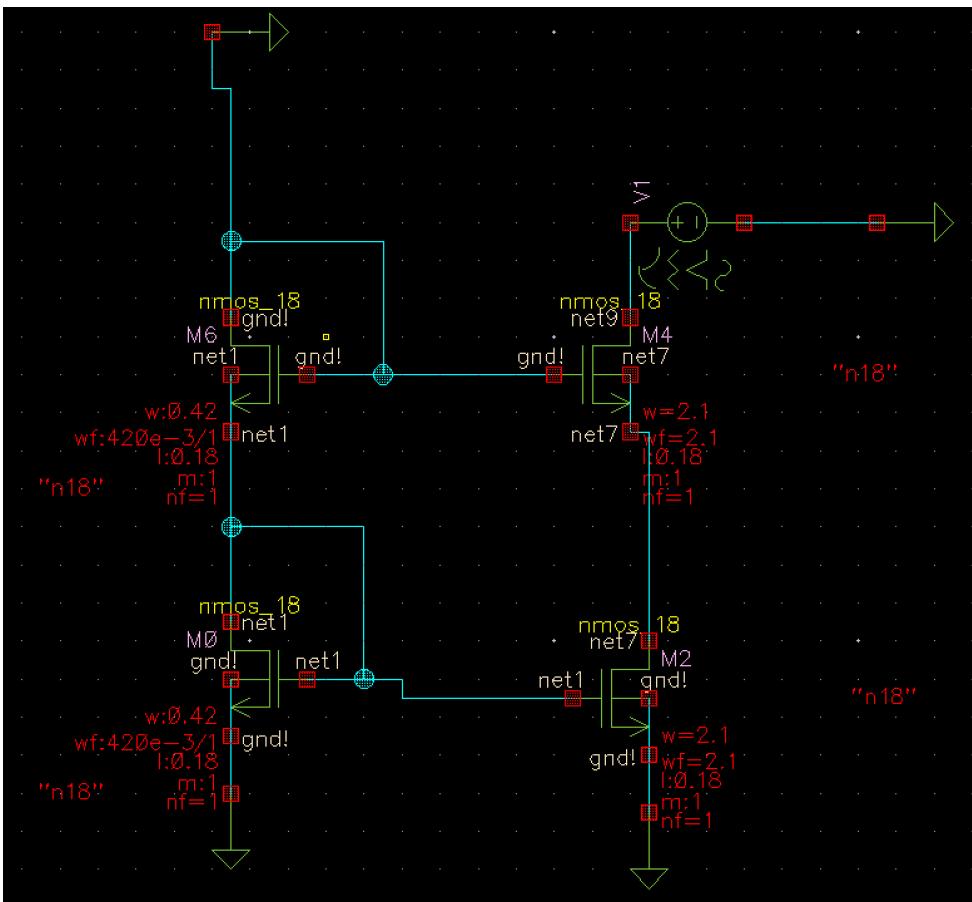
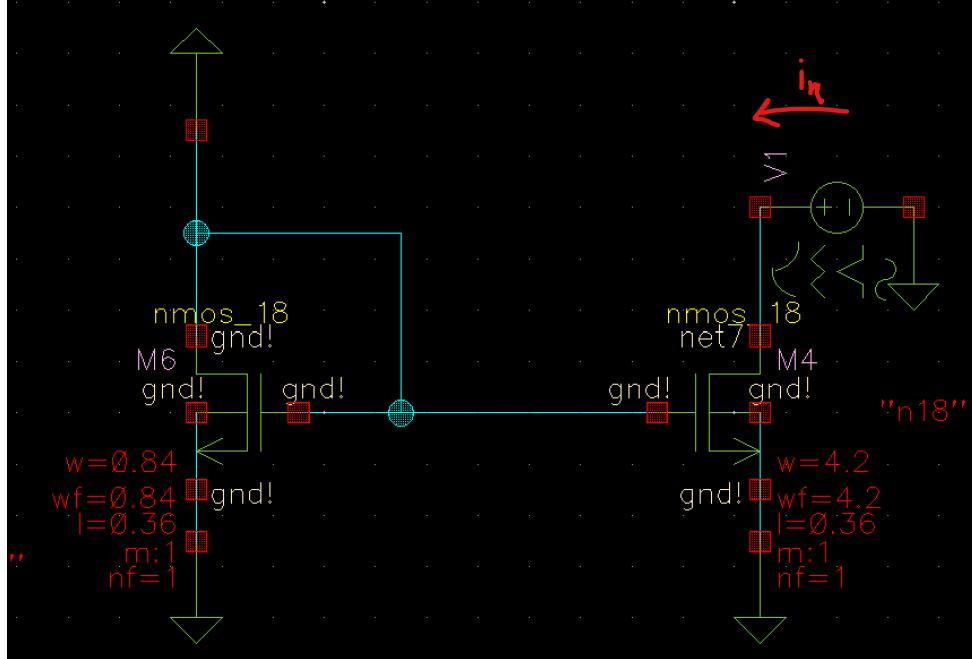


Voltage	Current(I)
<b>0.862 V</b>	<b>73.627uA</b>
<b>1.8 V</b>	<b>74.396uA</b>

$$\begin{aligned} \%error &= \frac{|I(1.8v) - I(\text{end of sat})|}{I(1.8v)} \times 100 \\ &= \frac{|74.396 - 73.627|}{74.396} \times 100 = 1.033\% \end{aligned}$$

4Q)

## Comparing Q2 (Simple Current Mirror) and Q3 (Cascode Current Mirror)



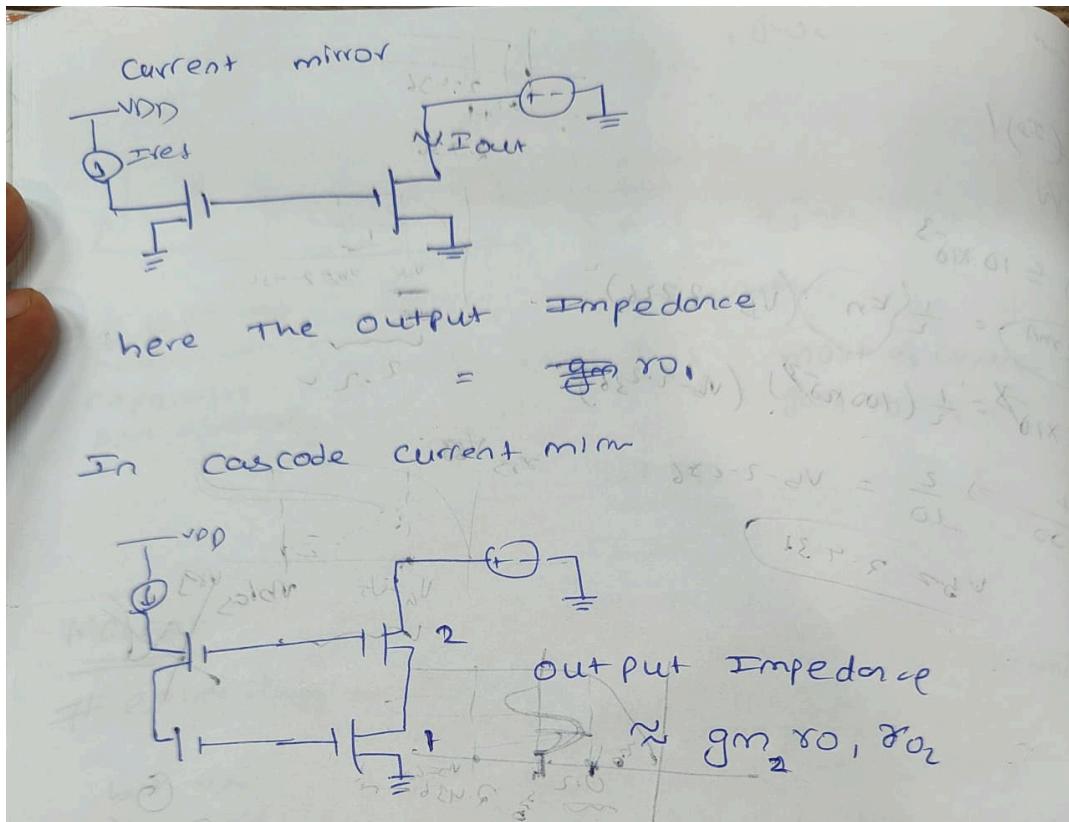
Basically i removed the current source from the 2ques circuit, 3 ques and excited a vsource ( $V_x$ ) across drain of second mosfet and calculating

$$\text{Output impedance} = V_x / i_x$$

$$\text{Output imp of 2nd ques} = \frac{1}{8.29997 \times 10^{-12}} = 12048236318.92 = 1.2 \times 10^{10}$$

$$\text{Output imp of 3rd ques} = \frac{1.2}{3.16635 \times 10^{-12}} = 378985266947.74 = 3.78 \times 10^{11}$$

### Concept and reasoning:



Why we need high o/p Impedance  $\Rightarrow$

here we need current source means  
should provide const current regardless  
of voltage  $v = IR$

$I = \frac{V}{R}$  when it's high

even when voltage fluctuations are  
there  $I$  don't change much

## Simple Current Mirror (Q2)

Advantages:

1. Simplicity: Uses fewer transistors (2), making it easy to design .
2. Lower Power Consumption and Smaller Area: Fewer devices generally means less power.

Disadvantages:

3. **Lower Output Impedance:** More variation in output current with changes in output voltage (less ideal current source). => Current can deviate due to transistor mismatches or voltage changes.
4. Affected more compared to cascode in channel-length modulation

## Cascode Current Mirror (Q2)

Advantages:

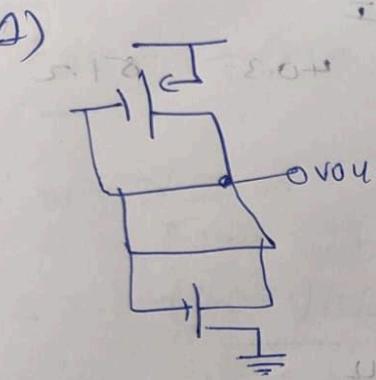
5. **High Output Impedance:** Much better at maintaining a constant current regardless of output voltage.
6. Less sensitive to channel-length modulation,

Disadvantages:

7. Complex design needed to tune various parameters of all mosfets to get desired output
8. Increased Power Consumption, Larger Silicon Area: More transistors increase power use.

1Q)

a. Designing Voltage divider circuit with  $V_{out} = 0.25V_{DD}$

2) 

$$I_1 = I_2 \xrightarrow{L = 0.8 \mu m, \beta = 0.5 A/m^2} 0.5 A$$

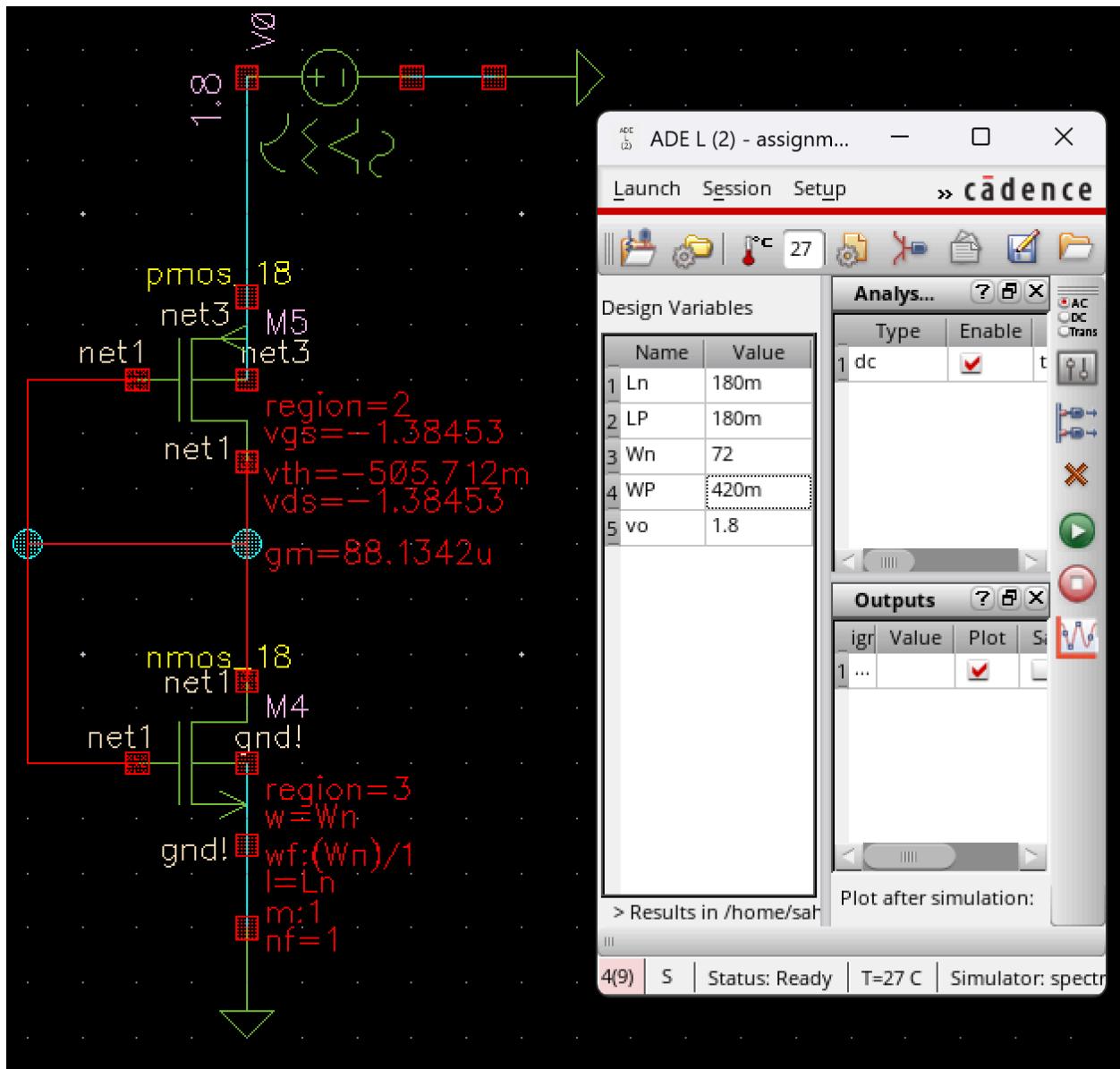
$$\frac{1}{2} (\mu_P C_{ox}) \left( \frac{W}{L} \right) (V_{DD} - V_{THP})^2 = \frac{1}{2} (\mu_N C_{ox}) \left( \frac{W}{L} \right) (V_{DD} - V_{TNP})^2$$

$$\frac{1}{2} (65) \left( \frac{W_P}{L_P} \right) (V_{DD} - V_{THP})^2 = (301) \left( \frac{W_N}{L_N} \right) (V_{DD} - V_{TNP})^2$$

approx  $V_{THP} = 0.5 + 0.6$   $V_{TNP} = 0.48$

$$\frac{W_P/L_P}{W_N/L_N} = \frac{(301)(V_{DD} - V_{TNP})^2}{(V_{DD} - V_{DD} - V_{out} - V_{THP})^2}$$

1st iteration



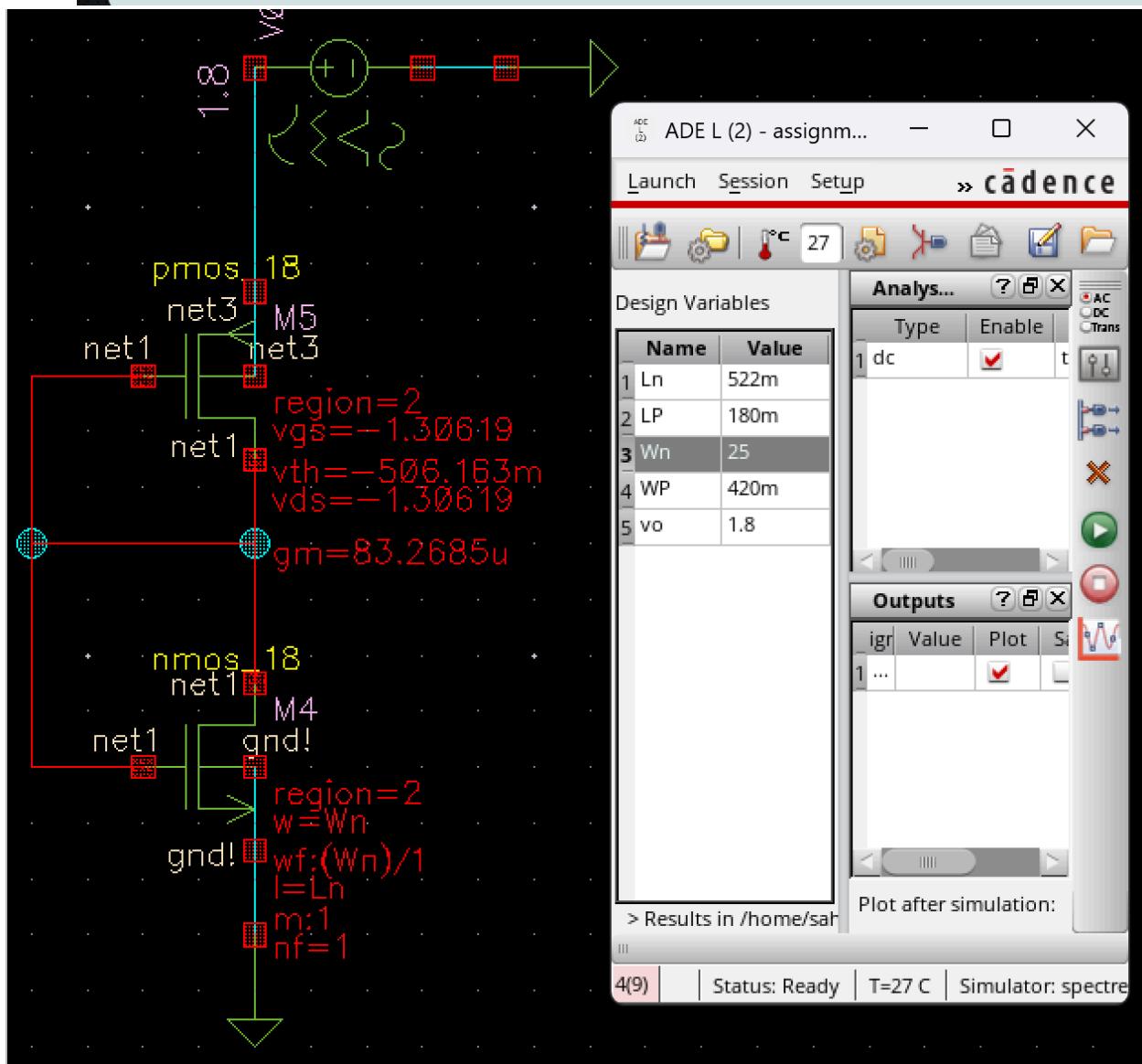
calculations:

$$Wn = \frac{65 \times (-0.45 + 1.8 - 0.5)^2}{301 \times (0.45 - 0.48)^2} \times 0.42 \\ \vdots \\ 72.810\ 077\ 519\ 38$$

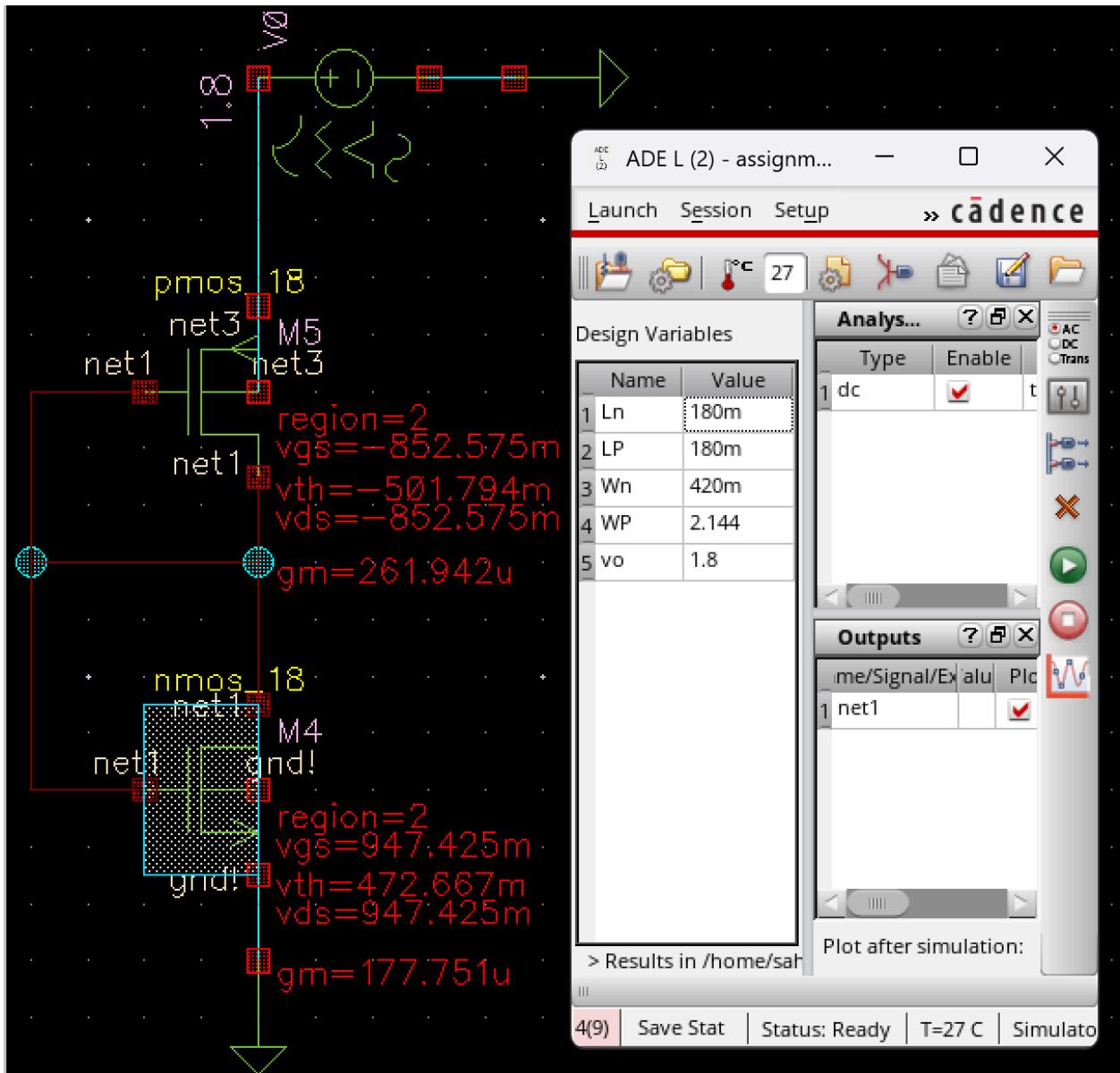
**The M4 mosfet in region 3 so i am tuning W,L such that M4,M5 in saturation**

2nd iteration (tuning the values to keep two mosfets in region 2)

$$W_n = \frac{65 \times (-0.45 + 1.8 - 0.5)^2}{301 \times (0.45 - 0.48)^2} \times \frac{0.42}{0.522} \times 0.18$$



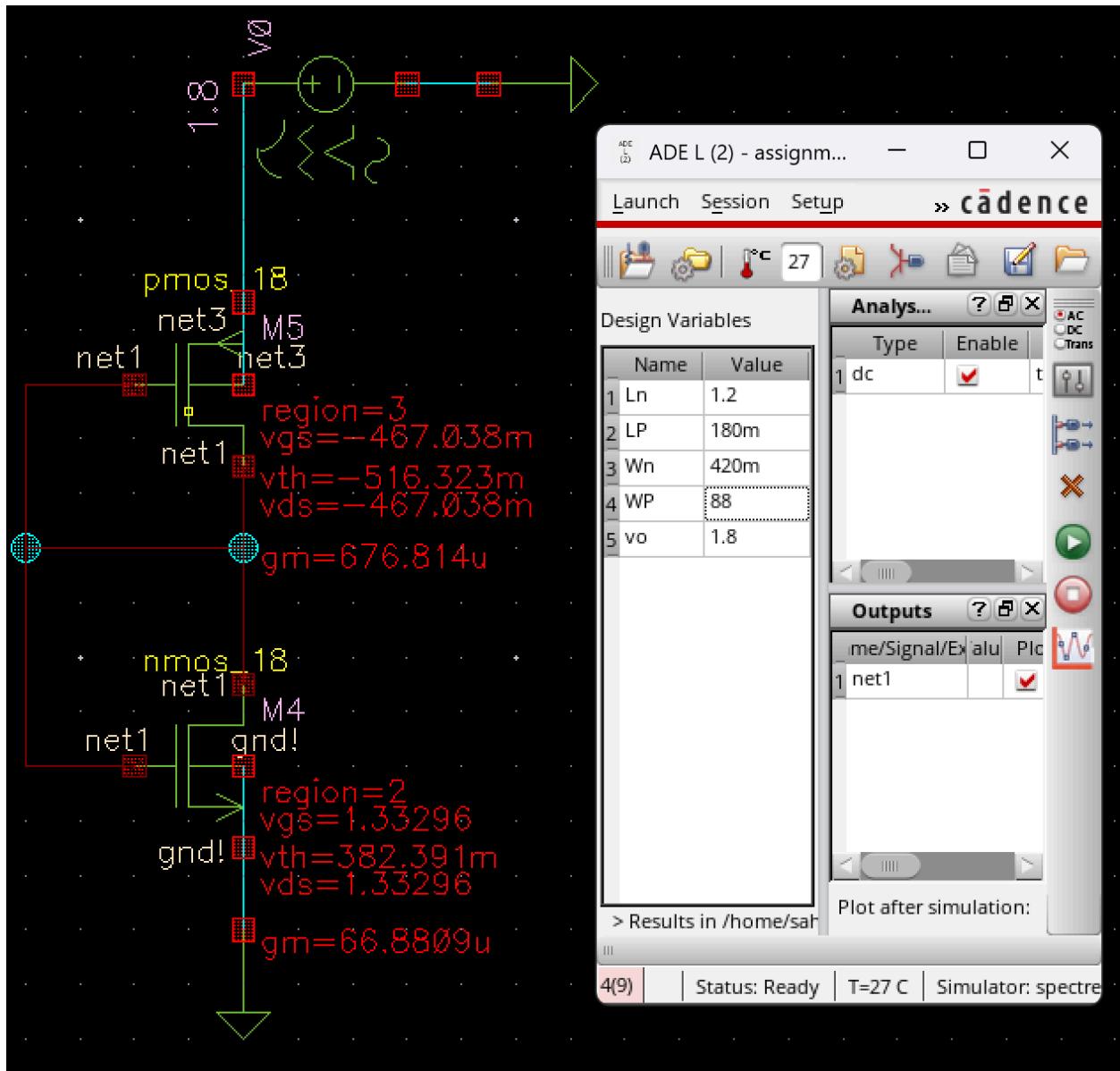
**b. Designing Voltage divider circuit with  $V_{out} = 0.5V_{DD}$**



$$65 \times \frac{(-0.9 + 1.8 - 0.5)^2}{301 \times (0.9 - 0.48)^2}$$

$$\begin{array}{r} 1 \\ \hline 0.195\ 870\ 153\ 16 \\ \times 0.42 \\ \hline \end{array}$$

c. Designing Voltage divider circuit with  $V_{out} = 0.75V_{DD}$



$$\left| \frac{65 \times (-1.35 + 1.8 - 0.5)^2}{301 \times (1.35 - 0.48)^2} \right| \\ \vdots \quad 0.000\ 713\ 260\ 81$$

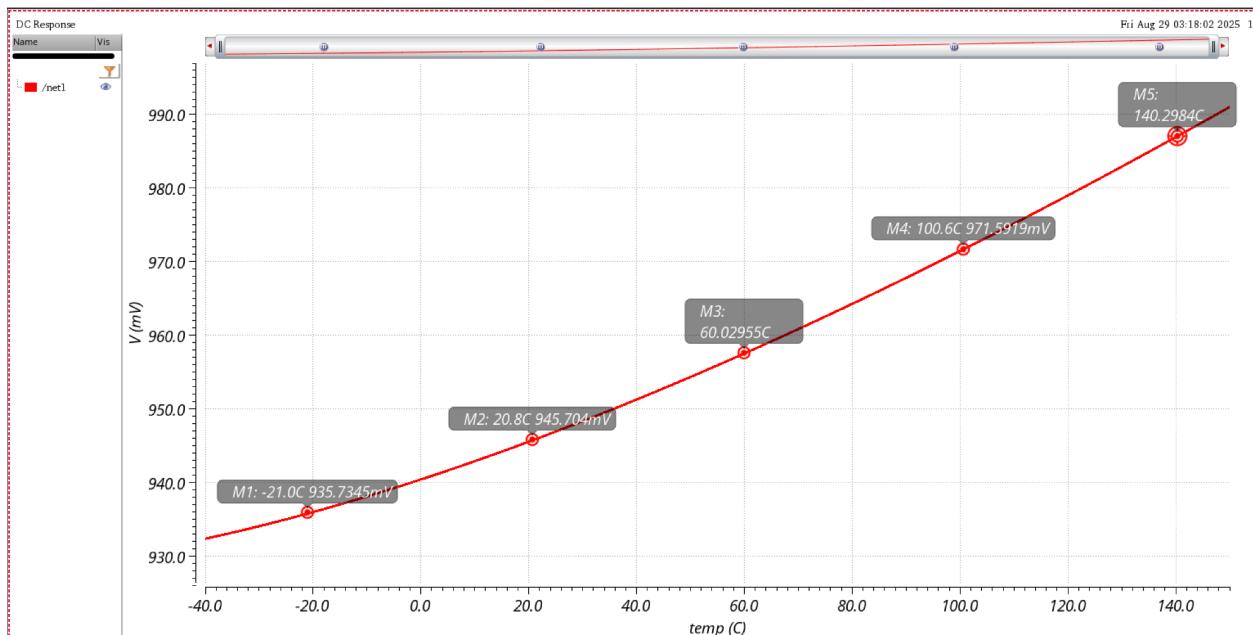
$$\frac{1}{0.000\ 713\ 260\ 81} \\ \vdots \quad 1\ 402.\ 011\ 698\ 918\ 38$$

$$\left(\frac{\omega_p}{L_p}\right) = (1402) \left( \frac{\omega_n}{L_n} \right)$$

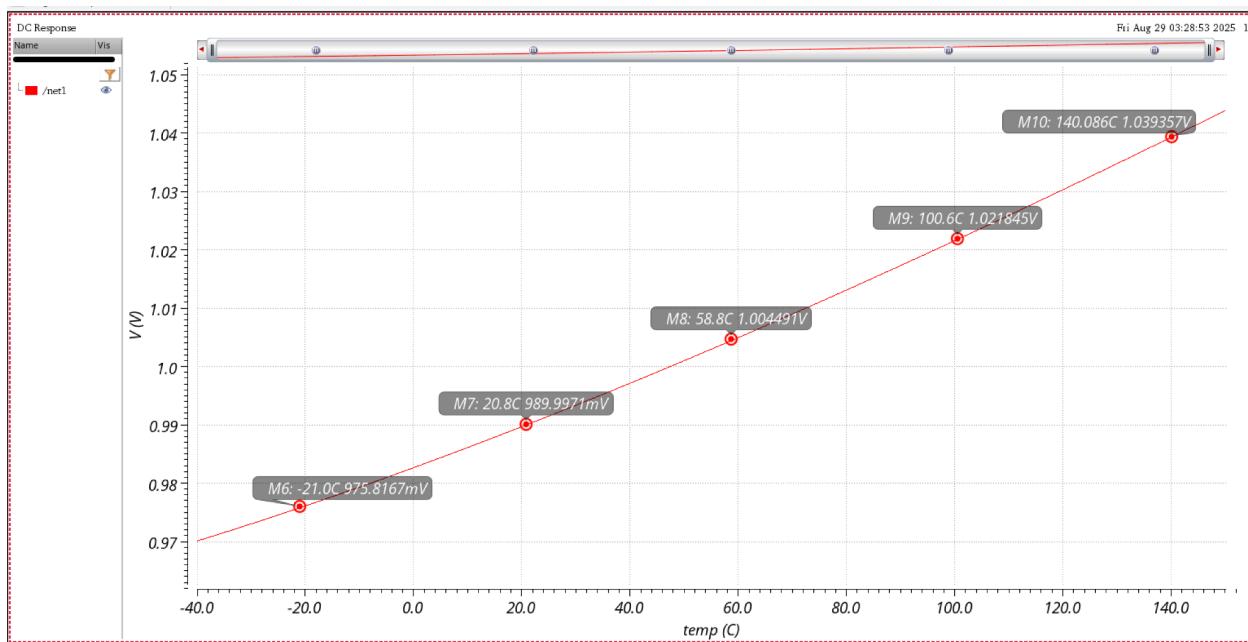
$$1\ 402.011 \times \frac{0.42}{1.2} \times 0.18 \\ \vdots \\ 88.326\ 693$$

**1b)**

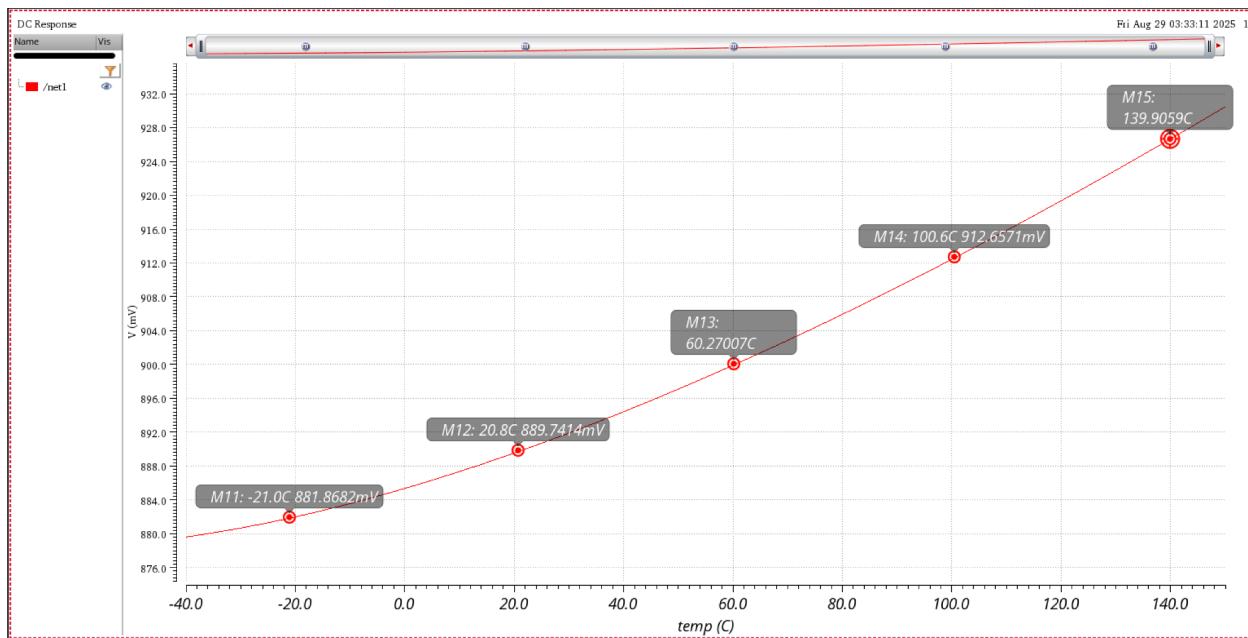
TT



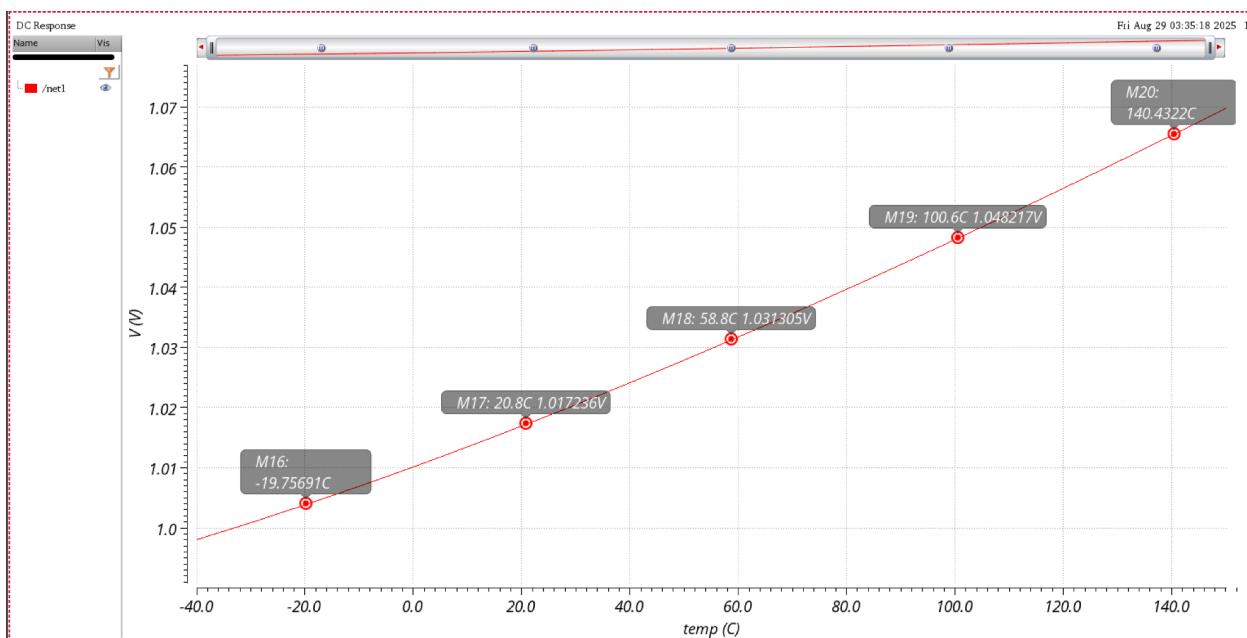
FF



FS



SF



SS

