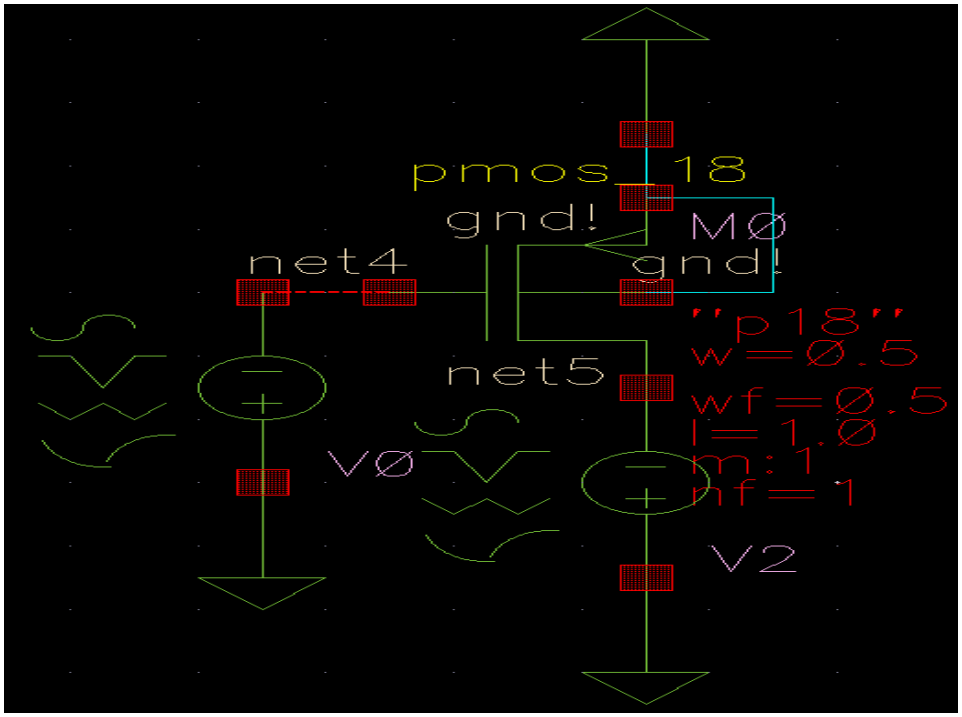
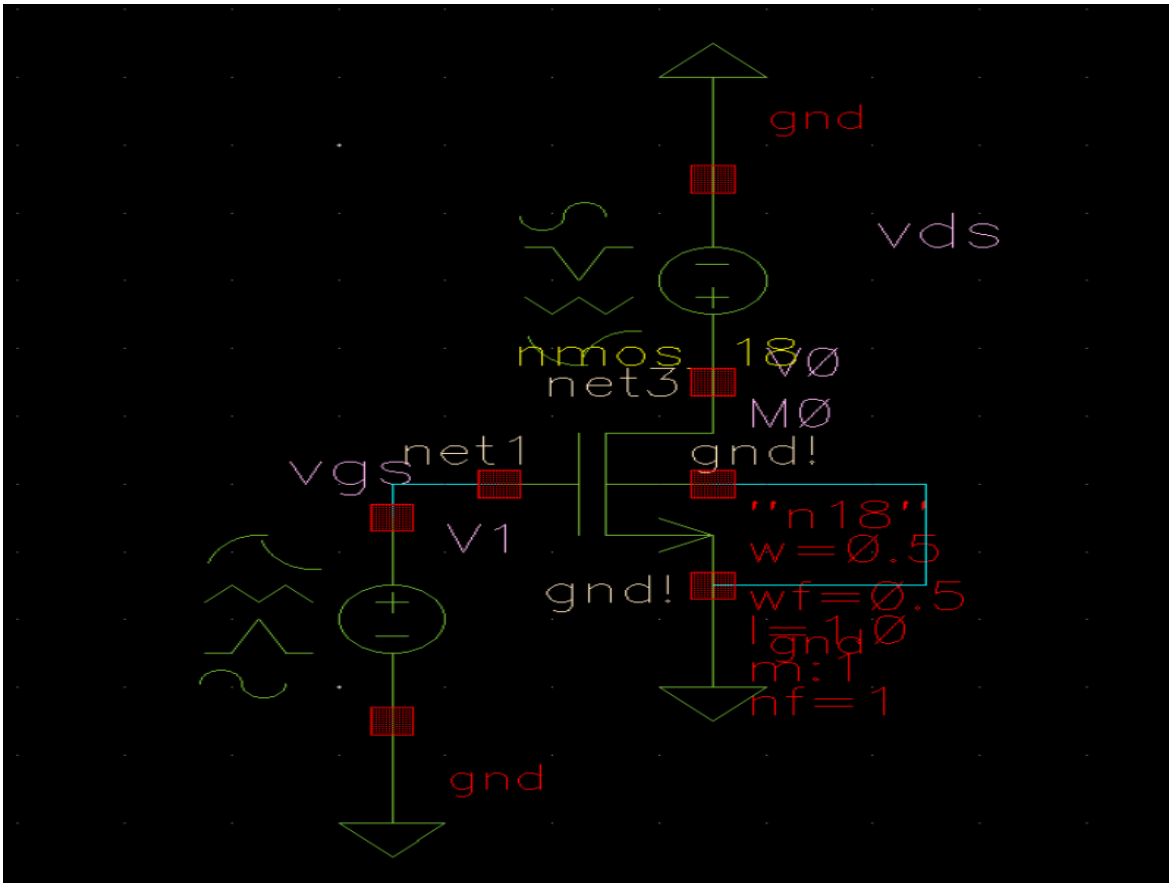
Analog CMOS IC Design (EE651)
23110064

1st Question

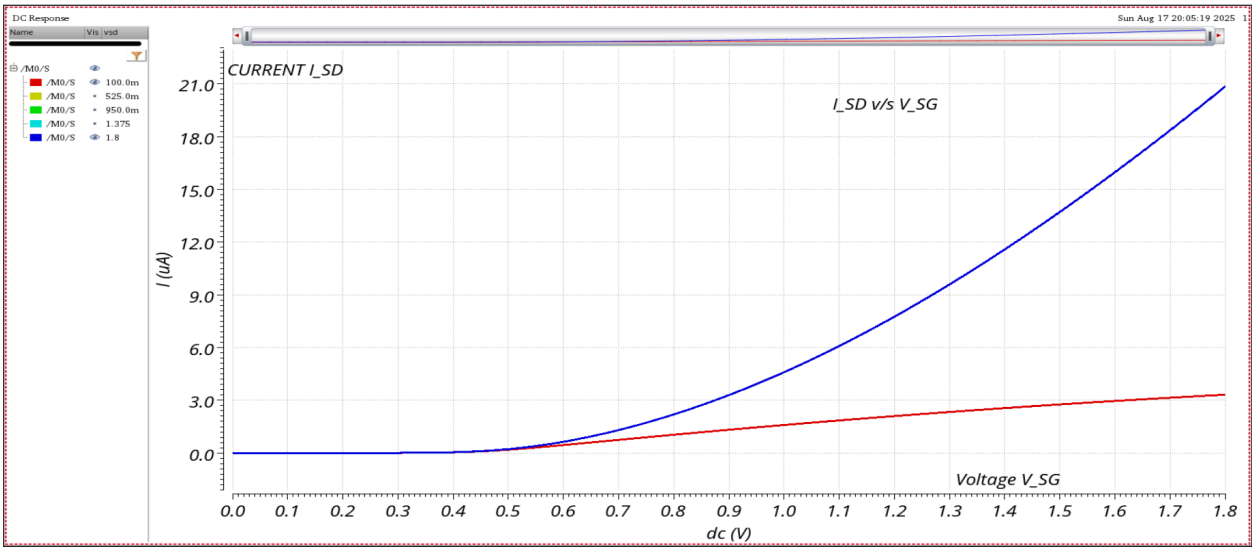
PMOS Schematic



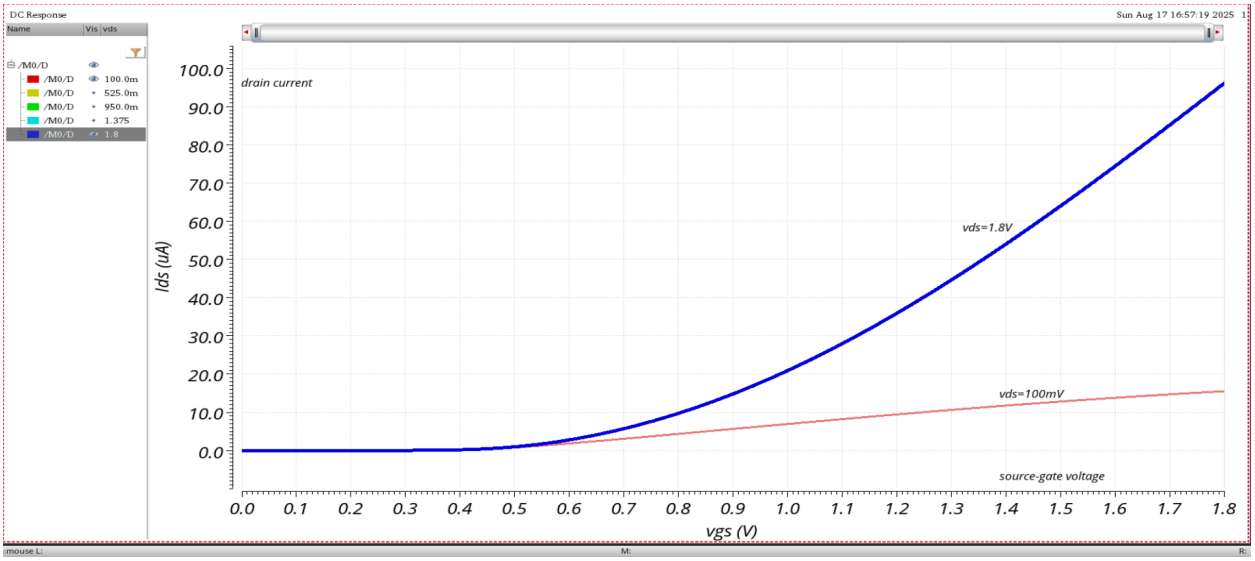
NMOS Schematic



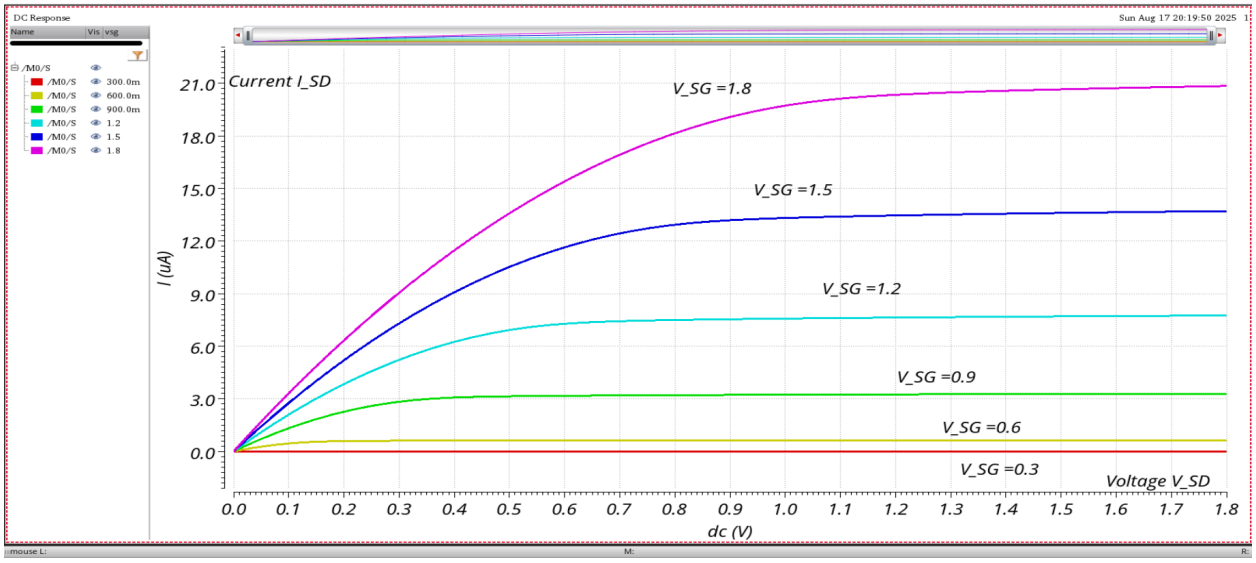
a)Transfer characteristics for P-type MOS Transistor:



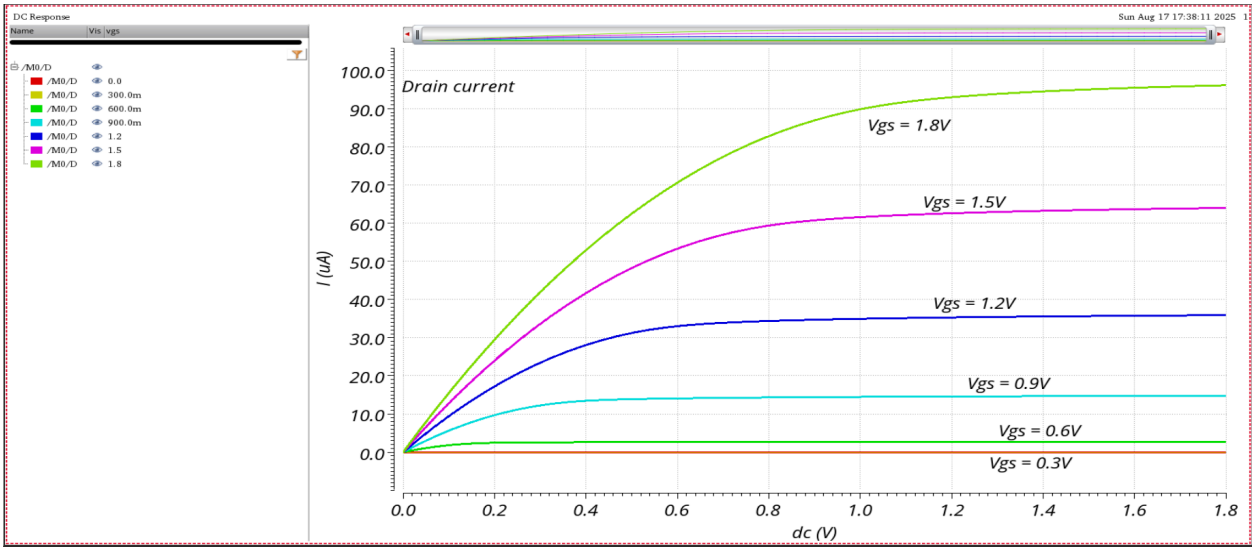
b)Transfer characteristics for n-type MOS Transistor:



c)Output characteristics for P-type MOS Transistor:



d)Output characteristics for P-type MOS Transistor:



Observations

Transfer Characteristics (ISD vs VSG):

- For both NMOS and PMOS devices, the transfer curves show that current remains very small in the subthreshold region and then increases rapidly once the applied gate bias exceeds the threshold voltage (VTH for NMOS, |VTP| for PMOS)
- the blue curve represents operation at VDS = 1.8V (saturation region), while the red curve corresponds to VDS = 0.1V (linear region). For both curves, as VSG (source-gate voltage) increases, the drain current ISD also increases. At low VSG, the current remains minimal due to the PMOS being off or in weak inversion. Once VSG exceeds the

threshold voltage, ISD rises much more steeply for the blue (high VDS) curve, indicating enhanced carrier injection and strong channel formation typical of the saturation regime.

- The red curve shows a more gradual increase in current for low VDS, demonstrating resistive behaviour in the linear region.

$$I_{SD} = \mu_p C_{ox} \frac{W}{L} \left[(V_{SG} - |V_{th}|) V_{SD} - \frac{1}{2} V_{SD}^2 \right]$$

For low VDS values, the quadratic term becomes negligible,so it shows resistive behavior

$$I_{SD} \approx \mu_p C_{ox} \frac{W}{L} (V_{SG} - |V_{th}|) V_{SD}$$

- Overall, the transfer plot confirms that a higher drain-source voltage allows the MOS transistor to achieve larger drain current upon gate activation, aligning with standard MOSFET theory.

Output Characteristics (ISD vs VSD for Various VSG):

- At low VSD, the transistor operates in the linear (ohmic) region. Here, ISD increases almost linearly with VSD for each VSG, reflecting the equation:

$$I_{SD} \approx \mu_p C_{ox} \frac{W}{L} (V_{SG} - |V_{th}|) V_{SD}$$

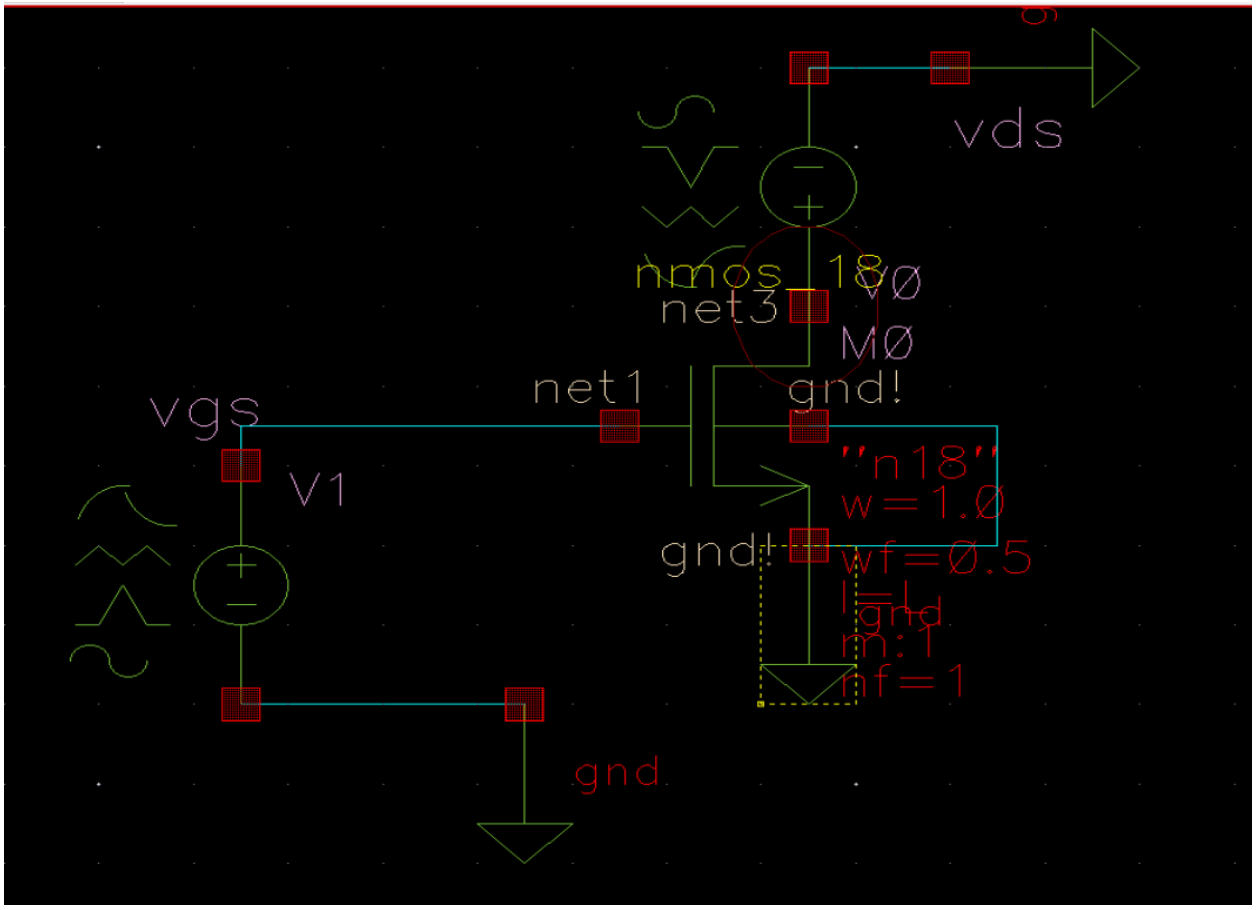
- As VSD increases and approaches $(VSG - |Vth|)$ the curves begin to bend and eventually saturate. In this saturation region, ISD becomes almost constant with further increases in VSD, described by:

$$I_{SD} = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} (V_{SG} - |V_{th}|)^2$$

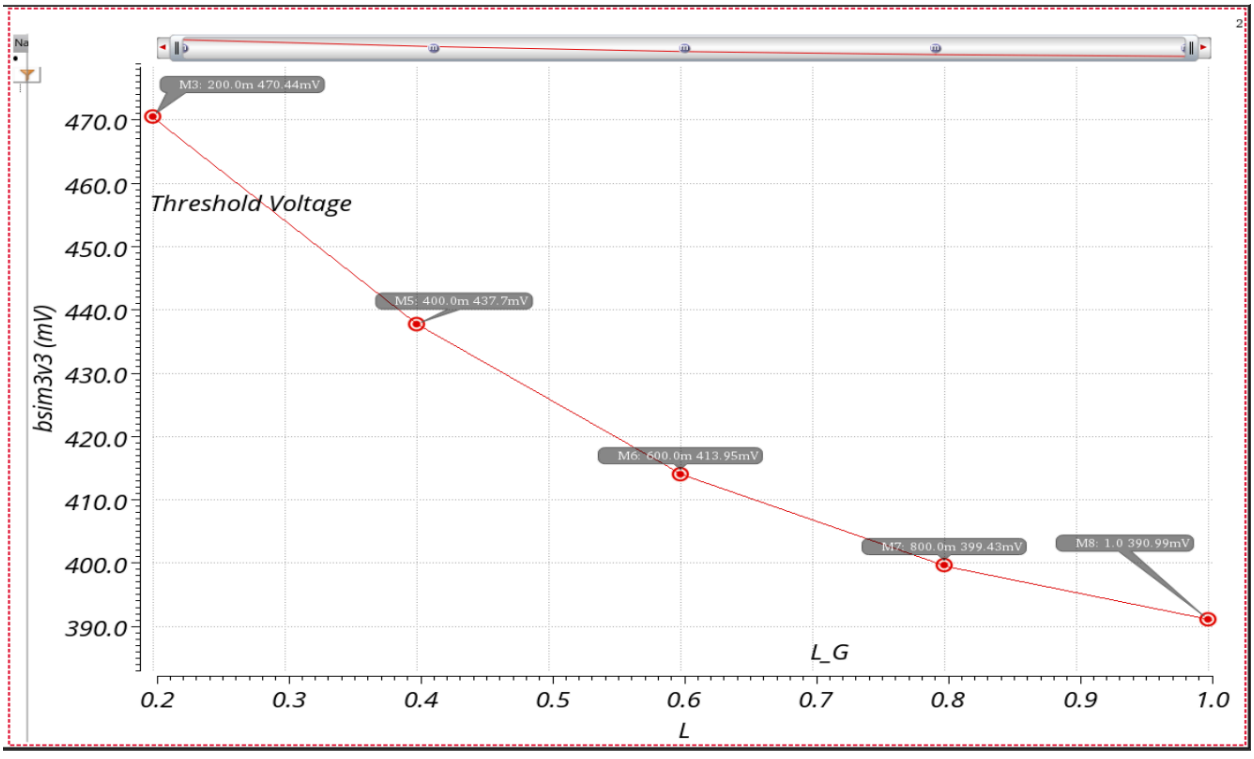
- The curves in this plot shift upward and to the right as VSG increases because a larger gate voltage,The rightward shift happens because the onset of saturation, marked by VSD = VSG – |Vth|, occurs at higher VSD values for higher VSG.
- In summary, higher VSG results in greater current and delays saturation, causing the curves to move up and right.

2nd Question

Schematic: NMOS



a)Threshold voltage v/s L for N-type MOS Transistor:



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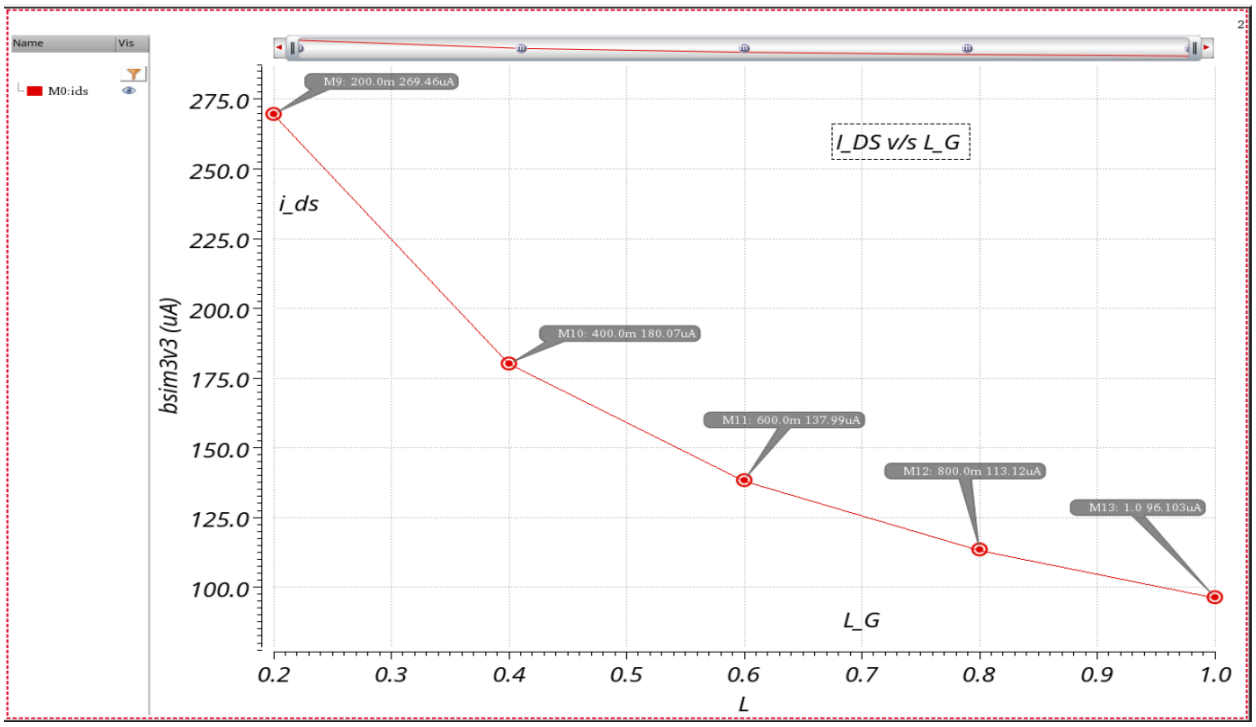
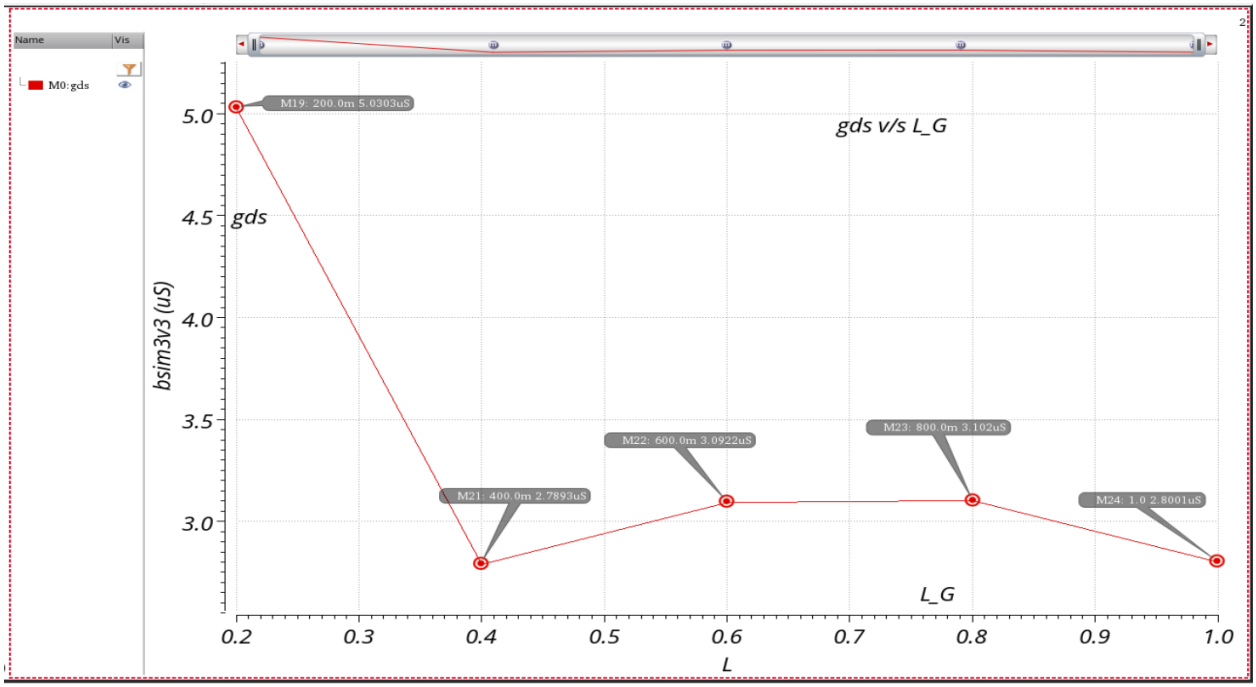
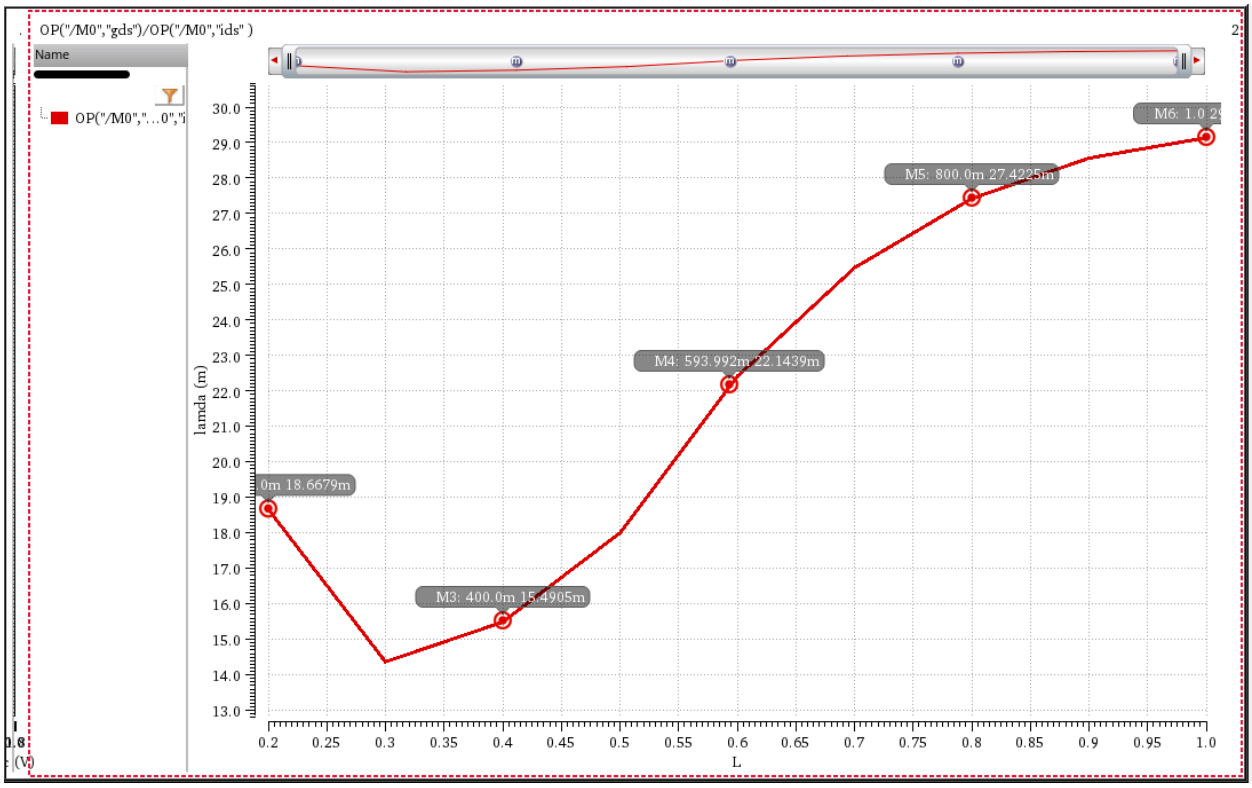


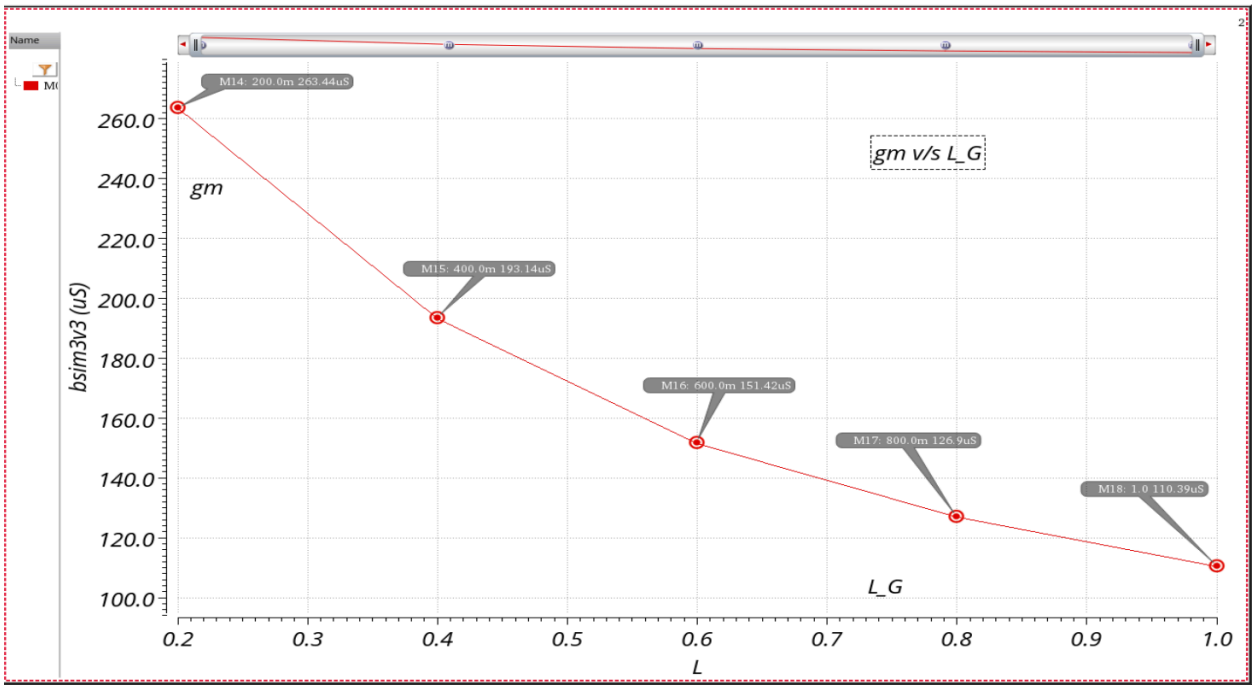
a) gds v/s L for N-type MOS Transistor:



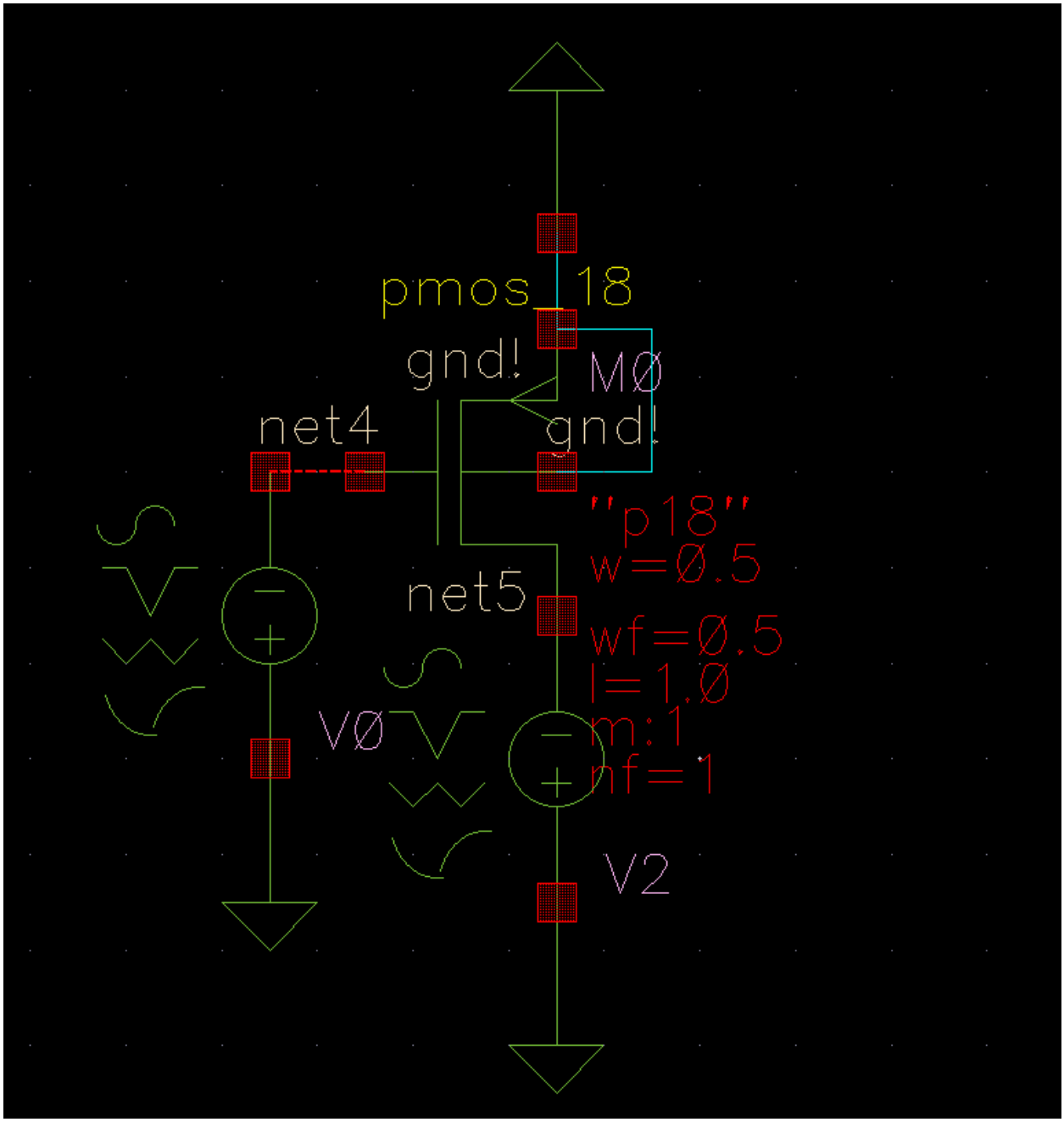
a) lamda v/s L for N-type MOS Transistor:



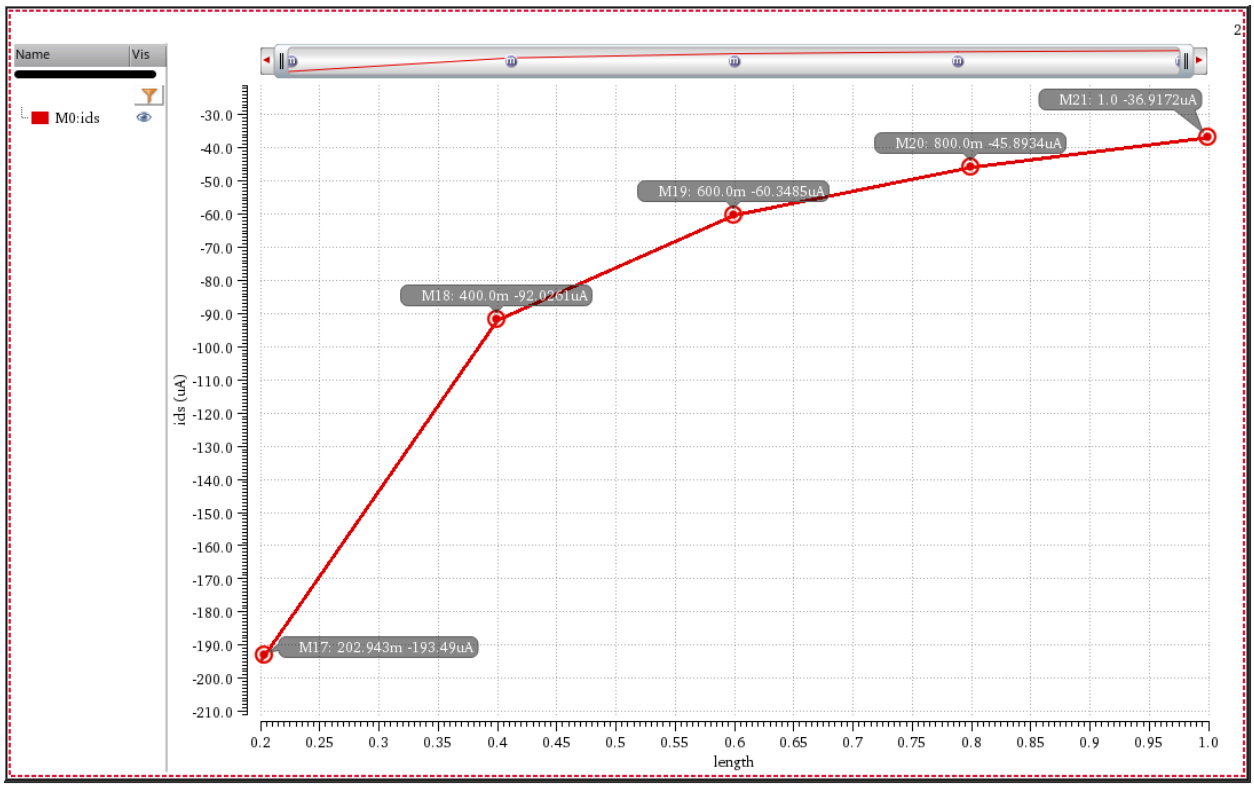
b)gm v/s L for N-type MOS Transistor:



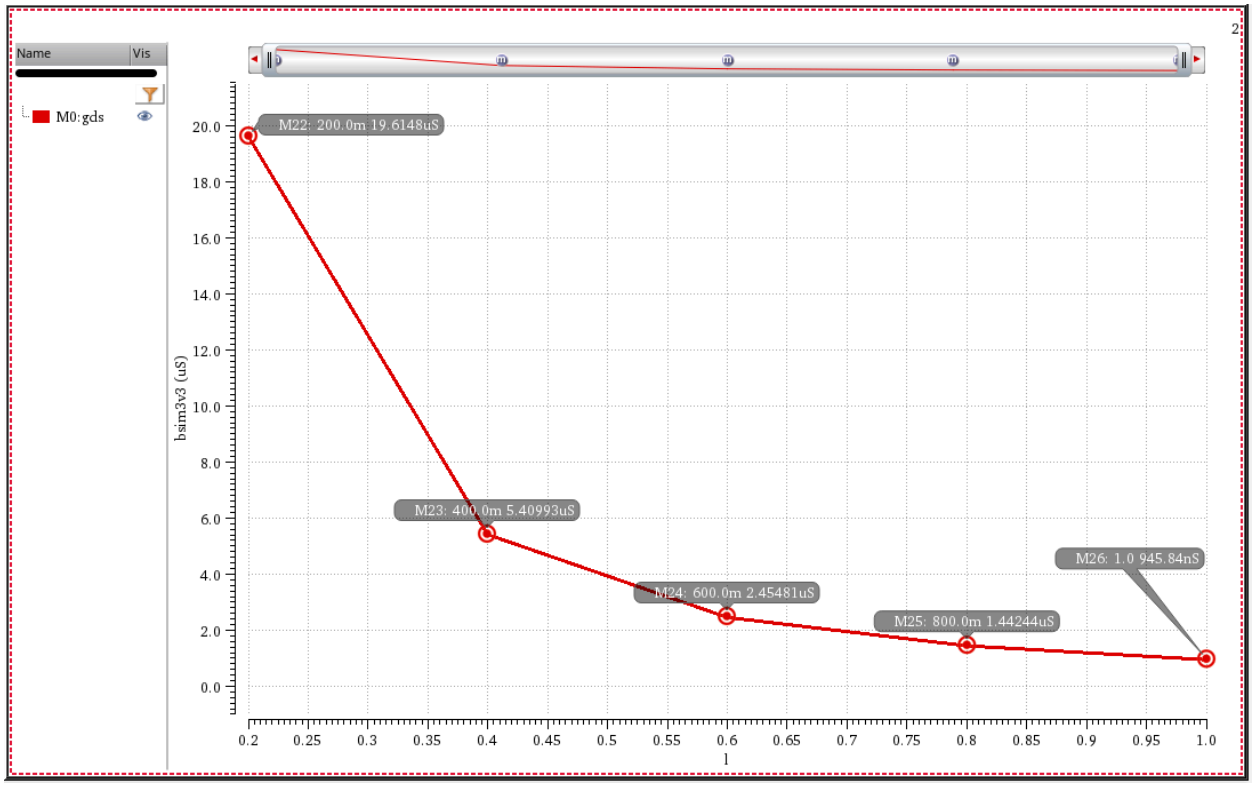
Schematic: PMOS



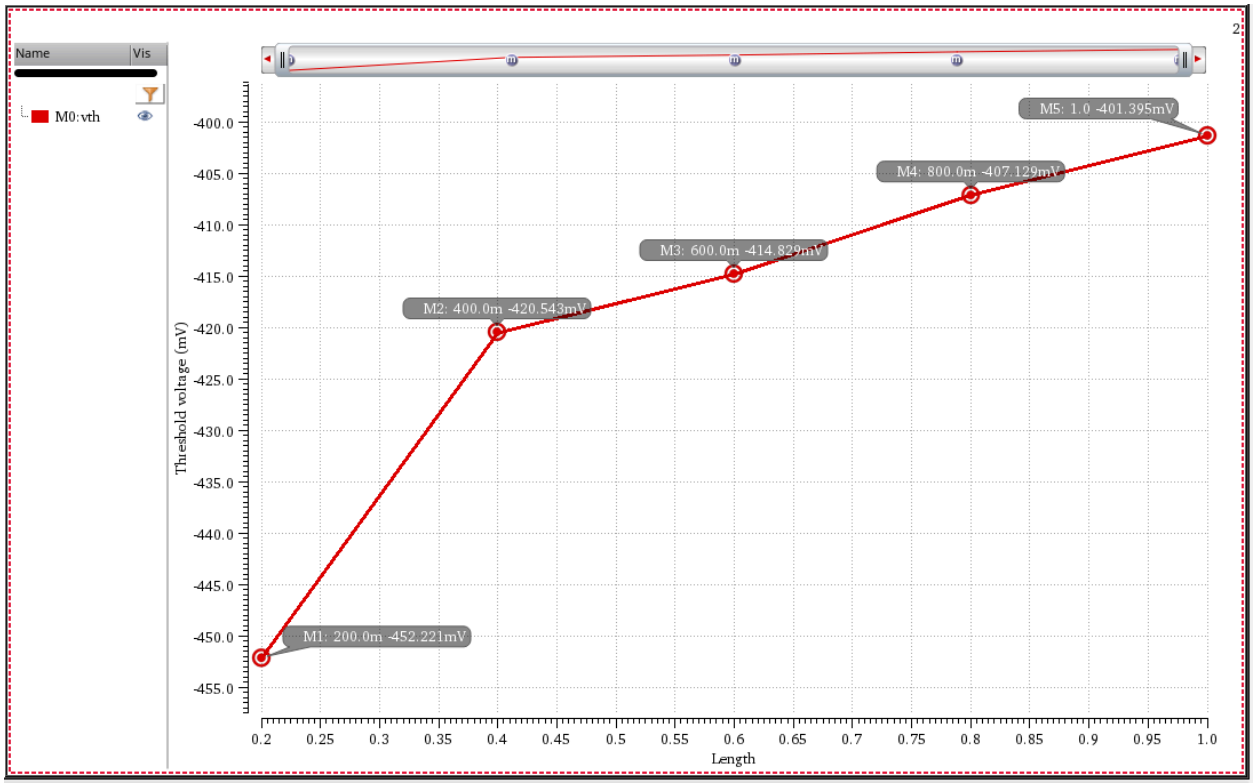
b) IDS v/s L for P-type MOS Transistor:



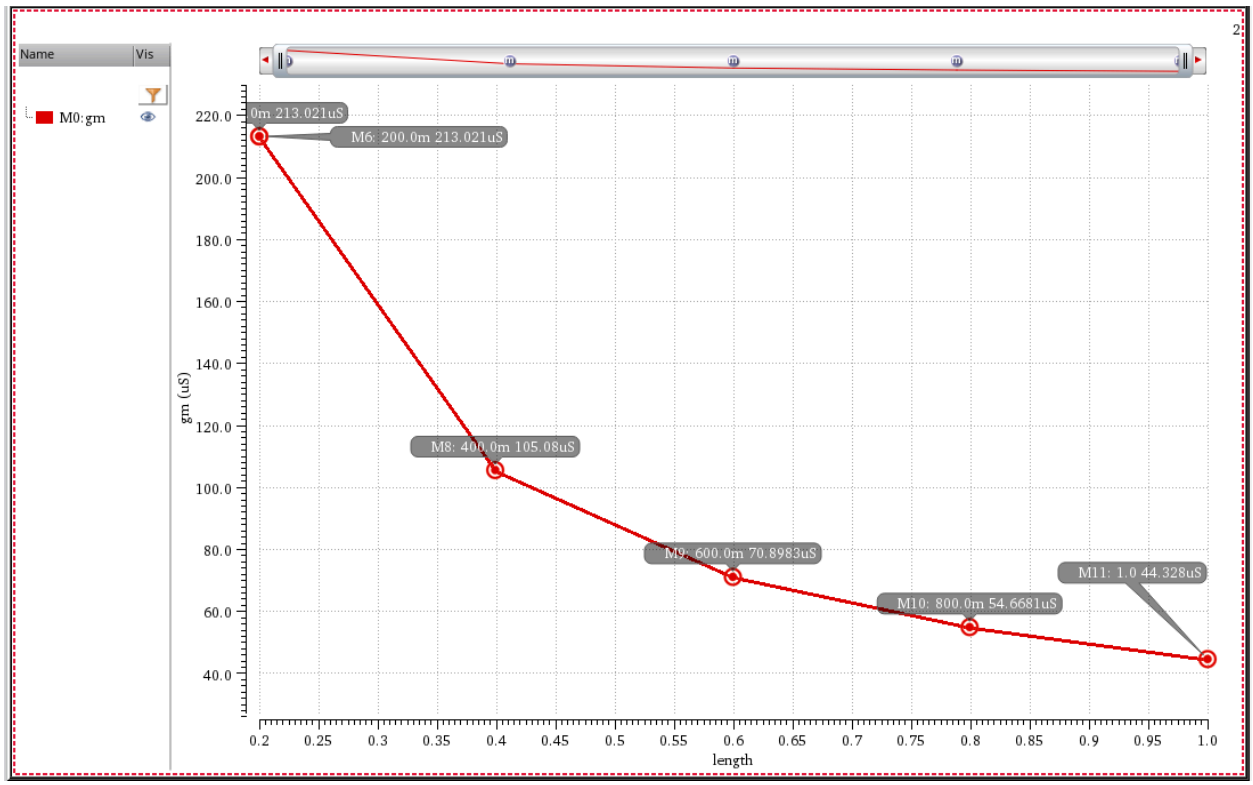
b) gds v/s L for P-type MOS Transistor:



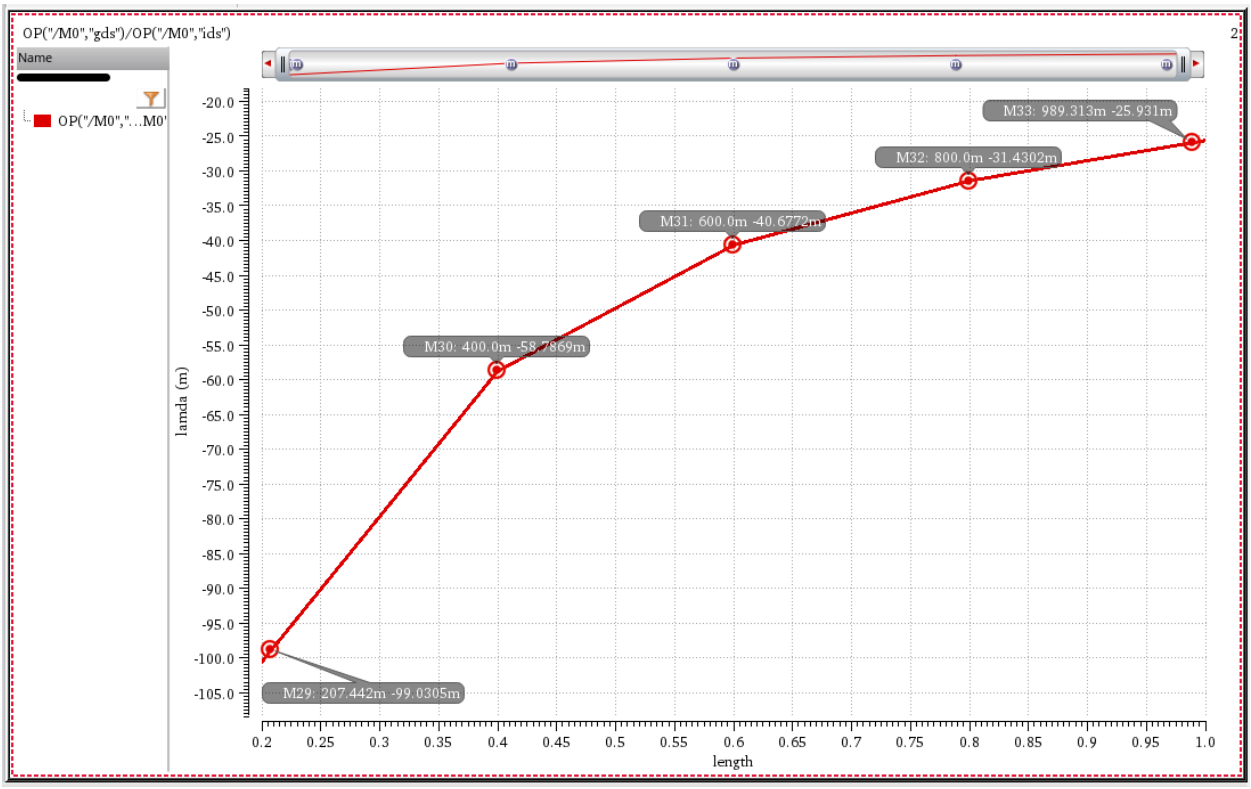
b)Threshold voltage v/s L for P-type MOS Transistor:



b) gm v/s L for P-type MOS Transistor:



b) lamda v/s L for N-type MOS Transistor:



OBSERVATIONS:

NMOS

Length	Vth(in mV)	Ids(µA)	gm(µS)	gds(µS)	λ(*10^-3) (V^-1)
200nm	470	269	263	5	18.6
400nm	437	180	193	2.7	15.4
600nm	413	137	151	3	22.14
800nm	399	113	126	3.1	27.4
1000nm	390	103	110	2.8	29.2

PMOS

Length	|Vth|(in mV)	|Ids|(µA)	gm(µS)	gds(µS)	|λ|(*10^-3)(V^-1)
200nm	452	193	213	19.6	99.03
400nm	420	92	105	5.4	58.78
600nm	414	60	70	2.4	40.67

800nm	407	45	54	1.4	31.43
1000nm	401	36	44	0.9	25.93

IDS vs LG:

Observation: Drain current decreases with increasing channel length.

$$I_{DS} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L_G}(V_{GS} - V_{th})^2$$

Here, IDS is inversely proportional to LG, so longer channels yield lower current for the same gate overdrive.

gm vs LG (Transconductance):

Observation: Transconductance falls as LG increases.

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \mu_n C_{ox}\frac{W}{L_G}(V_{GS} - V_{th})$$

Like drain current, is also inversely proportional to LG; shorter channels give higher transconductance.

Lamda vs LG

$$\lambda \approx \frac{\Delta L}{L}$$

Lambda is inversely related to channel length
=> Larger the lambda, increases output conductance

gds vs LG (Output Conductance)

Observation: Output conductance drops fast for short to moderate lengths, then stays nearly constant.

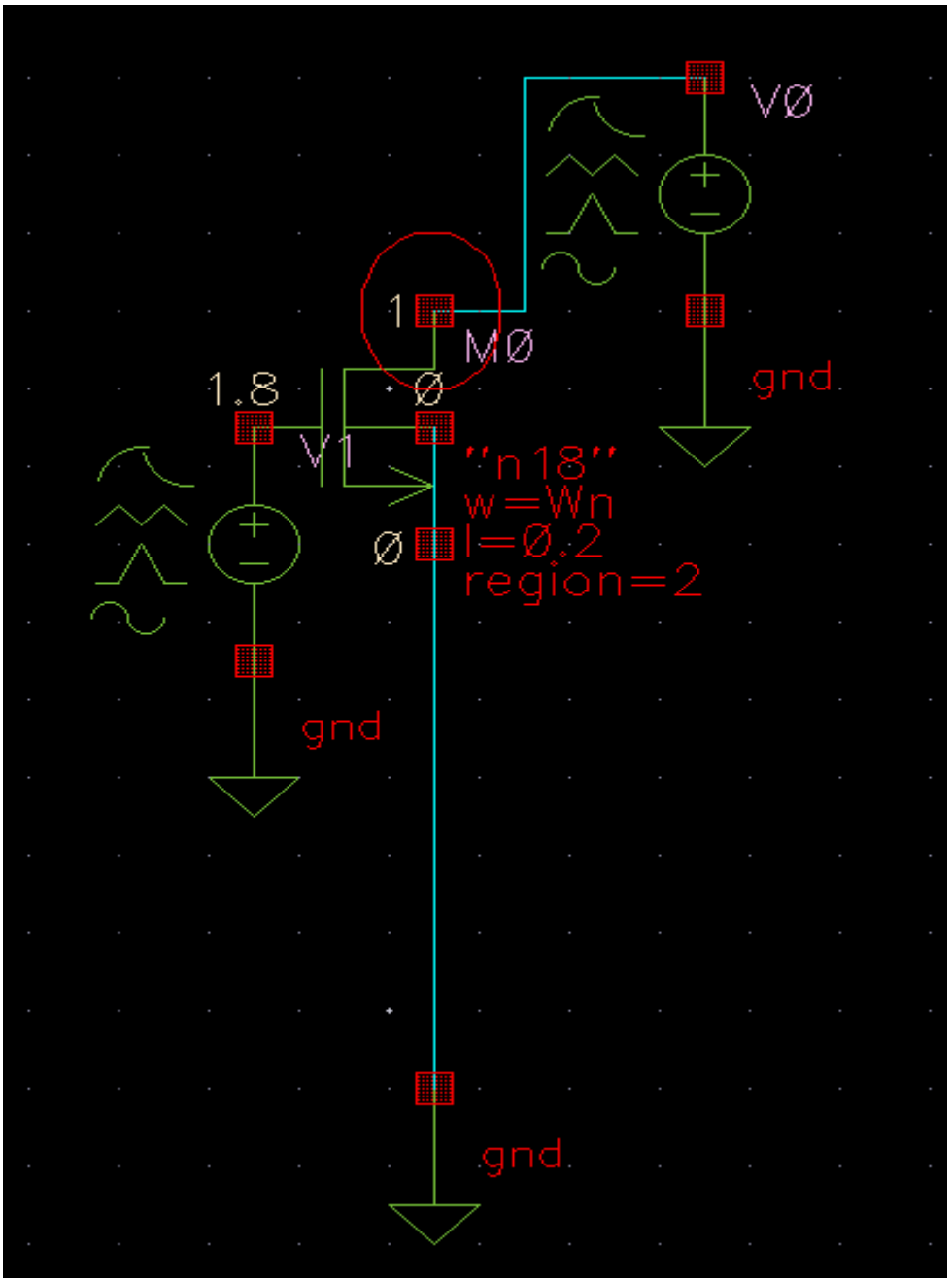
{In saturation (considering channel length modulation)}

$$g_{ds} = \lambda I_{DS}$$

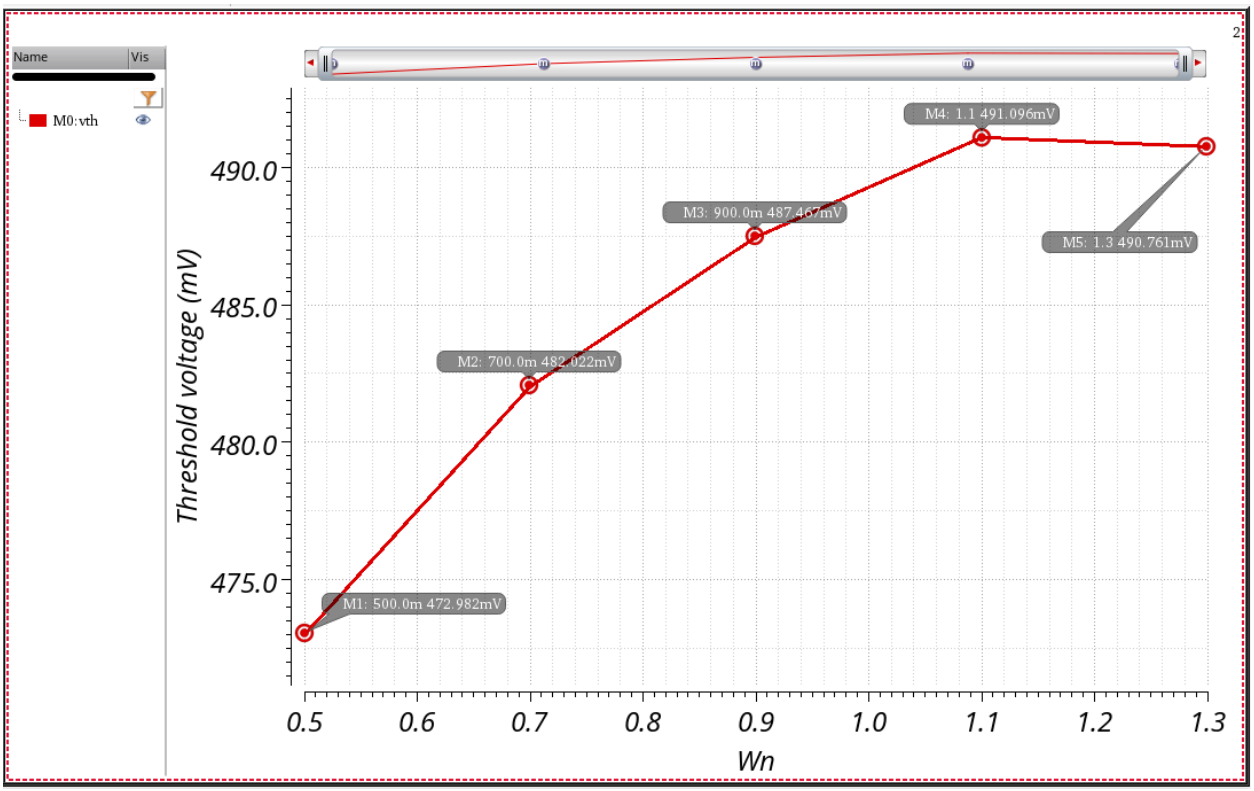
Channel length modulation parameter is higher for shorter channels, leading to higher gds, and as LG increases Channel length modulation parameter decreases and gds stabilizes

3rd Question

Schematic: NMOS



a)Threshold voltage v/s w for N-type MOS Transistor [LINEAR] :



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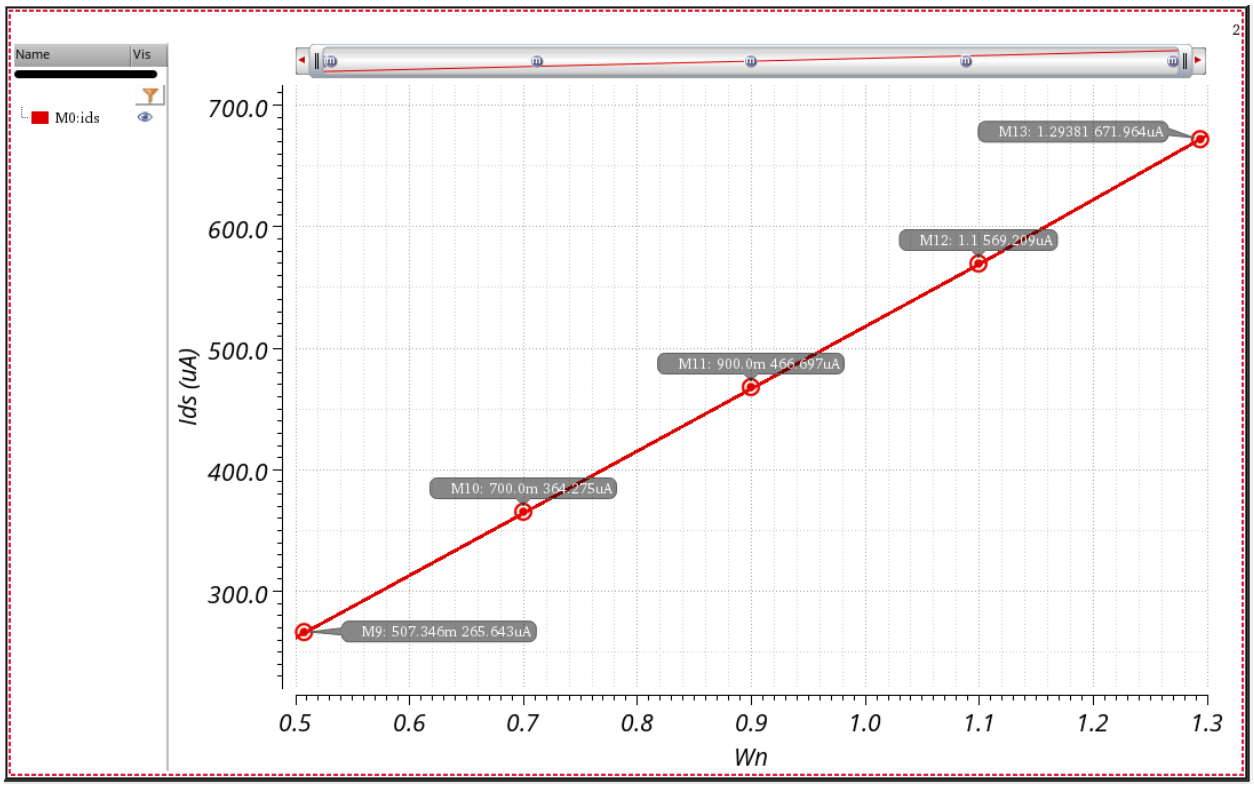

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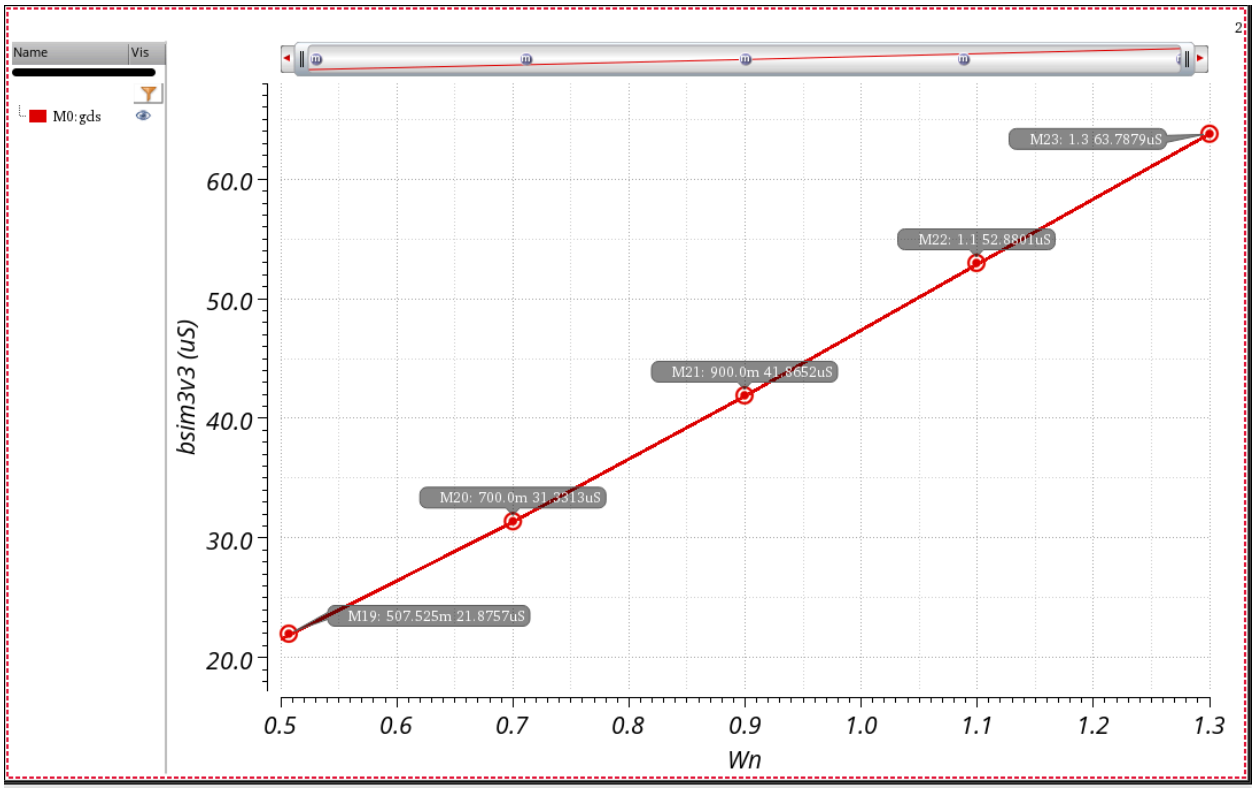
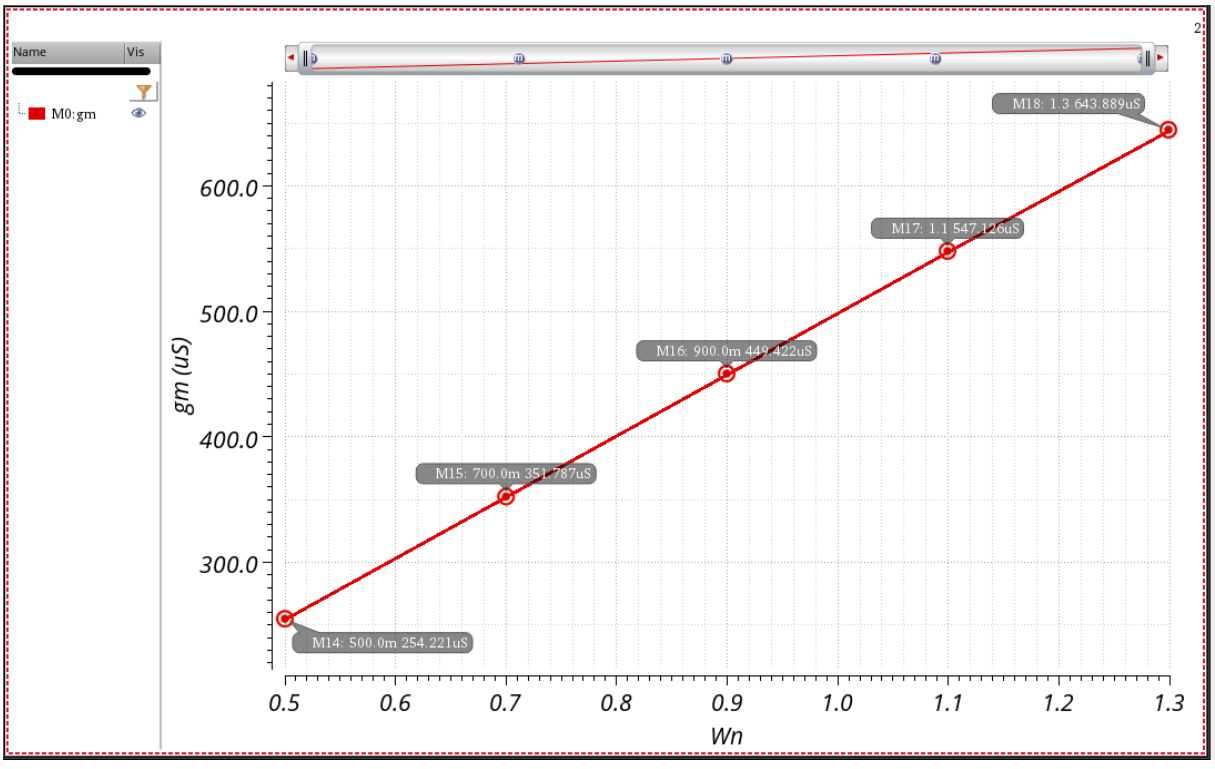
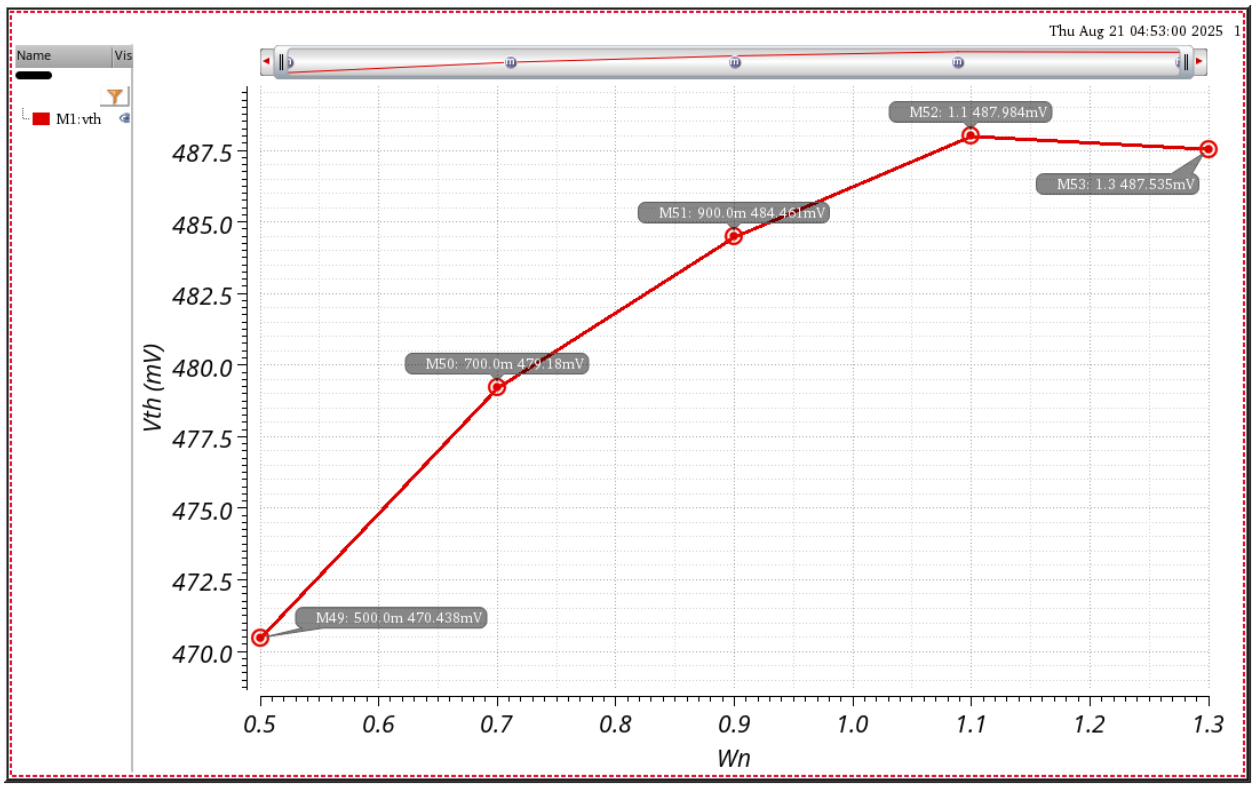


b)gm v/s w for N-type MOS Transistor [LINEAR]:



a)Threshold voltage v/s w for N-type MOS Transistor [SAT] :



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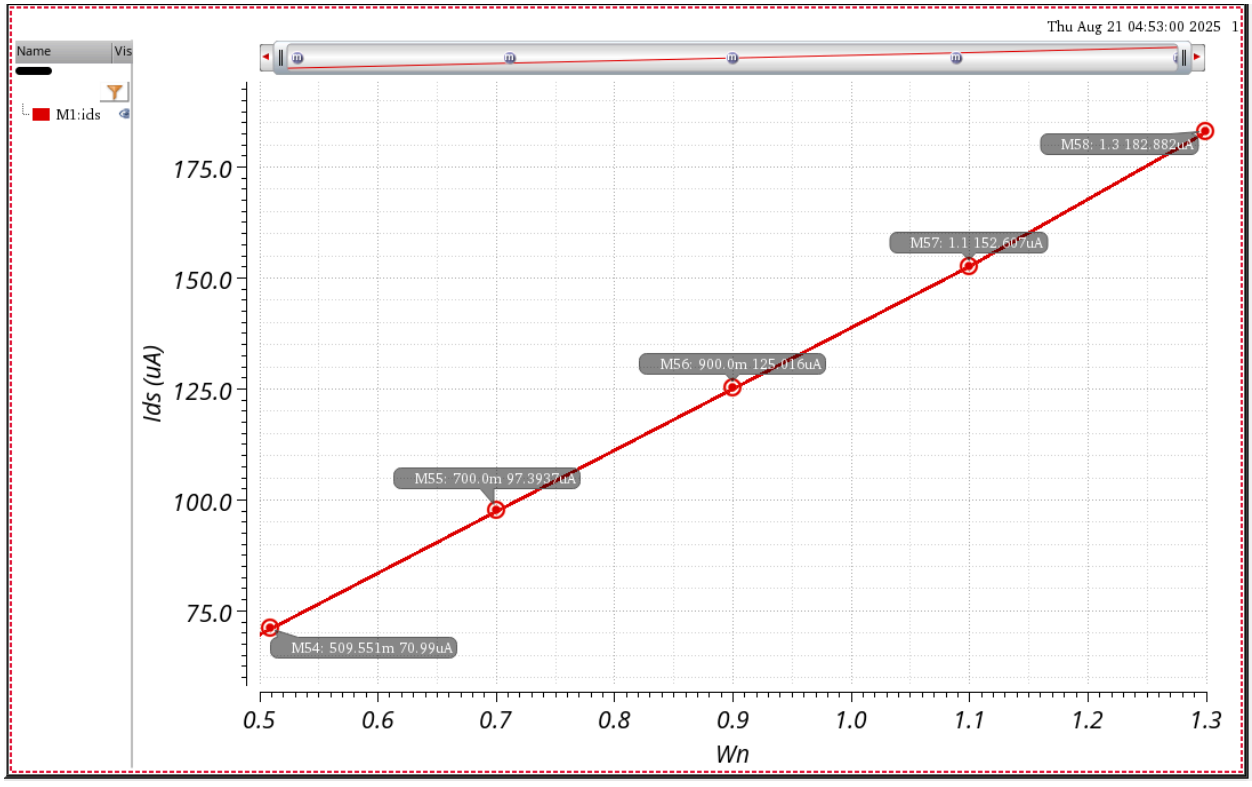

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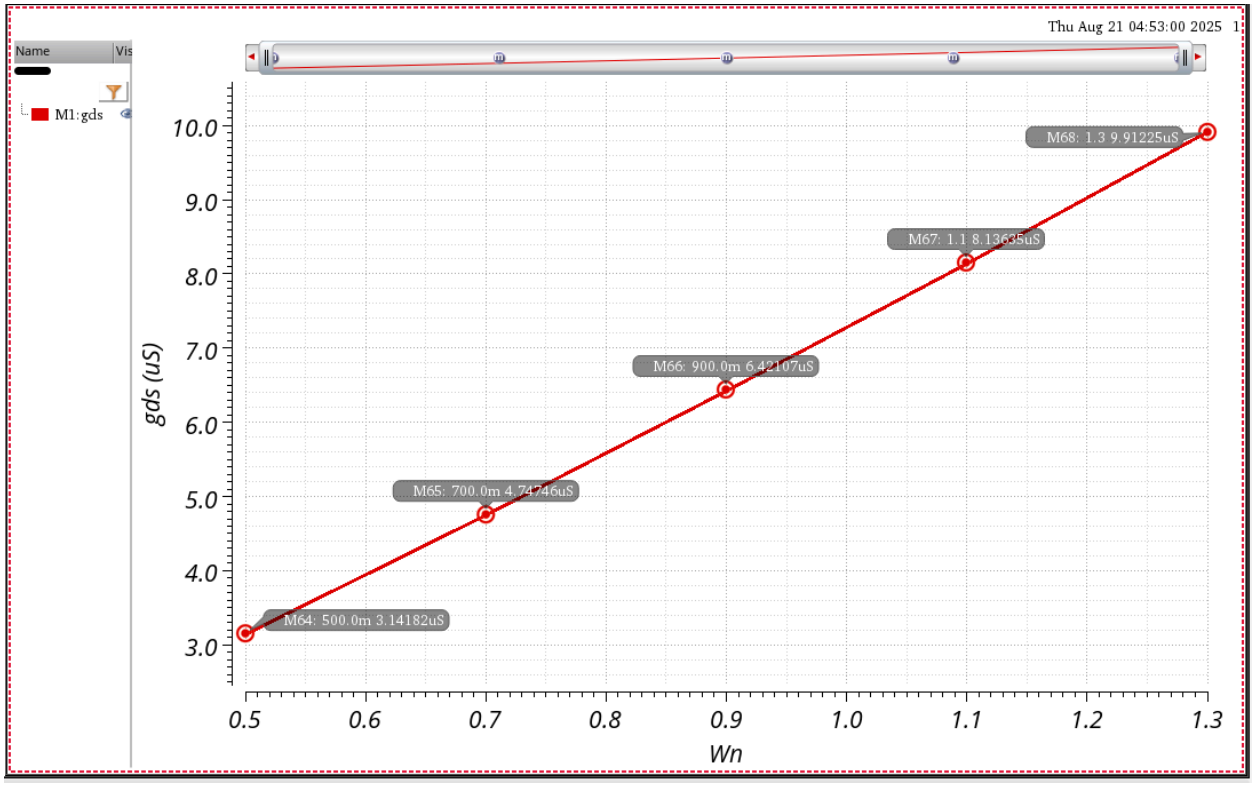

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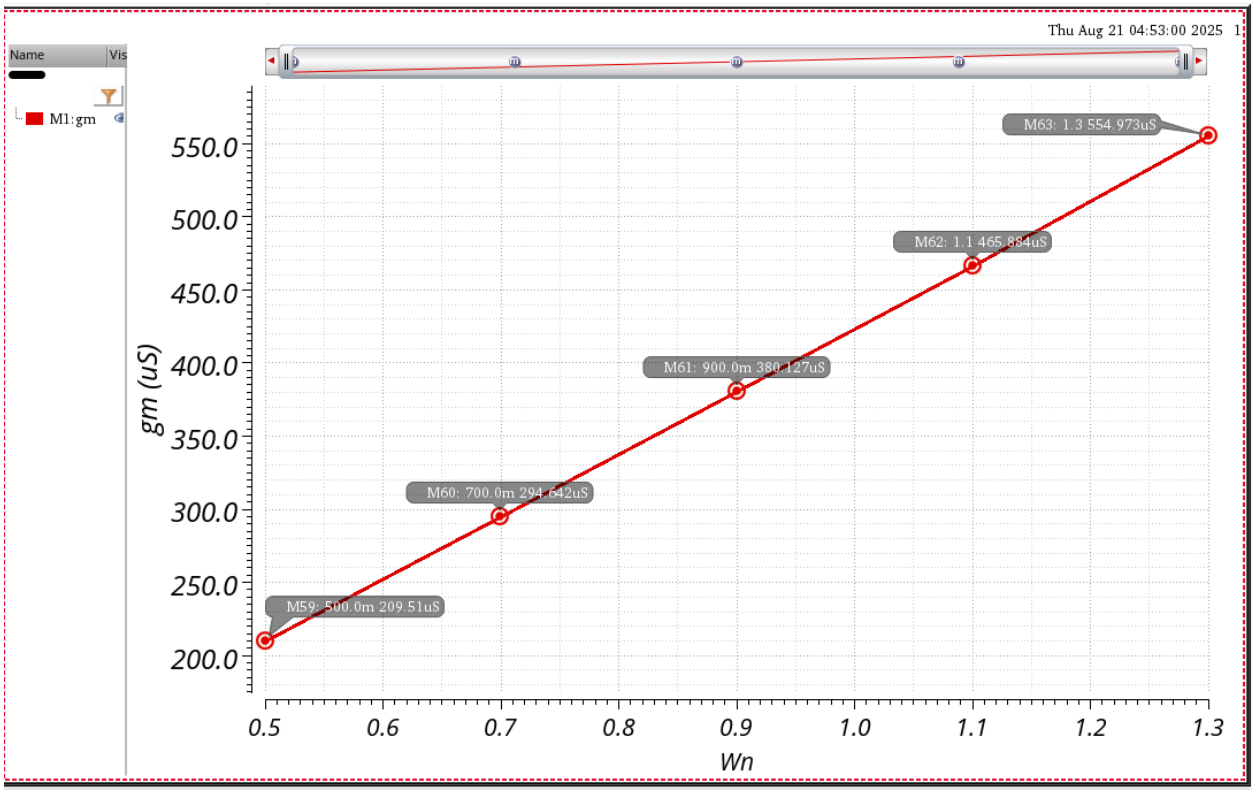
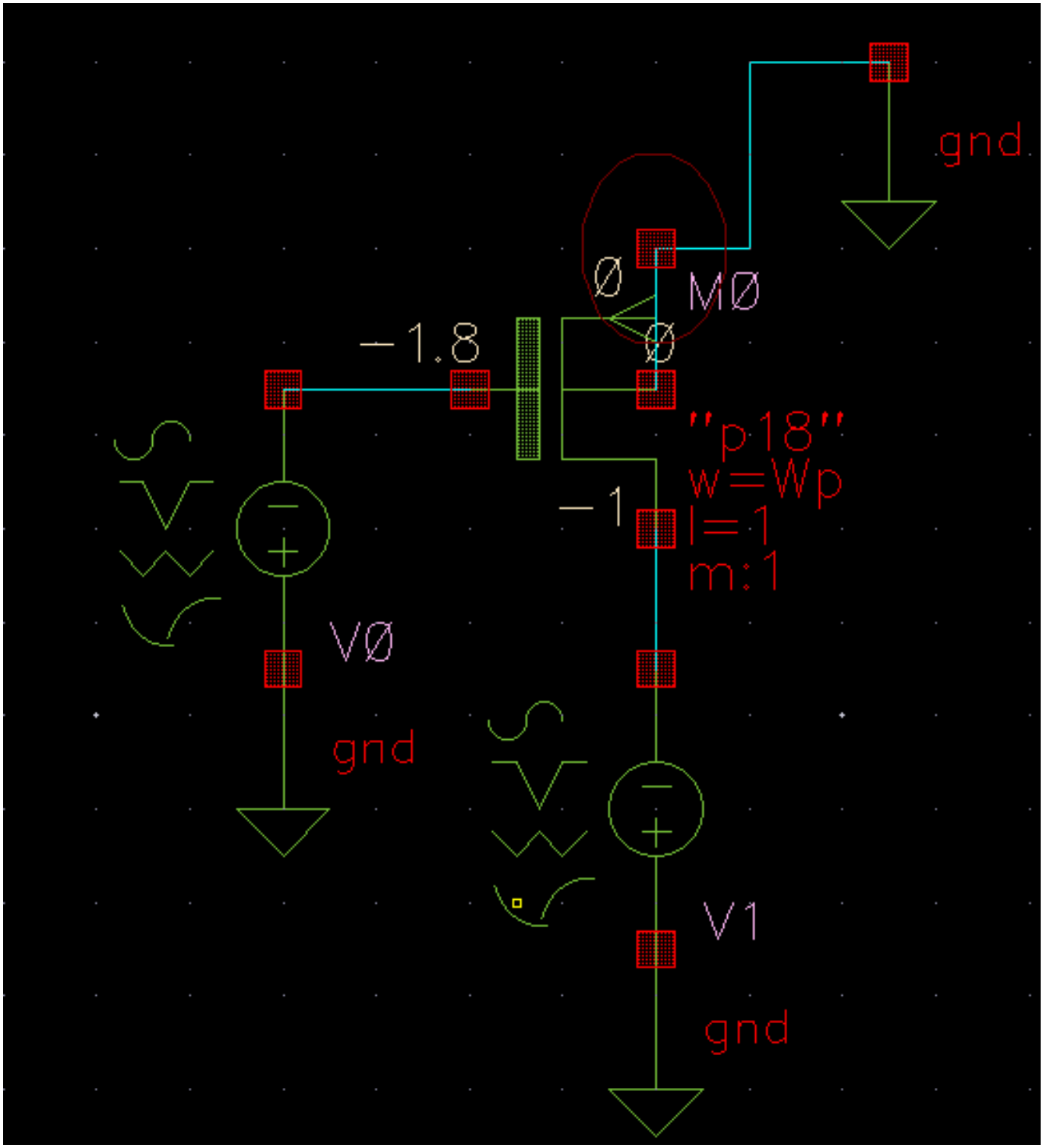


3rd Question

Schematic: pmos



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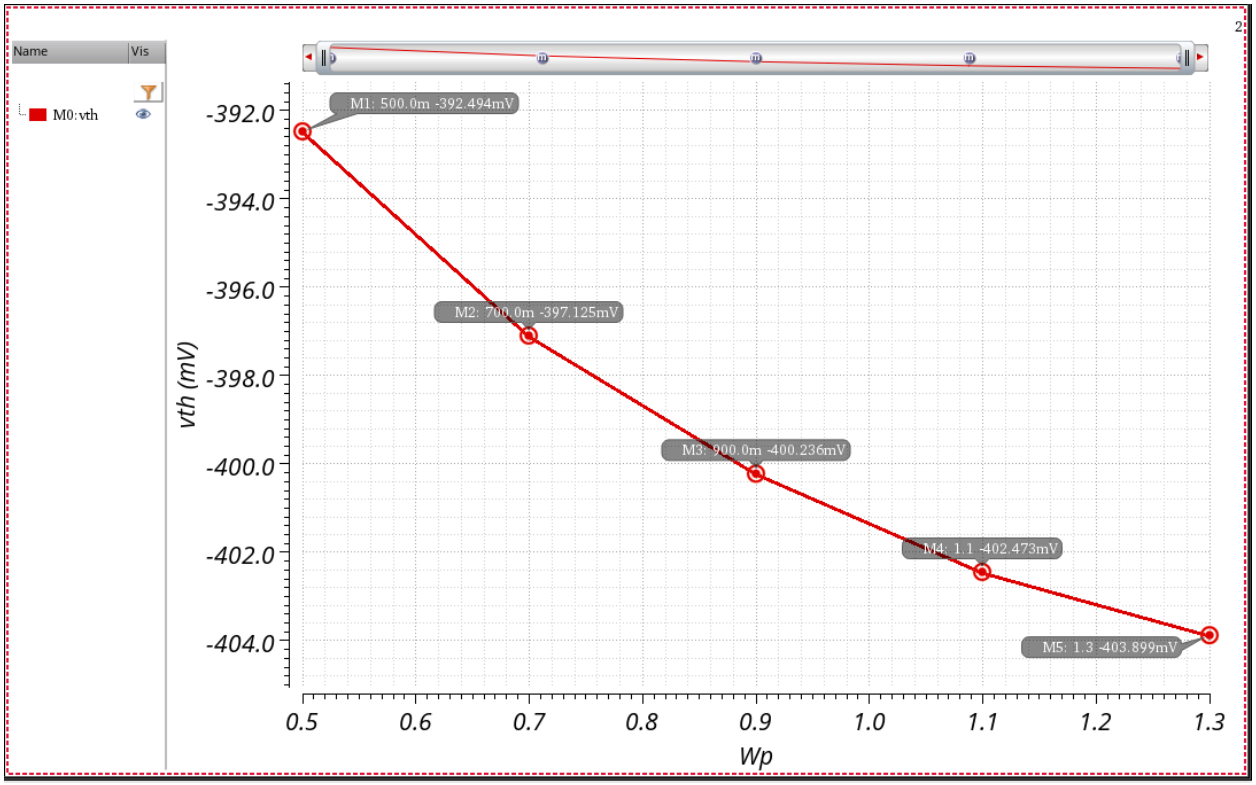

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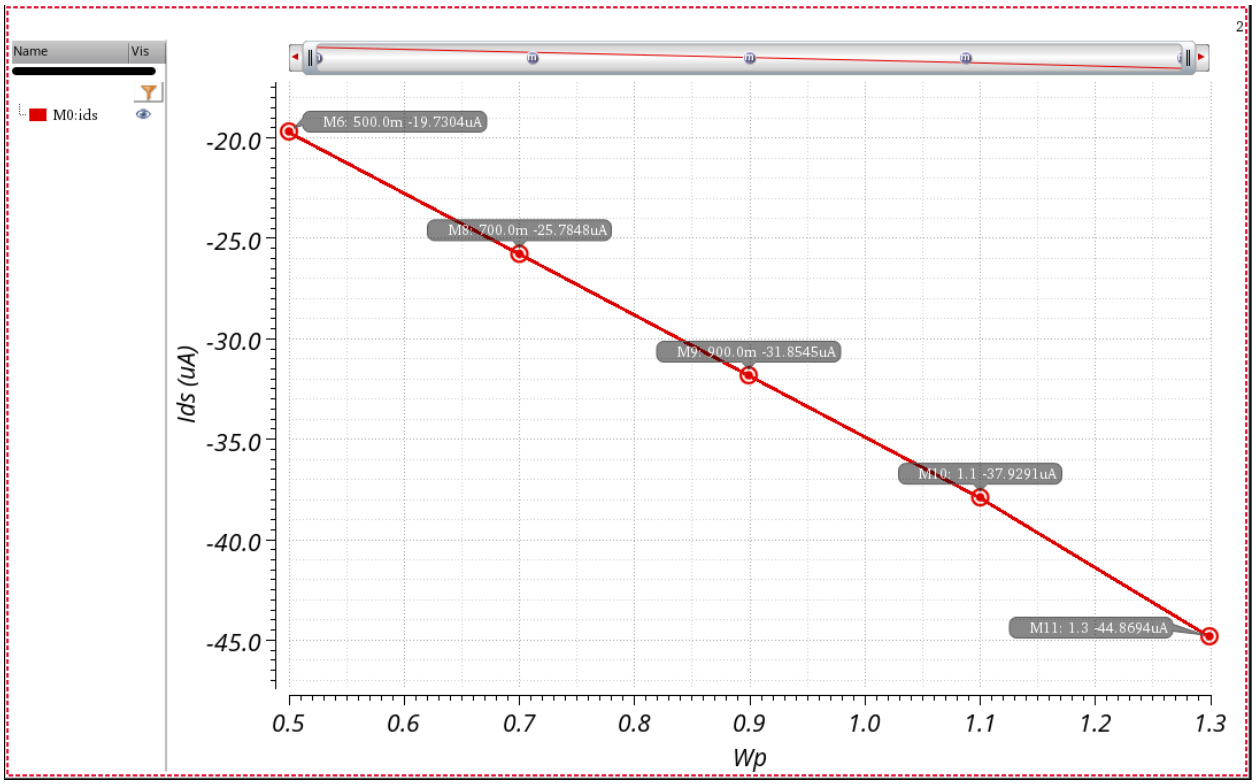

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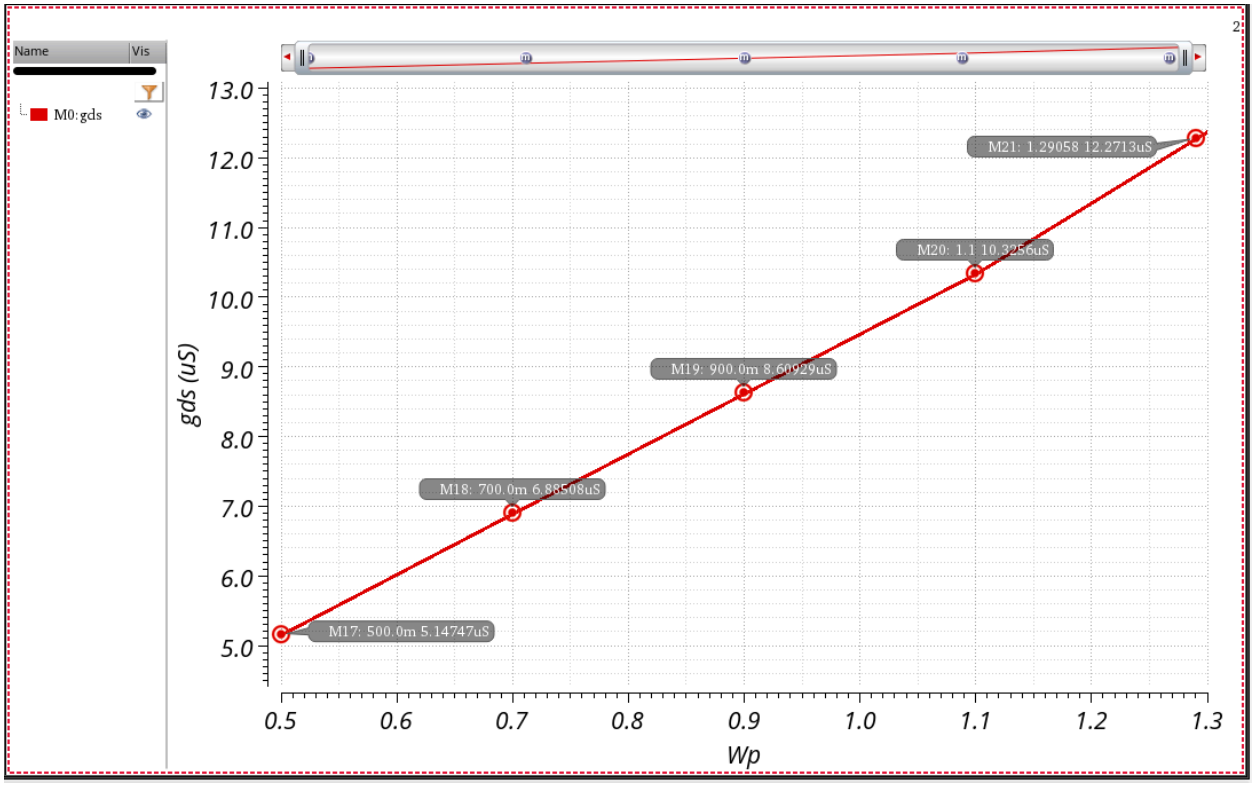

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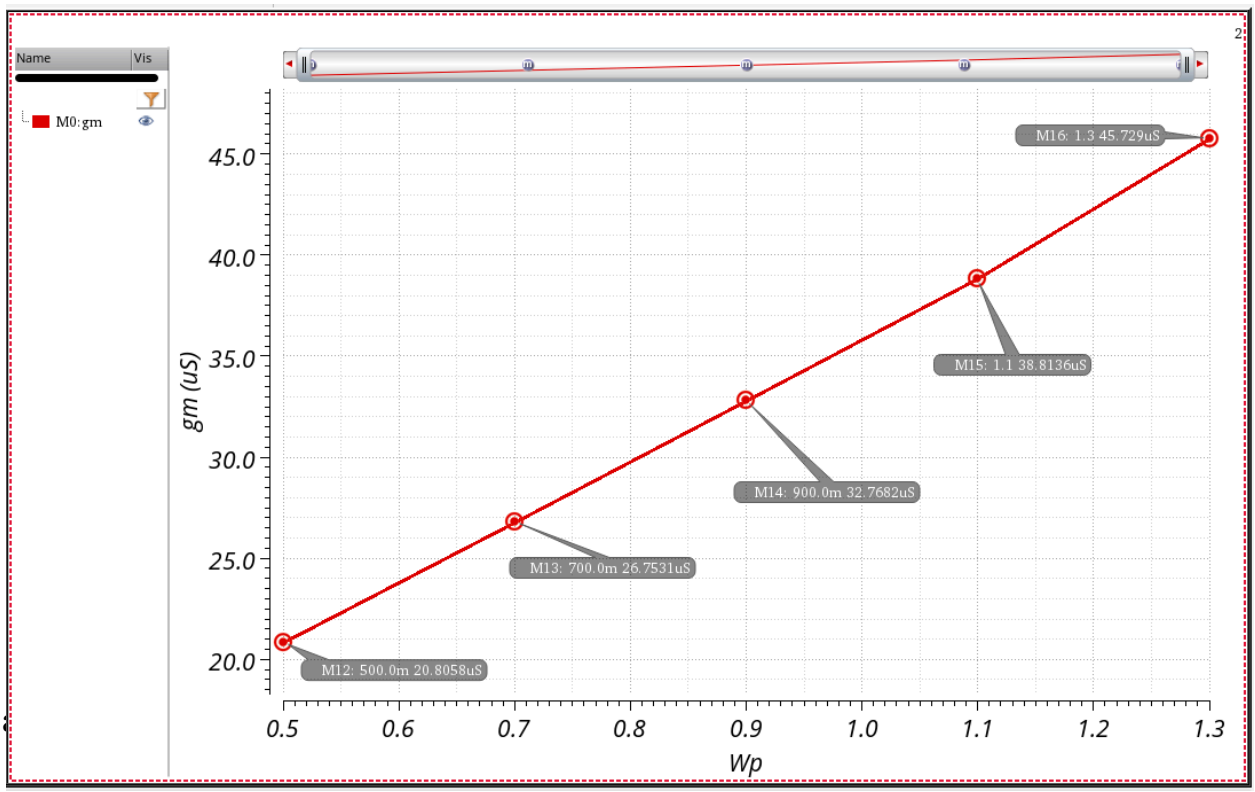

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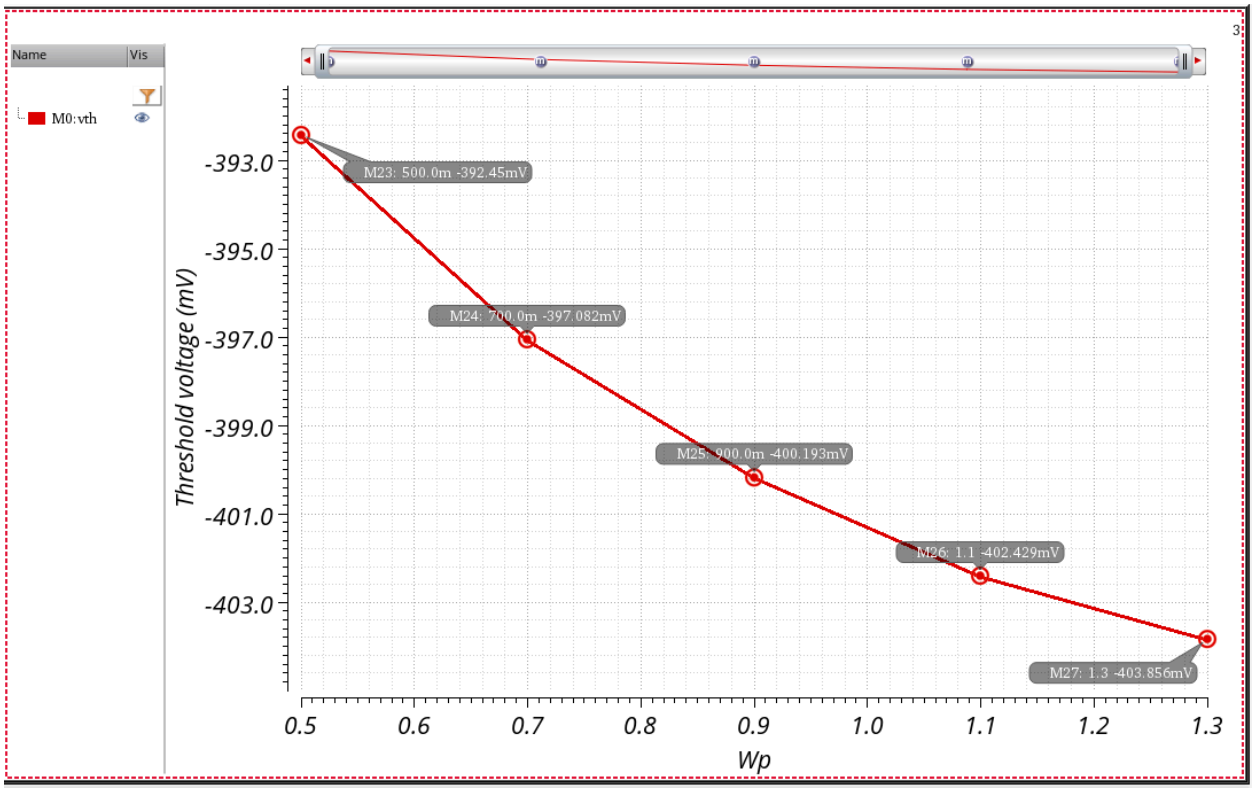

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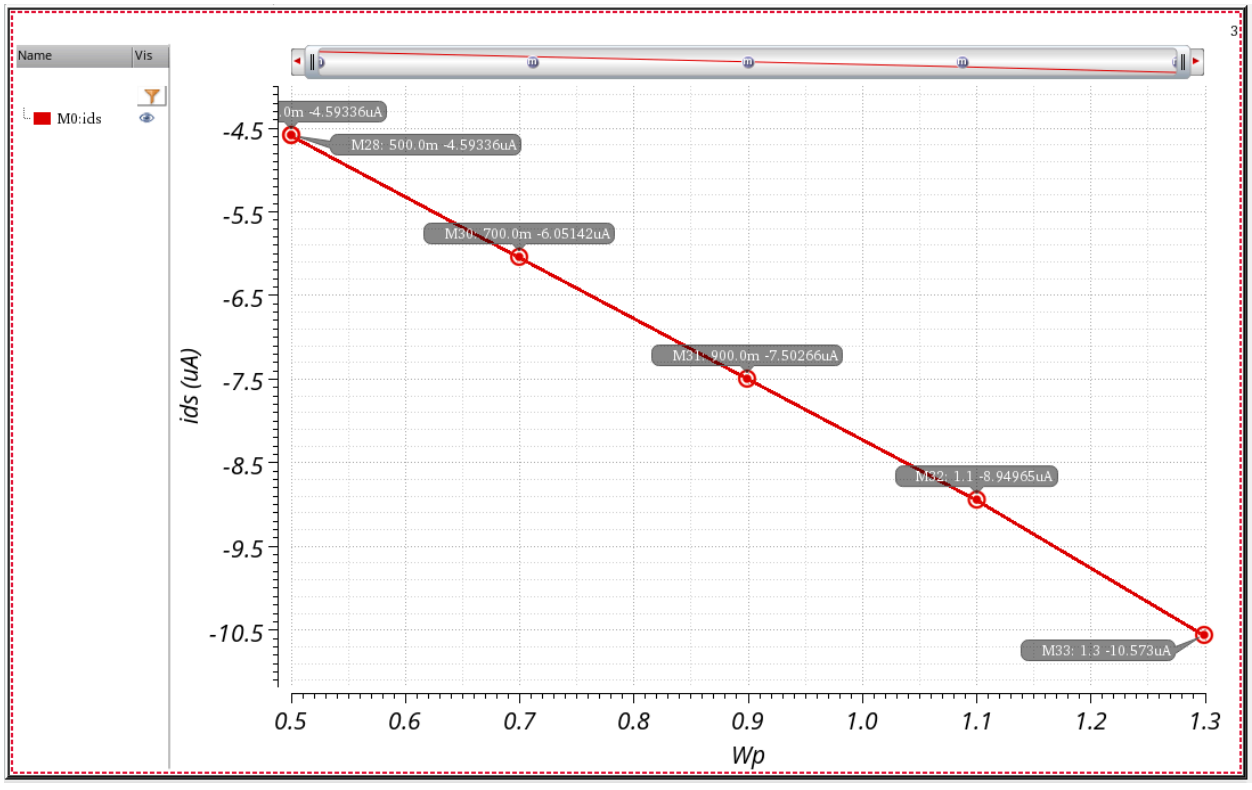

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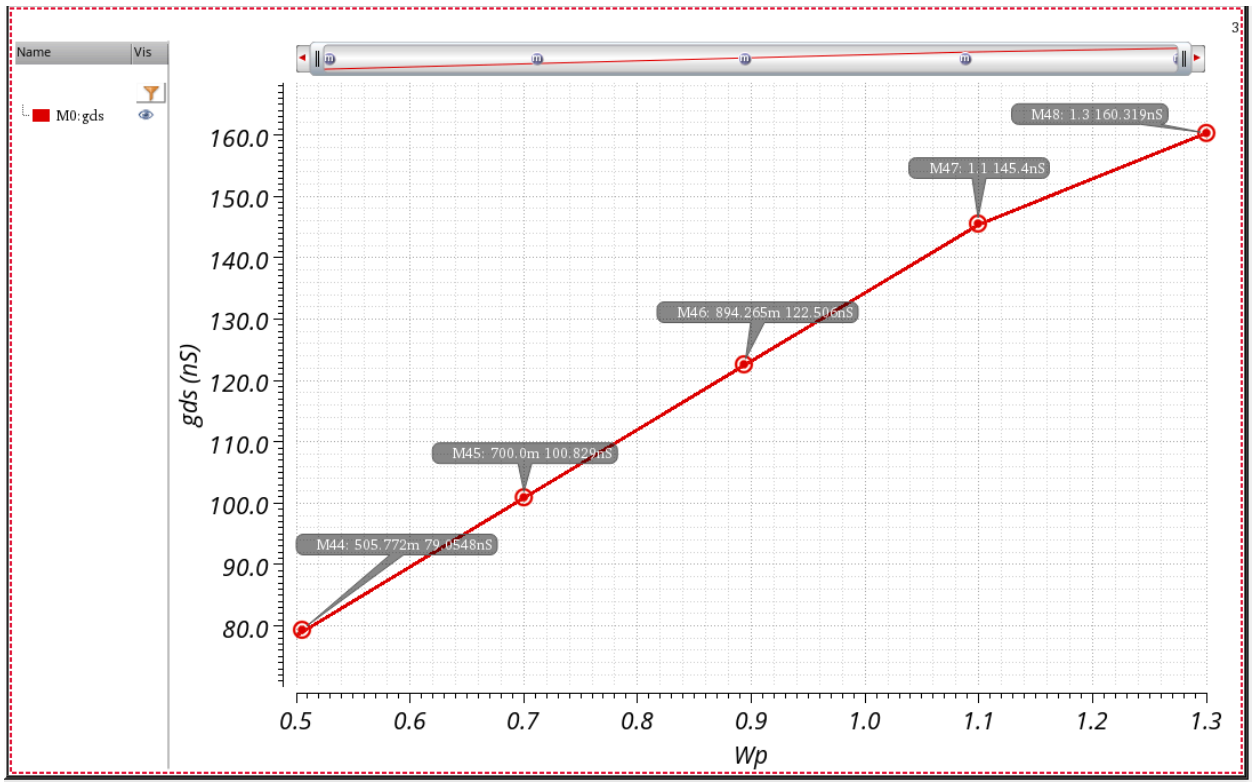
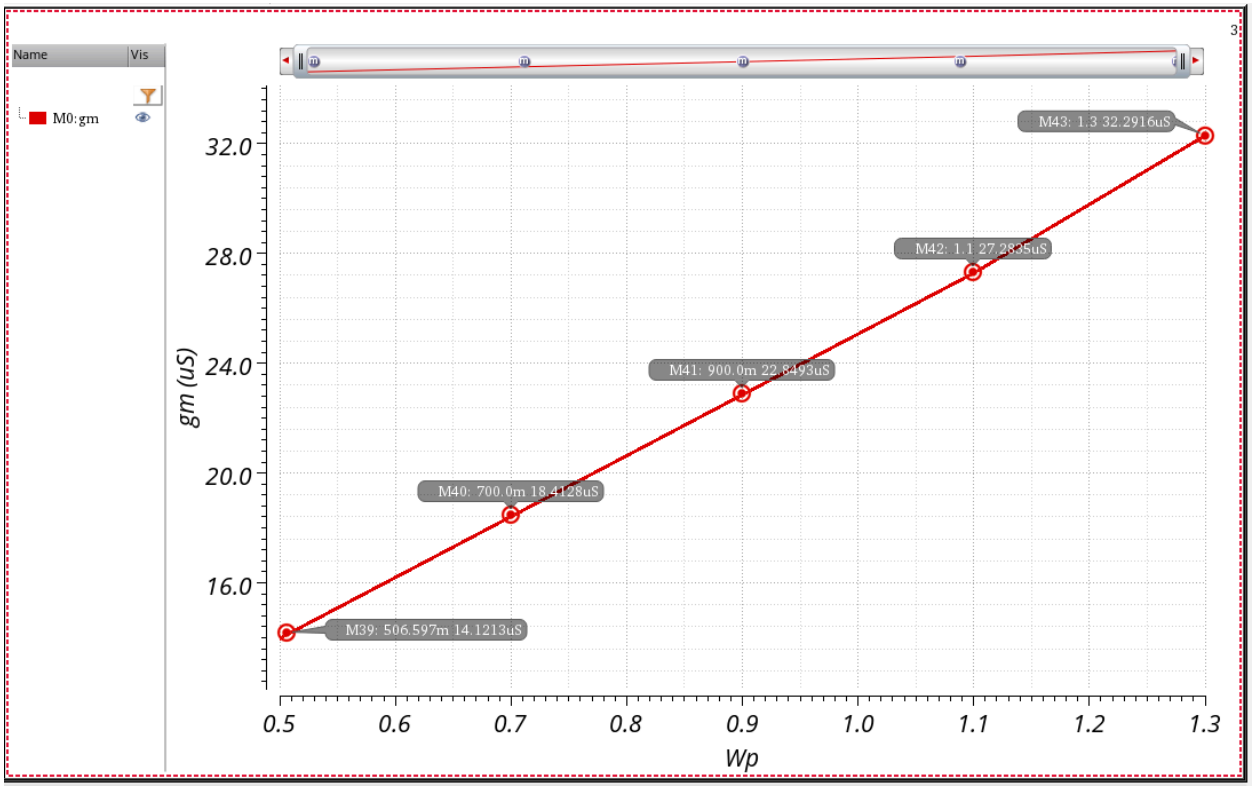


b)gm v/s w for P-type MOS Transistor [SAT]:



NMOS

Width	Vth(in mV)		Ids(µA)		gm(µS)		gds(µS)	
	Linear	Saturation	Linear	Saturation	Linear	Saturation	Linear	Saturation
500nm	472	470	265	70	254	209	21.8	3.1
700nm	482	479	364	97	351	294	31.3	4.7
900nm	487	484	466	125	449	380	41.8	6.4
1100nm	491	487	569	152	547	465	52.8	8.1
1300nm	490	487	671	182	642	554	63.7	9.9

PMOS

Width	|Vth|(in mV)		|Ids|(µA)		gm(µS)		gds(µS)	
	Linear	Saturation	Linear	Saturation	Linear	Saturation	Linear	Saturation
500nm	392	392	19	4.5	20	14	5.1	79
700nm	397	397	25	6	26	18	6.8	100
900nm	400	400	31	7.5	32	22	8.6	122
1100nm	402	402	37	9	38	27	10.3	145
1300nm	403	403	44	10.5	45	32	12.2	160

CALCULATING u_nC_{OX} VALUES

Used beff = u_nC_{OX} (W/L) [NMOS]
At Ln = 0.6µm, w = 1µm => beff = 425.2 µA/v2
=> u_nC_{OX} = 301

CALCULATING μ_pC_{ox} VALUES

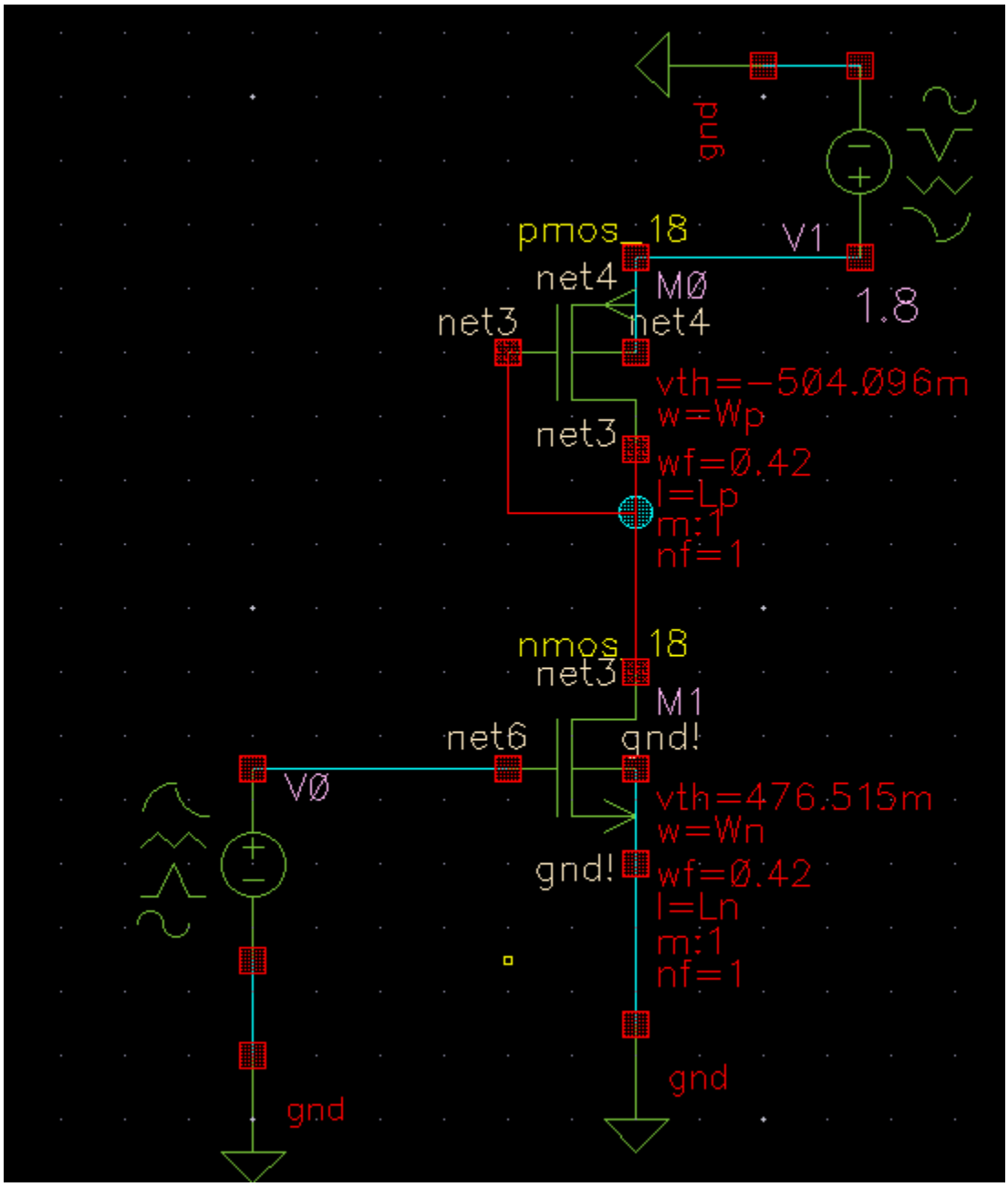
Used beff = μ_pC_{ox} (W/L) [PMOS]
At Lp = 0.2µm, w = 1µm => beff = 348 µA/v2
=> μ_pC_{ox} = 63.2

CALCULATED u_nC_{OX} and μ_pC_{ox} VALUES

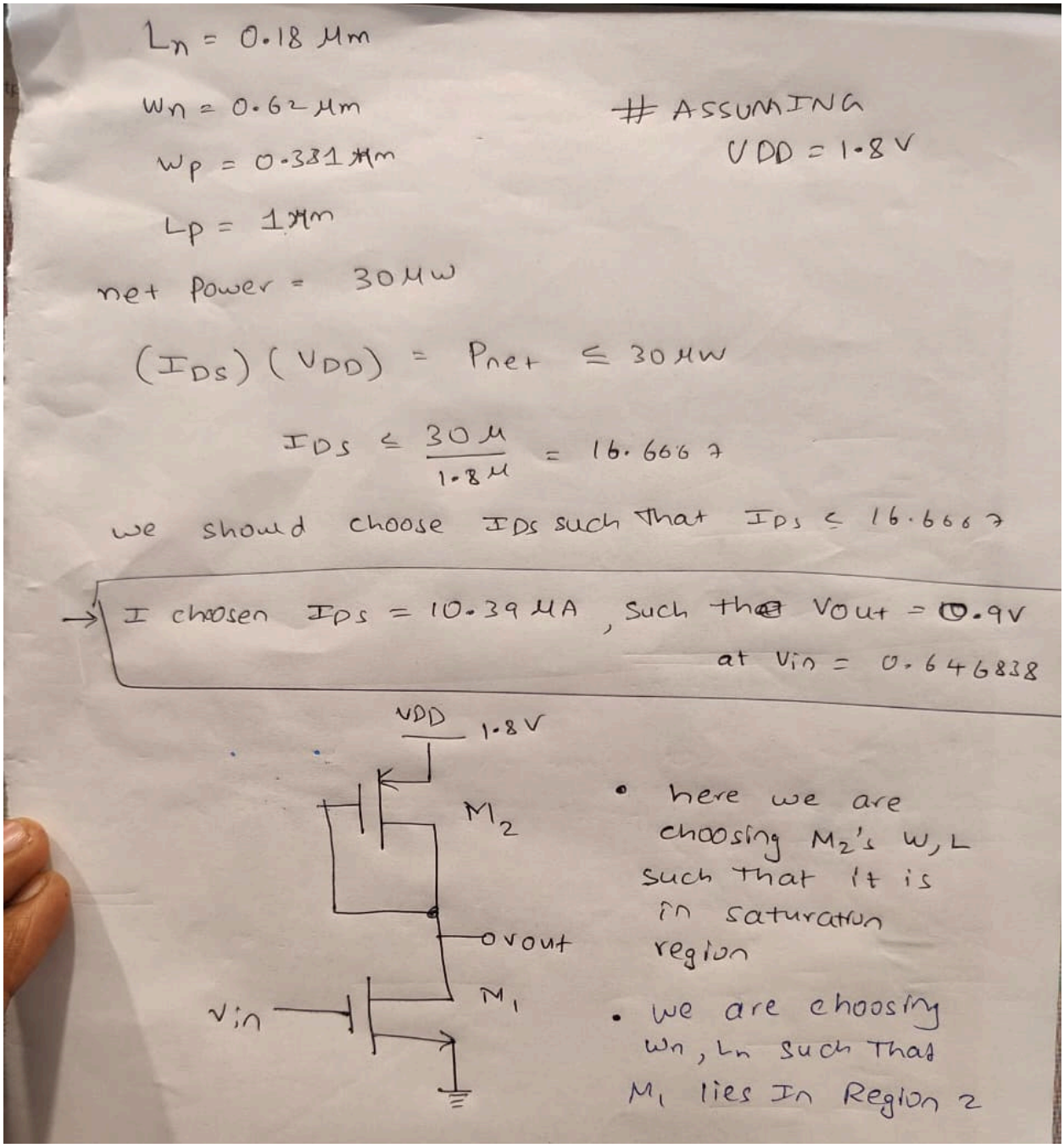
Type of MOS	u_nC_{OX} (µS)
NMOS	301
PMOS	63.2

4th Question

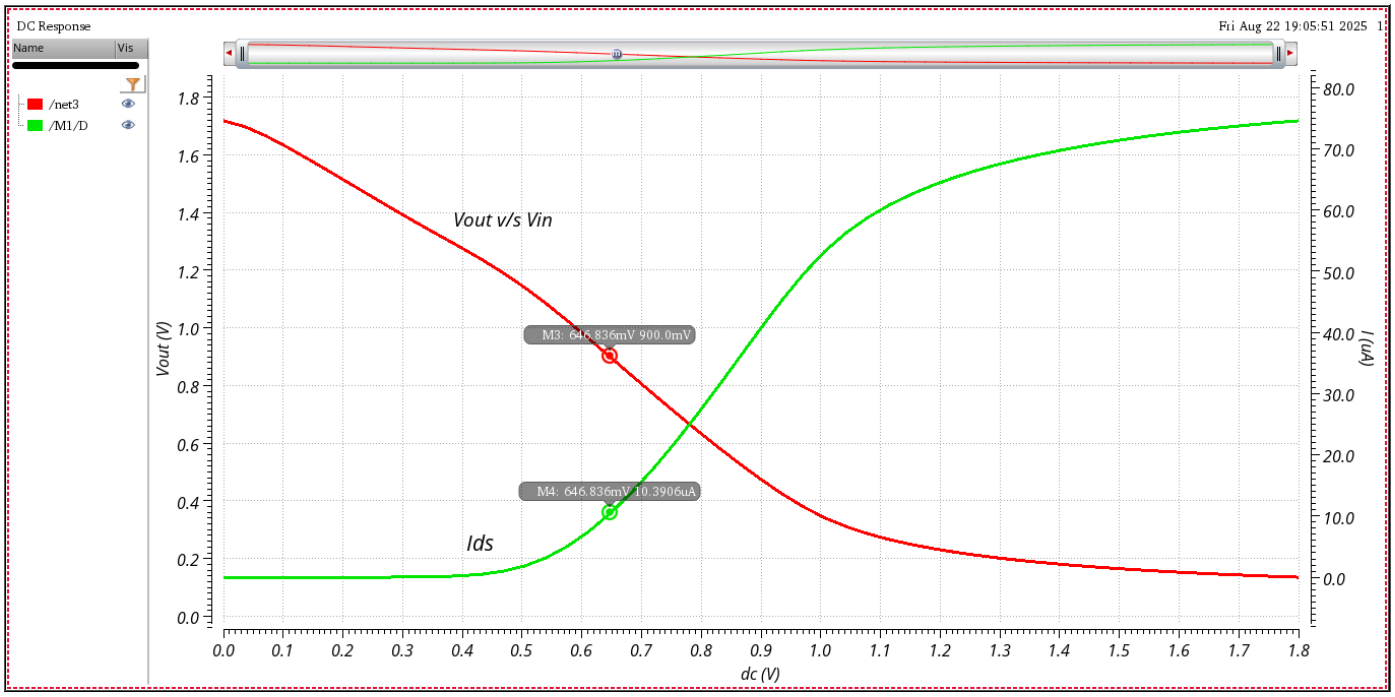
Schematic

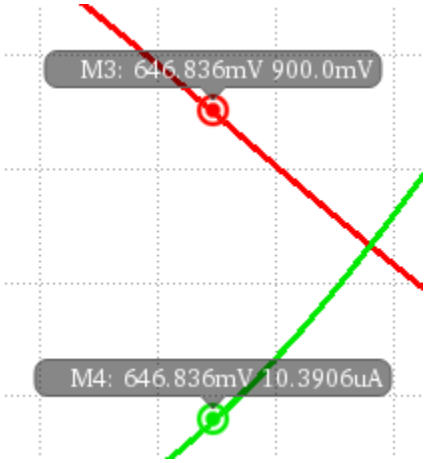


EXPLANATION



Ln = 0.18 μm
Wn = 0.62 μm
Wp = 0.381 μm
Lp = 1 μm



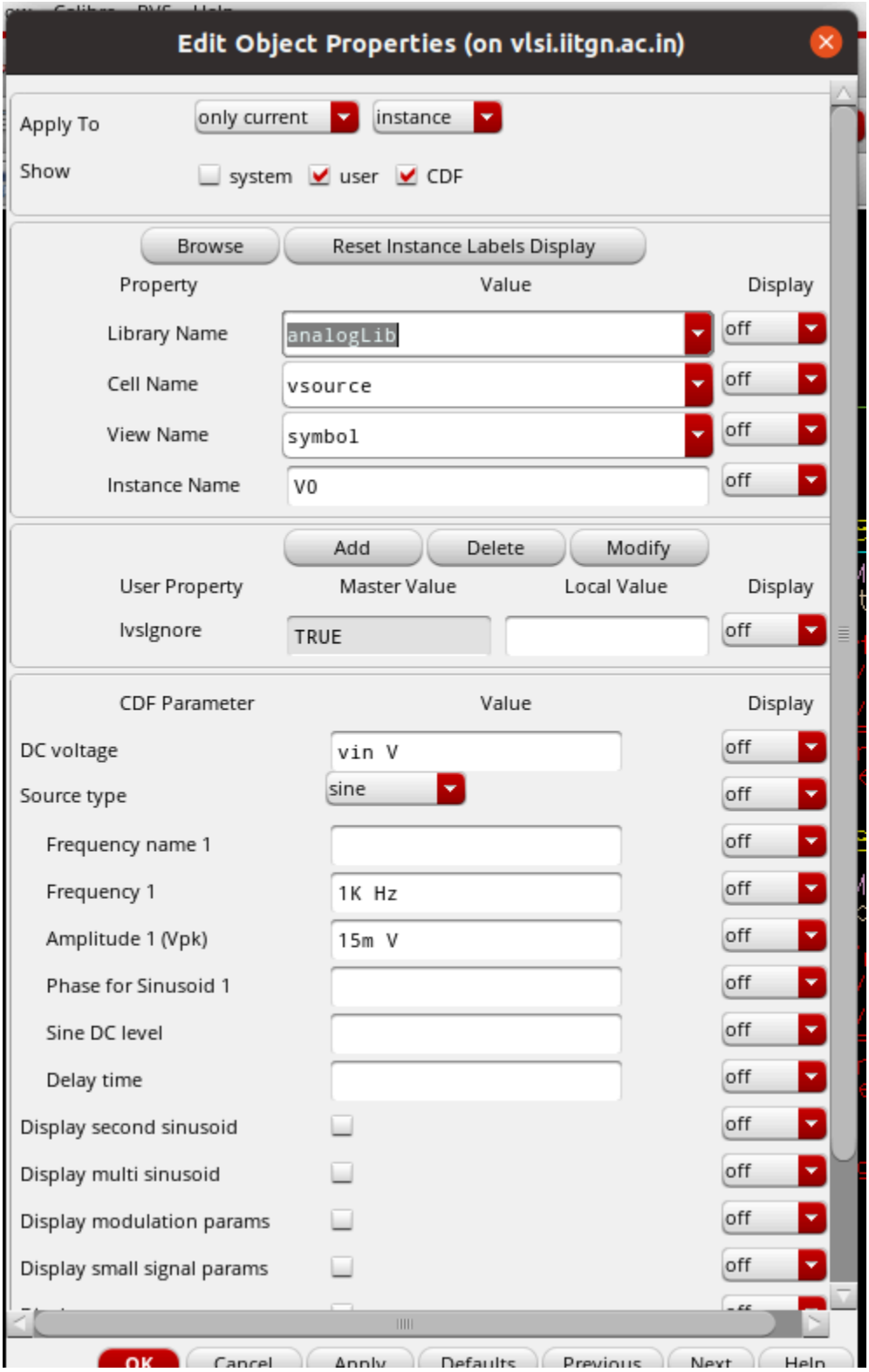


From the above plot we can extract the DC operating point which is 0.646 V
At the Vbias Ids = 10.39 µA
We chosen Ln,Wn,Lp,Wp such that the ids is < 16.67µA

POWER CONSUMPTION

I assumed VDD = 1.8V
P = (VDD)(10.39 µA)

P = (1.8v)(10.39 µA) = 18.702 µW **which is less than 30 µW**



CALCULATING GAIN OF AMPLIFIER

input/output	Vmin	Vmax
i/p	631.246	660.754
o/p	875.17	927.793

$$\text{Gain} = \frac{Vout(p-p)}{Vin(p-p)} = \frac{927.793-875.17}{660.754-631.246} = \frac{52.623}{29.508} = 1.8$$