Unit 1

Sr. No.	Reference	Reading sequence
1.	Performance and Numericals	Chapter 1: Hennessy Patterson (COAD)
2.	Instruction Format, General Discussion	Chapter 2: Hamacher Zaky (CO)
3.	Instruction Cycle, Subcycle	Chapter 14: William Stallings
4.	Data path and related concepts and Control Signal; Hardwired, Mircroprogrammed Control	Chapter 5: Hamachar Zaky (CO)
5.	Control unit operations	Chapter 20 & 21: William Stallings
6.	Data path and control signal for RISC-V instructions ADD, LOAD etc.	Chapter 4.1 to 4.4: Hennessy Patterson (COAD)

Unit 2

Sr. No.	Reference	Reading sequence
1.	Arithmetic for Computers	Chapter 3: Hennessy Patterson (COAD)
2.	Computer Arithmetic	Chapter 10: William Stallings
3.	Arithmetic	Chapter 9: Hamachar Zaky (CO)

Unit 3

Sr. No.	Reference	Reading sequence
1.	Large and Fast: Exploiting Memory Hierarchy	Chapter 5: Hennessy Patterson (COAD)
2.	Internal Memory, Cache Memory, External Memory	Chapter 4, 5, 6: William Stallings
3.	The Memory System	Chapter 8: Hamachar Zaky (CO)

Unit 4

Sr. No.	Reference	Reading sequence
1.	Input/Output Organization	Chapter 7: Hamachar Zaky (CO)
2.	A Top-Level View of Computer Function and Interconnection	Chapter 3: William Stallings
3.	Losely coupled and tightly coupled	Chapter 17.1. to 17.5 : William Stallings

Unit 5

Sr. No.	Reference	Reading sequence
1.	Pipelining	Chapter 4.5 to 4.8: Hennessy Patterson (COAD)
2.	Pipelining	Chapter 6: Hamachar Zaky (CO)
3.	Reduced Instruction Set Computers	Chapter 15: William Stallings

Unit 6

Sr. No.	Reference	Reading sequence
1.	Parallel Processors from Client to Cloud	Chapter 6: Hennessy Patterson (COAD)
2.	Multicore Computers GPGPU	Chapter 18.1 to 18.5: William Stallings Chapter 19.2 to 19.3: William Stallings