EXPERIMENT NO : 2

NAME : SAHIL TRIPATHI

AIM : Write a Verilog code for Half adder and Full adder using

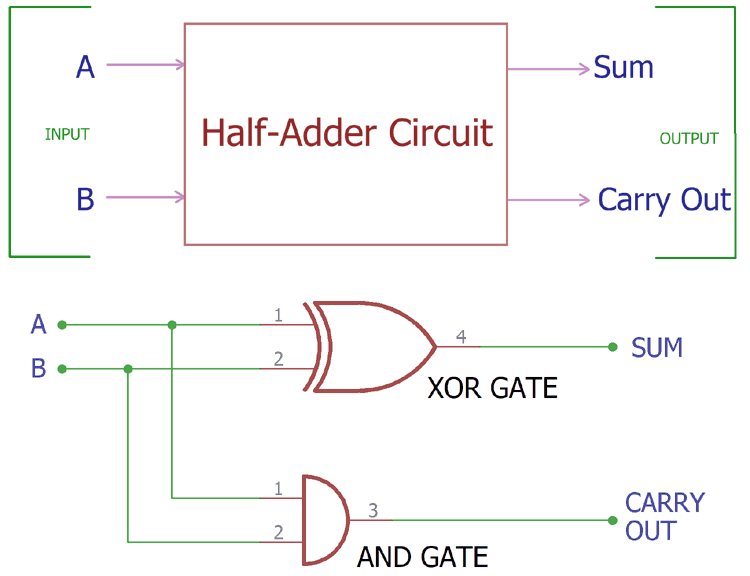
1. Data Flow Modeling
2. Gate Level Modeling

HALF ADDER –

TRUTH TABLE-

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | SUM | CARRY |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

CIRCUIT DIAGRAM



DATA FLOW (HALF ADDER)

module halfadderdataflow(

input a,

input b,

output sum,

output carry

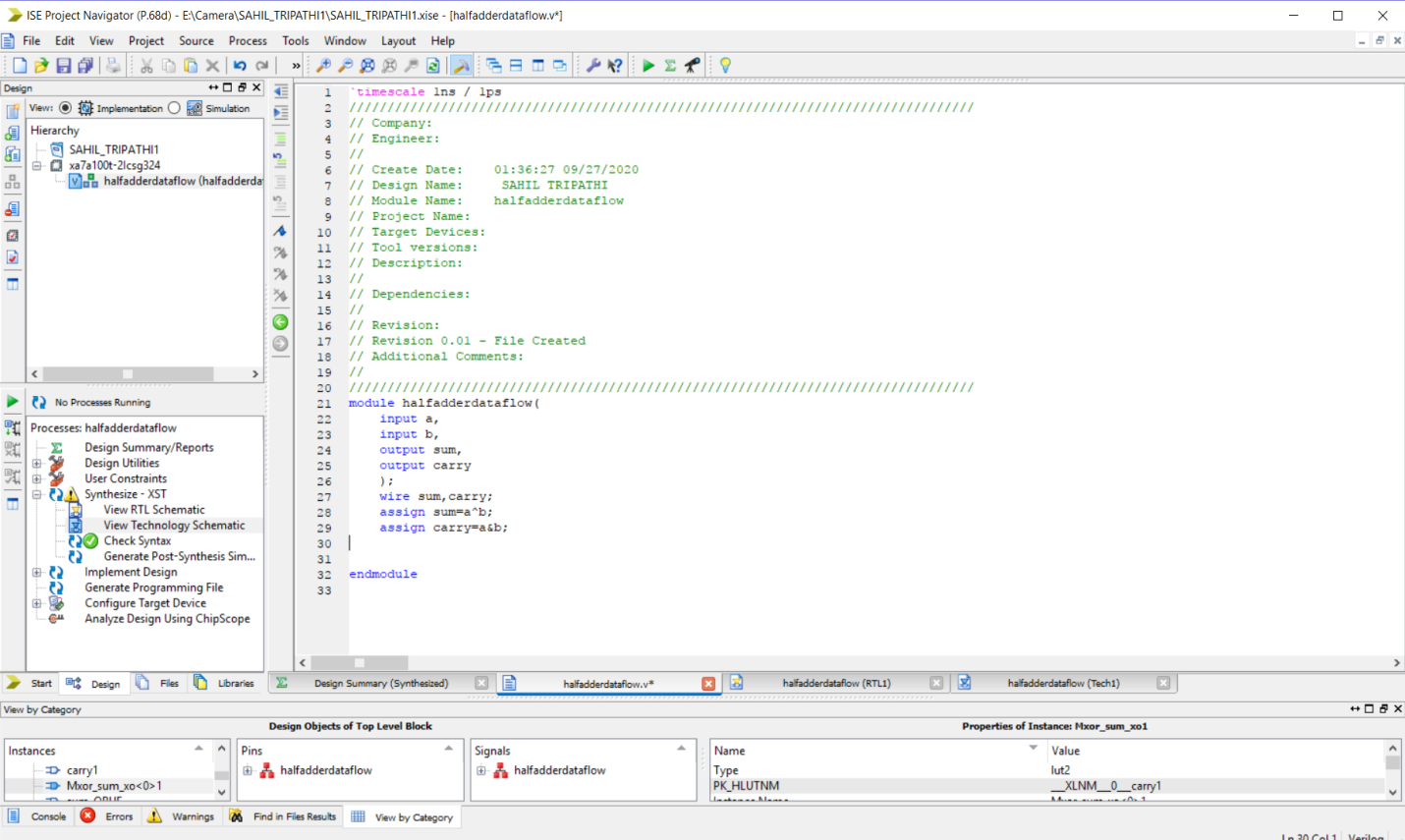
);

assign sum=a^b;

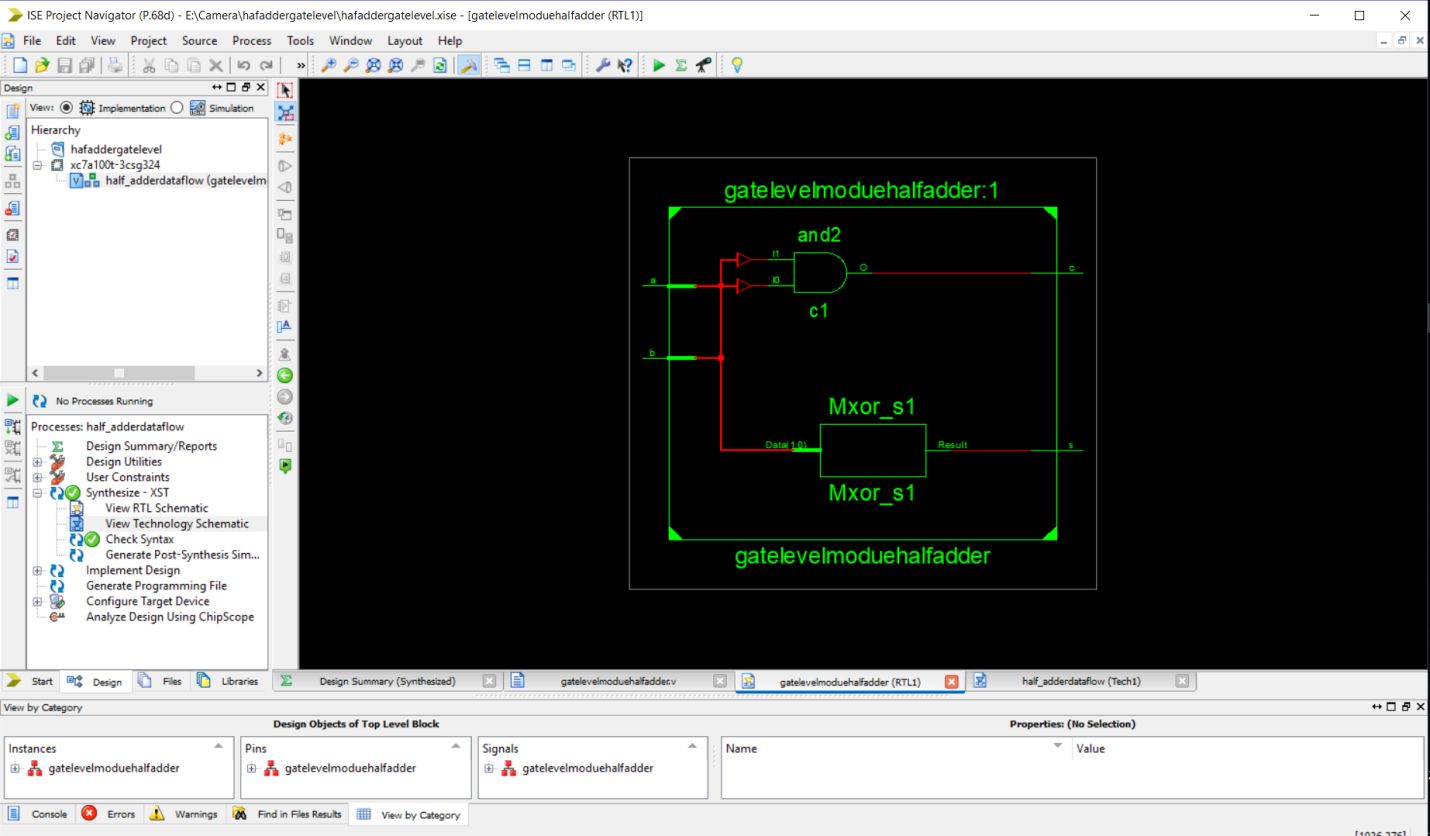
assign carry=a&b;

endmodule

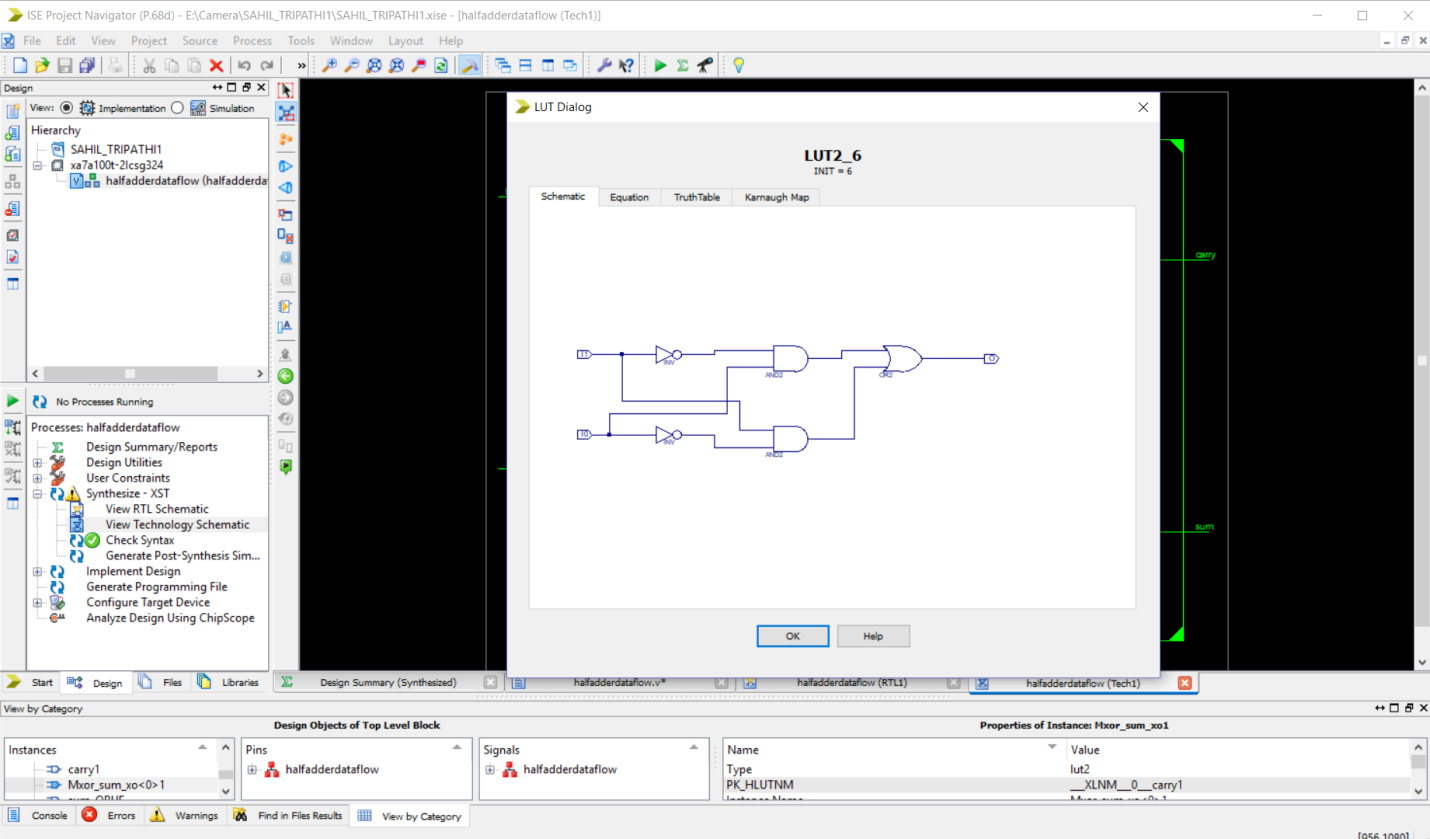
IMAGE OF CODE –

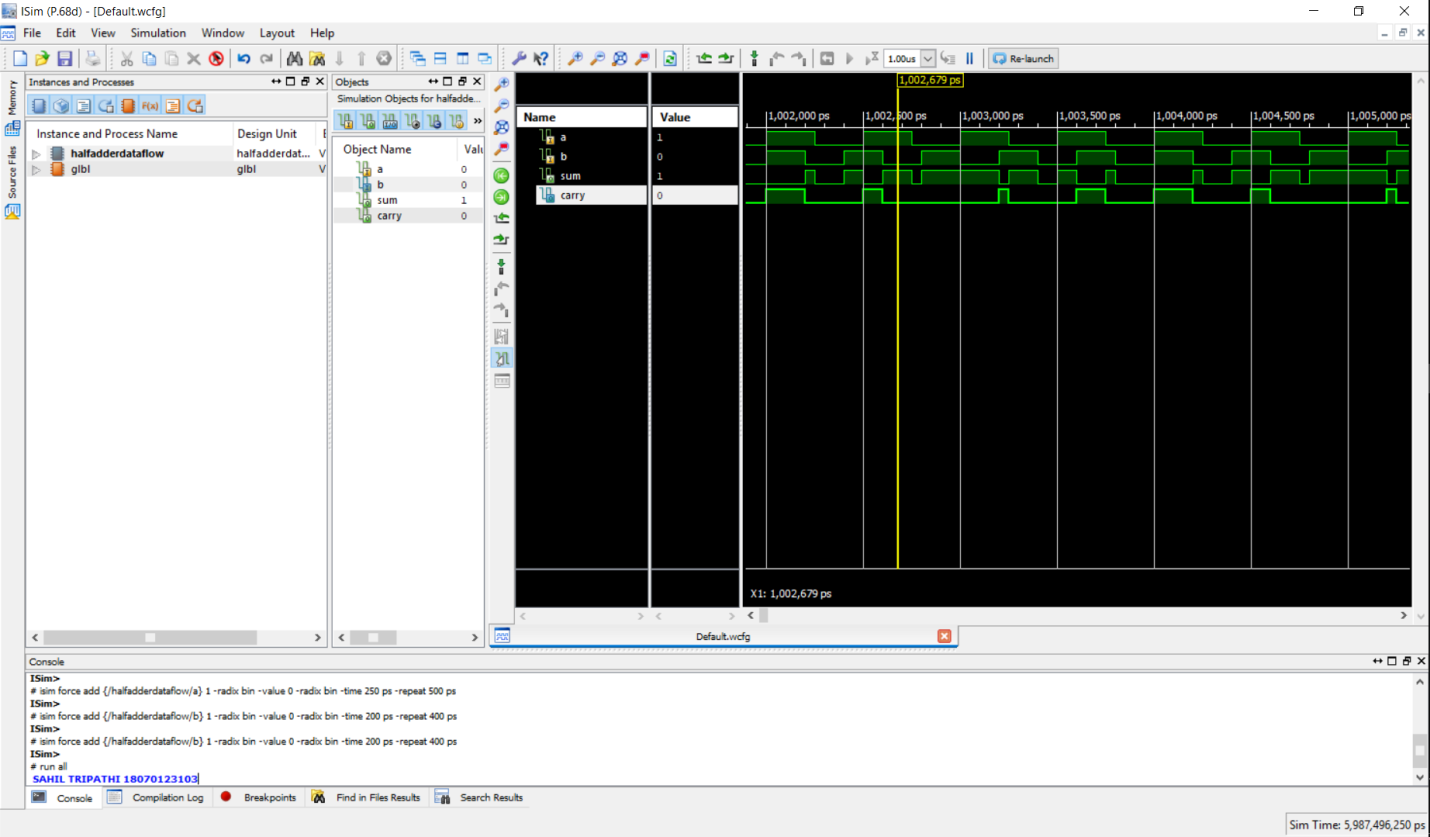


RTL SCHEMATICS



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SIMULATION 

HALF ADDER GATE LEVEL

module halfadder(a,b,sum,carry);

input a,b;

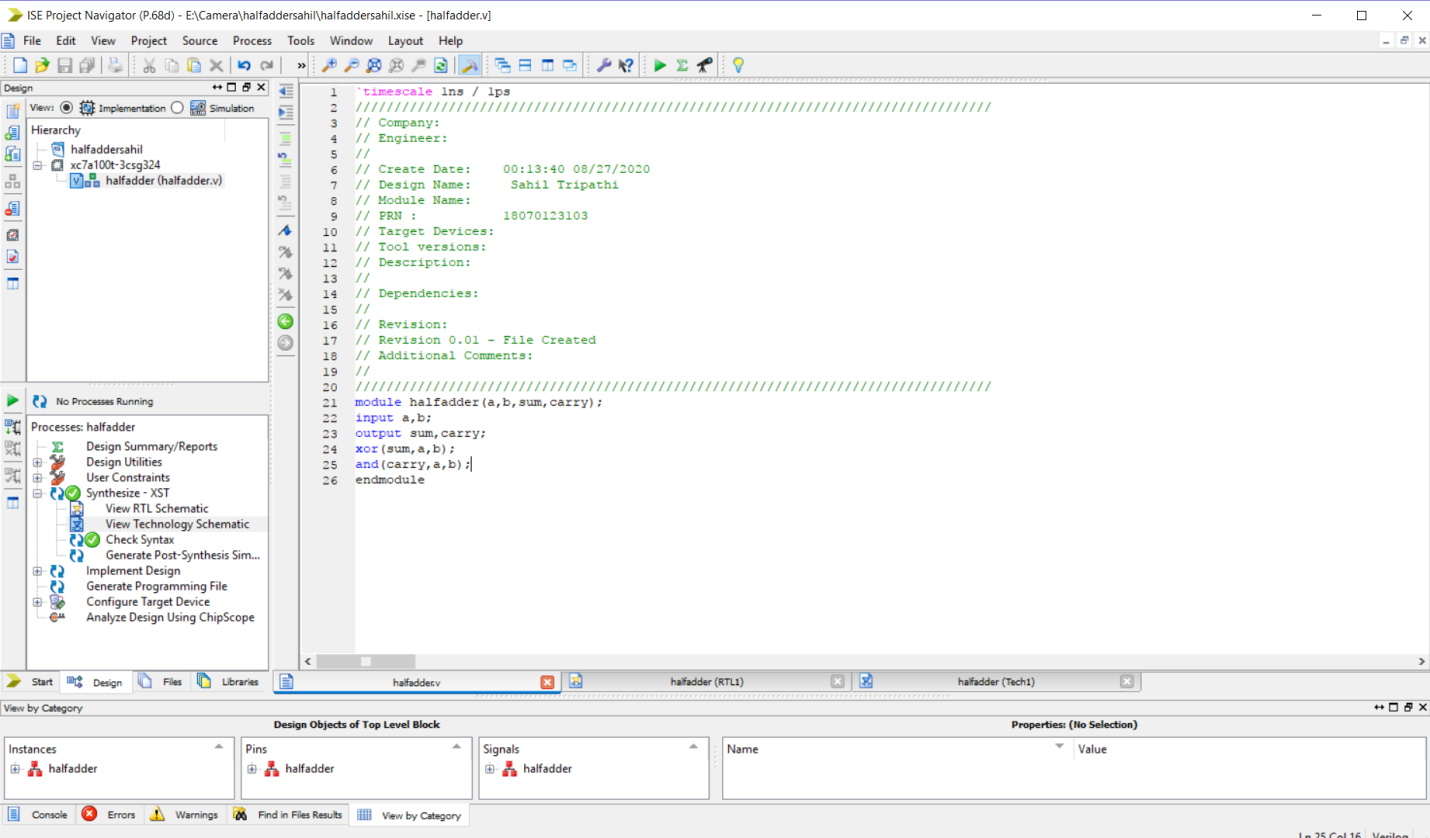
output sum,carry;

xor(sum,a,b);

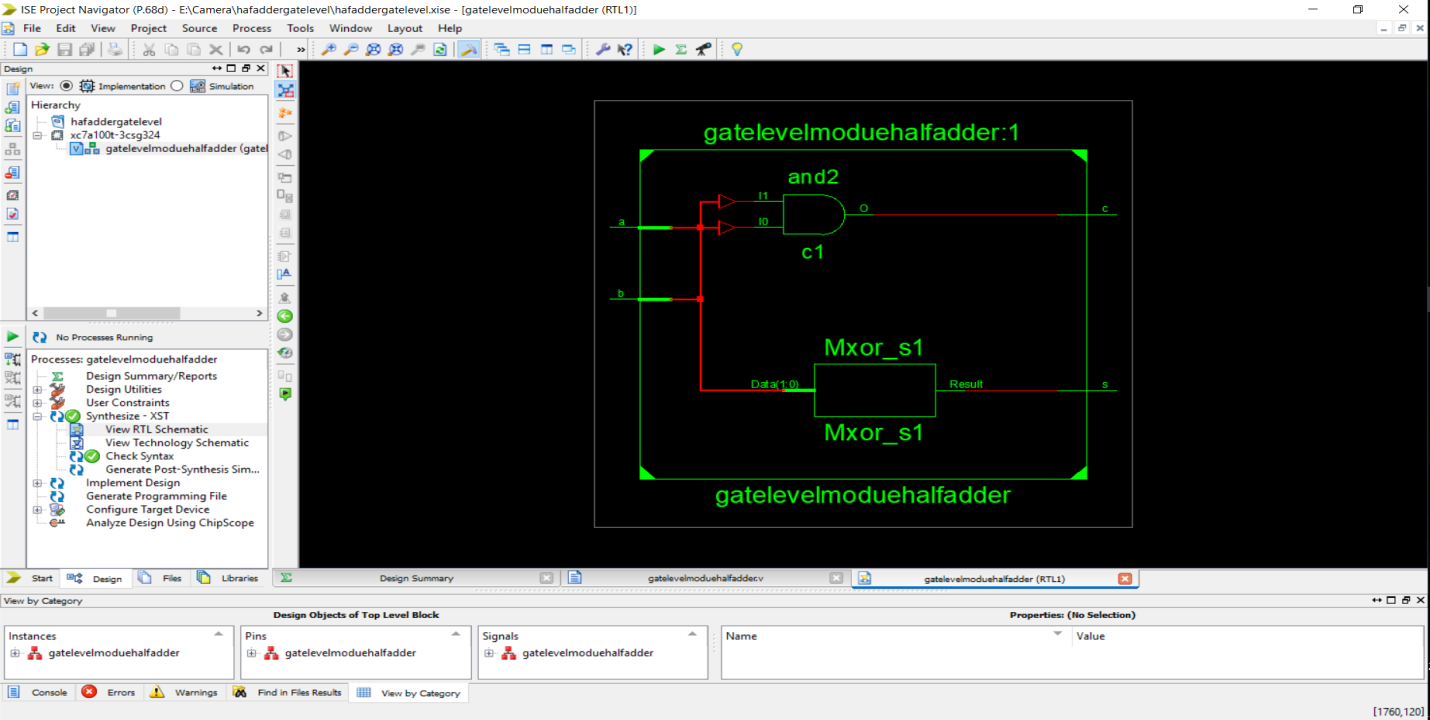
and(carry,a,b);

endmodule

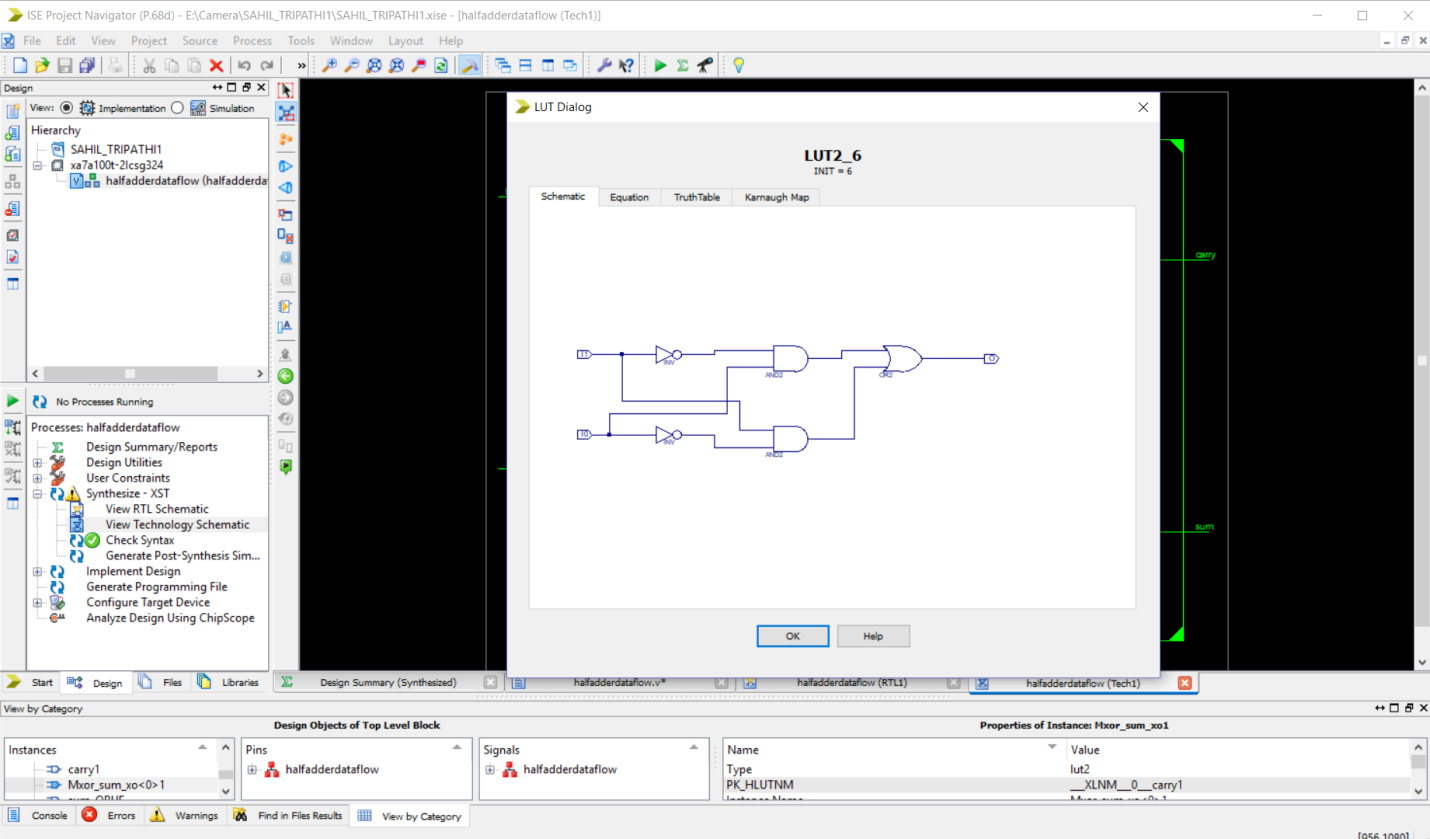
IMAGE OF CODE –



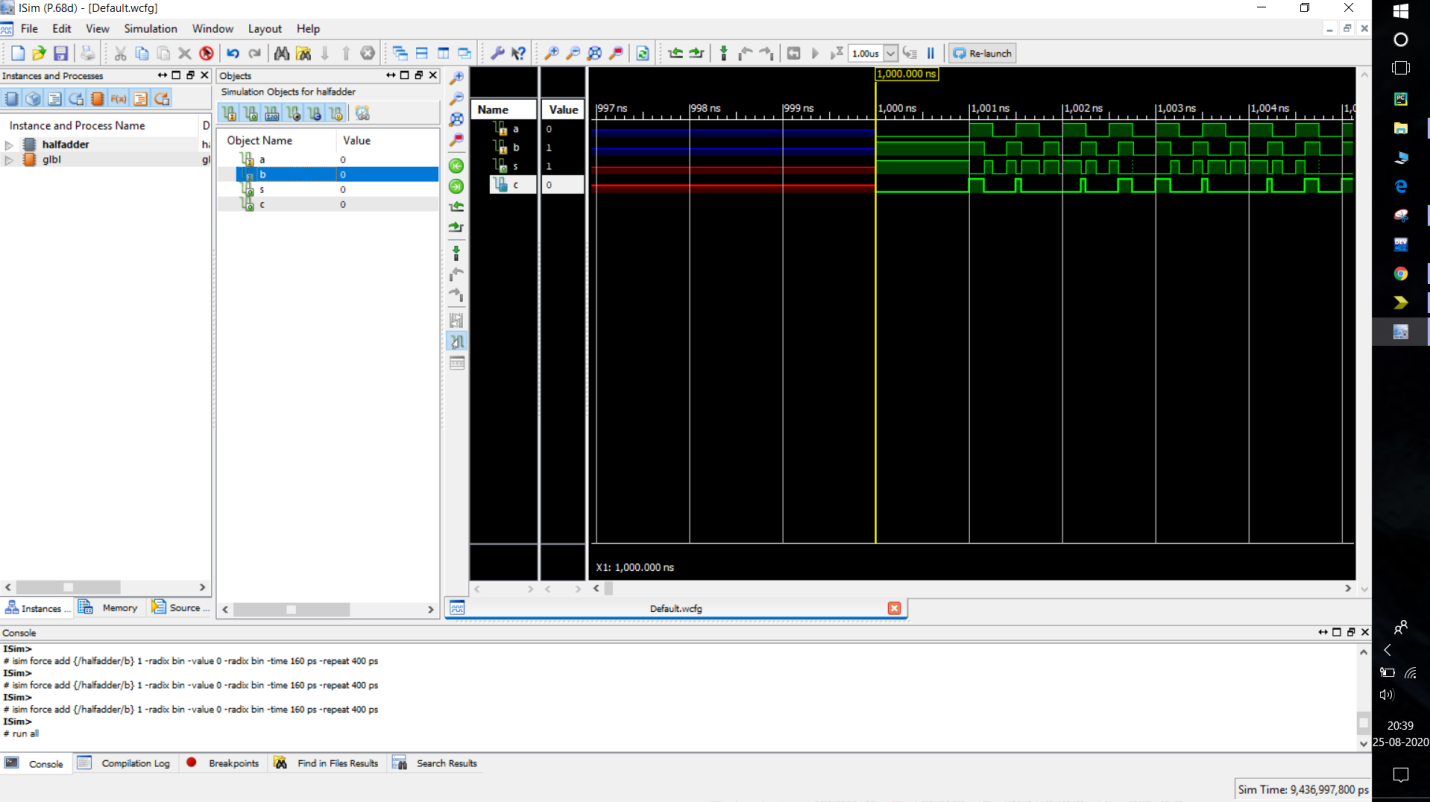
RTL SCHEMATICS



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SIMULATION



## FULL ADDER(Gate and Data flowing )

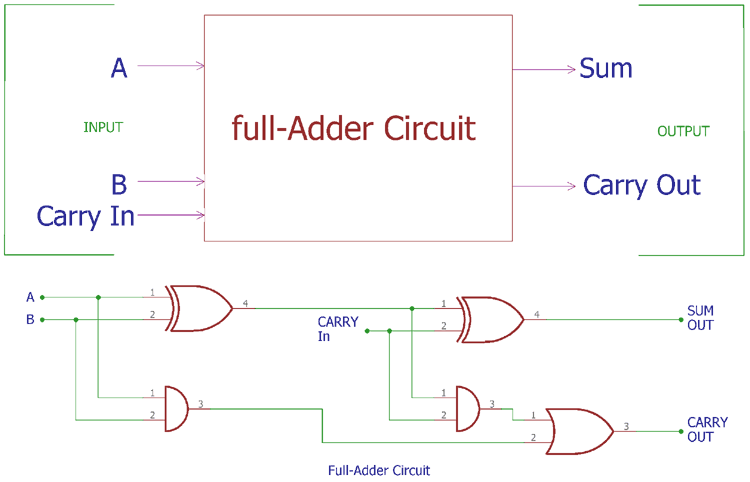
TRUTH TABLE FOR FULL ADDER

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | Ci | S | C0 |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

EQUATION OF SUM AND CARRY-

S=A XOR B XOR Ci

C=BCi + AB + ACi = AB+Ci(A XOR B)

CIRCUIT DIAGRAM

-FULL ADDER CODE (GATE LEVEL)

module fulladder(s,c,a,b,cin);

input a,b,cin;

output s,c;

wire x,y,z; // using to sshow internal conection

xor(x,a,b);

and(y,cin,x);

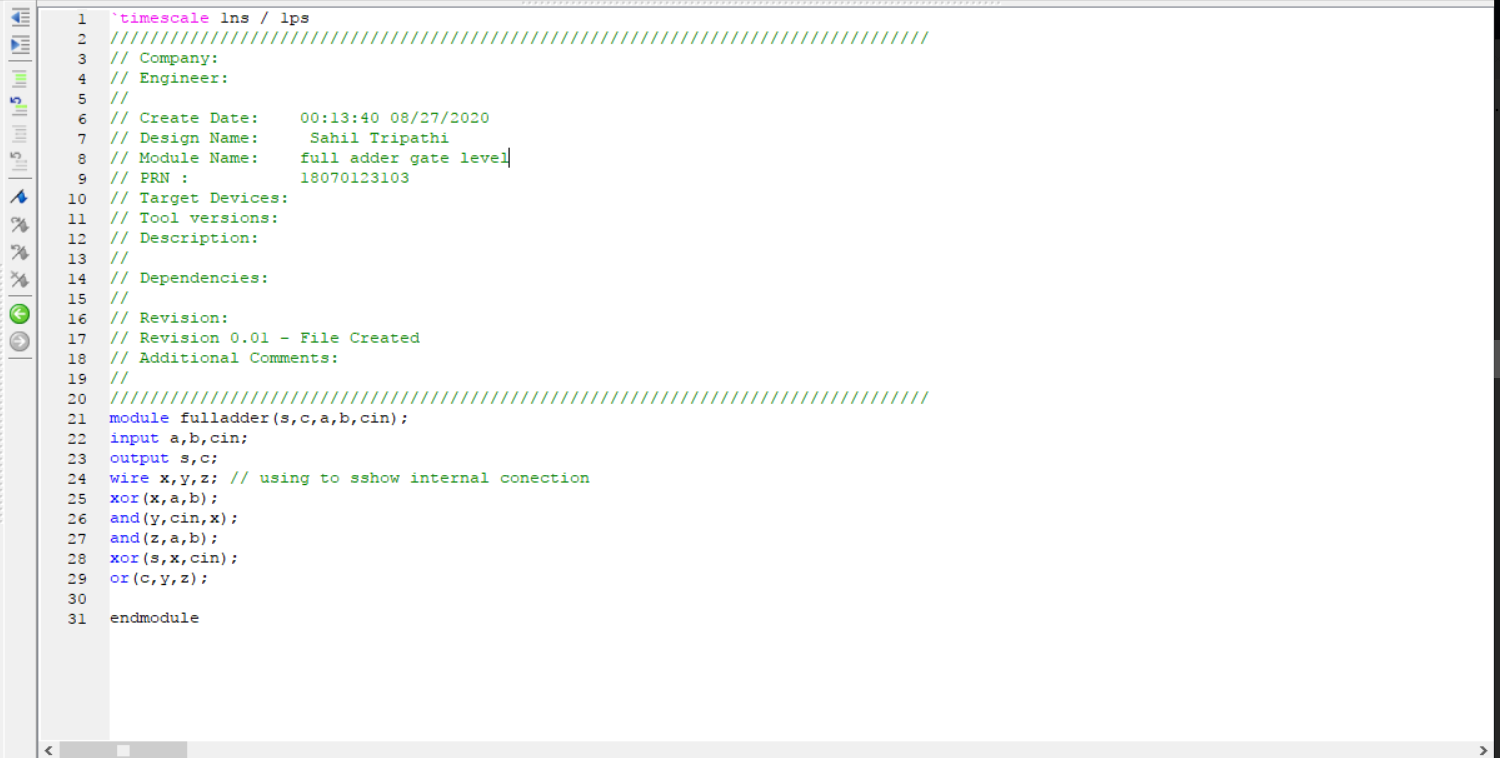
and(z,a,b);

xor(s,x,cin);

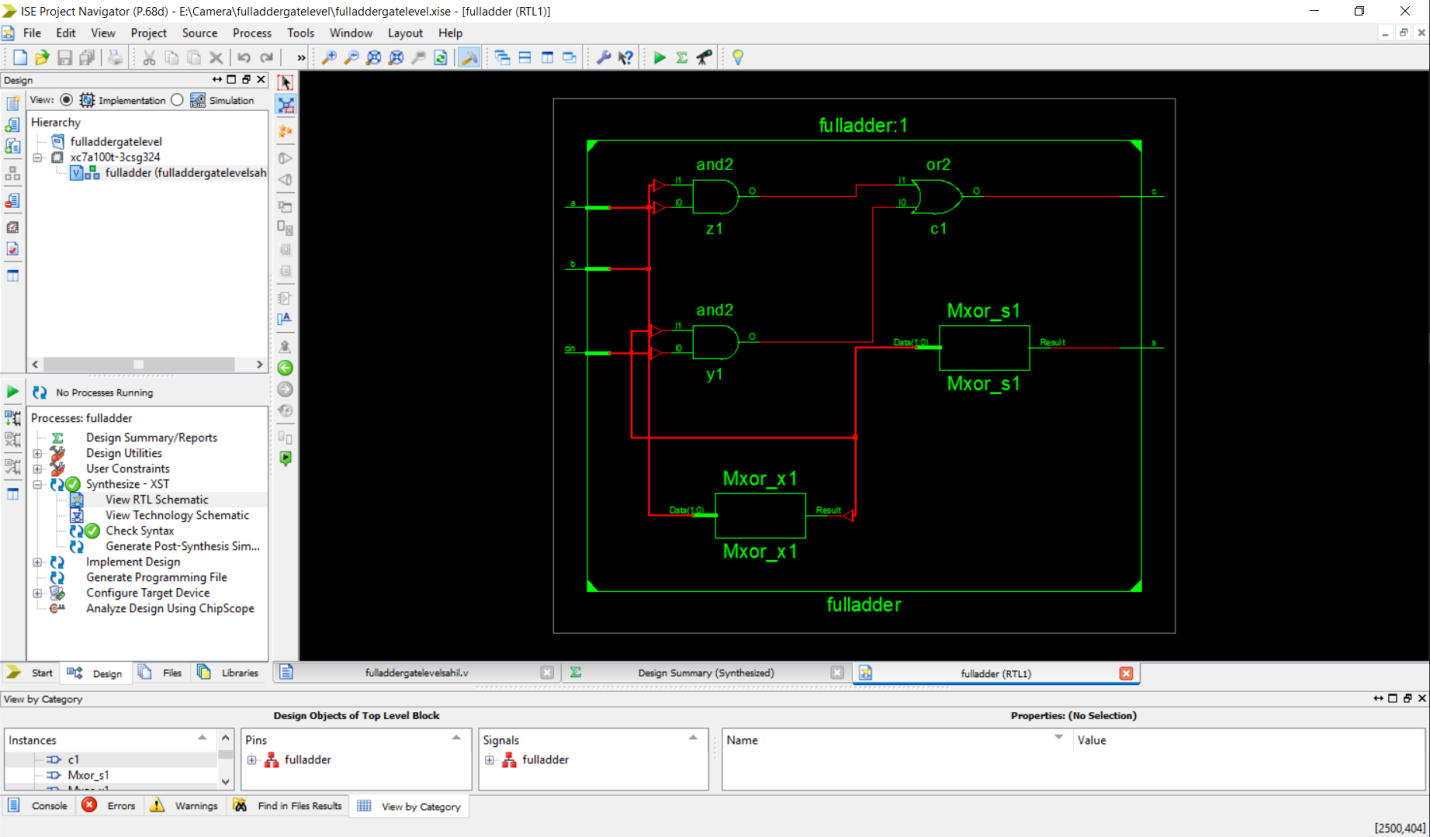
or(c,y,z);

endmodule

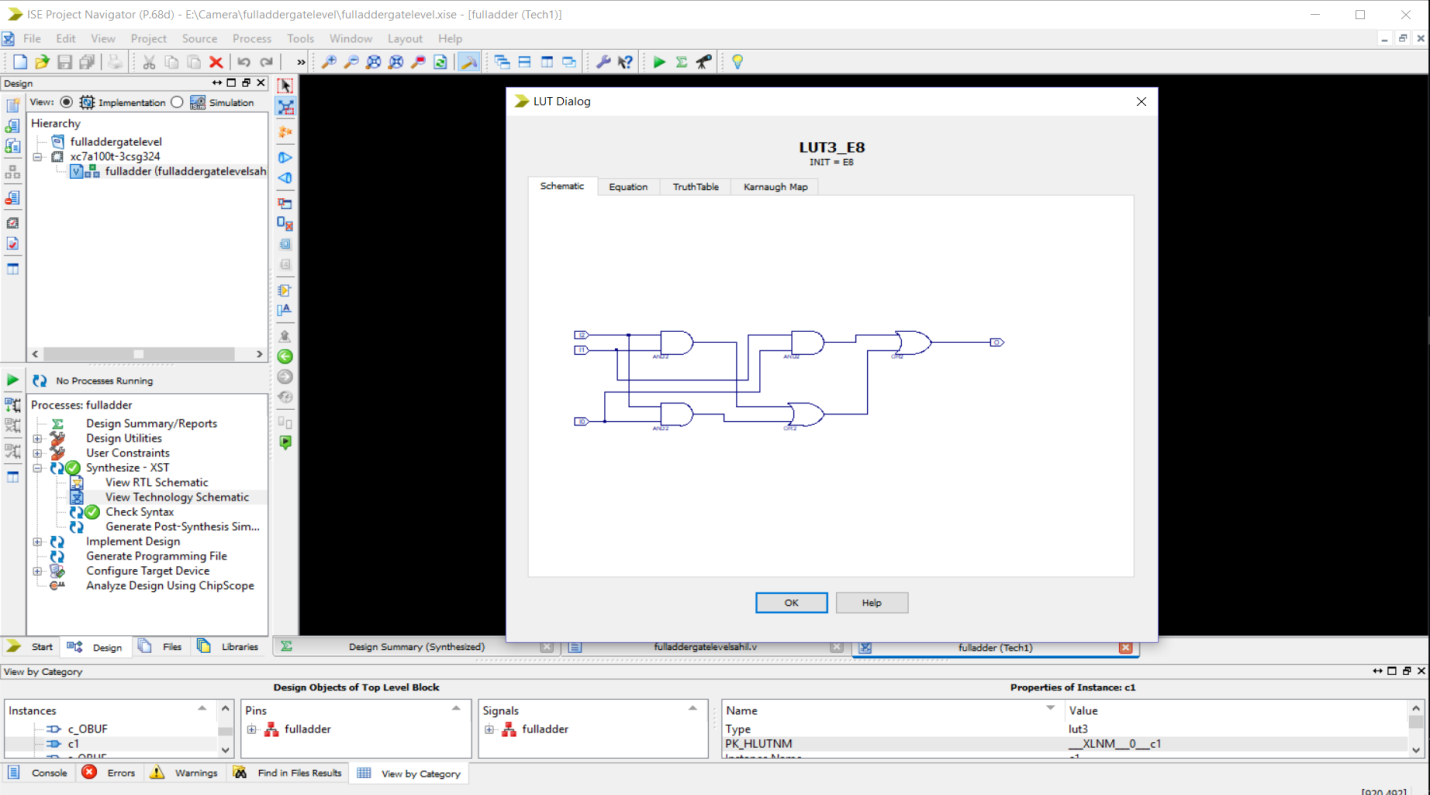
IMAGE OF CODE –



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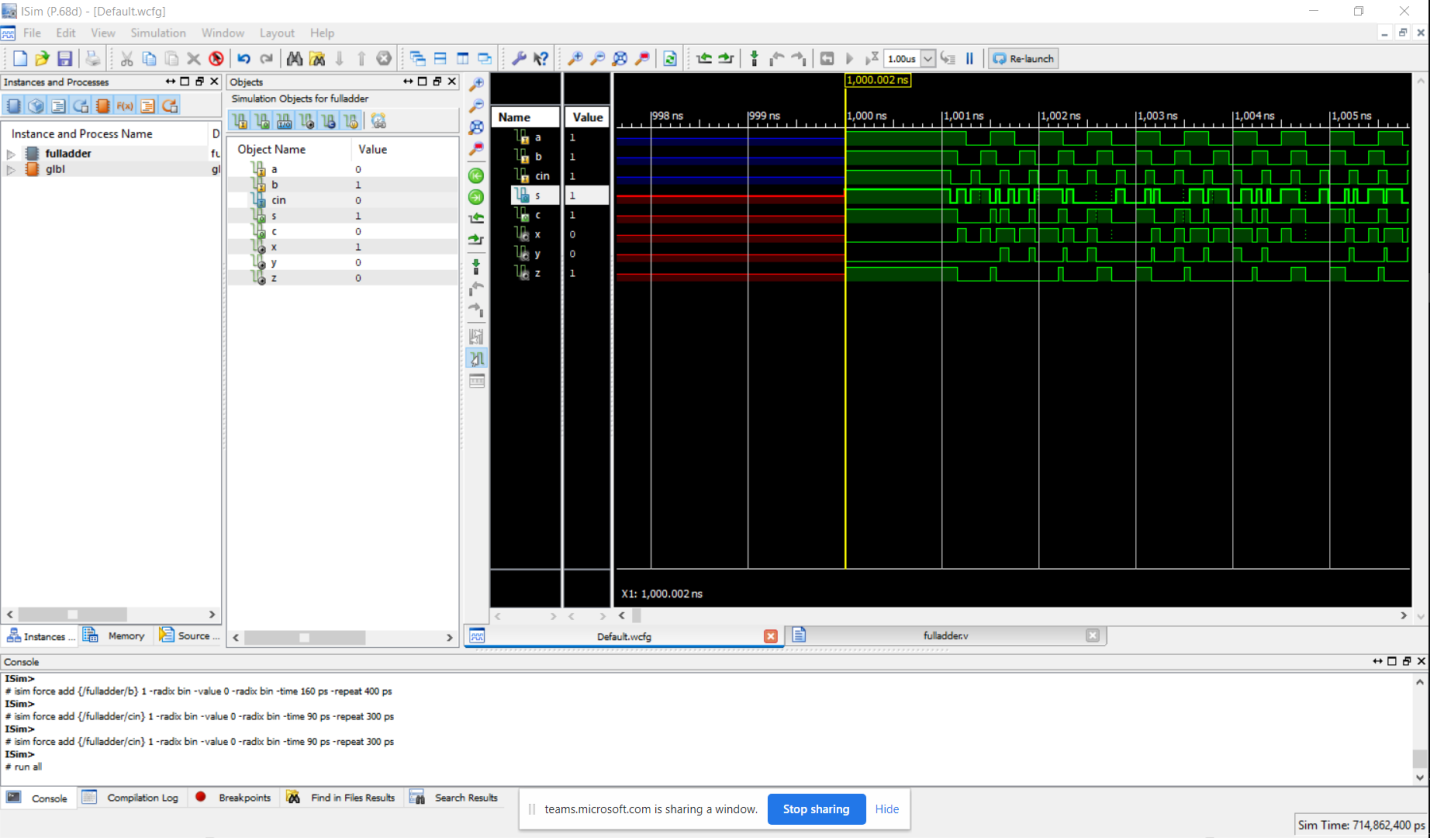


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FORCE CLOCK-



FULL ADDER USING DATA FLOW METHOD

**CODE –**

module fulladderdataflow(sum,carry,a,b,cin);

input a,b,cin;

output sum,carry;

wire x,y,z;

assign x=a^b; //A xor B

assign y=cin&x; //assignx And output

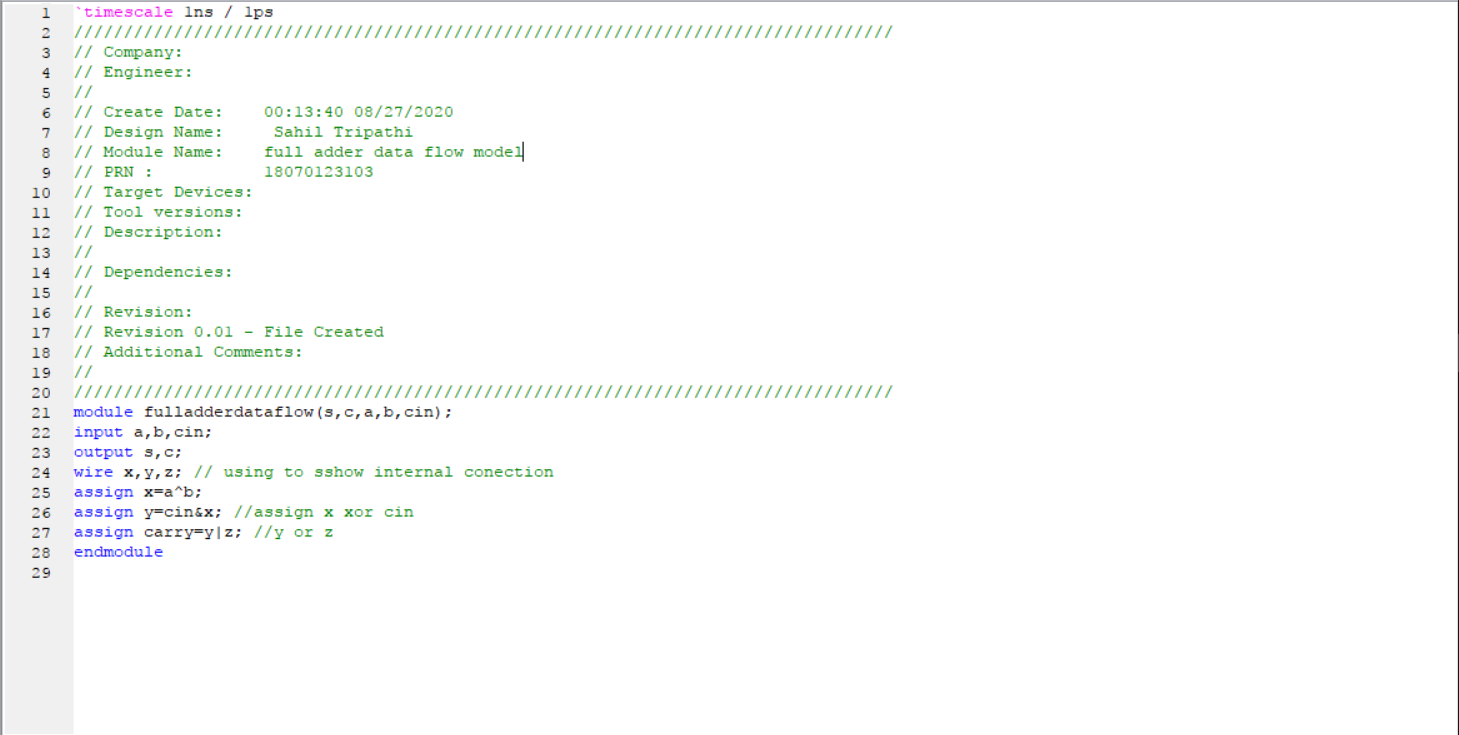
assign z=b&a;

assign sum=x^cin; //assign x xor cin

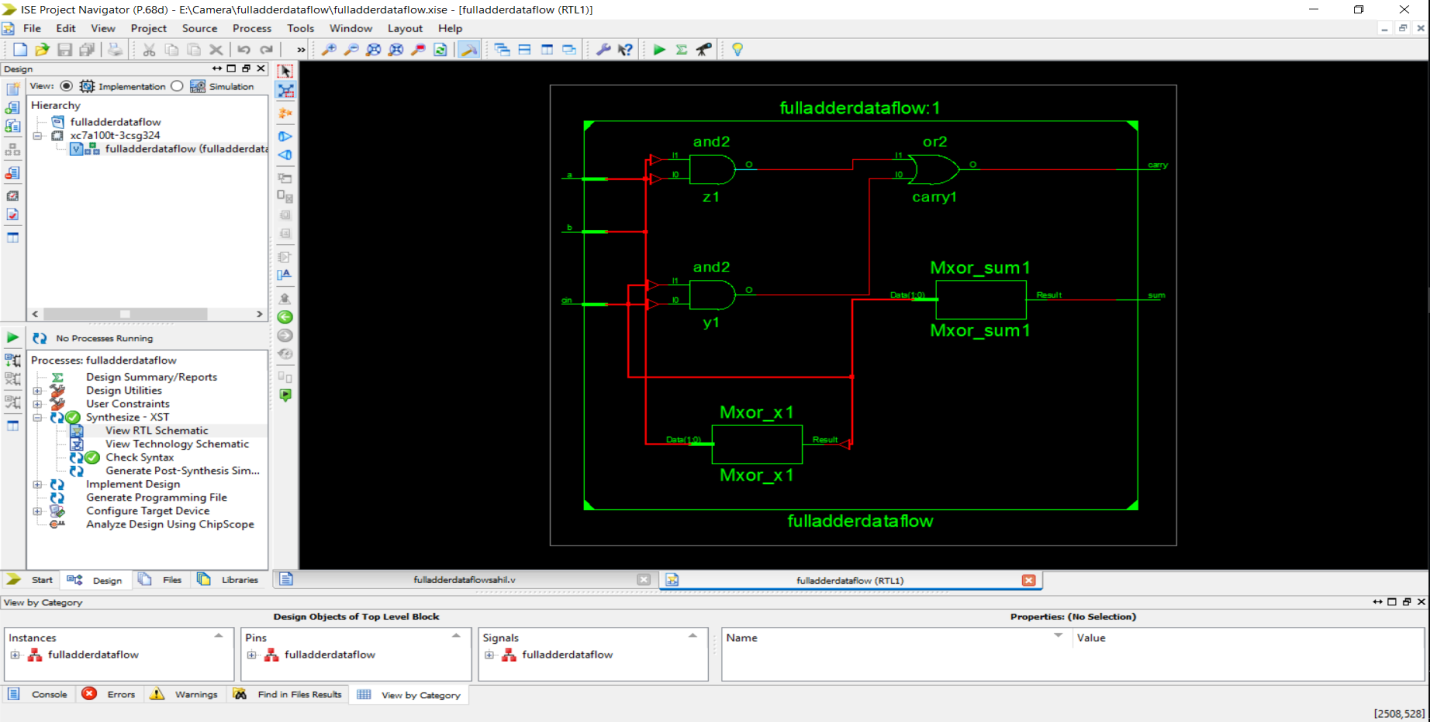
assign carry=y|z; // Y or Z

endmodule

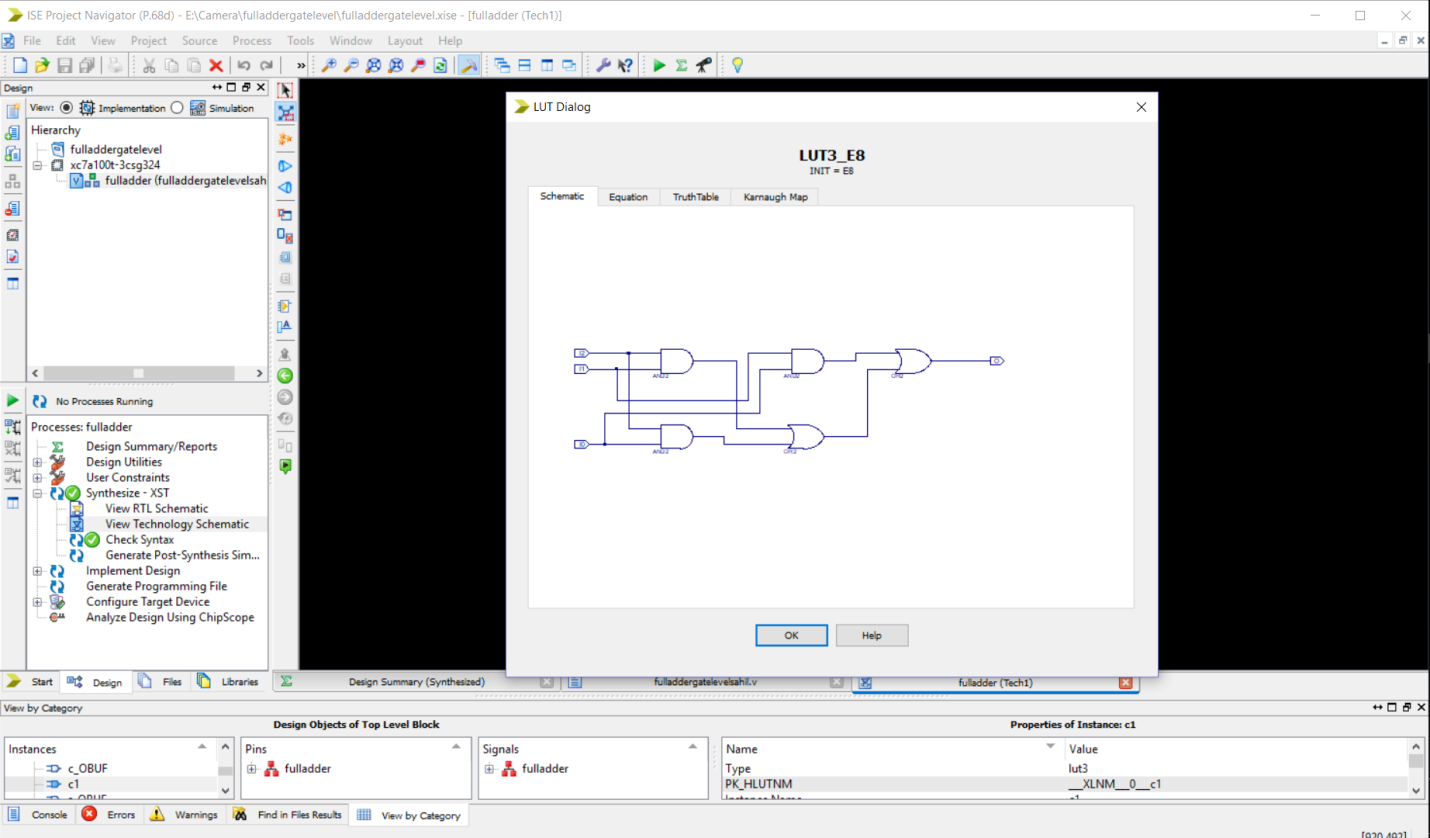
**IMAGE OF CODE**

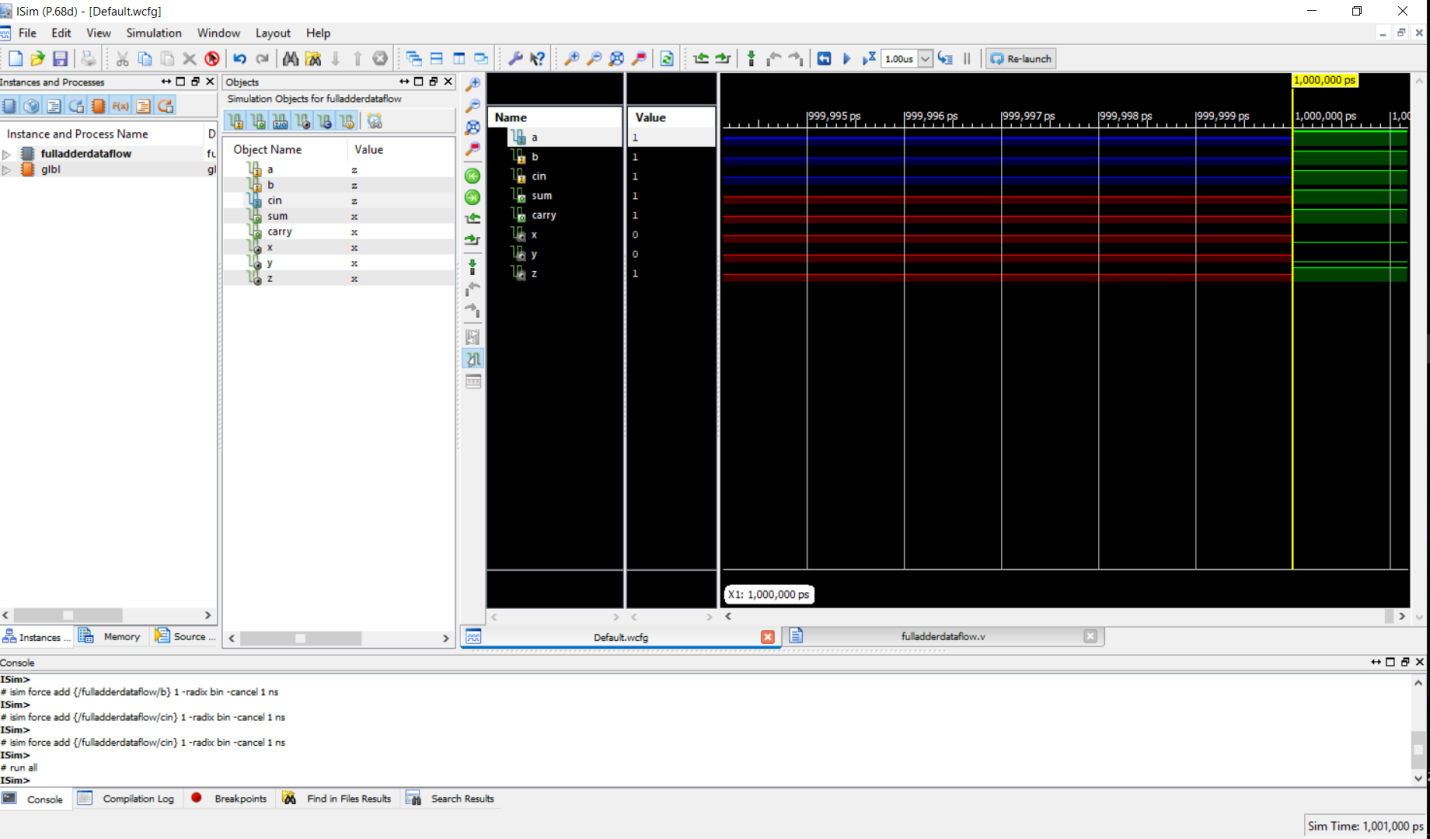


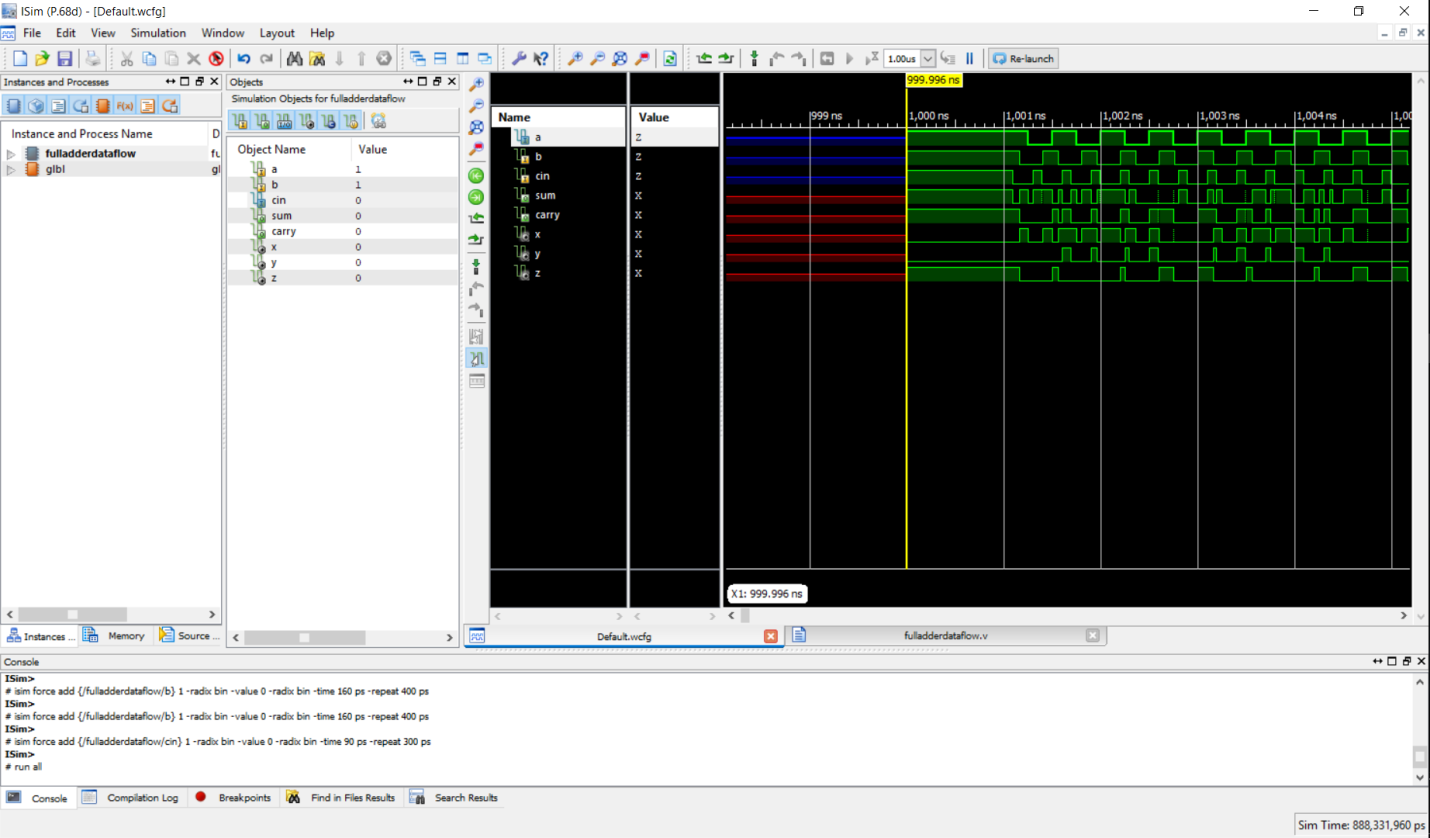
RTL IMAGE OF FULL ADDER DATAFLOW



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SO HENCE WE HAVE LEARNED HOW TO IMPLEMENT HALF & FULL ADDER AND SIMULATION IN XILIN SOFTWARE .